Product Specifications
July 1997 *(1 of 4)*

2.3 to 2.5 GHz +34 dBm Power GaAs FET

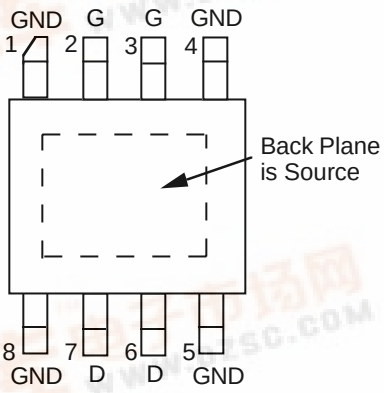
Features

- ❑ High Gain
- ❑ +34 dBm Power Output
- ❑ Proprietary Power FET Process
- ❑ >45% Linear Power Added Efficiency
- ❑ +29 dBm with 30 dBc Third Order Products
- ❑ Surface Mount SO-8 Power Package

Applications

- ❑ ISM Band Base Stations and Terminals
- ❑ PCS/PCN Base Stations and Terminals
- ❑ Wireless Local Loop

Package Diagram



Description

The CFK2162-P5 is a high-gain FET intended for driver amplifier applications in high-power systems, and output stage usage in medium power applications at power levels up to +34 dBm. The device is easily matched and provides excellent linearity at 2 Watts. Manufactured in Celeritek's proprietary power FET process, this device is assembled in an industry standard surface mount SO-8 power package that is compatible with high volume, automated board assembly techniques.

Specifications (TA = 25°C)

The following specifications are guaranteed at room temperature in Celeritek test fixture at 2.5 GHz.

Parameters	Conditions	Min	Typ	Max	Units
V_d = 8V, I_d = 800 mA (Quiescent)					
P_{-1dB}		33.0	34.0	—	dBm
SSG		11.0	12.0	—	dB
3rd Order Products (1)		26	30	—	dBc
Efficiency	@ P1dB	—	40	—	%
V_d = 5V, I_d = 350 mA (Quiescent)					
P_{-1dB}		—	30.0	—	dBm
SSG		—	9.0	—	dB
V_d = 5V, I_d = 1200 mA (Quiescent)					
P_{-1dB}		—	32.5	—	dBm
SSG		—	10.0	—	dB

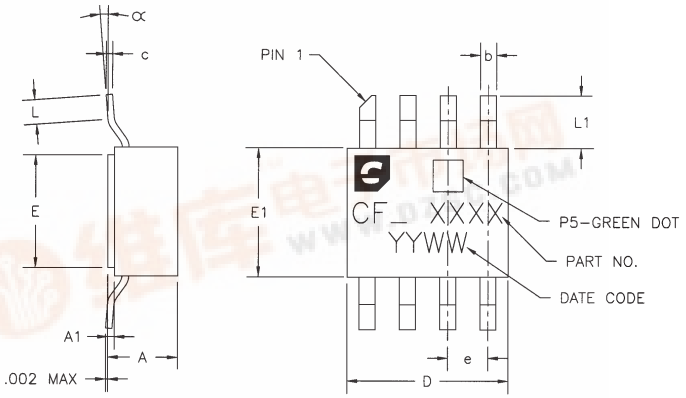
Parameters	Conditions	Min	Typ	Max	Units
g_m	Vds = 2.0V, Vgs = 0V	—	1700	—	mS
I_{dss}	Vds = 2.0V, Vgs = 0V	—	2.8	—	A
V_p	Vds = 3.0V, Ids = 65 mA	—	-1.8		Volts
BV_{GD} (3)	Igd = 6.5 mA	18	20	—	Volts
Θ_{JL} (2)	@150°C TCH	—	10	—	°C/W

Notes:
1. Sum to two tones with 1 MHz spacing = 29 dBm.
2. See thermal considerations information on page 4.
3. Max (+V_g) and (-V_g) under linear operation. Max potential difference across the device in RF compression ($2V_d$ + |-V_g|) not to exceed the minimum breakdown voltage (V_{br}) of +18V.

Absolute Maximum Ratings

Parameter	Symbol	Rating
Drain-Source Voltage	V_{DS}	12V (3)
Gate-Source Voltage	V_{GS}	-5V
Drain Current	I_{DS}	Idss
Continuous Dissipation	P_T	10W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	-65°C to +175°C

SO-8 Power Package Physical Dimensions



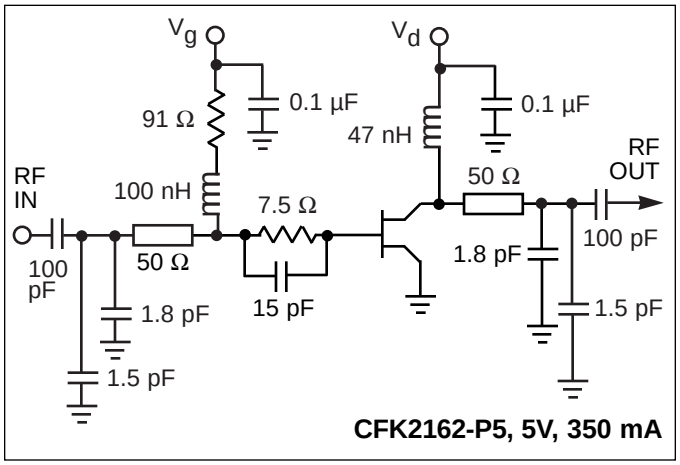
DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A		.086[2.184]	.100[2.540]
A1	.005[.1270]	.008[.2032]	.011[.2794]
b	.017[.4318]	.020[.5080]	.023[.5842]
c	.007[.1778]	.008[2032]	.009[.2286]
D	.195[4.953]	.200[5.080]	.205[5.207]
E	.135[3.429]	.140[3.556]	.145[3.683]
E1	.155[3.937]	.160[4.064]	.165[4.191]
e		.050[1.270]	
L	.020[.5080]		.040[1.016]
L1	.055[1.397]	.065[1.651]	.075[1.905]
α	0°		8°

DIMENSIONS IN INCHES [MILIMETERS]

Typical Scattering Parameters (TA = 25°C, Vds = 5 V, Ids = 350 mA)

Frequency (GHz)	S_{11} Mag	S_{11} Ang	S_{21} Mag	S_{21} Ang	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.6	0.946	-162.45	4.973	86.73	0.017	11.14	0.739	172.95
1.0	0.946	-176.06	2.885	73.75	0.018	9.37	0.748	169.73
1.8	0.927	172.61	1.873	54.47	0.023	1.6	0.707	161.84
1.9	0.922	169.71	1.828	50.82	0.023	-0.79	0.70	158.98
1.5	0.938	178.31	2.055	63.25	0.02	4.93	0.73	167.15
2.0	0.918	166.09	1.777	46.63	0.025	-1.23	0.694	155.54
2.1	0.914	161.9	1.722	42.23	0.024	-4.64	0.69	151.93
2.2	0.912	157.79	1.664	37.59	0.026	-9.26	0.689	148.15
2.3	0.914	153.46	1.578	34.07	0.023	-17.03	0.703	143.83
2.4	0.914	148.95	1.503	29.83	0.023	-21.0	0.707	139.91
2.5	0.918	145.37	1.431	26.13	0.023	-22.87	0.714	137.02
2.6	0.921	141.59	1.344	22.16	0.022	-28.45	0.722	134.0
2.7	0.923	138.23	1.254	18.61	0.022	-28.3	0.735	131.62
3.0	0.941	132.34	1.033	10.11	0.022	-27.73	0.76	128.69
3.5	0.957	134.66	0.803	6.12	0.02	-21.78	0.787	132.92
4.0	0.94	138.76	0.803	1.66	0.023	-20.57	0.74	136.51
(TA = 25°C, Vds = 5 V, Ids = 1200 mA)								
0.6	0.95	-165	5.311	84.94	0.014	13.61	0.747	17.19
1.0	0.951	-177.94	3.044	72.23	0.014	14.39	0.749	168.92
1.8	0.935	171.39	1.98	53.44	0.018	10.27	0.703	161.07
1.9	0.931	168.6	1.93	49.72	0.019	5.75	0.696	158.27
2.0	0.929	165.15	1.88	45.76	0.02	7.43	0.69	154.9
2.1	0.925	161.29	1.822	41.44	0.02	4.37	0.686	151.32
2.2	0.924	157.02	1.757	36.86	0.021	2.36	0.687	147.44
2.3	0.92	152.84	1.765	32.59	0.02	-5.07	0.679	144.99
2.4	0.923	148.35	1.673	28.03	0.021	-71.14	0.684	141.21
2.5	0.923	144.9	1.603	24.44	0.021	-9.31	0.692	138.25
2.6	0.927	141.0	1.503	20.51	0.02	-11.55	0.702	135.31
2.7	0.93	137.72	1.406	16.94	0.02	-14.27	0.711	132.91
3.0	0.947	131.72	1.09	9.25	0.018	-17.77	0.757	127.79
3.5	0.961	133.41	0.853	4.59	0.017	-13.03	0.779	131.26
4.0	0.945	137.83	0.85	0.36	0.021	-8.72	0.73	134.73
(TA = 25°C, Vds = 8 V, Ids = 800 mA)								
0.6	0.941	-164.65	5.654	83.55	0.015	10.74	0.676	174.61
1.0	0.947	-177.32	3.25	70.11	0.015	8.2	0.688	171.96
1.8	0.93	171.59	2.058	49.6	0.018	6.89	0.652	165.68
1.9	0.927	168.63	2.006	45.54	0.019	3.81	0.644	163.07
2.0	0.923	165.04	1.99	41.52	0.019	-1.07	0.639	159.85
2.1	0.919	160.94	1.885	36.76	0.02	-1.68	0.635	156.23
2.2	0.917	156.65	1.714	32.35	0.02	-2.32	0.636	152.38
2.3	0.921	153.49	1.779	29.48	0.018	-14.97	0.642	148.42
2.4	0.921	149.12	1.688	24.79	0.018	-16.28	0.648	144.43
2.5	0.925	145.41	1.616	21.01	0.017	-20.8	0.656	141.59
2.6	0.927	141.65	1.518	16.92	0.017	-23.5	0.667	138.37
2.7	0.933	138.32	1.417	13.24	0.017	-25.79	0.681	136.05
3.0	0.944	131.73	1.116	3.58	0.018	-21.43	0.722	132.33
3.5	0.96	134.09	0.857	-1.39	0.016	-16.54	0.762	136.36
4.0	0.942	137.96	0.841	-6.32	0.02	-10.57	0.723	140.71

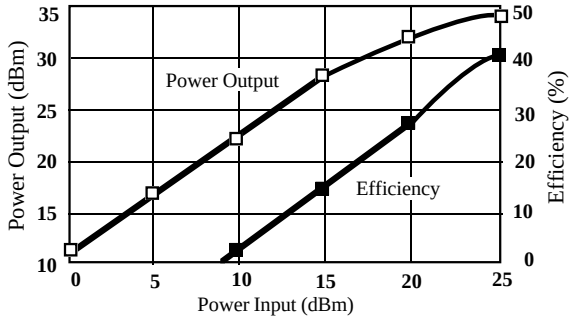
RF Match Data shown in the performance graphs was taken in the test circuits shown at right and on page 3. Layout is important for proper operation. Phase length of input and output 50Ω line varies as a function of exact desired frequency of operation. Output shunt inductor effects output performance. Celeritek recommends the use of a high impedance printed inductor Lambda/4 in length. Please contact the factory for an evaluation board and/or more detailed application support.



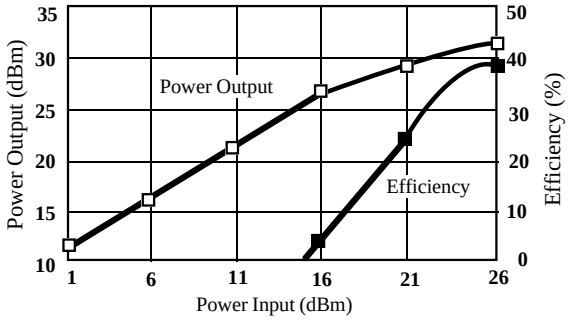
CFK2162-P5, 5V, 350 mA

Typical Performance

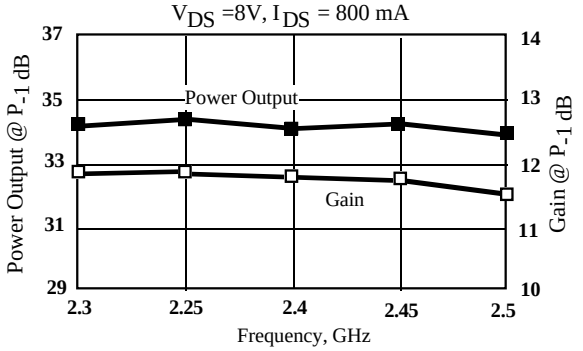
Power Output & Power Added Efficiency vs Power Input
2.45 GHz, V_{DS} = 8 V, I_{DS} = 800 mA



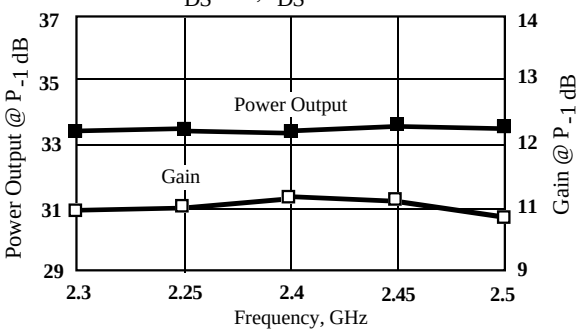
Power Output & Power Added Efficiency vs Power Input
2.45 GHz, V_{DS} = 5 V, I_{DS} = 1.2 A



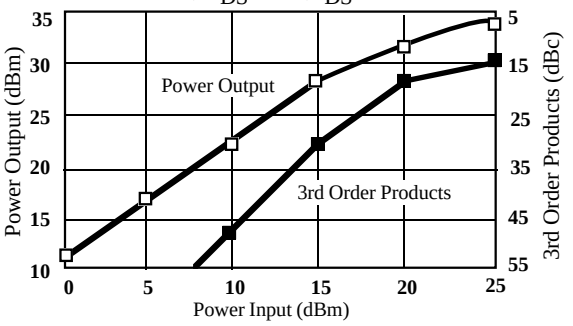
Power Output and Gain vs Frequency
V_{DS} =8V, I_{DS} = 800 mA



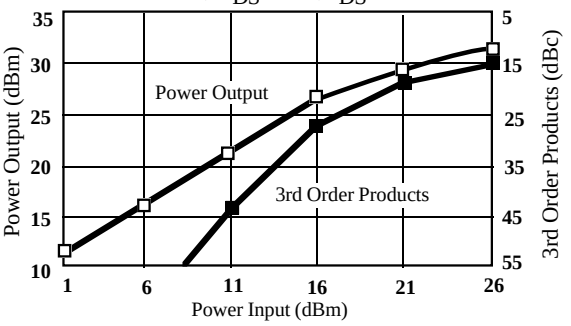
Power Output and Gain vs Frequency
V_{DS} =5V, I_{DS} = 1200 mA

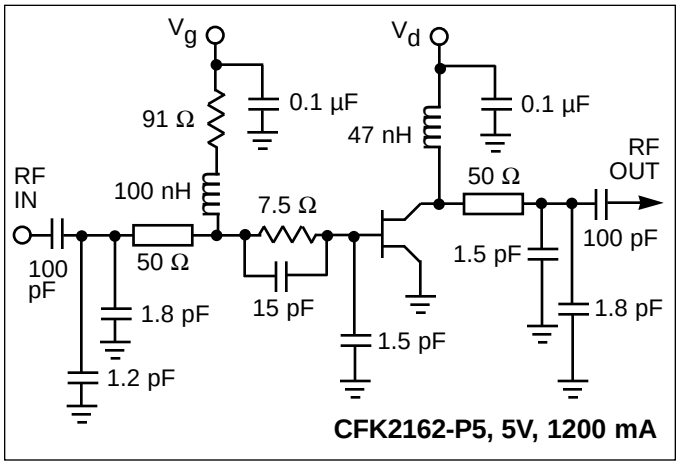


Power Output & 3rd Order Products vs Power Input
2.45 GHz, V_{DS} = 8 V, I_{DS} = 800 mA

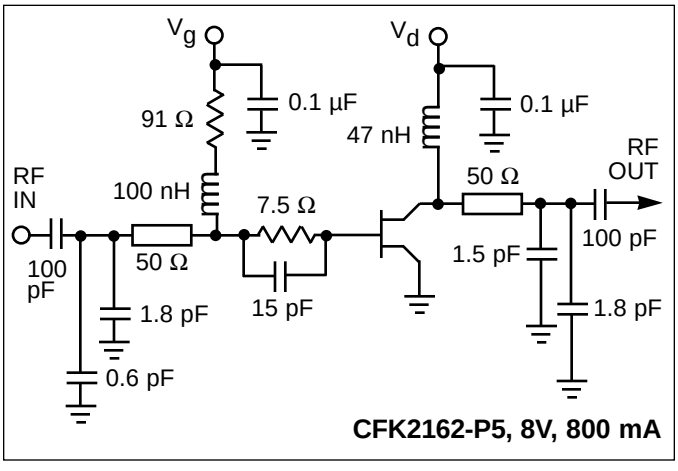


Power Output & 3rd Order Products vs Power Input
2.45 GHz, V_{DS} = 5 V, I_{DS} = 1.2 A





CFK2162-P5, 5V, 1200 mA



CFK2162-P5, 8V, 800 mA

Thermal Considerations

The data shown was taken on a 31 mil thick FR-4 board with 1 ounce copper on both sides. The board was mounted to a base-plate with 3 screws as shown. The screws bring the top side copper temperature to the same value as the baseplate. The thermal resistance to the indicated reference lead, Θ_{JL}, is 10°C/W. The thermal resistance to the reference screw is 12°C/W.

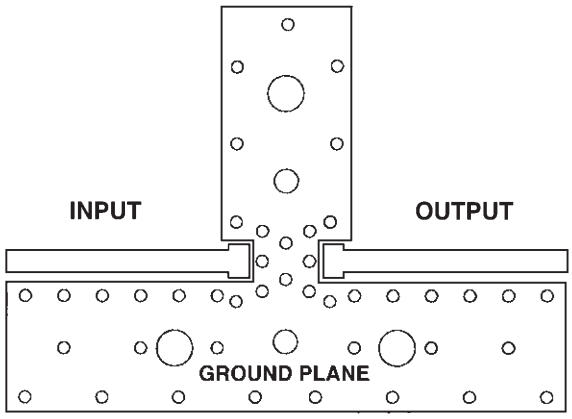
1. Use 1 or 2 ounce copper if possible.

2. Solder all eight leads of the CFK2162-P5 package to the appropriate electrical connection.

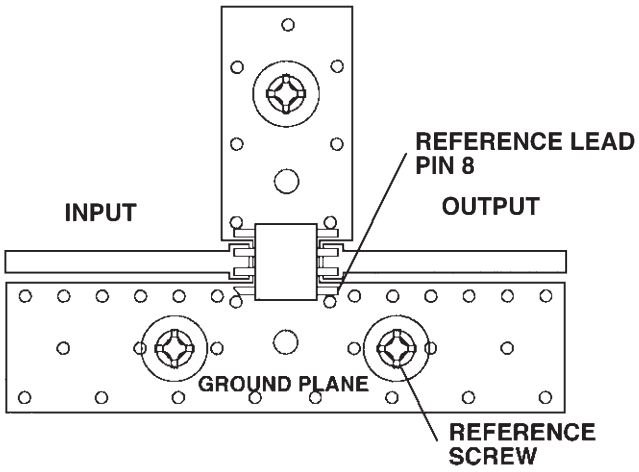
3. Solder the copper pad on the backside of the CFK2162-P5 package to the ground plane.

4. Use a large ground pad area with many plated through-holes as shown.

5. If possible, use at least one screw no more than 0.2 inches from the CFK2162-P5 package to provide a low thermal resistance path to the baseplate of the package.



BOARD LAYOUT



THERMAL MOUNTING DIAGRAM

Ordering Information

The CFK2162-P5 power stage is available in a SO-8 surface mount package. Devices are available in tape and reel. Ordering part numbers are listed.

Part Number for Ordering	Function	Package
CFK2162-P5	**2.3 - 2.5 GHz Power Stage**	**SO-8 surface mount power package**
CFK2162-P5-000T	**2.3 - 2.5 GHz Power Stage**	**SO-8 surface mount power package in tape and reel**