National Semiconductor

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CGS410 Programmable Clock Generator

General Description

The CGS410 is a programmable clock generator which produces a variable frequency clock output for use in graphics, disk drives and clock synchronizing applications. The CGS410 produces output clocks in CMOS and differential formats. The user is able to program the differential output levels to best suit the levels of the interfacing device. A common configuration allows PCLK to emulate positive ECL logic levels, eliminating the need for TTL to ECL translation.

The CGS410 is referenced off the XTLIN input which can be configured for either external crystal or external oscillator support. All internal frequency generation is referenced from the XTLIN input. The CGS410 can also be driven by EXTCLK as desired. EXTCLK may serve as the source from a fixed clock (for passthru mode), or as an external VCO input.

The CGS410 contains three internal user-selectable low pass filters (LPFs). A fourth option allows for the use of an external LPF configuration. Use of the internal filters greatly simplifies layout, reduces board real estate, and minimizes part count. A programmable polarity charge pump allows the user to optimize the optional external LPF circuitry.

The primary loop structure of the CGS410 consists of programmable N and R dividers. Both are contiguous; N can be any value between 2 and 16383, and R can be any value between 1 and 1023. Additional dividers of the internal VCO allow individual programmability for the PCLK, CMOS_PCLK, and LCLK outputs.

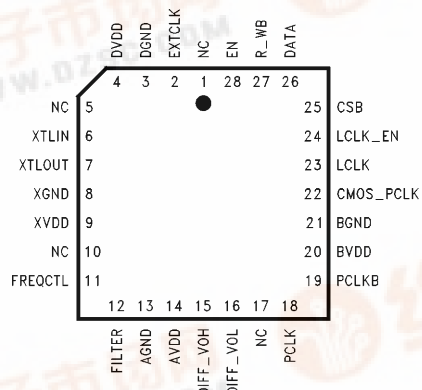
An additional advantage of the CGS410 is its ability to perform smooth, glitch-free clock output changes as the user selects passthru clock sources or changes the VCO frequency. A real-time synchronous load clock enable (LCLK_EN) control input allows for the enabling and disabling of the LCLK output. This is suitable for applications which require the removal of an active LCLK during the blanking portion of a screen refresh.

On power-up the XTLIN frequency is internally divided by two and routed to the PCLK outputs, providing a known power-up output frequency with a 50% duty cycle. The CGS410 is programmed by a serial stream of data. A serial bit read can verify the contents of the register.

Features

- Fully programmable frequency generator
- Provides frequencies to 135 MHz
- Configurable high-speed complementary clock outputs
- CMOS output clocks
- Glitch-free transitions for clock changes
- Powers up in a known state
- Single supply (+5V) operation
- Low current draw, ideal for battery applications
- Read/write control register
- Internal VCO and loop filters

Connection Diagram



TL/F/11919–1

Important Note: This device is sensitive to noise on certain pins, especially FREQCTL, FILTER, AVDD, and AGND. Special care must be taken with board layout for optimum performance.

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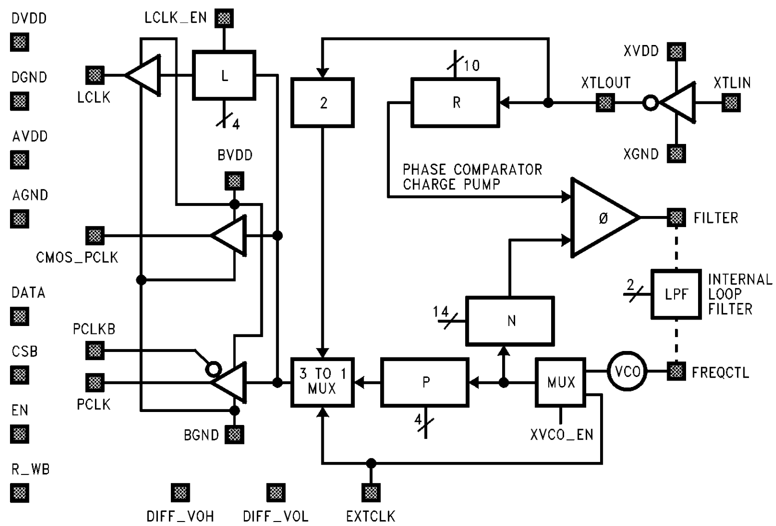
Table of Contents

1.0 Functional Description

The CMOS clock outputs are generated by a phase lock loop (PLL). The internal voltage controlled oscillator (VCO) derives a reference frequency from the crystal input (XTLIN) and produces a synthesized output. A programmable 1 to 16 divider and a passthru mux are positioned between the VCO and clock outputs, allowing a wide range of output frequencies without having to band switch the VCO. A load clock (LCLK) is also available. A synchronous LCLK control simplifies system frame buffer design.

With the CGS410 programmed to run in internal LPF mode, no external low pass filter components are required. There are three internal filters. If an external loop filter is desired, or if precise LPF parameters are required, the CGS410 can be programmed to use the external filter pin. The external filter requires two capacitors and one resistor. No external devices such as inductors or varactors are necessary. Frequency configuration is programmed through the internal N, R, P, and L dividers and the 3-to-1 MUX.

CGS410 Block Diagram



TL/F/11919–2

2.0 Pin Definitions

Symbol	Pin	I/O	Function
AGND	13	S	**Analog Ground.** This pin serves as the return for the analog circuitry. AGND should also serve as the external filter return reference as sourced by FILTER. AGND should be well referenced to DGND.
AVDD	14	S	**Analog VDD.** This pin sources the internal VCO, internal loop filter, and charge pump. Due to the sensitive nature of this pin, special care should be taken to filter out noise for best performance. AVDD should track DVDD to within ±5%.
BGND	21	S	**Buffer Ground.** Output buffer supply return. This serves as the return for the CMOS__PCLK and LCLK outputs. Best output performance is obtained when the CMOS__PCLK and LCLK reception devices are referenced to BGND.
BVDD	20	S	**Buffer VDD.** This positive power supply input sources LCLK, CMOS__ PCLK and the differential PCLK output pair. Care must be taken to properly bypass this input with BGND.
CMOS__PCLK	22	O	**CMOS PCLK Output.** This single-ended output is typically used to drive devices which require CMOS input characteristics.
CSB	25	I	**Clock for Serial Data Input and Output.** This input is TTL compatible edge sensitive. In the serial read or write operation, the falling edge latches the R__WB and EN states. The rising edge completes the shift and transfer operation.
DATA	26	I/O	**Data Input/Output.** This is a bi-directional I/O pin used to transfer data in and out of the CGS410 in a serial fashion. Data must be valid when each bit is clocked on the rising edge of the CSB input. DATA is TTL compatible for input mode; CMOS compatible for output mode.
DGND	3	S	**Digital Ground.** This pin serves as the return path for the internal CGS410 counter circuitry. This input should be well referenced to BGND.

2.0 Pin Definitions (Continued)

Symbol	Pin	I/O	Function
DIFF_VOH	15	O	**Differential High Voltage Load.** This output is connected to a load network which is ten times the value of the load network connected to the differential PCLK pins.
DIFF_VOL	16	O	**Differential Low Voltage Load.** This output is connected to a load network which is ten times the value of the load network connected to the differential PCLK pins.
DVDD	4	S	**Digital VDD.** This pin serves as the source for the internal CGS410 counter circuitry. This input should be well referenced to BVDD and bypassed to DGND.
EN	28	I	**An Active-High, Level-Sensitive TTL Compatible Input.** This input is sampled on the falling edge of CSB, EN high allows data to be transferred to the shadow register in the write mode or to the shift register in the read mode.
EXTCLK	2	I	**External Clock.** When the internal multiplexer is set to EXTCLK mode, the crystal and phase-locked loop are bypassed, and this TTL compatible input will drive the PCLK outputs and the L divider input. If the external VCO mode is invoked, EXTCLK drives the P and N dividers. When this input is not selected, it should be driven to a high or low to avoid oscillations.
FILTER	12	O	**Filter Output.** This current source output is driven from the internal charge pump. This output is left floating in applications where only the internal low pass filters are used. FILTER is used for applications which require passive or active external LPF networks. For passive LPF networks, this output should be connected directly to FREQCTL input and the LPF network (see *Figure 3-7*).
FREQCTL	11	I	**Frequency Control.** FREQCTL is the VCO voltage control input. When in external loop filter mode, the voltage present on this input determines the VCO frequency. For applications which require only the internal filters, this input is left unconnected. This input is used for applications which require external networks for loop filtering. The input voltage range should not exceed AVDD, and not go below the AGND reference.
LCLK	23	O	**Load Clock Output.** This CMOS compatible, non-gated output is typically used in video applications which require a programmable clock to produce lower output frequencies synchronous to PCLK. Typically, this is used to clock video shift registers or RAMDACs.
LCLK_EN	24	I	**Load Clock Enable.** This synchronous active high TTL compatible input selects whether the LCLK output is disabled or enabled. A HIGH level enables the LCLK output pin, while a LOW disables activity on the LCLK. In the disabled state LCLK is driven high or low depending on the logic state of the L counter when disabled. Refer to the LCLK_EN timing specification.
PCLK	18	O	**Differential PCLK Output.** This high speed output is configured to drive a host of devices requiring differential clock inputs. Output voltage swing is defined by the differential level control bit (Bit 1).
PCLKB	19	O	**Differential PCLK Output.** This high speed output is configured to drive a host of devices requiring differential clock inputs. Output voltage swing is defined by the differential level control bit (Bit 1).
R_WB	27	I	**Read/Write Select.** R_WB is a level sensitive TTL compatible input. When writing values to the chip, the R_WB would be sampled low on the falling edge of CSB. Conversely, when reading values, the R_WB would be sampled high on the falling edge of CSB.
XGND	8	S	**Crystal Ground.** This pin serves as the ground return for the internal oscillator circuitry. All external oscillator support, be it active or passive, should be tied to XGND for best performance.
XTLIN	6	I	**Crystal Input.** XTLIN is designed to operate with crystal, oscillator or ceramic resonator input. For crystal input applications, the crystal should be the fundamental parallel mode type. See the applications diagrams for more information.
XTLOUT	7	O	**Crystal Output.** This output is used as the Pierce Oscillator output for use with parallel mode crystals. An external resistor between XTLOUT and XTLIN will bias this stage to approximately XVDD/2. This output is left floating for applications which directly drive the XTLIN.
XVDD	9	S	**Crystal VDD.** This positive power supply input sources the internal oscillator circuitry. All external oscillator support, be it active or passive, should be referenced to XVDD for best performance. This supply input must track DVDD to within 5%.

3.0 Circuit Operation

The CGS410 programmable clock generator uses a crystal oscillator as a frequency reference to generate clock signals for video applications such as display systems or disk drive constant density recording. The reference may come from any source as long as input specifications are maintained. Both single-ended (CMOS) and differential clock outputs are generated. Both clock outputs are synchronized to simplify system timing. A unique combination of internal functions (such as the VCO, the crystal oscillator, a phase comparator, various programmable counters, and a readable 47-bit serial control register) allows for versatility and ease of design.

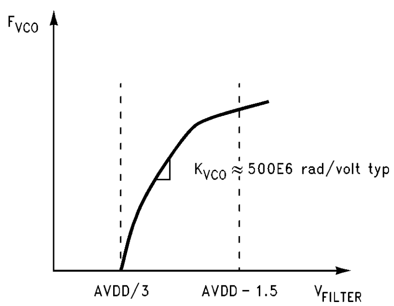
3.1 INTERNAL VCO OPERATION

No external VCO inductor or capacitor components are required for operation, simplifying PC board layout requirements. P counter programmability is contiguous from 1 to 16, although a 50% duty cycle will be created only if the P modulus is an even number, or if the P modulus is 1.

3.1.1 VCO Tuning Characteristics

The CGS410 VCO requires an input voltage to set the proper operating frequency. The input voltage is the direct result of charge sourced or sinked off the LPF network. The function of the LPF is to convert the charge to voltage (see "Loop Filter Characteristics"). The VCO requires the input voltage to be set in the linear portion of the input range. The VCO output frequency is a function of the VCO gain (F_{VCO}) and the range of the input voltage.

Normal, or linear VCO operation will place the input voltage range from AVDD/3 (the lowest frequency response) to approximately AVDD − 1.5V (the highest frequency response). The linear operating range is illustrated in *Figure 3-1* with VCO output frequency (F_{VCO}) expressed as a voltage filter input (V_{FILTER}).



TL/F/11919–3

FIGURE 3-1. Linear Operating Range

Applying an input voltage beyond the intended range will force the VCO to rail high or low. Input voltages which exceed AVDD, or go negative with respect to AGND, can damage the CGS410.

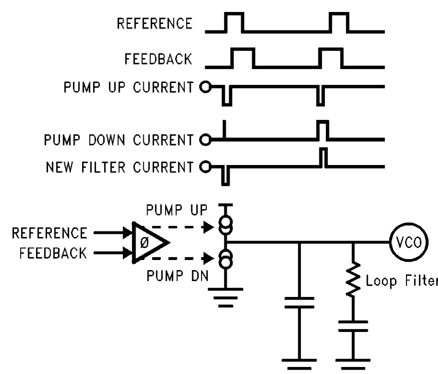
3.2 CRYSTAL OSCILLATOR OPERATION

The XTLIN and XTLOUT pins are used in conjunction with an external crystal, two capacitors, and two resistors to form an external oscillator tank circuit. The crystal should be a fundamental parallel mode type. XTLOUT serves as the driving source to the crystal. Consideration should be given to avoiding crystal overdrive situations. XTLOUT should show an output waveform well within the XVDD and XGND boundary conditions. The elements forming the crystal tank should be low-leakage devices. Capacitor values (per crystal leg) will typically fall within the range of 10 pF–40 pF.

The crystal oscillator divide-by-2 output may be directed to appear at the clock outputs depending on the state of the 3 to 1 MUX. On power up, both differential and CMOS_PCLK outputs will reflect half the oscillator frequency input. The XTLIN pin can be driven from a variety of sources, including ECL, TTL, or CMOS logic. Attach a coupling capacitor into the XTLIN pin when using a TTL or small-signal source (such as ECL). Please see application diagrams for details. The CGS410 may be used to genlock to an external clock source.

3.3 PHASE COMPARATOR OPERATION

The phase comparator compares the difference in clock edges between the internal N and R counter outputs. The difference results as either a charge source (pump-up), or charge sink (pump-down). The amount of charge is directly proportional to the phase difference (see *Figure 3-2*). The phase comparator controls the VCO by comparing the phase of a derived signal from a known accurate reference source such as a crystal or an external reference signal. In genlocking situations, the reference source may be a constant stream of pulses such as an external HSYNC.



TL/F/11919–4

FIGURE 3-2. Phase Comparator/Charge Pump

The VCO-derived signal is divided by N, and applied to one phase comparator input. The R divider output serves as the other phase comparator reference input. The comparator functions as a three-state machine: providing a pump-up state when R leads N, and a pump-down state when N leads R. This situation exists only when there is a difference between the two input edges. The VCO frequency is then increased or decreased in the closed loop system. At all other times, the phase comparator is in a tri-state condition.

The direction and amount of charge on the FILTER pin is proportional to the difference in the phase comparator input edges. The charge flow is made up of correction pulses. The resulting correction pulses are converted to a voltage as dictated by the LPF network. Selection of LPF components characterizes the resulting voltage and phase response.

3.0 Circuit Operation (Continued)

The CGS410 allows the user to select the quantity of charge pump current and its direction. Specifying the direction of charge flow is useful in situations where an external filter and/or VCO is incorporated. See the applications section for an example. In situations where external networks lack the charge sensitivity, the amount of charge can be increased at the user's discretion.

3.4 PROGRAMMABLE DIVIDER OPERATION

The CGS410 has four internal dividers (R, N, P, and L) which are programmed serially via the internal control register.

The R (reference) divider provides a reference frequency from either a crystal or an externally generated clock source. The divisor range is contiguous and varies from 1 to 1023. The modulus selected is the direct binary equivalent loaded in the serial control register at bit locations 24–33.

The internal N divider provides a means of locking the VCO with a constant tuning resolution that is independent of the pixel system. Its contiguous modulus range is 2 to 16383.

The P (postscaling) divider provides a means of generating an output over a wide frequency range from a VCO which has a fixed frequency range. The modulus selections of the P divider range from 1–16 inclusive. The modulus of this divider is programmed with serial control register bits 16–19. The PCLK outputs are square when the P modulus is 1, 2, 4, 6, 8, 10, 12, 14, or 16. If the P modulus is 3, 5, 7, 9, 11, 13, or 15, the PCLK outputs are low one less count than it is high. For example, dividing by modulus 5 would result in three counts high and two counts low.

The L (load) divider provides a means of generating a load clock by dividing the PCLK by a modulus ranging from 1–16 inclusive. The modulus of the load divider is programmed with serial control register bits 20–23. The L clock output is derived from the output of the internal MUX, so whichever output is selected by the mux will be divided by L. The L clock can be asynchronously disabled/enabled by a serial bit. The LCLK outputs are square when the L modulus is 1, 2, 4, 6, 8, 10, 12, 14, or 16. If the L modulus is 3, 5, 7, 9, 11, 13, or 15, the LCLK is high one less count than it is low. For example, dividing by modulus 5 would result in three counts low and two counts high.

After setting the appropriate values of the registers, the CMOS PCLK output frequency can be calculated using the formula below:

$$F_{OUT} = \frac{F_{XTALIN} * N}{R * P}$$

3.5 CONTROL REGISTER OPERATION

The CGS410 serial control register consists of 47 bits, each of which control various internal functions as described later in the section "Structure of the Internal Serial Control Register". All bit locations are RAM based, and are volatile during power cycling operations. The CGS410 contains an internal shadow register which directly reflects that of the serial shift register. The contents of the shadow register program the CGS410 parameters. The shadow register allows the user to write a stream of data to the serial shift register, then, for the last bit do a write followed by a transfer operation. The transferring operation allows all parameters to be loaded into the respective target registers in a single clock cycle. This ensures that changes in clocking parameters take place in a uniform manner.

Read operations are performed in the opposite sequence from that of write. Here, data is transferred from the shadow register to the serial shift register on the first bit, and serially shifted out thereafter.

Performing transfer operations is up to the discretion of the system programmer. In many instances the system may only require partial diagnostic information from the internal registers, and hence avoid a full serial transfer. This is easily accomplished by transferring the data, then shifting only that portion required for the task. The sequence can easily be repeated without adverse affects on the shadow register. Bear in mind that the first data bit written will be the first bit read-out.

3.5.1 System Loading Sequence

All system access to the CGS410 takes place relative to the rising or falling edge of CSB. EN and R_WB must be stable and in the desired state prior to the falling edge of CSB, while data must be present, or sampled by the system CPU during the rising edge of CSB.

Serial write operations consist of setting both ENable and R_WB low for the first N-1 bits. Transfer of serial data to the latch register occurs when writing the N^{th} (last) bit. On the last bit-write bus cycle, set EN high. The CGS410 will shift in the last bit then perform a transfer to the shadow register. Once the transfer takes place the PLL will immediately begin to lock to the new values.

Serial read operations consist of setting ENable low and R_WB high for all bits. However, if the programmer wishes to refresh the data in the serial shift register, a transfer operation is performed when reading the first bit. On the first bit read bus cycle, set EN high. The CGS410 will transfer all data in the shadow resister to the shift register then shift out the first valid data bit. Note that the contents of the shadow register are unchanged by the read transfer with no effect on the CGS410 internal parameters or output clocks.

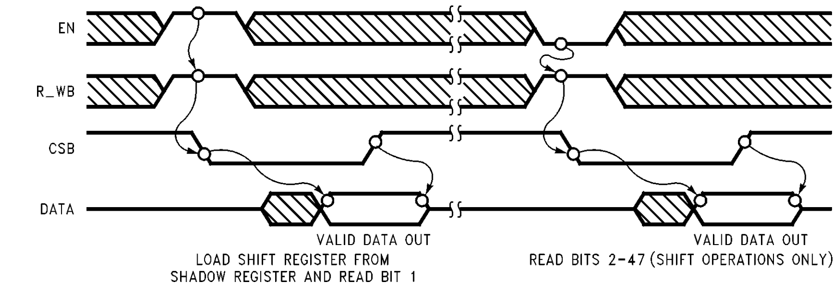
The rest of the serial read operation consists of shifting data bits 2–47. Each bit becomes valid at the DATA pin after CSB goes low and then shifts on the positive edge of CSB.

3.5.2 Structure of the Internal Serial Control Register

The following describes the bit structure of the Control Register. Where applicable, all programmable registers values are loaded with the LSB first.

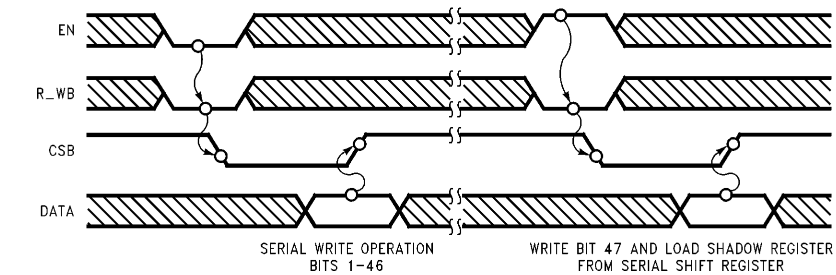
Serial Bit 1

Differential Level control. This bit sets an internal bias level to provide differential "large" (bit 1 high) or "small" (bit 0 low) signal swing. On power-up this bit is low (small signal swing).



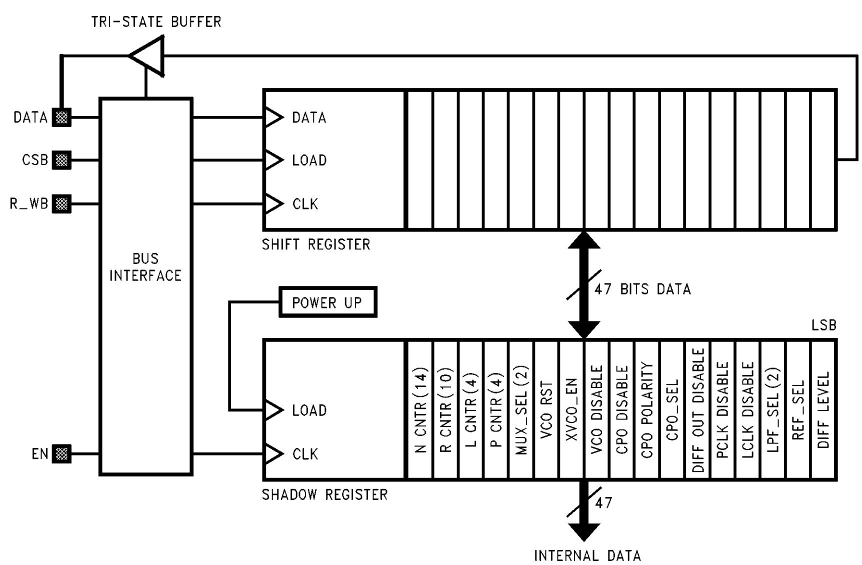
TL/F/11919–5

FIGURE 3-3. Control Register Read Operations



TL/F/11919–6

FIGURE 3-4. Control Register Write Operations



TL/F/11919–7

(Simplified functional representation only)

FIGURE 3-5. Control Register Architecture

3.0 Circuit Operation (Continued)

Serial Bit 2

Reference Select. A logic low configures XTLIN and XTLOUT for crystal mode. A logic high configures for EXTREF. On power-up this bit is low (crystal mode).

Serial Bits 3, 4

Loop Filter Select. LSB is loaded first. Bit values are mapped by the following:

Bit 4	Bit 3	
0	O	External Mode
0	1	500 kHz Reference
1	0	1.5 MHz Reference
1	1	5 MHz Reference

External mode selected on power-up.

Serial Bit 5

Load Clock (LCLK) Disable. A logic low enables LCLK. A logic high freezes the LCLK output low and disables the L counter. Note that this is different from the effects of the L clock enable pin, which is a synchronous disable and which only disables the output (leaving the counter operational). LCLK is enabled on power-up.

Serial Bit 6

PCLK Disable. A logic low enables CMOS_PCLK output. A logic high freezes CMOS_PCLK low. CMOS_PCLK is enabled on power-up.

Serial Bit 7

Differential (DIFF) Out Disable. A logic low enables Differential Output. A logic high causes both differential outputs to be driven below 400 mV. DIFF out is enabled on power-up.

Serial Bit 8

Charge Pump Output (CPO) Select. A logic low forces a 25 μA current pump. A logic high forces a 75 μA current pump. There is a 25 μA current pump on power-up.

Serial Bit 9

Charge Pump Output (CPO) Polarity. A logic low forces a "normal" output response, i.e., the charge pump sinks current when the feedback signal (N counter output) leads the reference signal (R counter output). A logic high forces an inverted response. CPO polarity is in normal mode on power-up.

Serial Bit 10

Charge Pump (CPO) Disable. A logic low enables charge pump activity. A logic high Tri-States CPO activity. CPO is enabled on power-up.

Serial Bit 11

Voltage Controlled Oscillator (VCO) Disable. A logic low enables VCO operation. A logic high disables VCO activity. VCO is enabled on power-up.

Serial Bit 12

External VCO Enable (XVCO_EN). A logic high enables the external VCO path. This bit is disabled on power-up.

Serial Bit 13

Voltage Control Oscillator (VCO) Reset. A logic high resets the VCO. This means that the charge pump output is clamped to AGND to guarantee that the loop filter is discharged. VCO reset is high (enabled) on power-up. A logic low places the VCO in normal operating mode. In order for the PLL to lock, this bit must be returned low after power-up.

Serial Bits 14, 15

Internal clock MUX_SEL. LSB (bit 14) is loaded first. This MUX selects which clock signal is passed to the clock outputs. Bit values are mapped by the following:

Bit 15	Bit 14	
0	0	XTAL/2 Mode
0	1	P Counter Mode
1	0	External Clock Mode (Passthru)
1	1	Not Used

The XTAL/2 mode is selected on power-up.

Serial Bits 16–19

P counter modulus select. LSB bit 16 is loaded first. The P modulus range is 1–16 continuous. Serial bits 16–19 are loaded with the desired modulus value − 1 (i.e., 0–15). P counter divides by modulus 4 on power-up.

Serial Bits 20–23

L counter modulus select. LSB bit 20 is loaded first. The L modulus range is 1–16 continuous. Serial bits 20–23 are loaded with the desired modulus value − 1 (i.e., 0–15). L counter divides by modulus 4 on power-up.

Serial Bits 24–33

R counter modulus. LSB (bit 24) is loaded first. The R counter divides continuously by the binary value loaded. Modulus range is 1–1023 inclusive. R is initialized at 20 on power-up. Loading R = 0 is undefined.

Serial Bits 34–47

N counter modulus. LSB (bit 34) is loaded first. The N counter divides by the binary value loaded. Modulus range is 2–16383 inclusive. N is initialized at 120 on power-up. Loading N = 0 or N = 1 is undefined.

3.5.3 Power-Up Conditions

At power-up the control register bits are set to provide initial operating conditions as follows:

1. All clock outputs are active.
2. The differential PCLK and CMOS_PCLK outputs function at a rate of XTAL/2. The LCLK functions at a rate of XTAL/8.
3. The status of the internal register reflects the following:
   N = 120
   R = 20
   P = 4 (bits 16–19 = 3)
   L = 4 (bits 20–23 = 3)
4. All other programmable bits are low, except VCO_RPST which is set high.

3.0 Circuit Operation (Continued)

Note that with VCO__PST high, the charge pump output voltage is clamped to AGND. This condition will prevent the PLL from locking. *Proper VCO lock operation will require the user to reset this bit*.

3.6 LOOP FILTER CHARACTERISTICS

The function of the low pass filter (LPF) is to transform the CPO charge output into a DC voltage seen on the VCO input. A variety of LPF configurations exist. This particular architecture is suited towards a C/RC type of configuration. *Figure 3-7* shows such an architecture. The desired Bode plot of gain and phase is shown in *Figure 3-6* with 20 dB/decade slope at ω_o for stability at unity gain.

Capacitor C_2 governs the PLL's ability to reject instantaneous bit jitter. This represents the high frequency pole. R_1 and C_1 determine the low frequency zero. When R_1, C_1 and C_2 values are properly calculated, ω_o will fall in the −20 dB/decade flattened response and will help track out the 1/f noise inherent in the VCO. An added benefit is that the LPF phase response is symmetrical at this frequency. Increasing or decreasing C_2 will move the high frequency pole up or down, likewise with the R_1 and C_1 combination. Converging and expanding the pole pairs will result in a underdamped or overdamped filter. Resistive component R_1 directiy affects this response.

Loop filter components can vary somewhat to conform to the given application requirements. Underdamping the loop response causes decreased loop stability (ultimately resulting in loop oscillation), but will decrease lock time, an advantage in applications where lock time is critical. On the other hand, overdamping the filter response leads to decreased phase noise while increasing the loop lock time.

Generally, setting C_2 at 1/10th to 1/50th the value of C_1 will provide reasonable loop response.

Selecting the appropriate loop filter depends on the frequency at the phase comparator. The most effective filtering ranges for the three internal filters are:

Loop Filter 1: 0.3 MHz–1.0 MHz ($80 < N < 500$)

Loop Filter 2: 1.0 MHz–3.0 MHz ($30 < N < 80$)

Loop FIlter 3: 3.0 MHz–6.0 MHz ($15 < N < 30$)

Best performance (lowest phase noise) is obtained by programming F_{REF} to fall somewhere in the middle of any of these frequency ranges.

3.6.1 Loop Filter Calculations

Several constraints need to be known in order to determine the external loop filter components for external loop filter operation: the loop divide ratio (N), the phase comparator gain (K_p), the VCO gain (K_o) the loop bandwidth (ω_o), and the phase margin (F).

The constants for the CGS410 are as follows:

K_o = 500E6 rad/v

K_p = 4 μA/rad when CPO SEL (bit 8) = 0
12 μA/rad when CPO SEL (bit 8) = 1

The variable parameters for the CGS410 are as follows:

N = N counter modulus

R = R counter modulus

f_{XTAL} = frequency at XTLIN pin (in Hz)

N is equal to the VCO frequency divided by the frequency input at F_{REF}. The loop bandwidth (ω_o) is recommended to be about 1/30th of the F_{REF} frequency (times 2π radians). Most users will find the following set of equations give good loop filter values for frequency synthesis applications:

$R_1 = (0.23 \bullet N \bullet f_{XTAL})/(K_p \bullet K_o \bullet R)$

$C_1 = (68.4 \bullet K_p \bullet K_o \bullet R^2)/(N \bullet f_{XTAL}{}^2)$

$C_2 = C_1/20$

The following equations can be used for different cutoff frequencies and phase margins.

For F = 57 degrees phase margin:

$R_1 = (1.1 \bullet N \bullet \omega_o)/(K_p \bullet K_o)$

$C_1 = (3 \bullet K_p \bullet K_o)/(N \bullet \omega_o{}^2)$

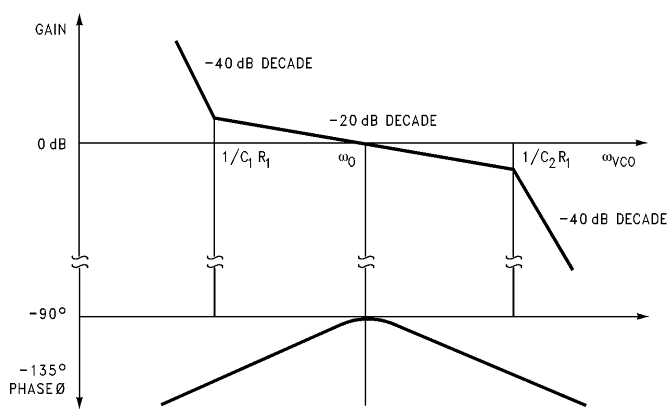
$C_2 = (0.15 \bullet K_p \bullet K_o)/(N \bullet \omega_o{}^2)$ (1/20th C_1 value)

For a phase margin other than 57 degrees:

$R_1 = (\text{Cosec F} + 1) \bullet (N \bullet \omega_o)/(2 \bullet K_p \bullet K_o)$

$C_1 = (\text{Tan F}) \bullet (2 \bullet K_p \bullet K_o)/(N \bullet \omega_o{}^2)$

$C_2 = (\text{Sec F} - \text{Tan F}) \bullet (K_p \bullet K_o)/(N \bullet \omega_o{}^2)$

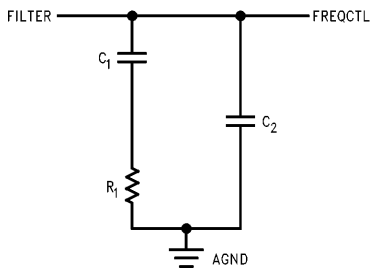


TL/F/11919–8

FIGURE 3-6. Bode Plot of Loop Filter Response

3.0 Circuit Operation (Continued)

The values R_1, C_1 and C_2 refer to the following filter configuration:



TL/F/11919–9

FIGURE 3-7. External Low Pass Filter

The above equations refer to the low pass filter loop response associated with a single phase comparator reference frequency. In many situations the CGS410 will be required to generate many output frequencies. Best performance is obtained by matching the filter to the required frequency. This may require different LPF component values for each configuration. In most instances, selection of any of the CGS410's three internal filters will satisfy the LPF requirements. A fourth option allows the use of an external configuration.

When generating a wide range of output frequencies, a phase margin of approximately 60 degrees should be maintained for a theoretically stable system. In practice, wide variation is possible. Note that the equations expressed above are functions of only N, ω_o, K_p and K_o. PCLK output frequency is NOT included. Since the CGS410 allows the use of an external loop filter as well as three internal filters, there should always exist a configuration of counter values that will produce a quality clock output without the need to externally switch loop filter values.

3.7 CLOCK DEGLITCHING CONSIDERATIONS

The CGS410's automatic deglitching function ensures that the clock output pulse width will be no shorter than the briefest clock high or low time currently programmed. Deglitching the clock outputs allows the system to maintain proper state throughout the clock change cycle.

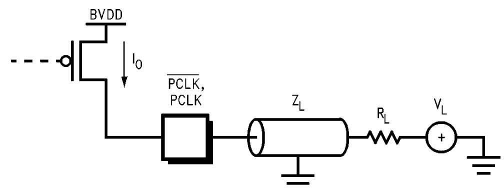
When the user loads the shadow register with a code that changes the state of serial bits 14 through 19 (the P counter modulus or the internal clock MUX select), the deglitching process is automatically initiated. The PCLK outputs are temporarily frozen and then are restarted several PCLK periods later synchronous to the new output frequency.

3.8 CONFIGURABLE DIFFERENTIAL OUTPUT BUFFERS

For proper operation, a 10:1 resistive relationship will exist between the DIFF__VOH/VOL pin loads and the PCLK differential loads. Adhering to this relationship will provide the correct voltage drive at the PCLK differential outputs.

3.9 TERMINATION CONSIDERATIONS

Each differential PCLK output serves as a current source to a resistive termination network. The termination network matches the characteristic impedance as seen by the PCLK system trace. Proper network component selection also biases the differential output stage to maintain the proper V_{OH} and V_{OL} values. The most common network uses a resistive pull-up/pull-down combination (see *Figure 3-9*). The combination of the resistive devices provides a DC Thevenin equivalent with a specified voltage output and load resistance.



TL/F/11919–10

FIGURE 3-8. Termimation

Figure 3-8 illustrates the electrical model for driving the differential PCLK outputs down a transmission line. It terminates in a Thevenin equivalent consisting of a resistance (R_L) and a source voltage (V_L). Modulating the output driver gate modulates the output PMOS source current (I_O). The combination of source current and load resistance results in an output voltage. For properly terminated systems, the characteristic impedance of the signal line (Z_L) should closely approximate the effective R_L. When using a Thevenin equivalent circuit (see *Figure 3-8*), the effective R_L is described as the open circuit voltage divided by the short circuit current:

$$R_L = V_{OC}/I_{SC} = (R_1 \bullet R_2)/(R_1 + R_2)$$

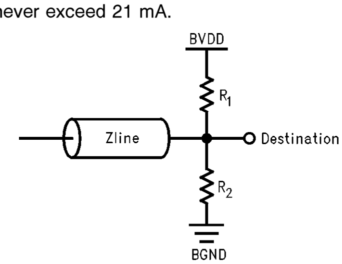
In addition to maintaining the proper resistance, the resistors must be selected to provide the proper V_L for the circuit. The resistors should be selected such that V_{OL} can be reached. V_{OL} is the most important parameter. The following rule will apply:

$VL < V_{OL}$, where typically V_L = is 150 mV–500 mV below the V_{OL}.

V_L is calculated as the open circuit voltage:

$$V_L = V_{OC} = BVDD \bullet R_2/(R_1 + R_2)$$

In all the equations, the output PMOS source current (I_O) should never exceed 21 mA.



TL/F/11919–11

FIGURE 3-9. Pull-Up/Pull-Down DC Termination

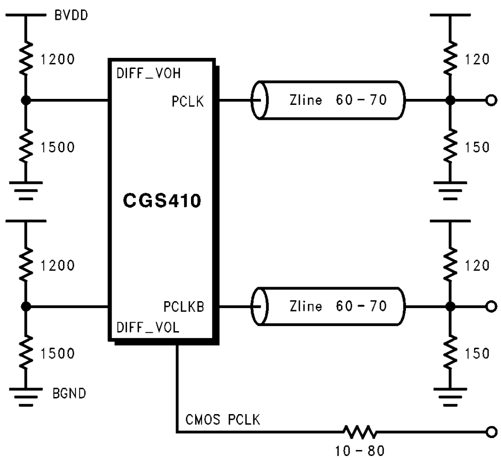
Figure 3-10 illustrates a typical termination that will assume the V_{OH} and V_{OL} requirements are met without overdriving the CGS410 outputs. The value of V_{OL} must meet the requirements of the destination device. For positive ECL logic,

3.0 Circuit Operation (Continued)

the resistive termination is normally set to provide a voltage of 3V. This is readily accomplished with $R_1 = 220$ and $R_2 = 330$. With the control register differential level (bit 1) equal to 0, the output V_{OL} = BVDD * 0.642V or 3.21V at BVDD = 5V. The V_{OH} is typically BVDD * 0.824V or 4.12V at BVDD = 5V. In this example,

$$\begin{aligned} I_{O(MAX)} &= (V_{OH} - V_L)/R_L \\ &= (4.12 - 3)/132 \\ &= 9.5 \text{ mA} \end{aligned}$$

Generation of V_{OH} requires the maximum I_O. Since the CGS410 can provide up to 21 mA of output source for V_{OH}, this is well within driving specifications.



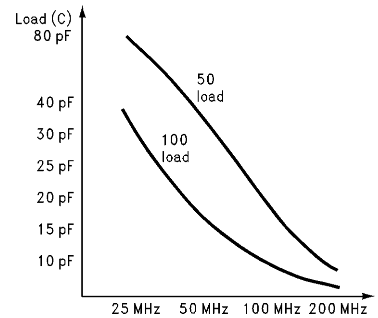
TL/F/11919–12

FIGURE 3-10. Typical Termination (Bit 1 = 0)

Other factors which influence the differential output response include the characteristic impedance of the line (Z_L) and capacitive loads. The characteristic impedance of the "stripline" connecting the CGS410 output to the destination device input should match the Thevenin equivalent of the line termination to assure maximum power transfer, glitch-free clock outputs and reduced EMI.

Capacitive loading will affect the rise and fall times of the output waveform. The current required is: i C V/T.

Figure 3-11 indicates typical loading parameters used for driving differential output capacitive loads for frequencies from 25 MHz to 200 MHz with a 1V differential voltage swing. In addition, the resulting graph bases the voltage slew rate (v/t) for 1/10 of the operating frequency period. The graph illustrates the fact that as the output frequency and capacitance increase, the amount of source current must also increase to maintain reasonable slew rates.



TL/F/11919–13

FIGURE 3-11. PCLK/PCLKB Load vs. Frequency

CMOS_PCLK drive requirements vary greatly from those of the PCLK differential counterparts because the output buffer size and the output impedance are higher. Best performance is usually obtained by placing a series resistor on the output and then driving to the receiving device. Selection of the resistor is best obtained on an empirical basis. Normally, resistor sizes starting in the 10Ω–80Ω range provide a good start. *Figure 3-10* shows a typical termination scheme for 60–70 board impedance.

3.10 SYSTEM INTERFACE CONSIDERATIONS

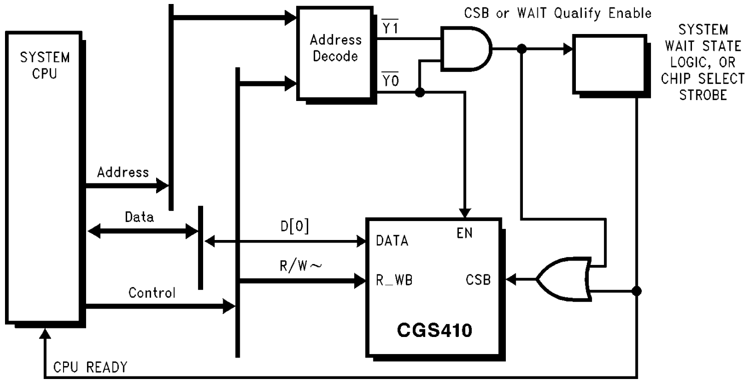
The CGS410 data bus can be managed by a wide variety of controllers. If a serial data source is not available from the controller, external serializing circuitry, or slight bus modification may be required.

Figure 3-12 illustrates a generic hardware system implementation where the CGS410 control signals are qualified through a memory map. In this example, the CGS410 is mapped into two address locations. This particular mapping scheme allows:

1) typical read/write operations to execute through one mapped port,
2) transfer operations to execute through the second mapped port (see Figure 3-12).

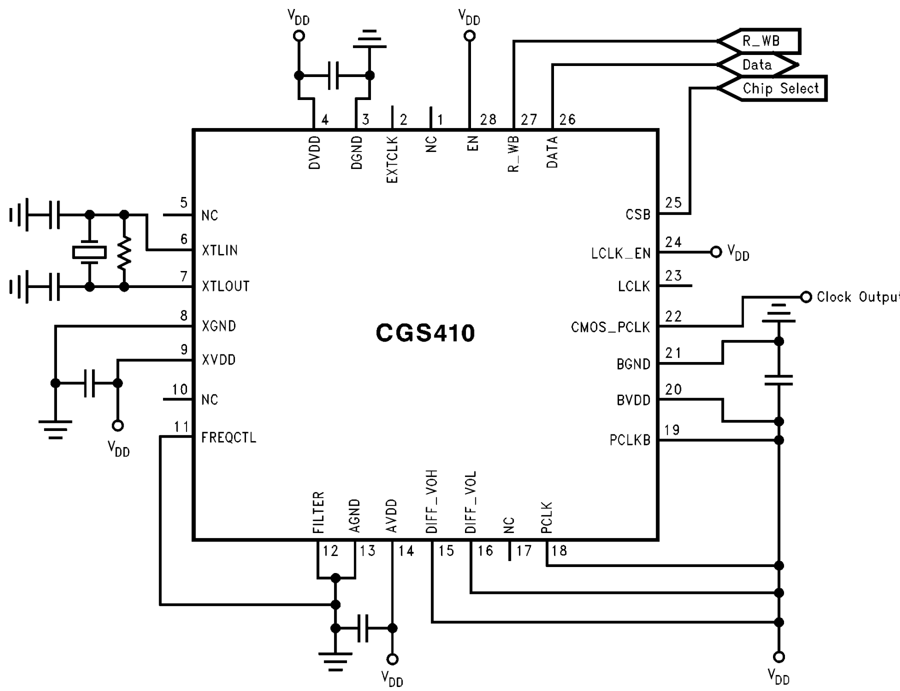
Depending on the system configuration, CGS410 control signals such as R_WB may be connected directiy to a qualified CPU strobe R/W~. In this example, the system bus data line zero D[0] serves as the DATA port of the CGS410. The control signal EN may be derived from address decode select logic, and can maintain any state during non-CGS410 accesses.

The control signal CSB requires the greatest attention because it is the CGS410's clocking agent. Care must be taken to ensure that no activity takes place on this input during non-CGS410 accesses. Note that when this input is strobed, all control and data present at the CGS410 must conform to the respective rising and falling edges of this signal as specified in the timing diagrams in this data sheet. CSB may be generated from a variety of system sources. A qualified CPU WAIT may serve as one source. Other timing requirements may need a timing generator (such as a two-state machine) to generate CSB.



TL/F/11919-14

FIGURE 3-12. Serial Interface Example



TL/F/11919-15

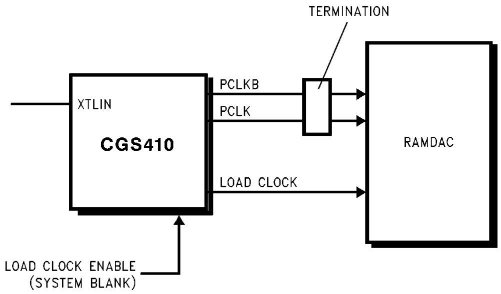
FIGURE 3-13. Minimum Cost, <80 MHz CGS410 Implementation

3.11 APPLICATIONS

Many applications exist which can use the synthesized clock capability of the CGS410. Because of the CMOS nature of the device, it can maintain high frequency clock rates while consuming little current. This allows use of the CGS410 in battery powered systems.

Application requirements for the CGS410 are largely dictated by the user. *Figure 3-13* illustrates a low cost implementation. Pulling the PCLK outputs to BVDD will turn the outputs off. In this configuration, DIFF__VOH and DIFF__VOL are also tied to BVDD. CMOS__PCLK serves as the frequency output source. Note also that all LCLK, EXTCLK, FILTER and crystal functions can be modified to address the needs of the application.

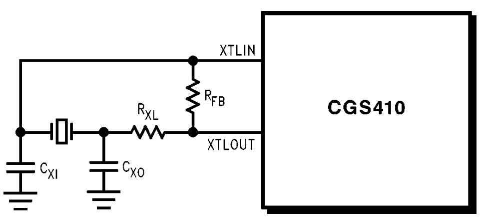
Figure 3-14 shows the common clock drive requirements for a video-based system. The CGS410 provides all clocking sources. LCLK provides a synchronized low-frequency submultiple of PCLK for driving the RAMDAC load data requirements. In addition, LCLK can easily be used to drive the respective frame buffer array which clocks the display data. The Load Clock Enable (LCLK__EN) can be used to disable load clock pulses during screen blanking intervals.



TL/F/11919–16

FIGURE 3-14. Common Video Application

Figure 3-15 shows the Pierce Oscillator configuration when using an external crystal. The feedback resistor placed between XTLIN and XTLOUT biases the input. The additional resistor in the diagram serves to limit the amount of power dissipated by the crystal. This value is based upon crystal drive specifications. In most circumstances this resistor is not required. The two capacitors off the crystal leg serve to form the crystal tank. These components, combined with the electrical function of the crystal, form the additional 180 degree phase shift required for oscillation.



TL/F/11919–18

FIGURE 3-15. Crystal Configuration

Component values depend on the crystal manufacturer specifications. C_{XI} and C_{XO} will typically range from 10 pF to 30 pF. Resistor R_{XL} limits the amount of current flow into the external crystal tank R_{XL} is usually between 100Ω and 600Ω. In many instances this component may be eliminated. The feedback resistor (R_{FB}) biases the internal inverter so proper oscillation can take place. Recommended values are from 10k to 100k.

In systems where the lowest possible phase noise is required, a high-Q, external VCO may be implemented. An example is illustrated in *Figure 3-16.* Here the CGS410 provides the phase comparison, the first stage charge pump output, and the user programmable divider circuitry. In these types of configurations, EXTCLK can be driven with a small sinusoidal input. EXTCLK is capacitively coupled, while the VCO is DC terminated. An external OP-AMP such as National Semiconductor's LM324 provides the additional VCO voltage input range required. In this example, the OP-AMP is biased by the resistor divider. In most instances, the voltage present on the OP-AMP "+" input is half the OP-AMP source voltage. The OP-AMP feedback consists of a C/RC network which provides the voltage input characteristics of the VCO.

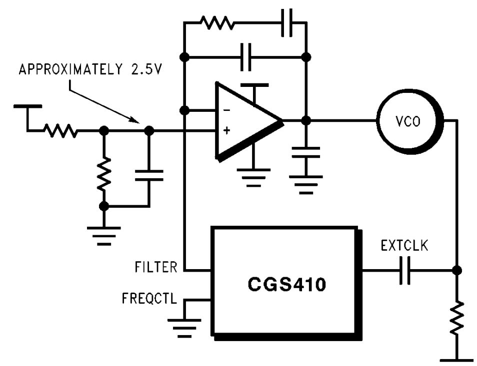


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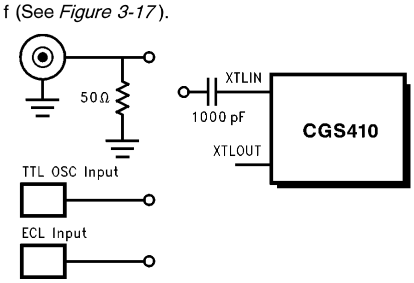
FIGURE 3-16. CGS410 Using an External Loop Filter and VCO

The designer may drive the CGS410 XTLIN in a variety of configurations. In most instances XTLIN is capacitively coupled to remove any DC effects from the source. Typical capacitor values will vary depending on the frequency and desired waveform at the XTLIN input. In most instances this value ranges from several hundred pF up to approximately 0.01f (See *Figure 3-17*).



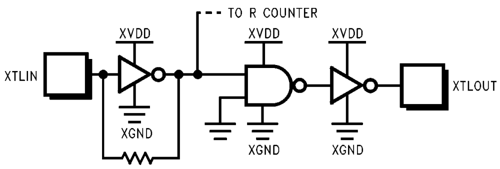
TL/F/11919–20

FIGURE 3-17. External XTLIN Drive Options

3.0 Circuit Operation (Continued)

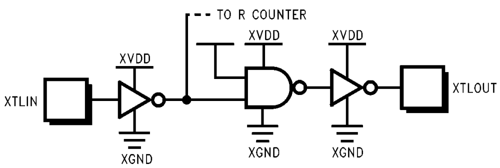
3.12 INPUT/OUTPUT STRUCTURES

XTLIN/XTLOUT
(REF__SEL = 1)

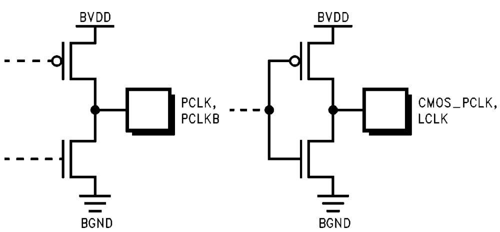


TL/F/11919–21

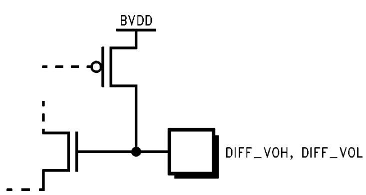
XTLIN/XTLOUT
(REF__SEL = 0)



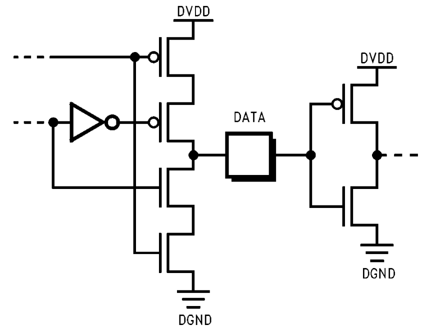
TL/F/11919–22



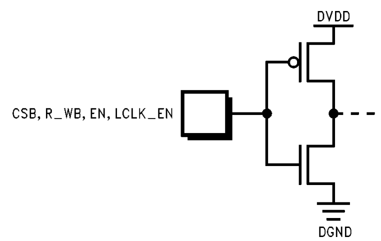
TL/F/11919–23



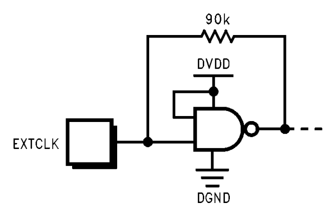
TL/F/11919–24



TL/F/11919–25



TL/F/11919–26



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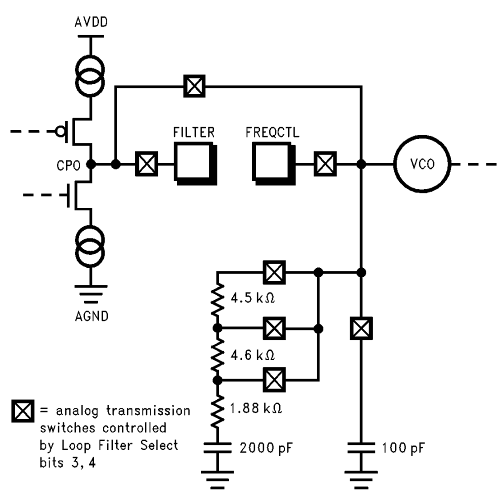


TL/F/11919–28

4.0 Device Specifications

4.1 ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +6.3V
DC Input Voltage (V_{IN})	−1.5V to V_{DD} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{DD} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	+20 mA
DC Output Current, per pin (I_{DD})	+35 mA
DC V_{DD} or GND Current, per Pin (I_{DD})	+70 mA
Storage Temperature Range (T_{STG})	−165°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
Typical θ_{JA} 0 LFM	50°C/W
225 LFM	36°C/W
500 LFM	30°C/W
900 LFM	29°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

4.2 RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
Supply Voltage (V_{DD})	4.75	5.25	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{DD}	V
Operating Temperature Range (T_A)	0	70	°C
VCO Frequency (f_{VCO})	65	135	MHz
Crystal Frequency (f_{XTL}) (Note 3)		35	MHz
Differential PCLK Frequency (f_{PCLK})		135	MHz
CMOS PCLK Frequency (f_{CMOS})		65	MHz
LCLK Frequency (f_{LCLK})		65	MHz

Note 3: Crystal should be parallel mode, fundamental type. This specification also applies to externally driven references.

4.3 DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, unless otherwise specified

Symbol	Parameter	Pin Name	Conditions	Min	Typ	Max	Units
V_{IH}	Minimum High Level Input Voltage	CSB, EXTCLK, DATA, EN, LCLK__EN, R__WB		2.0			V
		XTLIN	XVDD = 5.0V	3.5			V
V_{IL}	Minimum Low Level Input Voltage	CSB, EXTCLK, DATA, EN, LCLK__EN, R__WB				0.8	V
		XTLIN	XVDD = 5.0V			1.5	V
V_{OH}	Minimum High Level Output Voltage	DIFF V_{OH}	DIFF Level Bit = 0(1)		BVDD • 0.824		V
			DIFF Level Bit = 1(1)		BVDD • 0.825		V
		XTLOUT	I_{OH} = −400 μA	XVDD − 0.3			V
		DATA	I_{OH} = 6 mA	DVDD − 0.5			V
		CMOS__PCLK, LCLK	I_{OH} = 2 mA	BVDD − 0.3			V
V_{OL}	Maximum Low Level Output Voltage	DIFF__V_{OL}	DIFF Level Bit = 0(1)		BVDD • 0.642		V
			DIFF Level Bit = 1(2)		BVDD • 0.490		V
		XTLOUT	I_{OL} = 400 μA			0.3	V
		DATA	I_{OL} = 6 mA			0.5	V
		CMOS__PCLK, LCLK	I_{OL} = 2 mA			0.3	V
$V_{O(DIFF)}$	Output Voltage Swing PCLK, PCLKB		DIFF Level Bit = 0(3)		0.900		V
			DIFF Level Bit = 1(3)		1.650		V
I_{IN}	Maximum Input Current	CSB, DATA, EN, LCLK__EN, R__WB	V_{IN} = V_{DD} or GND, V_{IH} or V_{IL}			10	μA
		EXTCLK			100		μA
		XTLIN, FREQCTL	REF__SEL = 0		0.1	1.0	μA
I_{OZ}	Maximum Output TRI-STATE® Leakage Current	FILTER			0.1	1.0	μA
I_{SOURCE}	Charge Pump Source Current	FILTER	CPO__SEL = 0(4)	−15	−25	−35	μA
			CPO__SEL = 1(4)	−50	−75	−120	μA

4.0 Device Specifications (Continued)

4.3 DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, unless otherwise specified (Continued)

Symbol	Parameter	Pin Name	Conditions	Min	Typ	Max	Units
I_{SINK}	Charge Pump Sink Current	FILTER	CPO_SEL = 0(4)	15	25	35	μA
			CPO_SEL = 1(4)	50	75	120	μA
I_{DD}	Maximum Supply Current	DVDD, BVDD, XVDD, and AVDD	V_{DD} = 5.25V(5)		45		mA

Note 1: 50 Load to BVDD − 2V

Note 2: 50 Load to BVDD − 3V

Note 3: BVDD = 5.0V

Note 4: AVDD = 5.0V

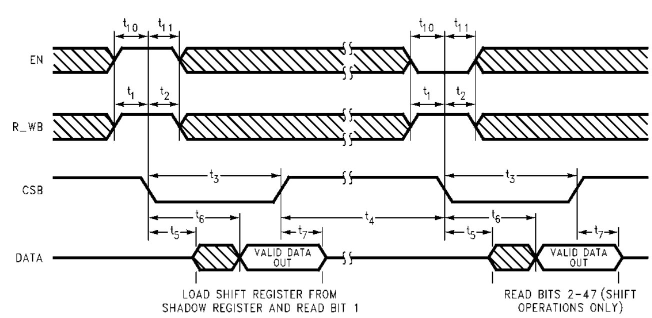
Note 5: PCLK and PCLKB terminated with 50 to BVDD − 2V
DIFF_VOH and DIFF_VOL terminated with 500 to BVDD − 2V
DIFF Level (Bit 0) = 0

4.4 AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_1	R_WB Setup to CSB Falling Edge		0			ns
t_2	R_WB Hold from CSB Falling Edge		10			ns
t_3	CSB low time (while writing data)		TBD	10		ns
t_4	CSB high time (while writing data)		TBD	10		ns
t_5	CSB asserted to Read Data Bus Driven (Note 1)		8			ns
t_6	CSB Asserted to Valid Read Data (Note 1)				40	ns
t_7	CSB Negated to Read Data TRI-STATE				15	ns
t_8	Write Data Setup to CSB Rising Edge		15			ns
t_9	Write Data hold from CSB rising edge		0			ns
t_{10}	EN Setup to CSB Falling Edge		0			ns
t_{11}	EN Hold from CSB Falling Edge		10			ns
t_{12}	LCLK_EN Setup to LCLK Rising Edge			6		ns
t_{13}	LCLK_EN Hold from LCLK Rising Edge			−4		ns
t_{14}	Skew from CMOS PLCK Rising Edge to LCLK Rising Edge			4		ns
t_{15}	Skew from CMOS PLCK Rising Edge to LCLK Falling Edge			5		ns
t_{16}	Skew from DIFF PCLK Rising Edge to LCLK Rising Edge			3		ns
t_{17}	Skew from DIFF PCLK rising edge to LCLK falling edge			4		ns

Note 1: C_L = 50 pF on DATA pin.

4.5 TIMING ISSUES

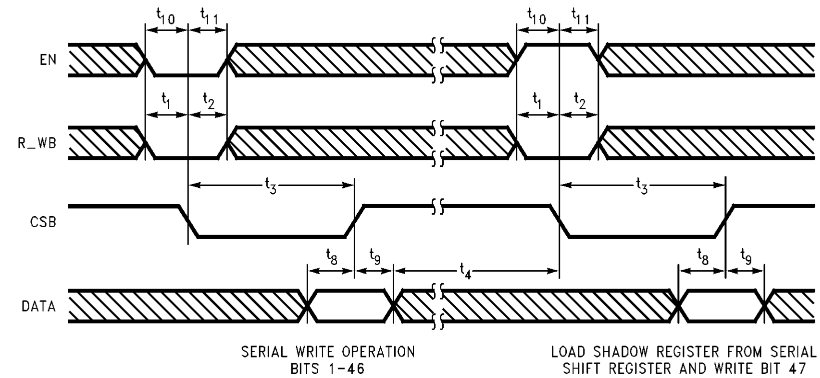


TL/F/11919–29

Note: In the system read cycle EN, R_WB and CSB are measured at 1.3V threshold voltage. DATA is a CMOS compatible output.

FIGURE 4-1. System Read Timing Specification

4.0 Device Specifications



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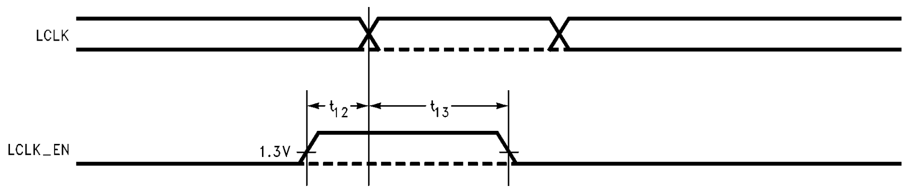
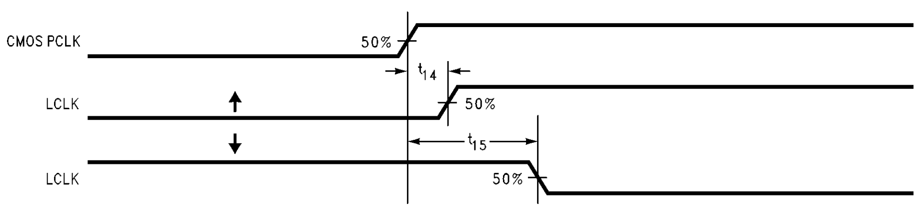
Note: In the system write cycle EN, R__WB and CSB are measured at 1.3V threshold voltage. DATA is a TTL compatible input.

FIGURE 4-2. System Write Timing Specification



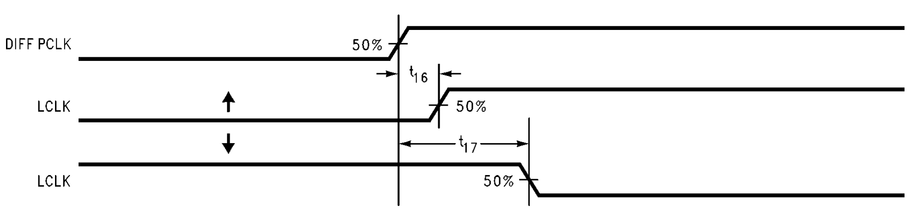
TL/F/11919–31

FIGURE 4-3. LCLK__EN Timing Specification



TL/F/11919–32

FIGURE 4-4. CMOS PCLK Output Skew Timing Specification



TL/F/11919–33

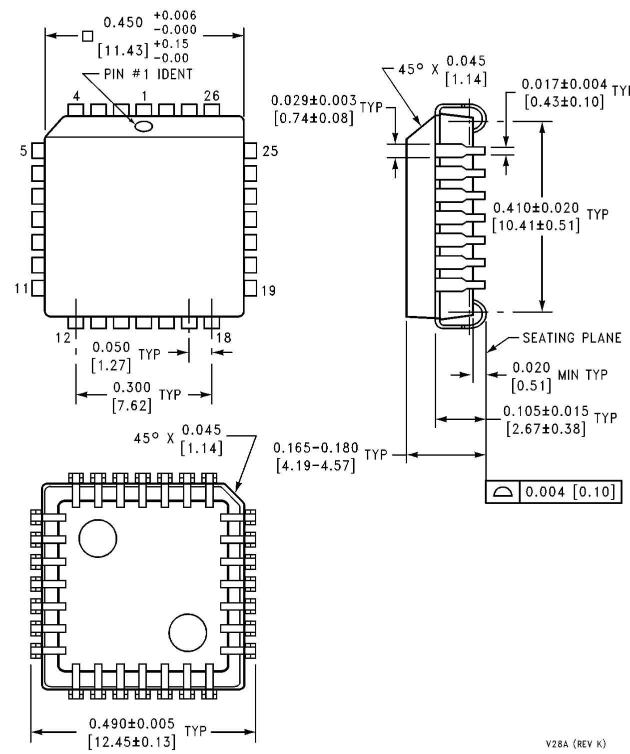
FIGURE 4-5. DIFF PCLK Output Skew Timing Specification

Ordering Information (Contact NSC Marketing for specific date of availability)

CGS 410 T V

- Family — CGS: Clock Generation and Support
- Device Type — 410
- Operating Temperature Range — T: Blank = Commercial, T = Industrial
- Packaging — V: V = PCC

Physical Dimensions inches (millimeters)



28-Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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