National Semiconductor

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CGS701AV
Commercial Low Skew PLL 1 to 8 CMOS Clock Driver
CGS701ATV
Industrial Low Skew PLL 1 to 8 CMOS Clock Driver

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CGS701ATV Industrial Low Skew PLL 1 to 8 CMOS Clock Driver

General Description

CGS701A is an off the shelf clock driver specifically designed for today's high speed designs. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from a 25 MHz–40 MHz crystal oscillator.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

The device includes a TRI-STATE® control pin to disable the outputs. This feature allows for low frequency functional testing and debugging.

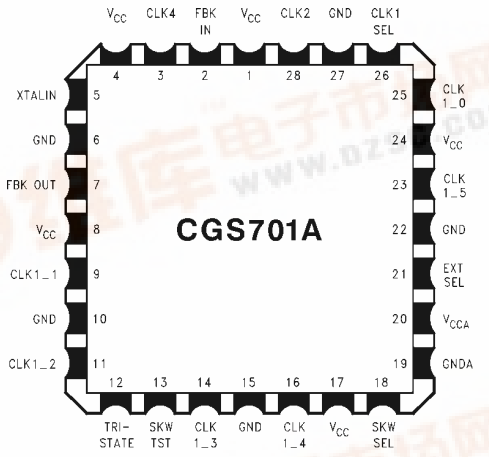
Also included, is an EXTSEL pin to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock__MUX to change its input from the output of the VCO and Counter to the external clock signal provided via SKWTST input pin. (continued)

Features

- Guaranteed: 400 ps pin-to-pin skew (t_{OSHL} and t_{OSLH}) on 1X outputs.
- Pentium® and PowerPC™ compatible
- ±300 ps propagation delay
- Output buffer of eight drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multifrequency bus applications
- Selectable output frequency
- Internal loop filter to reduce noise and jitter
- Separate analog and digital V_{CC} and ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive: +30/−30 mA I_{OL}/I_{OH}
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Guaranteed 2k volts ESD protection

Connection Diagram

Pin Assignment for PLCC



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Pin Description

PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	FBK IN	Feedback Input Pin
3	CLK4	4X Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	FBK OUT	Feedback Output Pin
8	V_{CC}	Digital V_{CC}
9	CLK1__1	1X Clock Output
10	GND	Digital Ground
11	CLK1__2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1__3	1X Clock Output
15	GND	Digital Ground
16	CLK1__4	1X Clock Output
17	V_{CC}	Digital V_{CC}
18	SKWSEL	Skew Test Selector Pin
19	GNDA	Analog Ground
20	V_{CCA}	Analog V_{CC}
21	EXTSEL	External Clock MUX Selector
22	GND	Digital Ground
23	CLK1__5	1X Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1__0	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

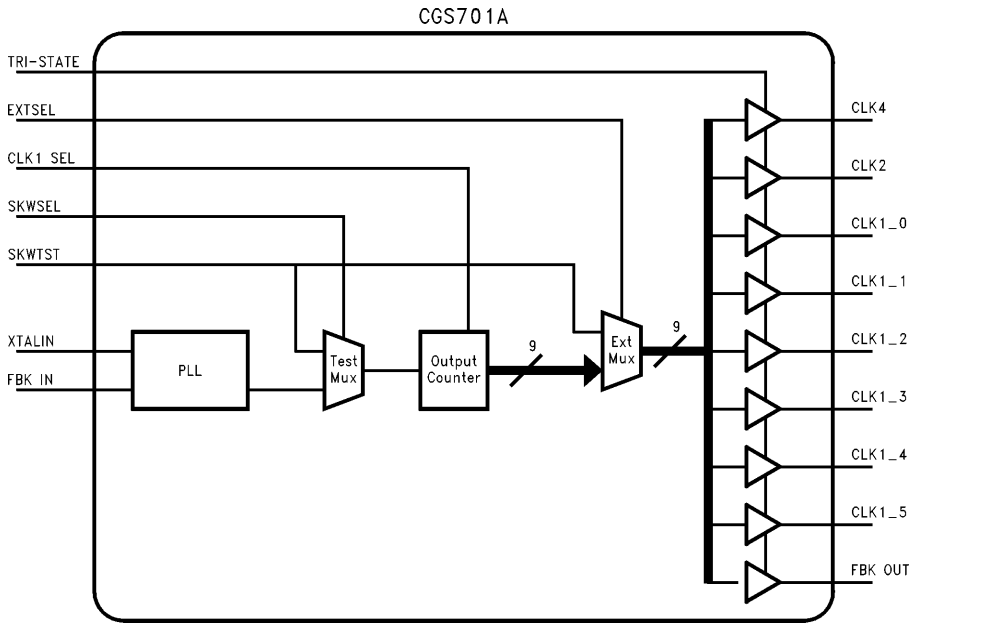
General Description (Continued)

CLK1SEL pin changes the output frequency of the CLK1__0 thru CLK1__5 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.

Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

In addition, another pin is added for increasing the test capability. SKWSEL pin allows testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is 1/2 and CLK1 frequencies are 1/4 respectively (refer to the Truth Table). In addition CLK1SEL functionality is also true under this test condition.

Block Diagram



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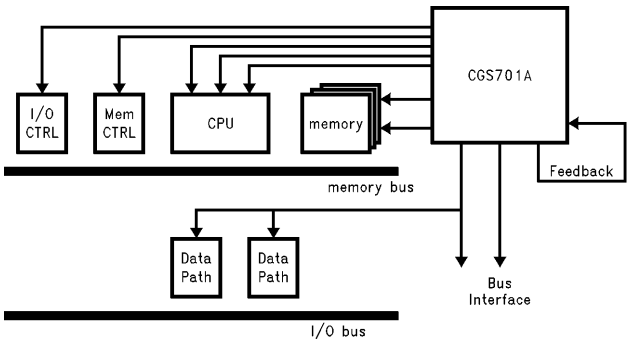
Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
*H	L	X	L	X	H	4 x f in	2 x f in	f in
*L	L	X	L	X	H	4 x f in	2 x f in	2 x f in
X	H	⎍	X	X	H	⎍	⎍	⎍
H	L	X	H	⎍	H	1 x f tst	½ x f tst	¼ x f tst
L	L	X	H	⎍	H	1 x f tst	½ x f tst	½ x f tst
X	X	X	X	X	L	Z	Z	Z

*Steady state phase, frequency lock

Typical Application



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Absolute Maximum Ratings (Note A)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±60 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note B)	1400 mW

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Frequency	25 MHz–40 MHz
Operating Temperature (T_A) SKWTST	0°C to +70°C
External Clock Frequency (Pin)	1 MHz–10 MHz
XTALIN Duty Cycle Range	25/75 (75/25)%
Input Rise and Fall Times (0.8V to 2.0V)	
XTALIN (Pin 5)	5 ns max
All Other Inputs	10 ns max

Typical θ_{JA}	LFM	°C/W
	0	54
	225	45
	500	38
	900	34

Note A: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note B: Power dissipation is calculated using 49°C/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed at 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1 being at 66 MHz. In addition, the ambient temperature is assumed 70°C.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	$V_{CC} = 4.5V–5.5V$, $T = 0°C$ to $70°C$			Units	Conditions
		Min	Typ	Max		
V_{IH}	Minimum Input High Level Voltage	2.0			V	
V_{IL}	Maximum Input Low Level Voltage			0.8	V	
V_{OH}	Minimum Output High Level Voltage	$V_{CC} - 0.1$			V	$I_{OUT} = -50\ \mu A$
		$V_{CC} - 0.6$				$I_{OH} = -30$ mA
V_{OL}	Maximum Output Low Level Voltage			0.1	V	$I_{OUT} = 50\ \mu A$
				0.6		$I_{OL} = 30$ mA
I_{OHD}	High Level Output Current	−50	−110	−170	mA	$V_{OH} = V_{CC} - 1.0V$
I_{OLD}	Low Level Output Current	50	110	170	mA	$V_{OL} = 1.0V$
I_{IN}	Leakage Current	−50		50	μA	$V_{IN} = 0.4V$ or $4.6V$
$I_{OZL/H}$	Output Leakage Current					
C_{IN}	Input Capacitance			10.0	pF	
I_{CC}	Quiescent digital + analog Current (No Load)		3.0	5.0	mA	$V_{IN} = V_{CC}$, GND
I_{CCT}	I_{CC} per TTL Input			2.5		$V_{IN} = V_{CC} - 2.1$, GND

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter				V_{CC} = 4.5V–5.5V F_{IN} = 25 to 40 MHz T = 0°C to +70°C C_L = Circuit 1 R_L = Circuit 1			Units	Notes
					Min	Typ	Max		
t_{rise}	Output Rise	CLK4 CLK2 CLK1	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V				2.0	ns	(Note 1, 7)
		All	0.8V to 2.0V				1.5		
t_{fall}	Output Fall	CLK4 CLK2 CLK1	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V				2.0	ns	(Note 1, 7)
		All	0.8V to 2.0V				1.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew		+ to + Edges + to + Edges + to + Edges	CLK1__CLK1 CLK1__CLK4 CLK2__CLK4			400 1000 1000	ps	(Note 2, 7)
t_{LOCK}	Time to Lock the Output to the Synch Input					20	100	μs	
t_{CYCLE}	Output Duty Cycle			CLK1 Outputs CLK2 Output CLK4 Output	49 49 35		51 51 65	%	(Note 3, 7)
J_{LT}	Output Jitter (Long Term)						0.3	ns	(Note 4, 7)
t_{PD}	Propogation Delay from XTALIN to FBKOUT				−0.3		+0.3	ns	(Notes 2, 4, 5, 6, 7)
F_{MIN}	Minimum XTALIN Frequency						15	MHz	
F_{MAX}	Maximum XTALIN Frequency						43	MHz	

Note 1: t_{rise} and t_{fall} parameters are measured at the pin of the device.

Note 2: Skew is measured at 50% of V_{CC} for CLK1 and CLK2 while it is being measured at 1.4V for CLK4. Limits are guaranteed by design.

Note 3: Output duty cycle is measured at $V_{DD}/2$ for CLK1 and CLK2 while it is being measured at 1.4V for CLK4. Limits are guaranteed by design.

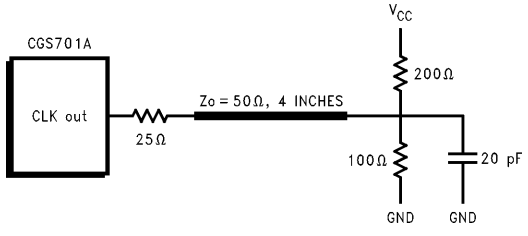
Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge over 1000 cycles. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 3* for further explanation.

Note 5: Measured from the ref. input to any output pin. The length of the feedback and XTALIN traces will impact this delay time.

Note 6: This parameter includes pin-to-pin skew, longterm jitter over 1000 cycles, part-to-part variation as well as propagation delay thru the device.

Note 7: The GNDA pins of the 701 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the V_{CCA} pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for the V_{CCA} pin.

Circuit 1. Test Circuit



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AC Electrical Characteristics (Continued)

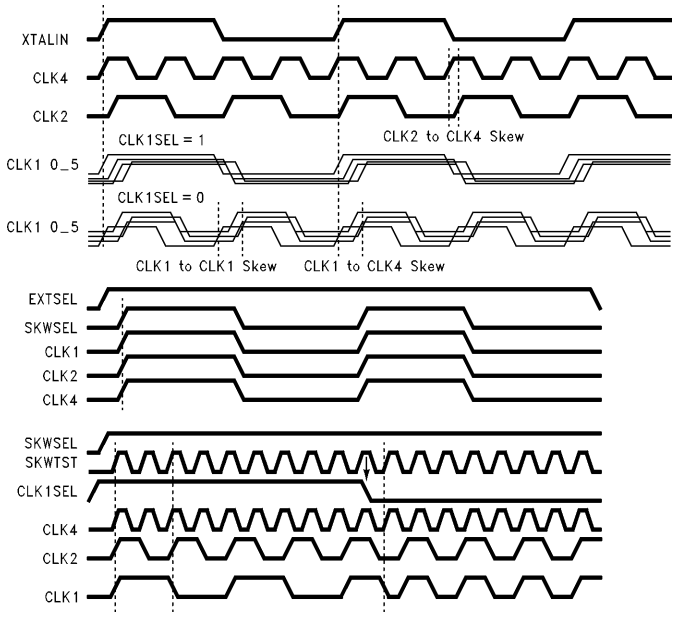

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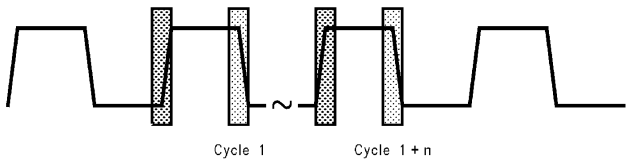
FIGURE 2. Waveforms



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Jitter = |Period(n) − Period(n+1)| = 300 ps for either the rising or falling edge, where n is 1 to 1000 cycles.

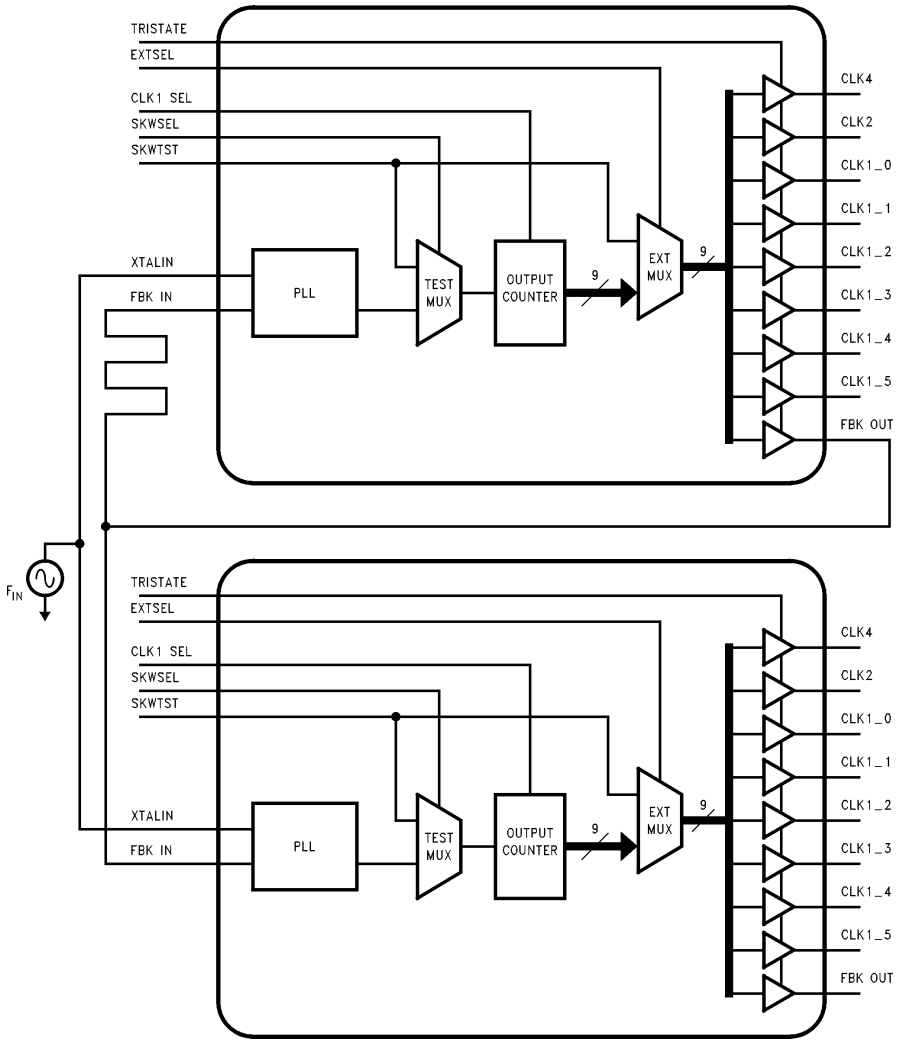
FIGURE 3. Jitter

APPLICATION REFERENCES AND BIBLIOGRAPHY:

Information relating to EMI, external feedback and general application issues are in the following application notes:

AN-968
AN-988 (EMI Application Note)
AN-640
AN-991

Application Example: Cascading CGS701A



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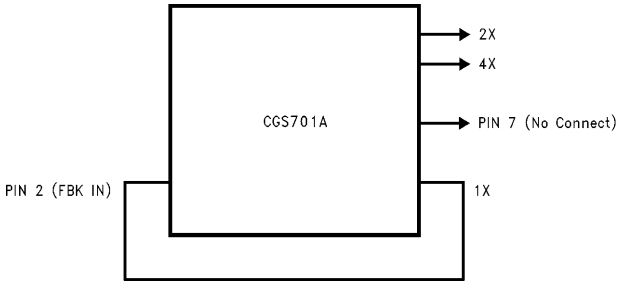
Application Example: External Feedback Option for the CGS701A

Any one of the 1X output clocks, (CLK1_0–CLK1_5), on the CGS701A can be used instead of the FBK OUT pin. When used in this configuration, pin 7 is a no connect and the 1X outputs can no longer be used in the 2X mode.



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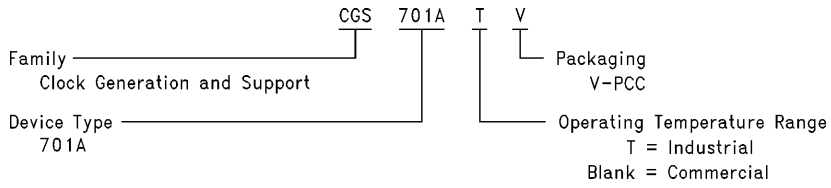
Ordering Information (Contact NSC Marketing for Specific Date of Availability)



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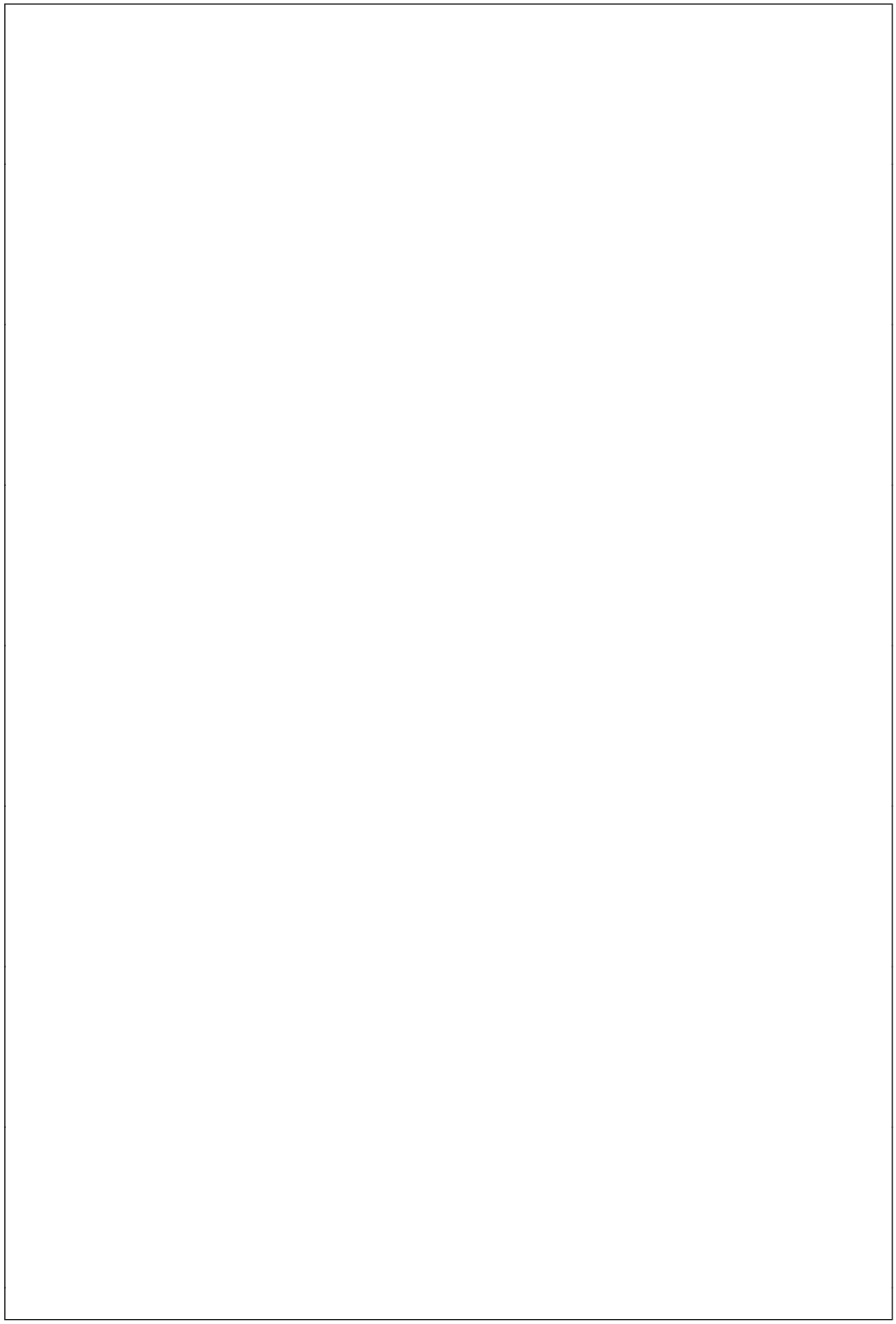
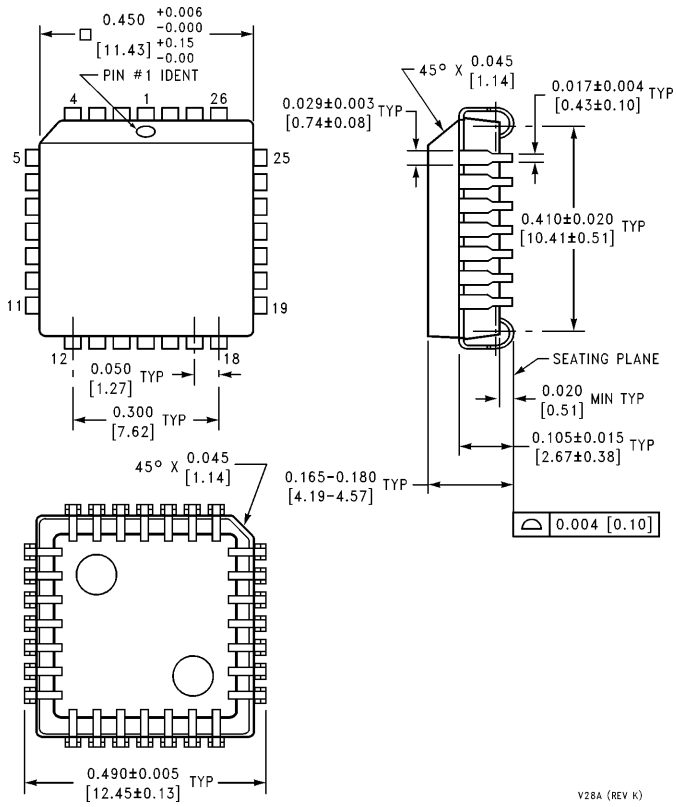


Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Molded Plastic Leaded Chip Carrier
Order Number CGS701AV or CGS701ATV
NS Package Number V28A

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