National Semiconductor

September 1995

CGS702V
Commercial Low Skew PLL 1 to 9 CMOS Clock Driver with Improved EMI

General Description

The CGS702 is an off-the-shelf clock driver specifically designed for today's high speed processors. It provides low skew outputs which are produced at different frequencies from three fixed input references. The CGS702 is a reduced EMI version of the CGS700. The XTALIN input pin is designed to be driven from three distinct crystal oscillators running at 25 MHz, 33 MHz or 40 MHz.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

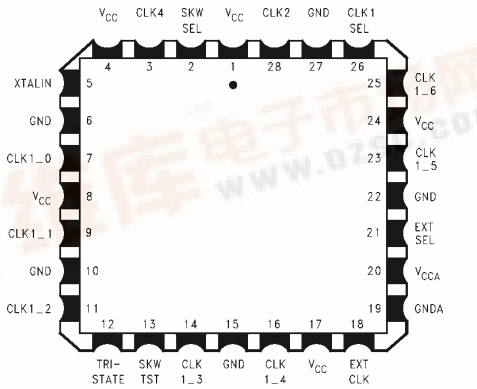
The device includes a TRI-STATE® control pin to disable the outputs while the PLL is still in lock. This function allows testing the board without having to wait to acquire the lock once the testing is complete. (Continued)

Features

- Reduced EMI compared to CGS700 (refer to EMI characteristics)
- Guaranteed and tested: 500 ps pin-to-pin skew (T_{OSHL} and T_{OSLH}) on 1x outputs
- Pentium™ and PowerPC™ compatible
- Output buffer of nine drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4x, 2x, 1x of the reference frequency for multi-frequency bus applications
- Selectable output frequency
- Internal loop filter to reduce noise and jitter
- Separate Analog and digital V_{CC} and Ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive: +30 mA/−30 mA I_{OL}/I_{OH}
- 28-pin PCC for optimum skew performance
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for PLCC



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Pin Description

PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	SKWSEL	Skew Test Selector Pin
3	CLK4	4x Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	CLK1__0	1x Clock Output
8	V_{CC}	Digital V_{CC}
9	CLK1__1	1x Clock Output
10	GND	Digital Ground
11	CLK1__2	1x Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1__3	1x Clock Output
15	GND	Digital Ground
16	CLK1__4	1x Clock Output
17	V_{CC}	Digital V_{CC}
18	EXTCLK	External Test Clock
19	GNDA	Analog Ground
20	V_{CCA}	Analog V_{CC}
21	EXTSEL	External Clock MUX Selector
22	GND	Digital Ground
23	CLK1__5	1x Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1__6	1x Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2x Clock Output

RRD-B30M105/Printed in U. S. A.

CGS702V Commercial Low Skew PLL 1 to 9 CMOS Clock Driver with Improved EMI

General Description (Continued)

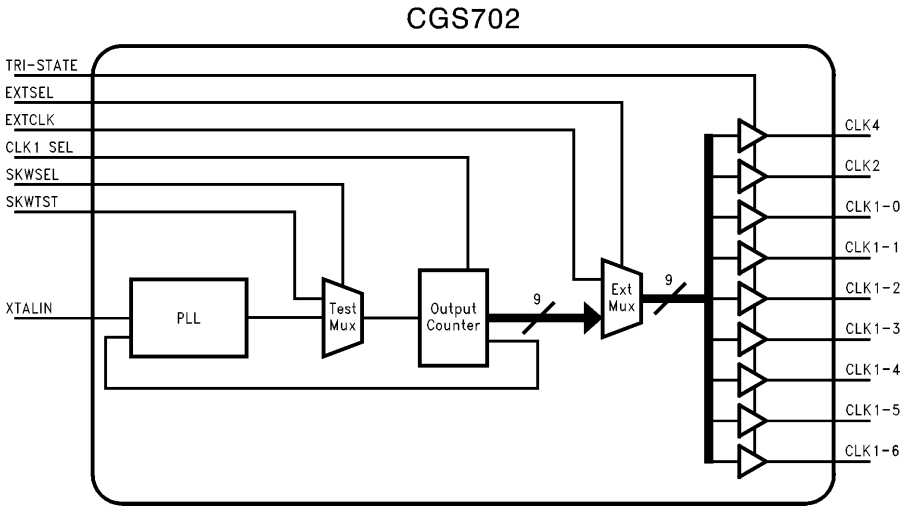
Also included, are two EXTSEL and EXTCLK pins to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock__Mux to change its input from the output of the VCO and Counter to the external clock signal provided via EXTCLK input pin.

CLK1SEL pin changes the output frequency of the CLK1__0,6 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.

Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

In addition two other pins are added for increasing the test capability. SKWSEL and SKWTST pins allow testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is ½ and CLK1 frequencies are ¼ respectively (refer to the truth table). In addition CLK1SEL functionality is also true under this test condition.

Block Diagram



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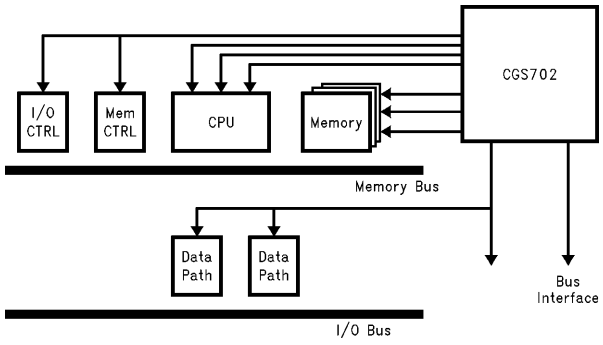
Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
H*	L	X	L	X	H	4x f_{IN}	2x f_{IN}	f_{IN}
L*	L	X	L	X	H	4x f_{IN}	2x f_{IN}	2x f_{IN}
X	H	⎍	X	X	H	⎍	⎍	⎍
H	L	X	H	⎍	H	1x f_{TST}	½x f_{TST}	¼x f_{TST}
L	L	X	H	⎍	H	1x f_{TST}	½x f_{TST}	½x f_{TST}
X	X	X	X	X	L	Z	Z	Z

*Steady state phase, frequency lock.

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CO} or I_{GND})	±60 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note 2)	1400 mW

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note 2: Power dissipation is calculated using 49°/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed at 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1's being at 66 MHz. In addition the ambient temperature is assumed 70° with power supply at 5.0V.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Crystal Frequency	25 MHz–40 MHz
Operating Temperature (T_A)	0°C to +70°C
External Clock Frequency (EXTCLK Pin)	1 MHz–10 MHz
XTALIN Duty Cycle Range	25/75 (75/25)%
Input Rise and Fall Times (0.8V to 2.0V)	
Crystal Input	5 ns max.
All Other Inputs	10 ns max.

Typical θ_{JA}	LFM	°C/W
	0	54
	225	45
	500	38
	900	34

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	V_{CC}	V_{CC} = 4.5V to 5.5V, T = 0°C to 70°C			Units
				Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage		4.5 5.5	2.0 2.0			V
V_{IL}	Maximum Input Low Level Voltage		4.5 5.5			0.8 0.8	V
V_{OH}	Minimum Output High Level Voltage	$I_{OH} = -50\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4		V
		$I_{OH} = -30$ mA	4.5 5.5	$V_{CC} - 0.6$ $V_{CC} - 0.6$			
V_{OL}	Maximum Output Low Level Voltage	$I_{OL} = 50\ \mu A$	4.5 5.5			0.1 0.1	V
		$I_{OL} = 30$ mA	4.5 5.5			0.6 0.6	
I_{OH}	High Level Output Current	$V_{OH} = V_{CC} - 1.0V$	4.5	50	110	170	mA
I_{OL}	Low Level Output Current	$V_{OL} = 1.0V$	4.5	50	110	170	mA
I_{IN}	Leakage Current	$V_{IN} = 0.4V$ or 4.6V	4.5 5.5	−50		50.0	μA
$I_{OZL/H}$	Output Leakage Current	$V_{IN} =$ GND $V_{OUT} = V_{CC}$ or GND	5.5	−5.0		+5.0	μA
C_{IN}	Input Capacitance		4.5 5.0			10.0	pF
I_{CC}	Quiescent Analog + Digital Current (No Load)	$V_{IN} = V_{CC}$ or GND	5.5		3	5.0	mA
I_{CCT}	I_{CC} per TTL Input	$V_{IN} = V_{CC} - 2.1$ or GND	5.5			2.5	

CGS702 AC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter			V_{CC} = 4.5V to 5.5V f_{IN} = 25 MHz to 40 MHz T = 0°C to 70°C C_L = Circuit 1 and 2 R_L = Circuit 1 and 2			Units	Notes
				Min	Typ	Max		
t_{RISE}	Output Rise	CLK4 CLK2 CLK1	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V			2.0	ns	(Note 1)
t_{FALL}	Output Fall	CLK4 CLK2 CLK1	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V			2.0	ns	(Note 1)
t_{SKEW}	Maximum Edge-to-Edge Output Skew	+ to + Edges + to + Edges + to + Edges	CLK1__CLK1 CLK1__CLK4 CLK2__CLK4			500 1000 1500	ps	(Note 2)
t_{LOCK}	Time to Lock the Output to the XTALIN Input					100	μs	
t_{CYCLE}	Output Duty Cycle		CLK1 Outputs CLK2 Output CLK4 Output	49 49 35		51 51 65	%	(Note 3)
J_{LT}	Output Jitter (Long Term)					300	ps	(Notes 4, 5)
J_{CC}	Output Jitter (Cycle to Cycle)	CLK1		−75		+75	ps	(Notes 4, 5, 6)
		CLK2			±250		ps	(Notes 4, 5, 7)
		CLK4			±250		ps	(Notes 4, 5, 7)
F_{MIN}	Minimum XTALIN Frequency					15	MHz	
F_{MAX}	Maximum XTALIN Frequency					43	MHz	

Note 1: t_{RISE} and t_{FALL} parameters are measured at the pin of the device

Note 2: Skew is measured at 50% of V_{CC} for CLK1 and CLK2. While it is measured at 1.4V for CLK4.

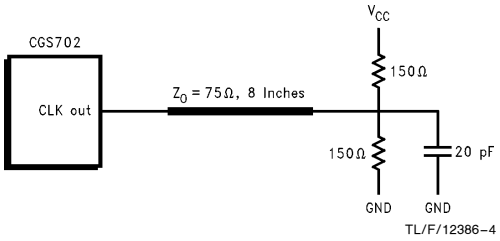
Note 3: Output duty cycle is measured at $V_{DD}/2$ for CLK1 and CLK2. While it is measured at 1.4V for CLK4.

Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge over 1000 cycles. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 2* for further explanation.

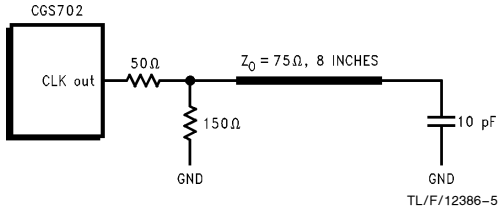
Note 5: The GNDA pins of the 702 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the V_{CCA} pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for V_{CCA} pin.

Note 6: Cycle to Cycle Jitter is measured at $V_{CC/2}$.

Note 7: Cycle to Cycle Jitter for CLK2 and CLK4 is only for 25°C, 5V measured @ $V_{CC/2}$.



Circuit 1. Test Circuit for CLK1 and CLK2



Circuit 2. Test Circuit for CLK4

CGS702 AC Electrical Characteristics (Continued)

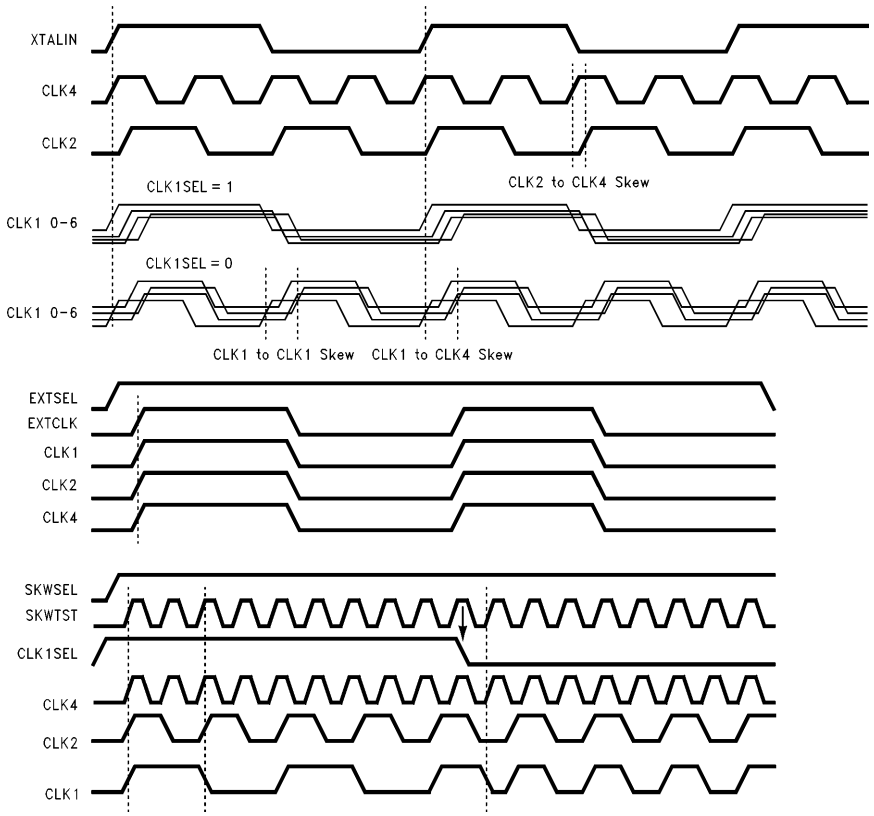


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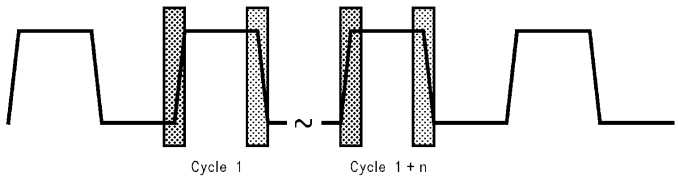
FIGURE 1. Waveforms



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Jitter = |Period(1) − Period(n+1)| for either the rising or falling edge, where n is 1 to 1000 cycles.

FIGURE 2. Jitter

Application References and Bibiliography

Information relating to EMI as well as general application hints are in the following application notes:

AN-988 (EMI App Note)
AN-640
AN-991

EMI Characteristics and Measurements for CGS702

MEASURING THE SPECTRAL CONTENT OF A LOGIC IC

In order to analyze the frequency, or spectral content of logic ICs, two measurement techniques have been developed. One method, *The Radiated Measurement Method,* is based on the system-level FCC certification test methodology, FCC Open Site Test (OST) 55. The radiated method utilizes a multilayer PCB with the IC-under-test is mounted on a grounded, adjustable table placed 3 meters from an antenna mast (see *Figure 3*). The IC's input is stimulated by a known periodic waveform and its output drives a typical PCB microstrip. The 75Ω microstrip is properly terminated to prevent reflections from affecting the IC's spectral content results.

The FCC certification test method is an *open field* measurement procedure. Therefore, the spectral content of the device-under-test (in this case, an IC) cannot be detected below the ambient level of radiation. The test-site is permanent and the average ambient noise level remains relatively constant.

The CGS700 and CGS702 were tested for EMI using the above method. A comparison of the EMI results in the form of spectral content is shown in *Figures 4* and *5*.

For more details on EMI, see Application Note AN-831.

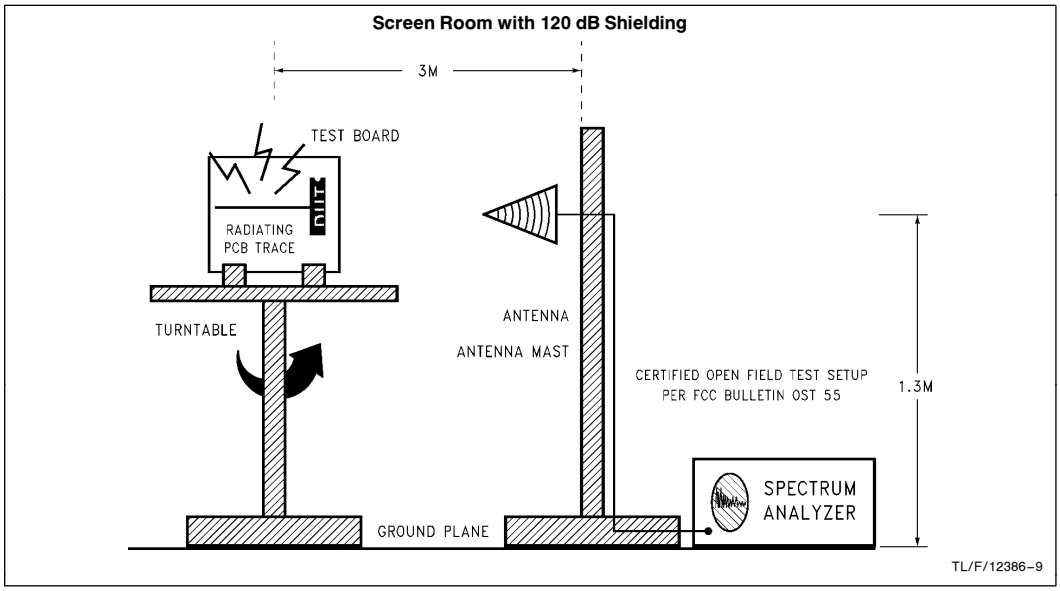
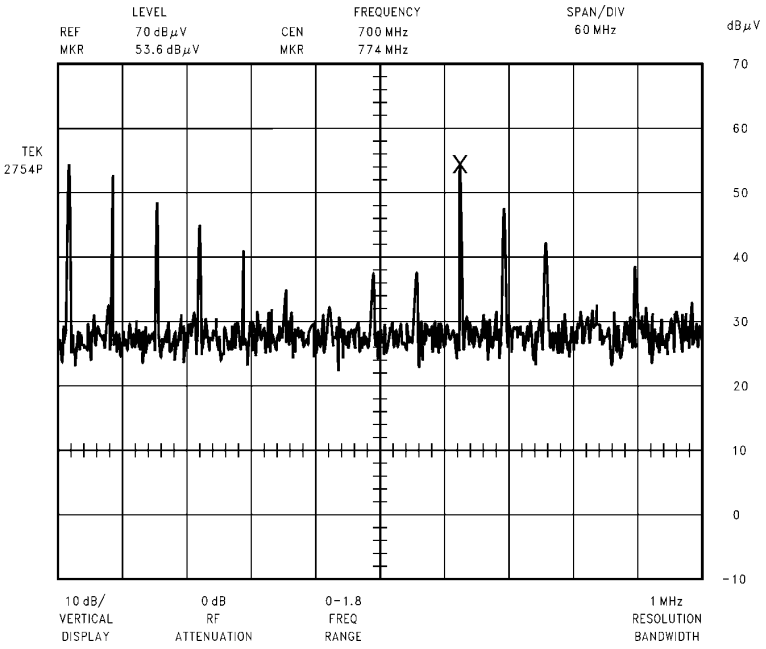


FIGURE 3. Radiated EMI Measurement Method

EMI Characteristics and Measurements (Continued)



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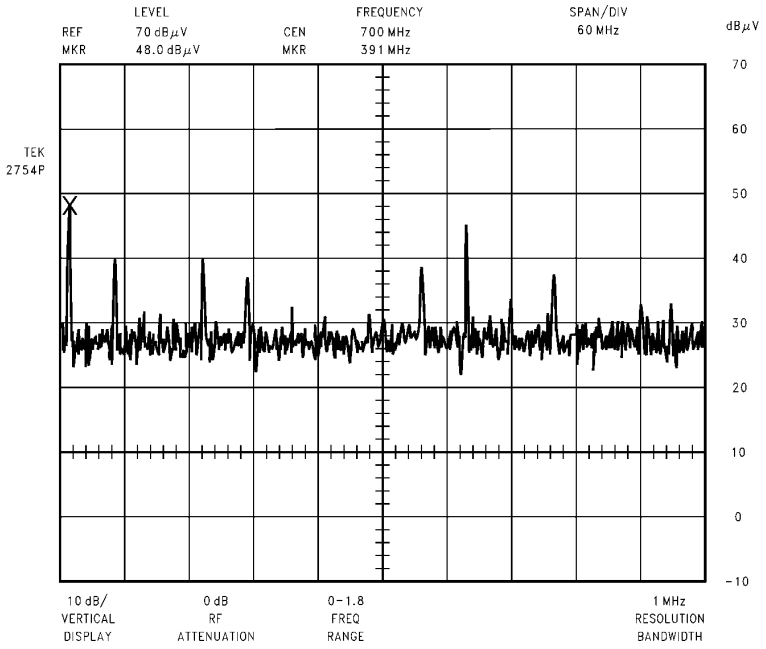
XTALIN = 40 MHz V_{CC} = 5V T = 25°C ANTENNA = HORIZONTAL

FIGURE 4. CGS700



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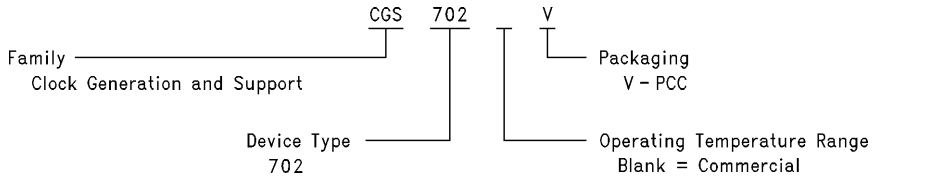
XTALIN = 40 MHz V_{CC} = 5V T = 25°C ANTENNA = HORIZONTAL

FIGURE 5. CGS702

Ordering Information

(Contact NSC Marketing for Specific Date of Availability)



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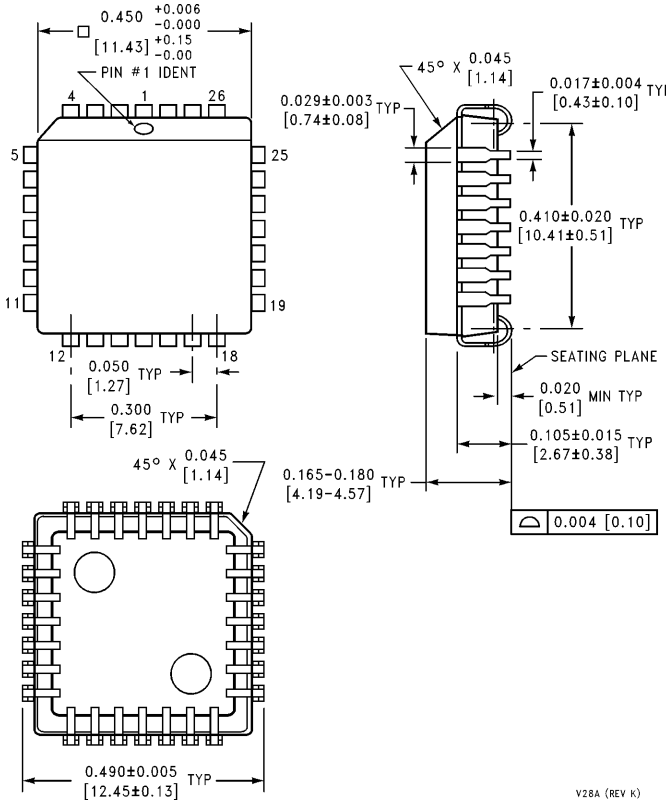
Physical Dimensions inches (millimeters)



28-Lead Molded Plated Leaded Chip Carrier
Order Number CGS702V
NS Package Number V28A

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