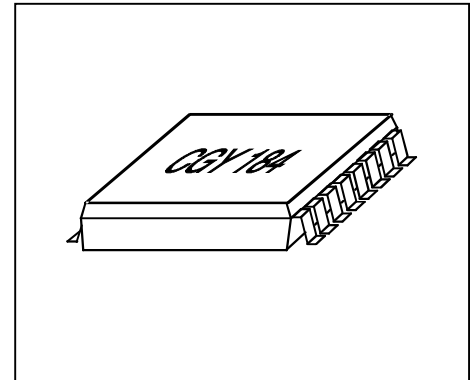


GaAs MMIC

Preliminary Data

- Power amplifier for PCN applications
- 2.5 W (34dBm) output power at 3.5 V
- Overall power added efficiency 43 %
- Fully integrated 4 stage amplifier
- Power ramp control
- Input matched to 50 ohms, simple output match



ESD: **E**lectrostatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (taped)	Package ¹⁾
CGY 184	CGY 184	Q62702G62	MW 16

Maximum ratings

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	9	V
Supply current	I_D	4	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
Pulse peak power dissipation duty cycle 12.5%, $t_{on}=0.577ms$	$PPulse$	tbd	W
Total power dissipation ($T_c \square 82\text{ °C}$) T_c : Temperature on case	P_{tot}	8.5	W

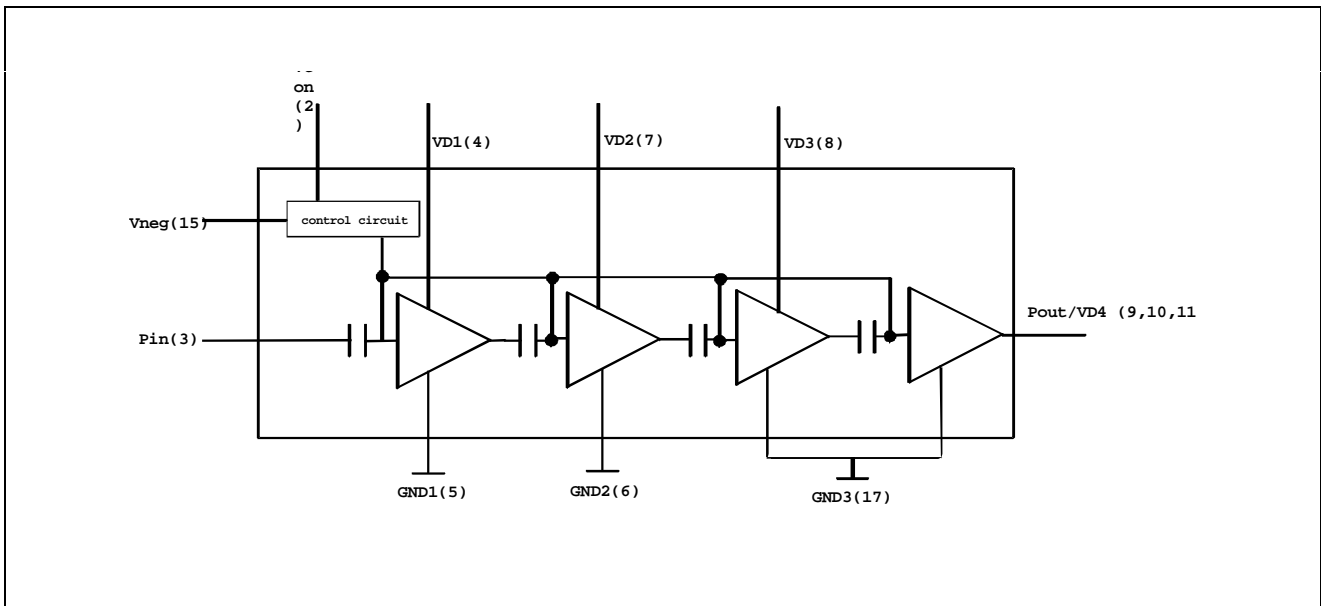
Thermal Resistance

Characteristics	Symbol	max. Value	Unit
Junction-Case ²⁾	R_{thJC}	≤ 8.5	K/W

¹⁾ Dimensions see page 14

²⁾ see also page 9

Functional block diagram



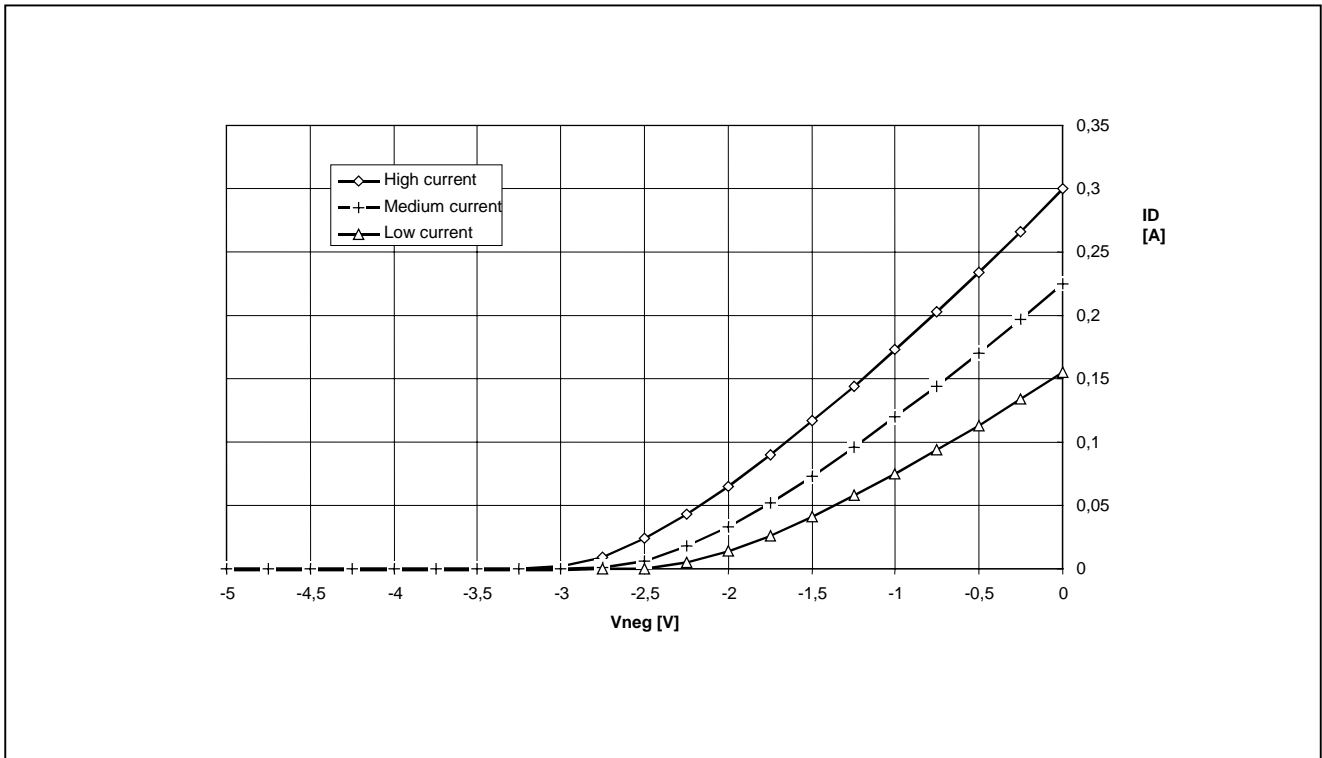
Pin #		Configuration
1	n. c.	
2	V_{con}	Control voltage for power ramping
3	P_{IN}	RF-input
4	V_{D1}	Drain voltage 1st stage
5	Gnd1	Ground pin 1st stage
6	Gnd2	Ground pin 2nd stage
7	V_{D2}	Drain voltage 2nd stage
8	V_{D3}	Drain voltage 3rd stage
9,10,11	P_{OUT}/V_{D4}	Drain voltage 4th stage and RF-output
12	n. c.	
13	n. c.	
14	n. c.	
15	V_{neg}	Block capacitor negativ voltage generator
16	n. c.	
(17)	GND3	Ground (backside of MW16 housing)

Electrical characteristics

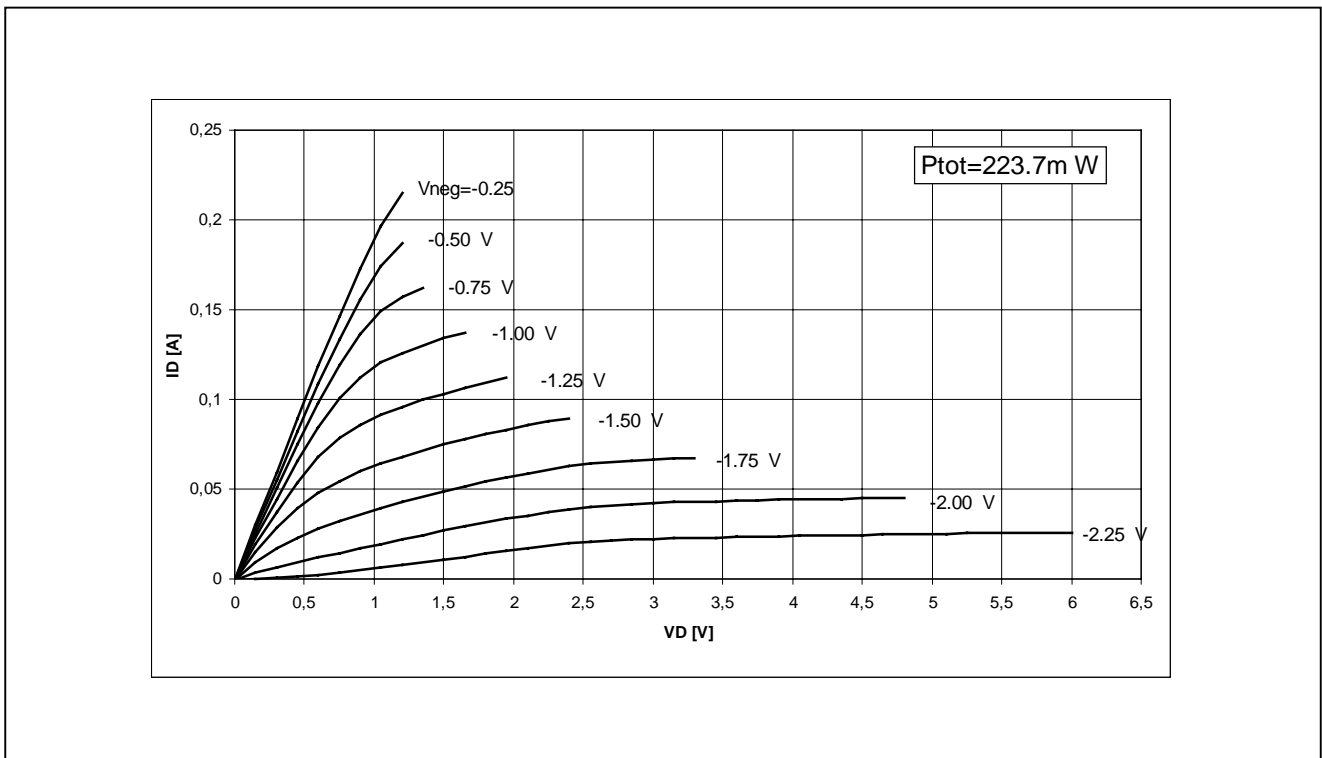
($T_A = 25^\circ\text{C}$, $f = 1.75\text{ GHz}$, $Z_S = Z_L = 50\text{ Ohm}$, $V_D = 3.5\text{V}$, $V_{aux} = 3.5\text{V}$, $V_{control} = 2.5\text{V}$, unless otherwise specified; pulsed with a duty cycle of 12.5%, $t_{on} = 577\mu\text{sec}$)

Characteristics	Symbol	min	typ	max	Unit
Supply current $V_D = 3.5\text{V}$; $P_{in} = 0\text{dBm}$	I_{DD}	-	1.67	-	A
Supply current neg. voltage gener. $V_{aux} = 3.5\text{V}$	I_{aux}	-	10	-	mA
Control Current	I_C		2	3	mA
Shut-off current ($V_C = 0\text{V}$, $V_D = 3.5\text{V}$, no RF- drive)	I_D		40		μA
Small signal gain $P_{in} = -10\text{dBm}$	G	-	40	-	dB
Power gain $V_D = 3.5\text{V}$; $P_{in} = 0\text{dBm}$	G	-	34	-	dB
Output Power $V_D = 3.5\text{V}$; $P_{in} = 0\text{dBm}$	P_O	-	34	-	dBm
Power gain $V_D = 3.5\text{V}$; $P_{in} = 0\text{dBm}$, $T = 85^\circ\text{C}$	G	-	33.7	-	dB
Output Power $V_D = 3.5\text{V}$; $P_{in} = 0\text{dBm}$, $T = 85^\circ\text{C}$	P_O	-	33.7	-	dBm
Overall Power added Efficiency $V_D = 3.5\text{V}$; ; $V_C = 2.5\text{V}$; $P_{in} = 0\text{dBm}$	η	-	43	-	%
Dynamic range ($P_{out,max} - P_{out,min}$) $V_C = 0.5 \dots 2.5\text{V}$		-	80	-	dB
Harmonics $V_C = 2.2\text{V}$, $P_{in} = 0\text{dBm}$	$2f_0$ $3f_0$	- -	-60 -40	- -	dBc
RX-Noise Power $V_C = 2.2\text{V}$; $P_{in} = 0\text{dBm}$; $f_{RX} = 1.805 \dots 1.88\text{GHz}$		-	-80	-	dBm/ 100kHz
Input VSWR $V_D = 3.5\text{V}$	-	-	1.8 : 1	-	-

DC-ID(Vneg) characteristics – typical values of stage 1 and 2, $V_D=3V$

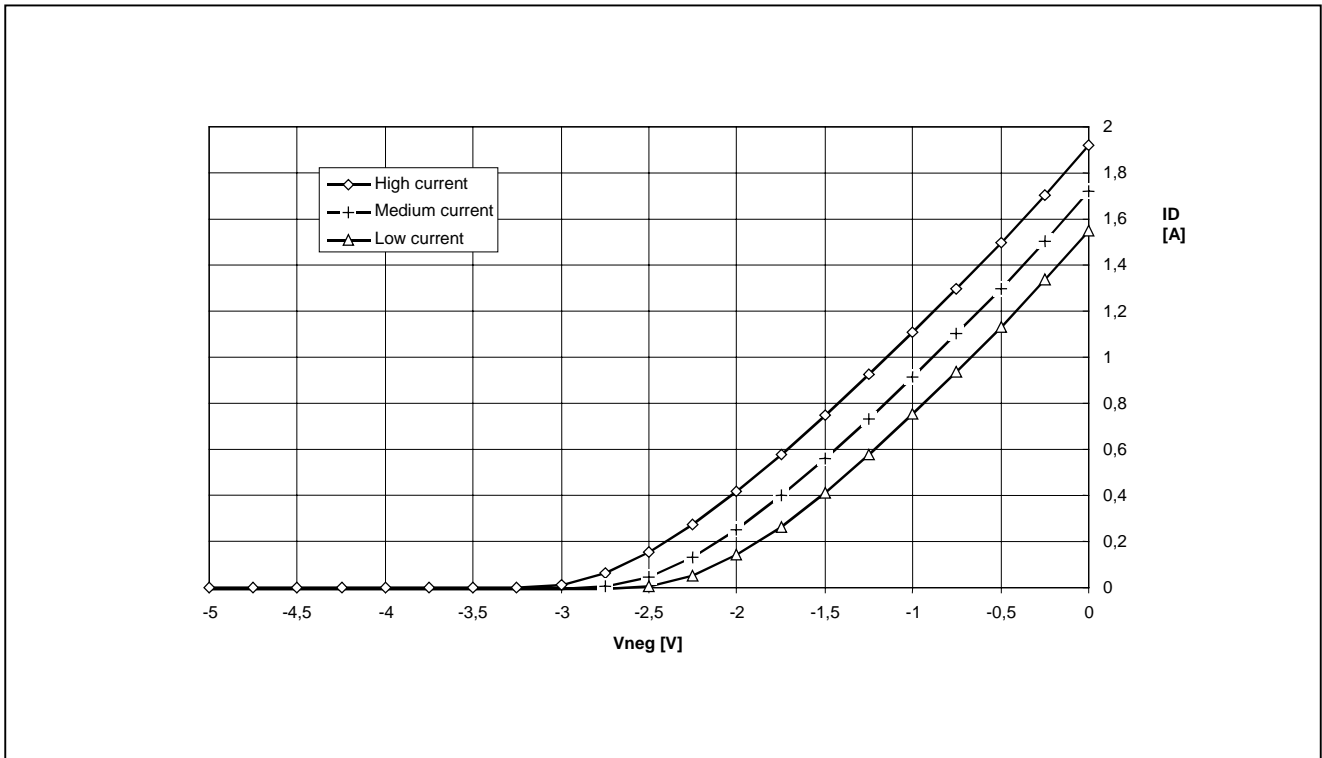


DC-Output characteristics – typical values of stage 1 and 2

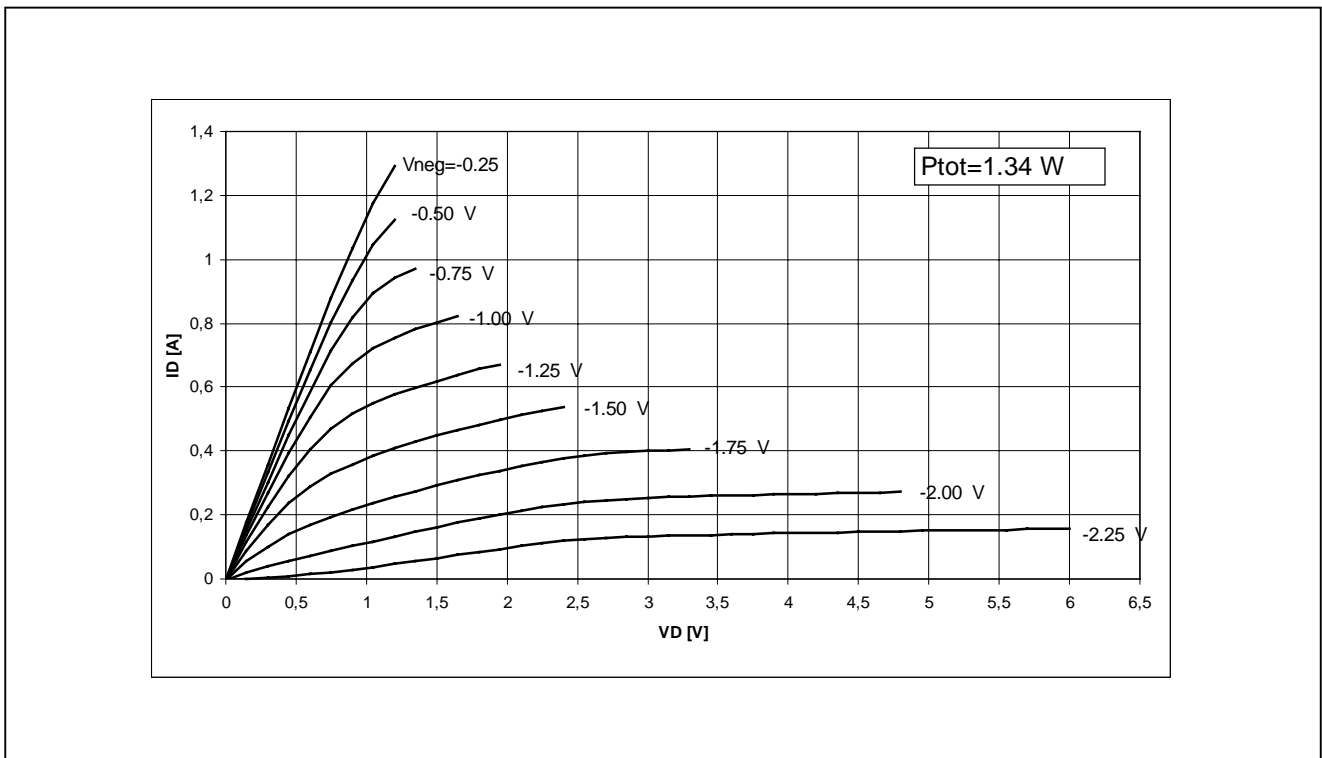


Pin 2(V_{con}) has to be open during measuring DC-characteristics

DC-ID(Vneg) characteristics – typical values of stage 3, VD=3V

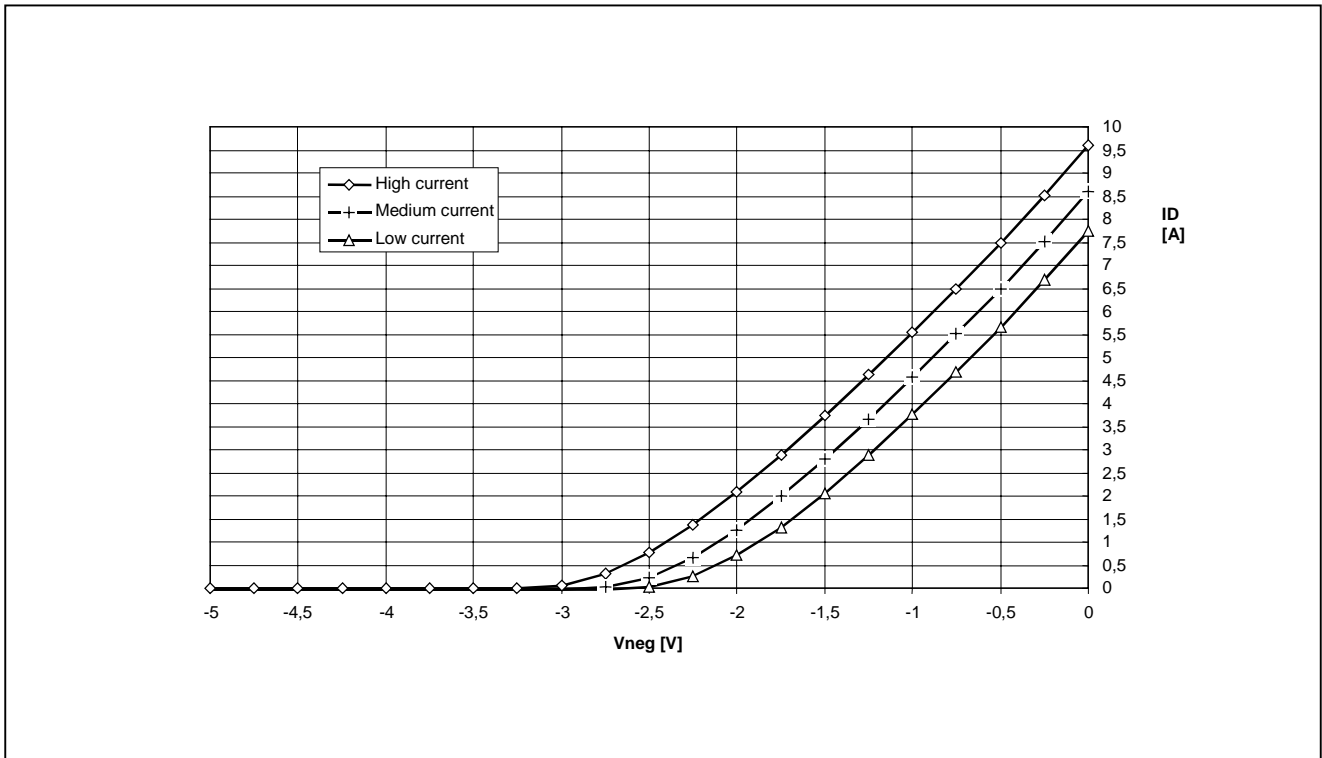


DC-Output characteristics – typical values of stage 3

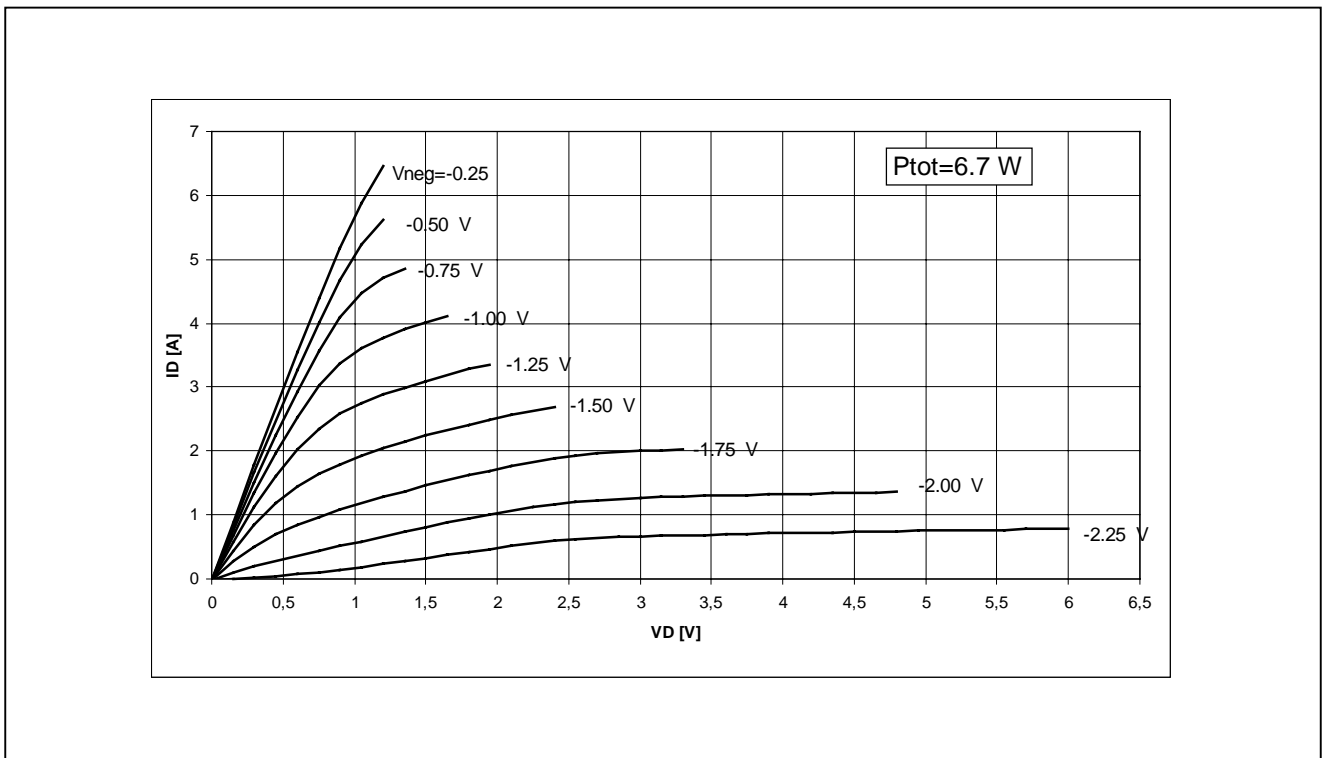


Pin 2(Vcon) has to be open during measuring DC-characteristics

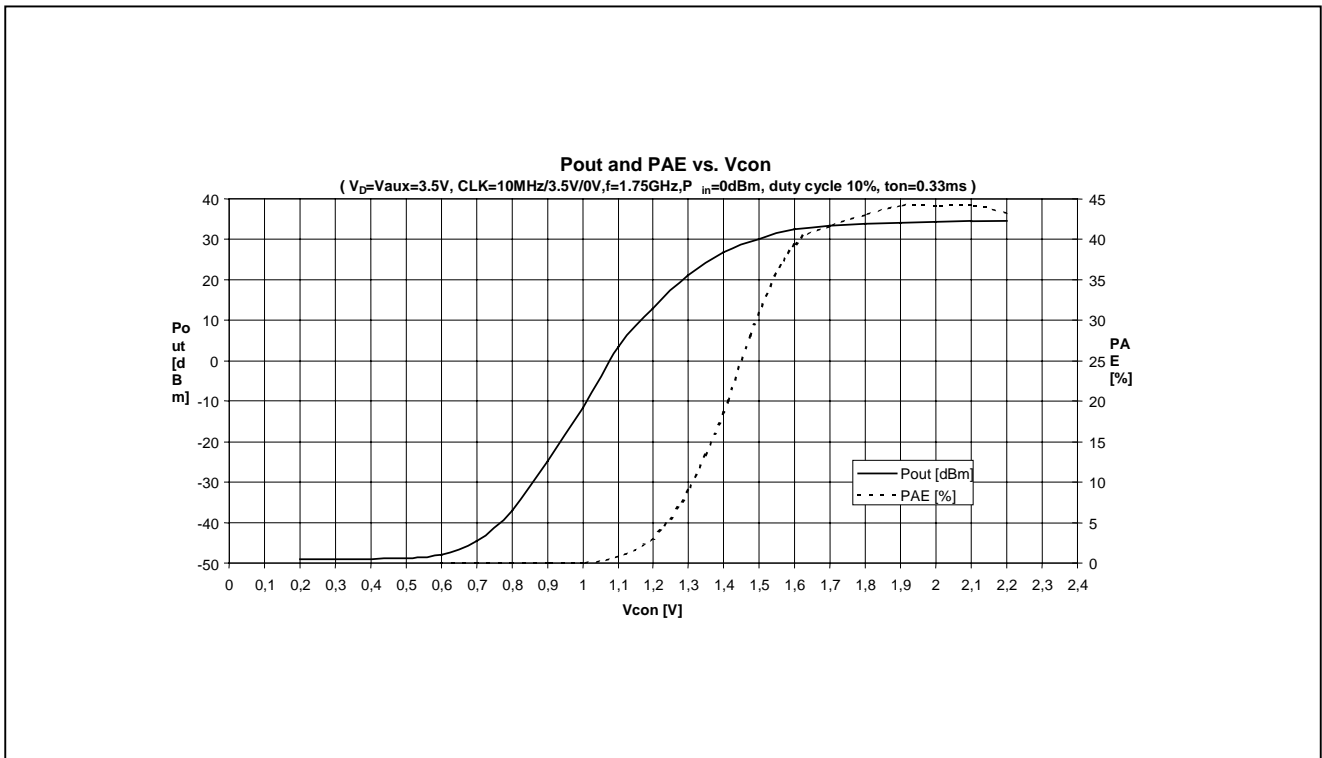
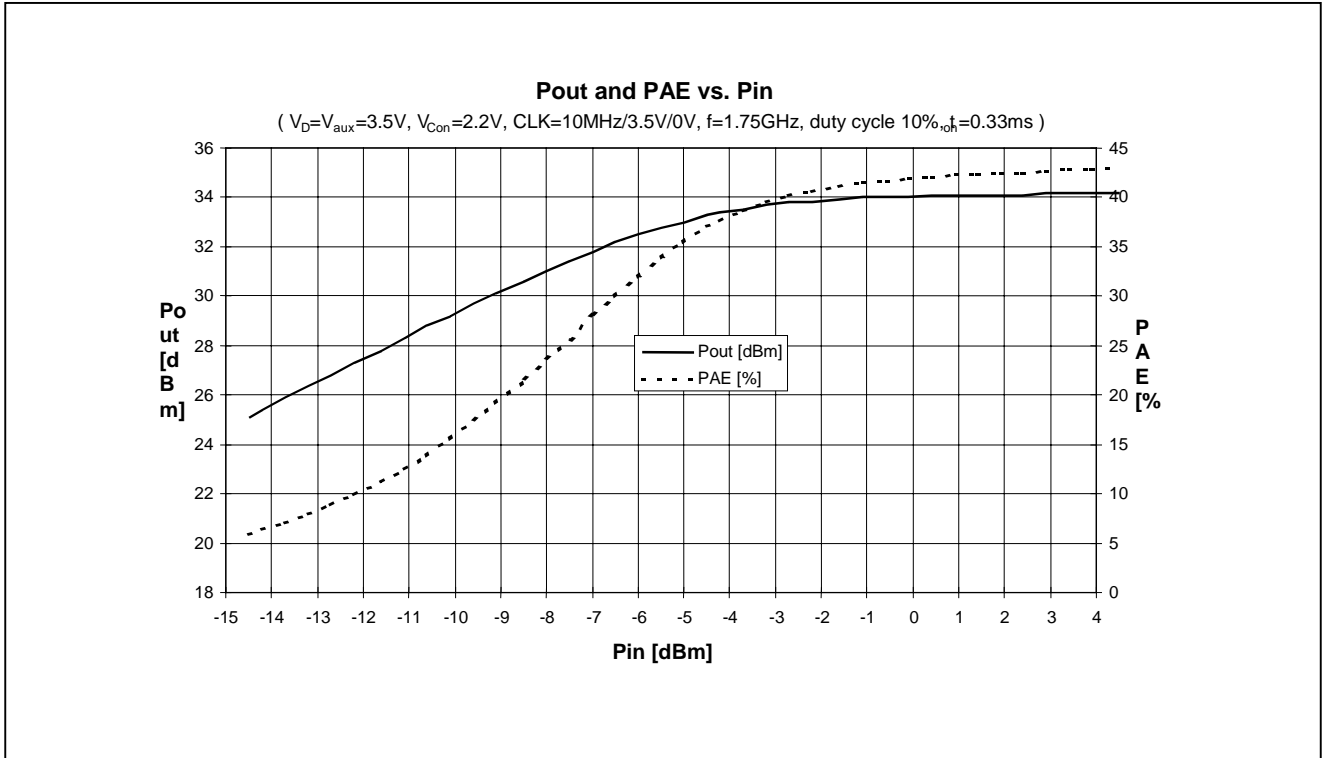
DC-ID(Vneg) characteristics – typical values of stage 4, VD=3V

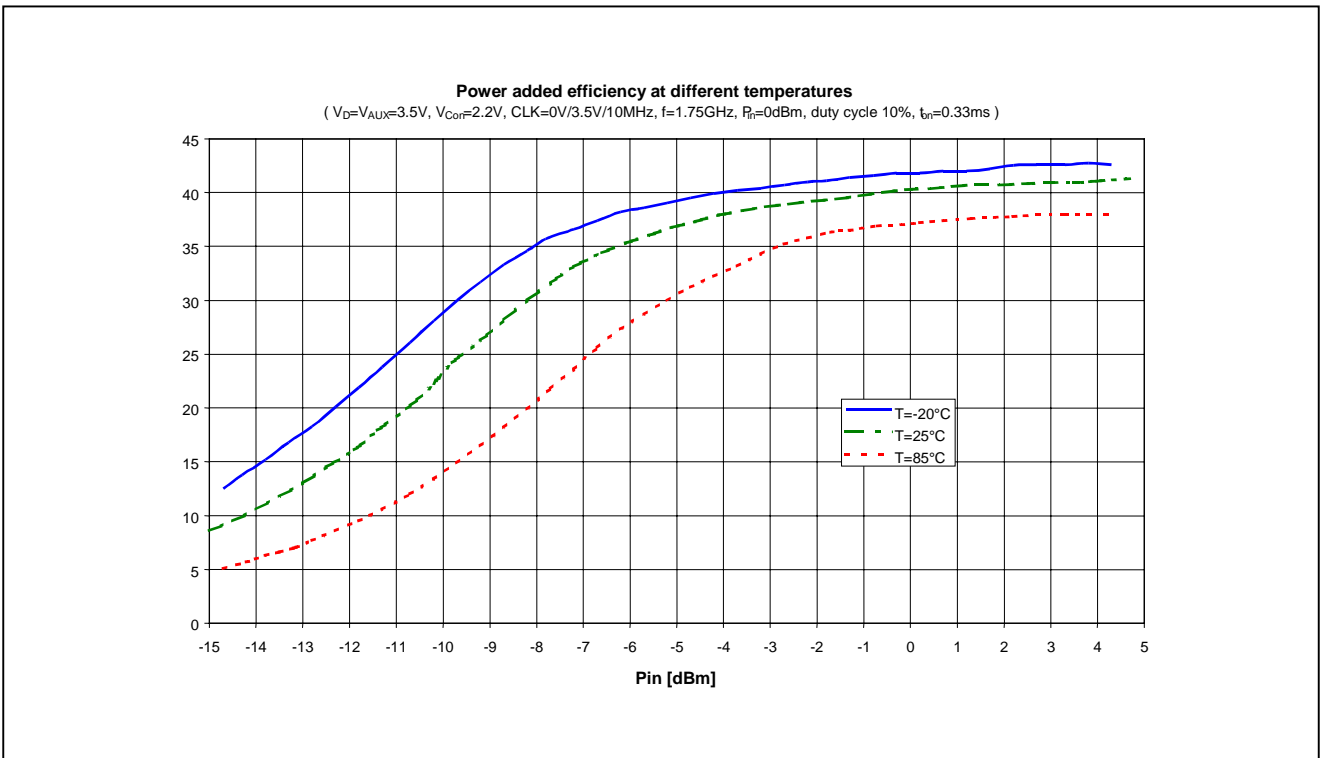
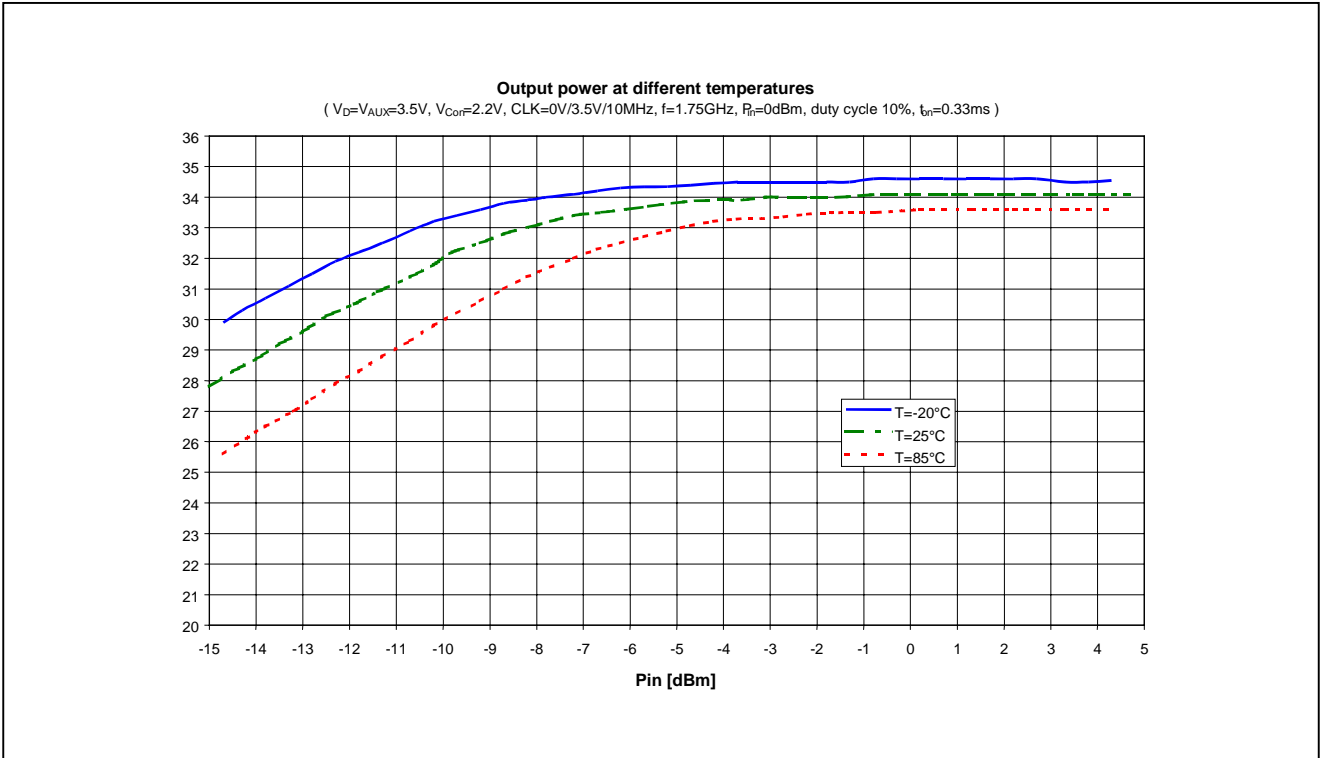


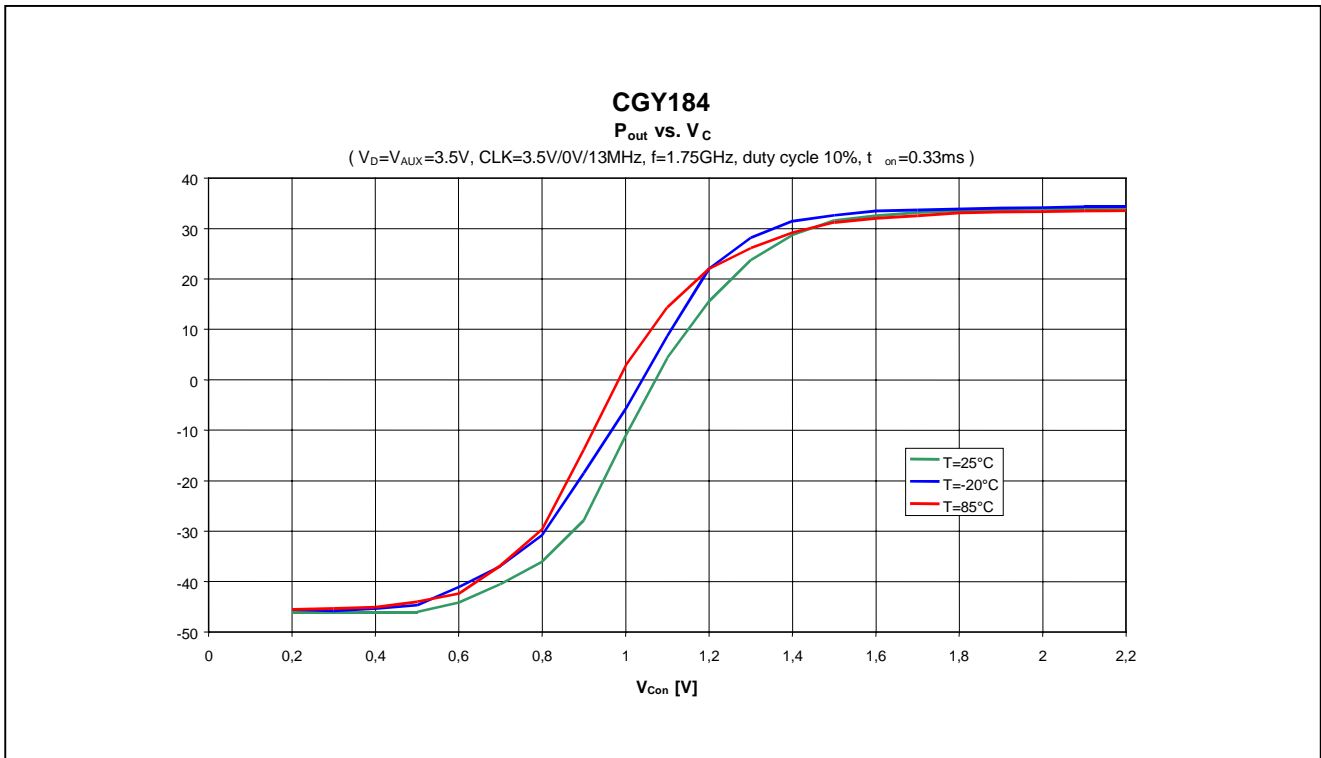
DC-Output characteristics – typical values of stage 4



Pin 2(Vcon) has to be open during measuring DC-characteristics



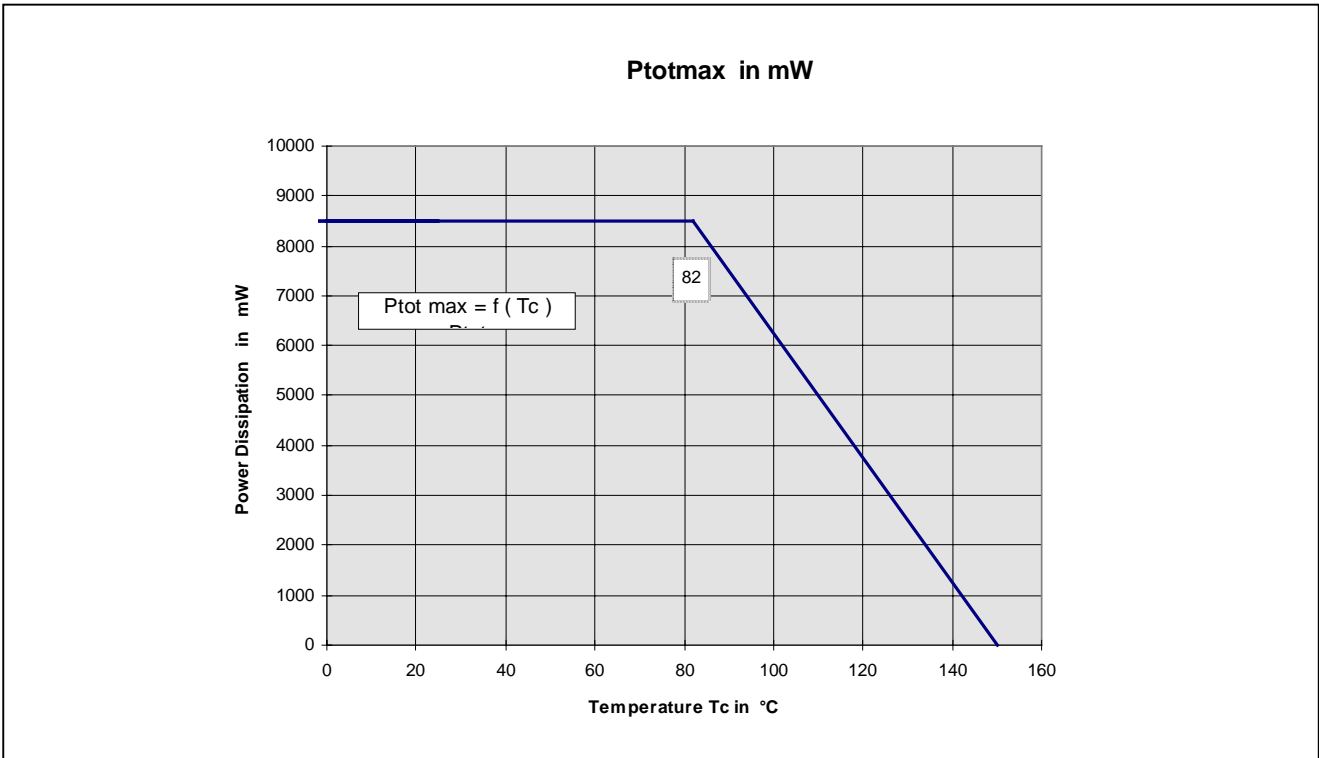
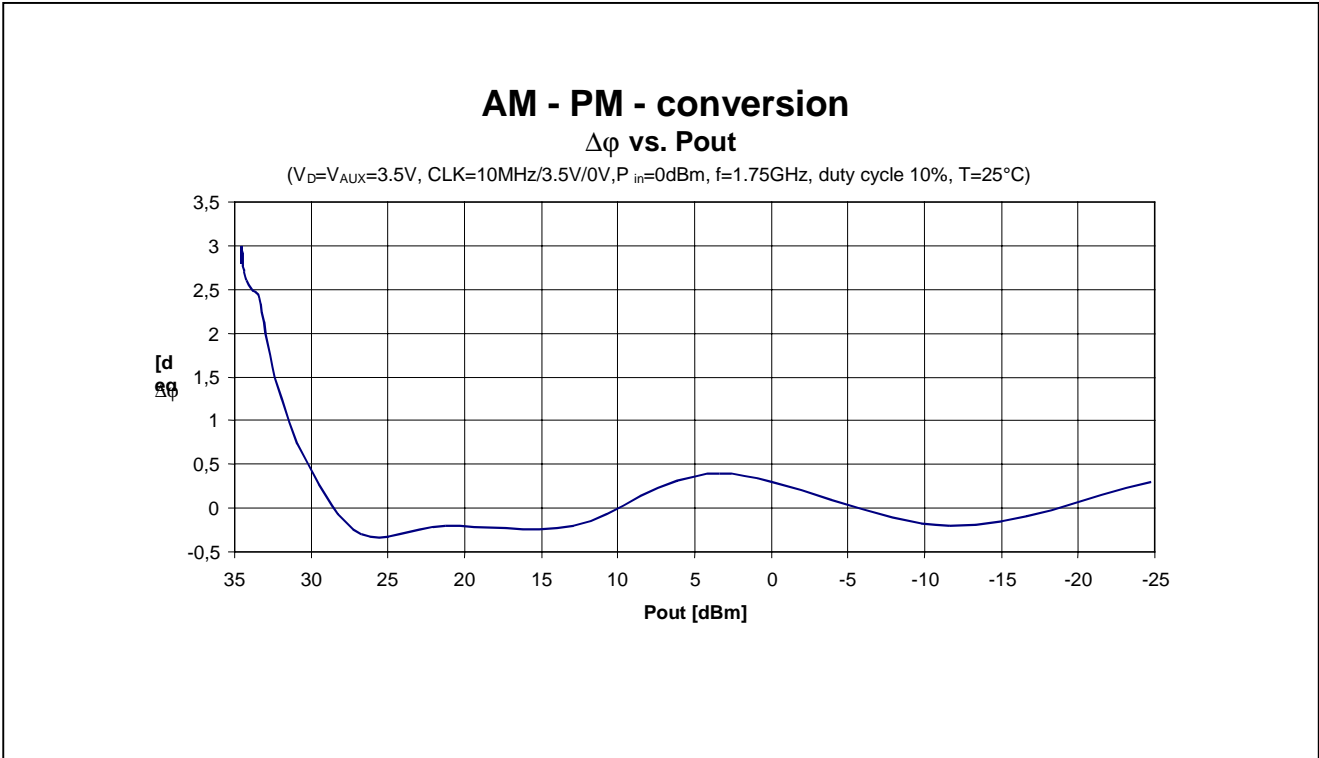




AM – PM Conversion:

(Conditions: V_D=V_{AUX}=3.5V, f=1.75GHz, CLK=10MHz/3.5V/0V, P_{out} controlled by V_{Con})

V _{Con} [V]	Δφ [deg/dB]	P _{out} [dBm]
2,2	2,8	34,53
2,1	3	34,53
2	2,7	34,37
1,9	2,6	34,2
1,8	2,5	33,87
1,7	2,4	33,37
1,6	1,5	32,37
1,5	0,5	30,2
1,4	-0,3	26,7
1,3	-0,2	21,2
1,2	-0,2	12,87
1,1	0,4	3,37
1	-0,2	-11,63
0,9	0,3	-24,8

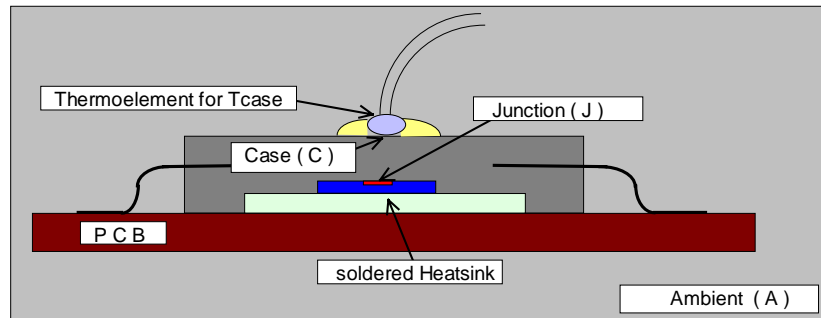


Thermal Resistance and Temperature Considerations:

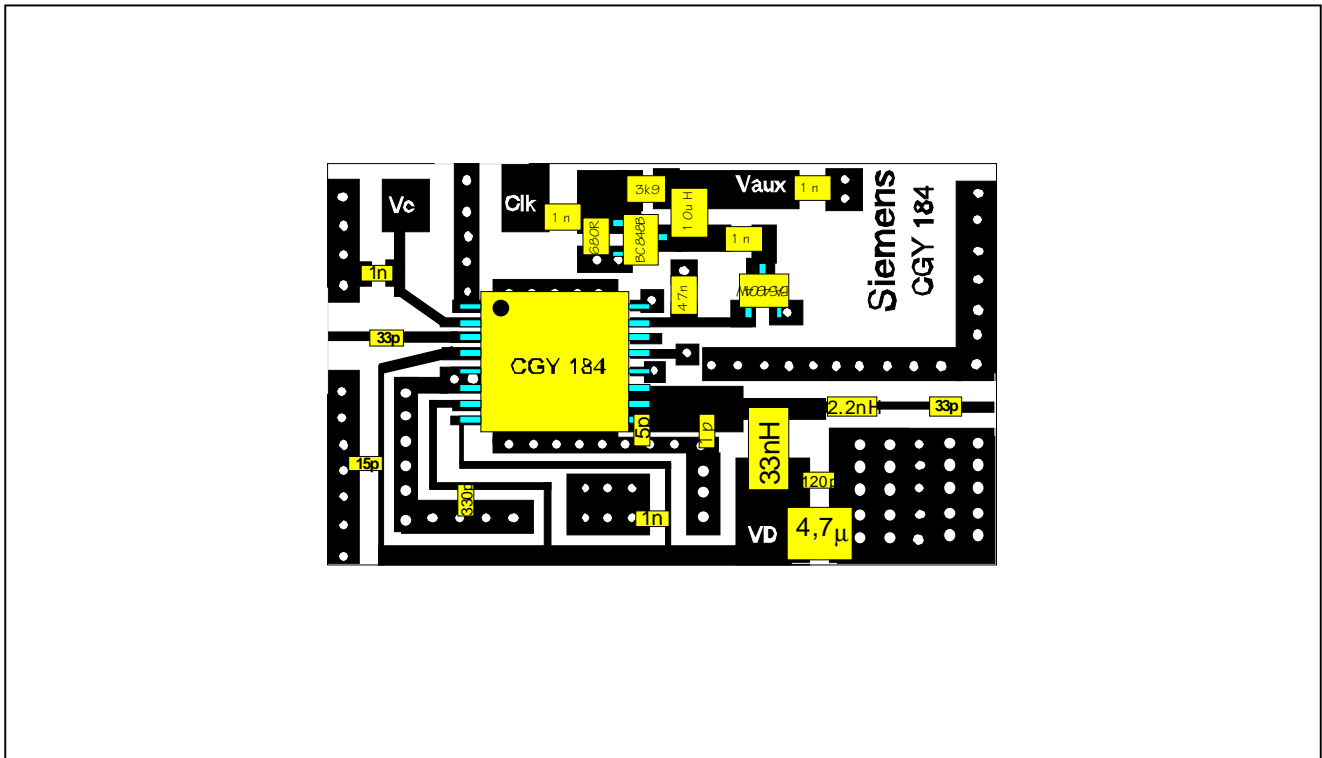
Because the MW16 heat sink is not easily accessible to a temperature measurement the thermal resistance is defined as R_{thJC} using the case temperature T_C

- Calculation of Junction Temperature T_J :

$$T_J = T_C + R_{thJC} * P_{tot}$$
- Measurement of Case Temperature T_C :
 T_C should be measured in operation at the upper side of the case where the temperature is highest. Small thermoelements $\leq 1\text{mm}$ (thin wires, thermopaste) and thermopapers with low heat dissipation are well suited.



CGY184 application board:



Layout size is 32mm x 19mm

Connections:

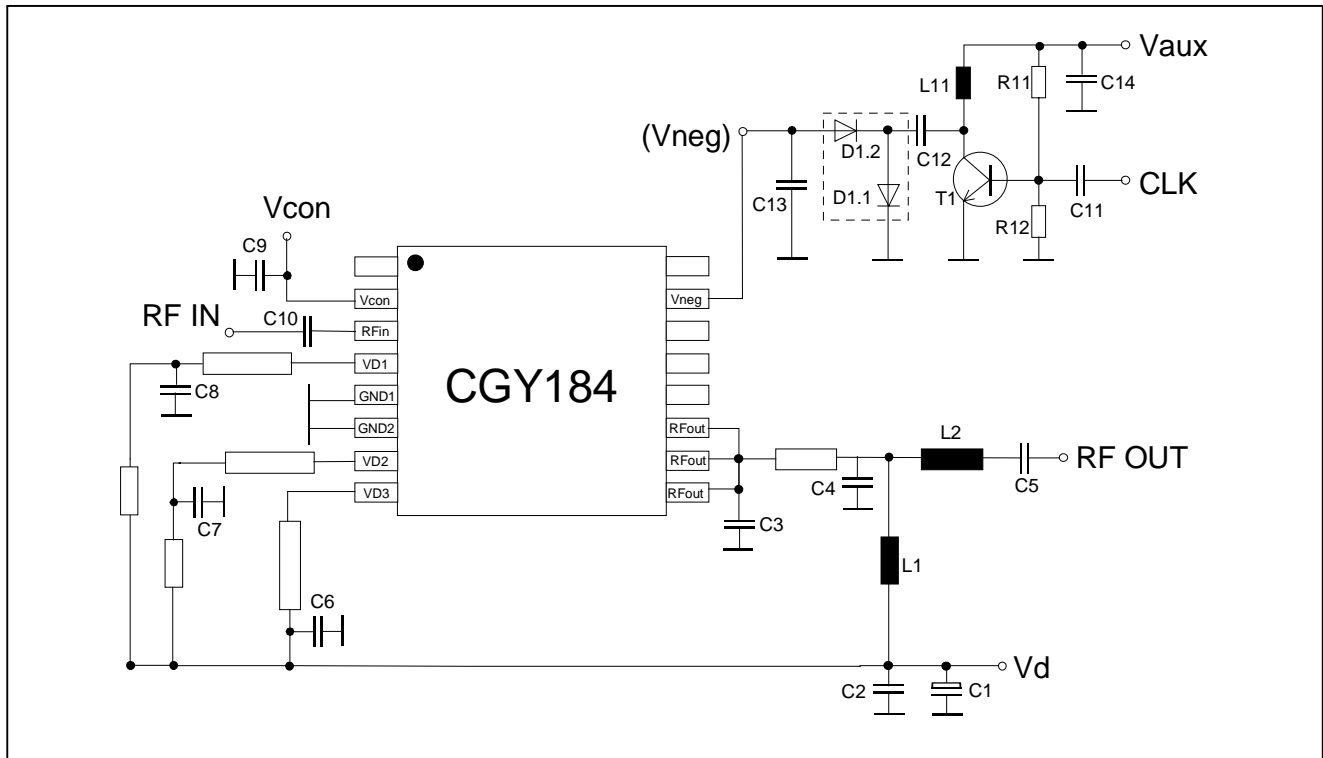
- Vd 2.7 to 6VDC, pulsed (PCN: 12,5% duty cycle, $t_{on}=0.577ms$)
- Vaux 2.7 to 6VDC
- Vcontrol 0.2 to 2.2VDC (0.2V: min Pout, 2.2V: max Pout)
- CLK 5 MHz to 15 MHz (with a 10uH inductor)
or 150 kHz to 250 kHz (with a 100uH inductor instead of the 10uH)
(rectangular signal, 50% duty, 0 Volt to Vd voltage level)

Power on sequence:

1. continuous clock (CLK) on
2. turn on Vaux ==> check negative voltage at pin#16 (-4.....-10V)
3. turn on Vcon (may be at the same time as 2)
turn on Drainvoltage Vd
turn on Input Power

Operation without using the negative voltage generator:

If you don't want to use the internal negative voltage generator, you can also apply -4....-6 V at pin#15 (Vneg-Pin). In this case the passive devices at the pins 1, 14 and 16 are not necessary (1 inductor and 3 capacitors).



Part List:

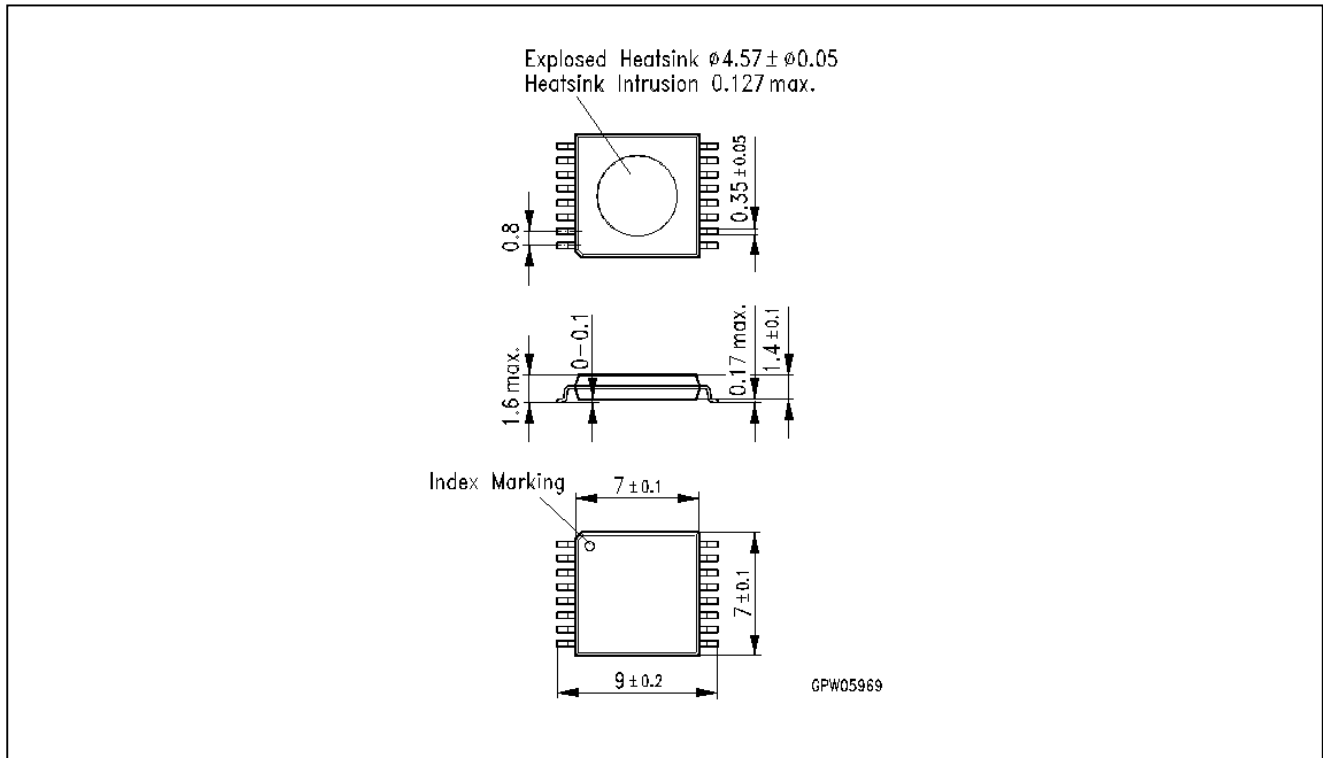
CGY184		Negative Voltage Generator	
L1	33nH*	D1	BAS40-04W
L2	2.2nH**	T1	BC848B
C1	4.7μF	L11	10uH***
C2	120pF	C11	1nF
C3	5pF	C12	1nF
C4	1pF	C13	47nF
C5	33pF	C14	1nF
C6	1nF	R11	3.8kOhm
C7	330pF	R12	680Ohm
C8	15pF		
C9	1nF		
C10	33pF		

* 33nH SMD-Inductor for drain3: Part Number BV1250 distribution by Horst David GmbH, 85375 Neufarn, Germany
Phone-No ..8165/9548-0 , Fax-No ..8165/9548-28

** Toko Type LL1608-FH Chip Induktor

*** Chip-Induktor Simid02
(Siemens-Matsushita Ordering-Code: B82422-A1103-K100)

Semiconductor Device Outline MW16



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