

DATA SHEET

CGY2010G; CGY2011G GSM 4 W power amplifiers

Objective specification
Supersedes data of 1995 Oct 25
File under Integrated Circuits, IC17

1996 Jul 08

GSM 4 W power amplifiers**CGY2010G; CGY2011G****FEATURES**

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < -129 dBm/Hz in GSM RX band
- Wide operating temperature range -20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

GENERAL DESCRIPTION

The CGY2010G and CGY2011G are GSM class 4 GaAs Monolithic Microwave Integrated Circuits (MMICs) power amplifiers specifically designed to operate at 4.8 V battery supply. These ICs also include a power sensor driver so that no directional coupler is required in the power control loop.

Both ICs have the same performance but are issued from different wafer fabs.

The PAs require only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. They can be switched off and their power controlled by monitoring the actual drain voltage applied to the amplifier stages.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz TDMA systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER ⁽¹⁾	MIN.	TYP.	MAX.	UNIT
V _{DD}	positive supply voltage	–	4.2	–	V
I _{DD}	positive peak supply current	–	1.8	–	A
P _{out(max)}	maximum output power	–	35.5	–	dBm
T _{amb}	operating ambient temperature	–20	–	+85	°C

Note

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

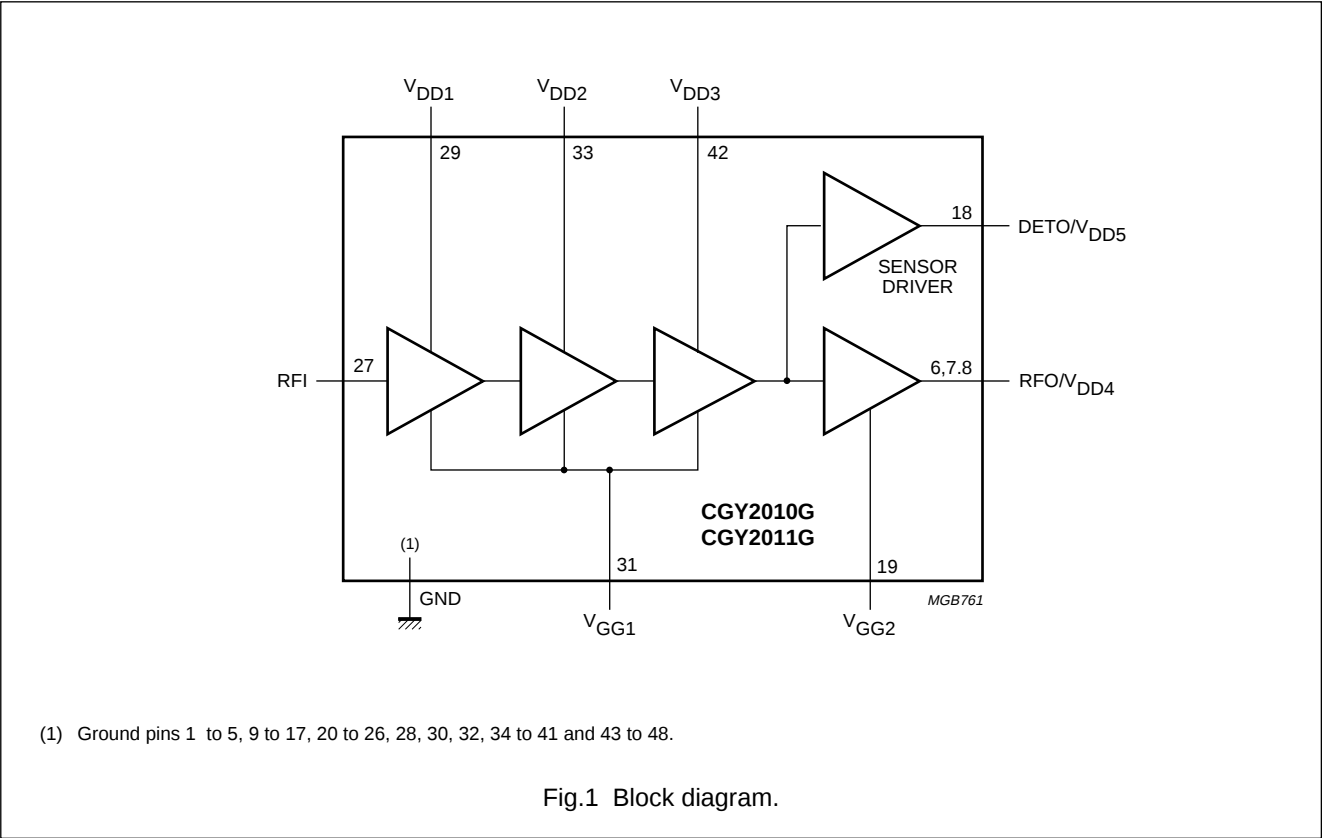
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2010G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
CGY2011G			

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BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V _{DD4}	6 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V _{DD5}	18	power sensor output and supply voltage
V _{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V _{DD1}	29	first stage supply voltage
GND	30	ground
V _{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V _{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V _{DD3}	42	third stage supply voltage
GND	43 to 48	ground

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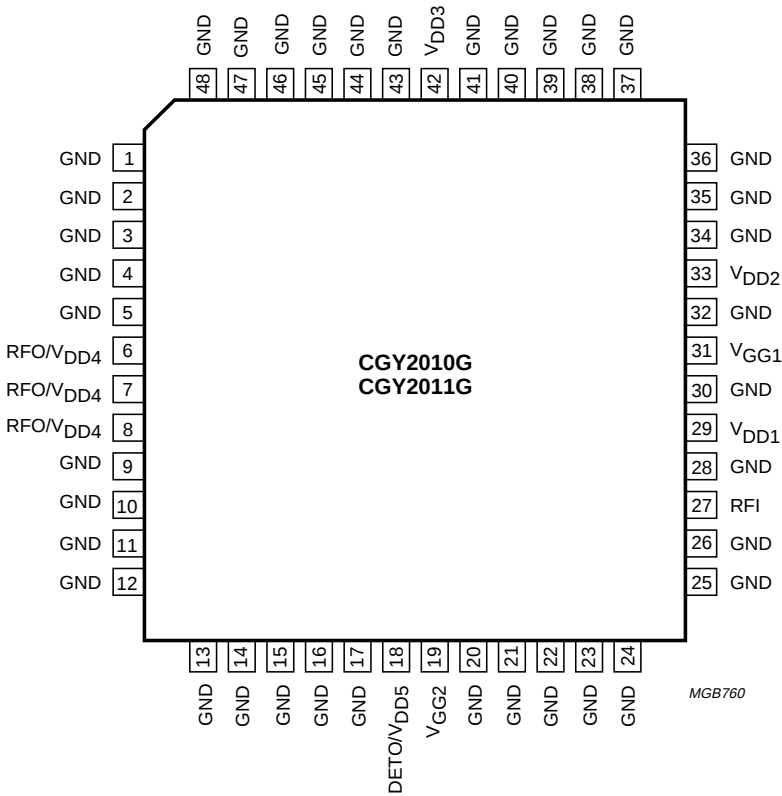


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION**Operating conditions**

The CGY2010G and CGY2011G are designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the "ETTS 300 577 specification", which are defined as follows:

- $t_{on} = 542.8 \mu s$
- $T = 4.3 ms$
- Duty cycle = 1/8

The devices are specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by means of a negative voltage applied at pins V_{GG1} and V_{GG2} . This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

Impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th j-c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

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DC CHARACTERISTICS

$V_{DD} = 4.5 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	4.2	5.5	V
I_{DD}	positive peak supply current		–	1.8	2.2	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

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AC CHARACTERISTICS

$V_{DD} = 4.5 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_{in}	input power		-1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	-6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{out(max)}$	maximum output power	$T_{amb} = 25 \text{ }^{\circ}\text{C}$; $V_{DD} = 4.5 \text{ V}$	34.5	35.5	–	dBm
		$T_{amb} = -20 \text{ to } +85 \text{ }^{\circ}\text{C}$; $V_{DD} = 4.2 \text{ V}$	32.5	–	–	dBm
η	efficiency	$V_{DD} = 4.2 \text{ V}$	–	45	–	%
$P_{out(min)}$	minimum output power	$V_{DD} < 0.1 \text{ V}$	–	–	-20	dBm
N_{RX}	output noise in RX band	$f_{RF} = 925 \text{ MHz}$ at $P_{out(max)}$	–	–	-117	dBm/Hz
		$f_{RF} = 935 \text{ MHz}$ at $P_{out(max)}$	–	–	-129	dBm/Hz
		$f_{RF} = 960 \text{ MHz}$ at $P_{out(max)}$	–	–	-129	dBm/Hz
H2	2nd harmonic level		–	-33	-30	dBc
H3	3rd harmonic level		–	-40	-37	dBc
Stab	stability	note 2	–	–	-70	dBc
Power sensor driver						
$P_{out(DET)}$	sensor driver output power	$R_L = 100 \text{ } \Omega$; relative to PA output power into 50 Ω load	–	-23	–	dBc
$\Delta P_{out(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

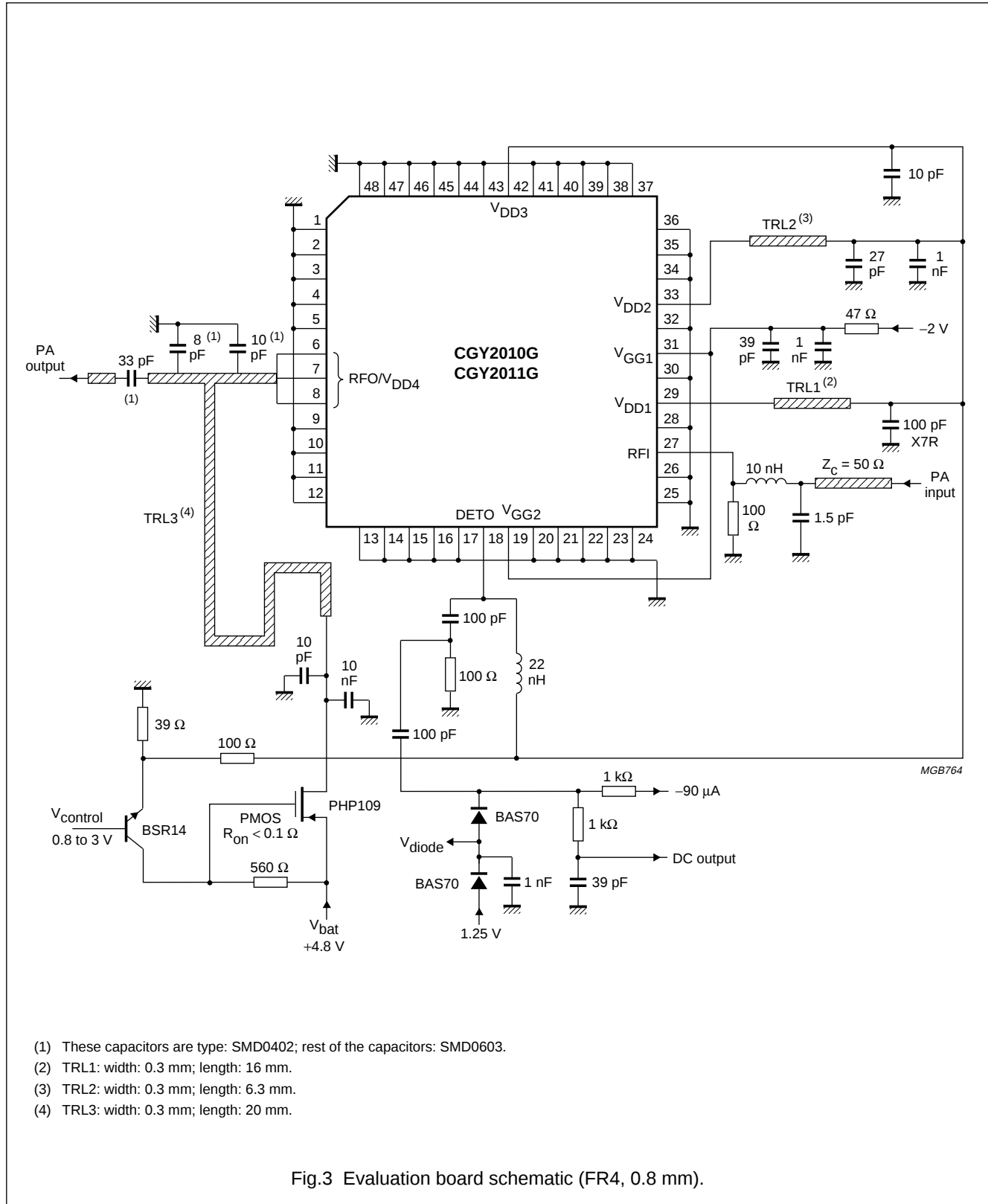
Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

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APPLICATION INFORMATION



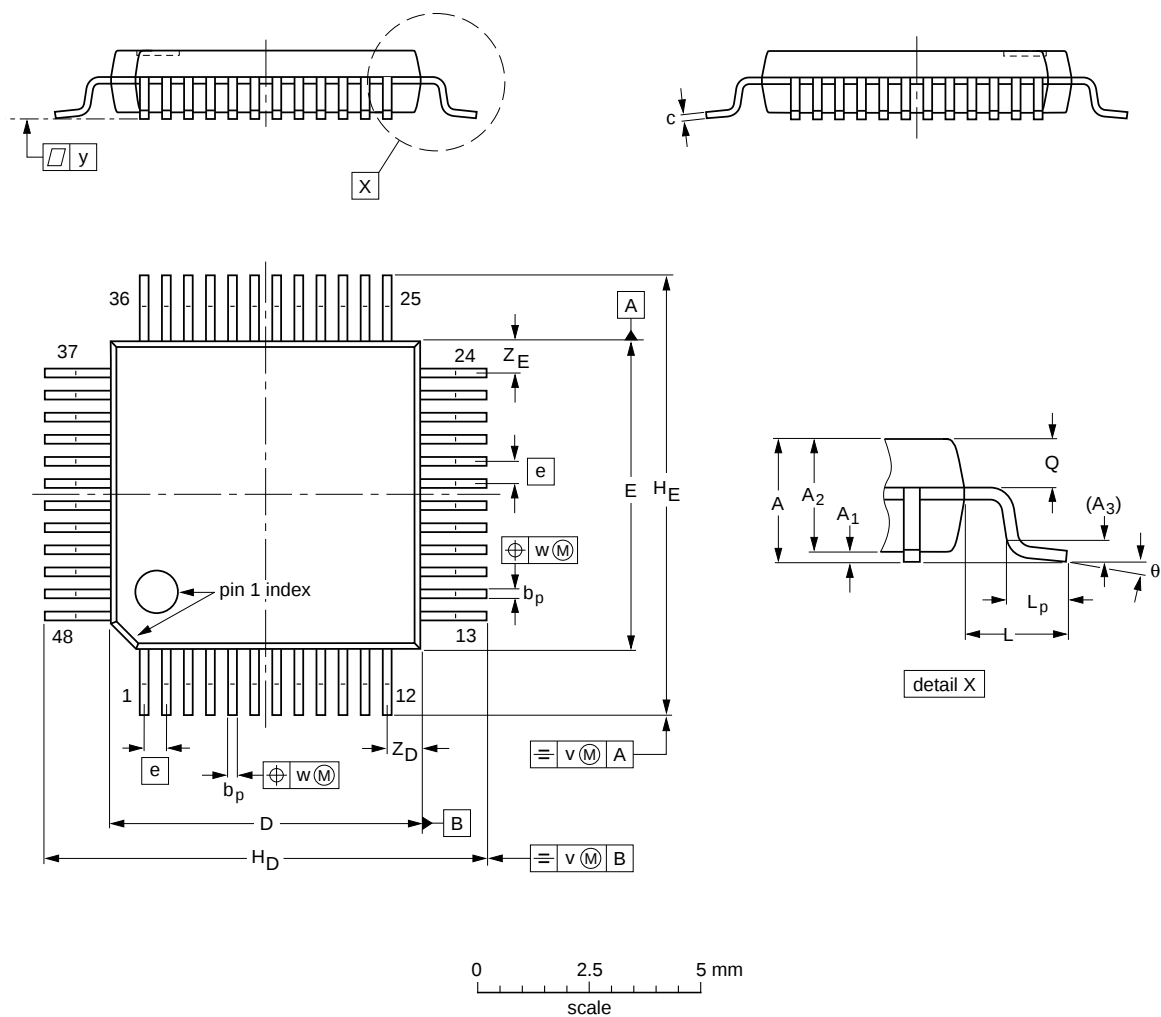
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

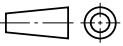


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	Q	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						93-06-15 94-12-19

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoprojekt, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
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Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
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Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
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Middle East: see Italy

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New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
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Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
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Ukraine: PHILIPS UKRAINE, 2A Akademika Koroleva str., Office 165,
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United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

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