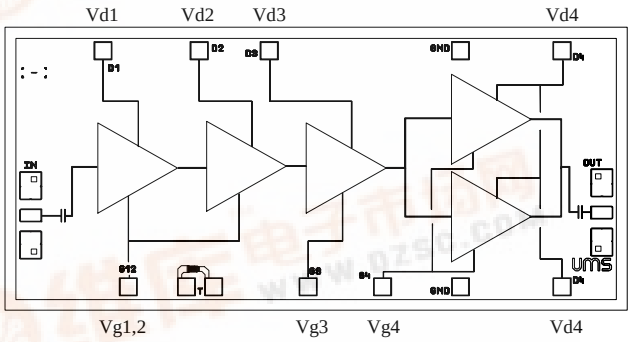
17.7-24GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

Description

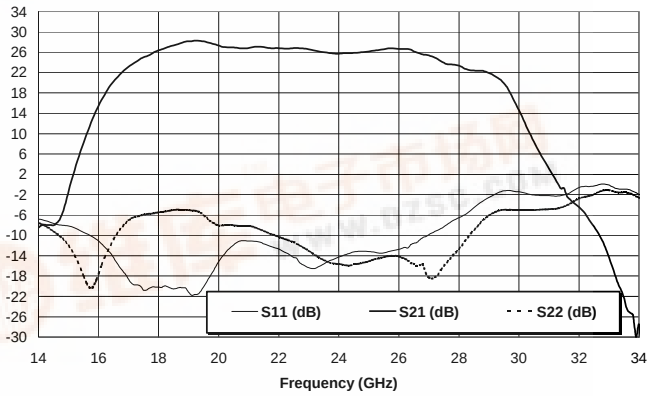
The CHA5290 is a high gain four-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Performances : 17.7 -24GHz
- 26dBm output power @ 1dB comp. gain
- 26 dB ± 1dB gain
- DC power consumption, 400mA @ 6V
- Chip size : 3.43 x 1.57 x 0.05 mm



Typical on jig Measurements

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17.7		24	GHz
G	Small signal gain		26		dB
P1dB	Output power at 1dB gain compression		26		dBm
Id	Bias current		400		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - B.P.46 - 91401 Orsay Cedex France
Tel. : +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Electrical Characteristics

Tamb = +25°C, Vd = 6V Id =400mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	17.7		24	GHz
G	Small signal gain (1)	24	26		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation		40		dB
P1dB	Pulsed output power at 1dB compression (1)	25	26		dBm
P03	Output power at 3dB gain compression (1)		27		dBm
PAE	Power added efficiency at 1dB comp.		18		%
VSWRin	Input VSWR (2)		3:1		
VSWRout	Output VSWR (2)		3:1		
Tj	Junction temperature for 80°C backside		165		°C
Id	Bias current @ small signal		400	500	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.
(2) Value representative for CW on jig measurement.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage with Pin max=-2dBm	6.25	V
Id	Maximum drain bias current	625	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Ig	Gate bias current	-2.5 to +2.5	mA
Vgd	Minimum negative gate drain voltage (Vg - Vd)	-8	V
Pin	Maximum input power overdrive (2)	3	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

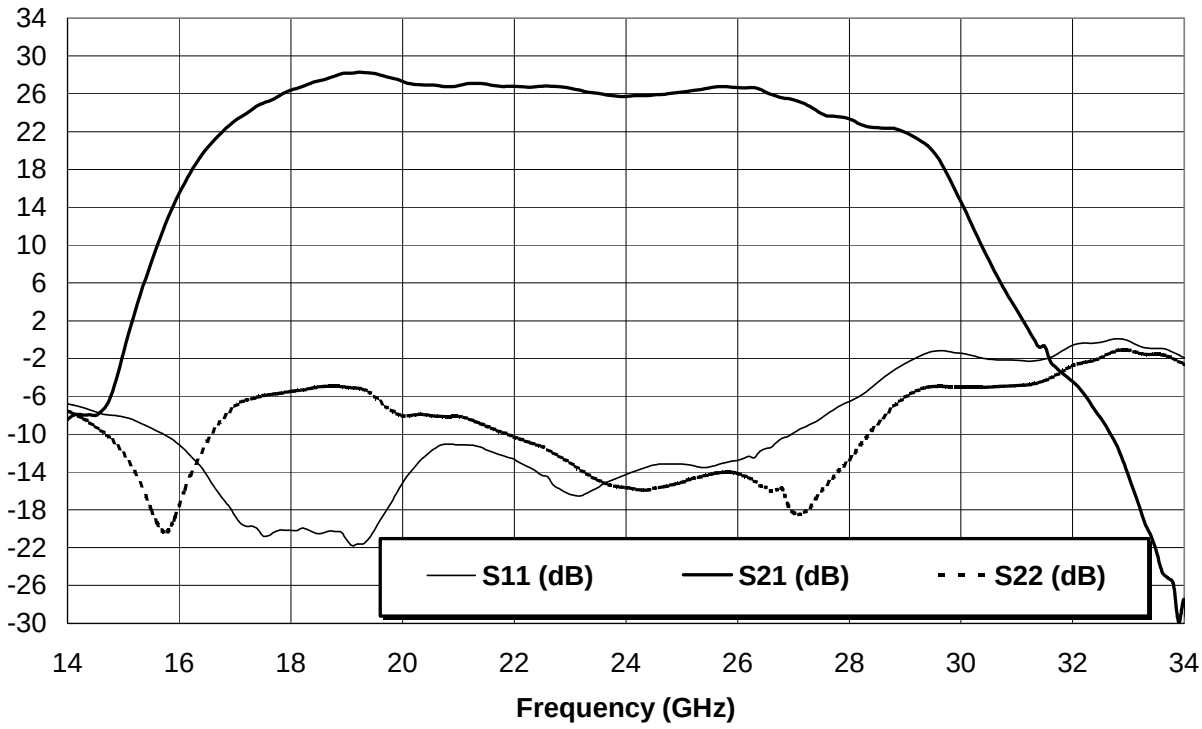
(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Route Départementale 128 , B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

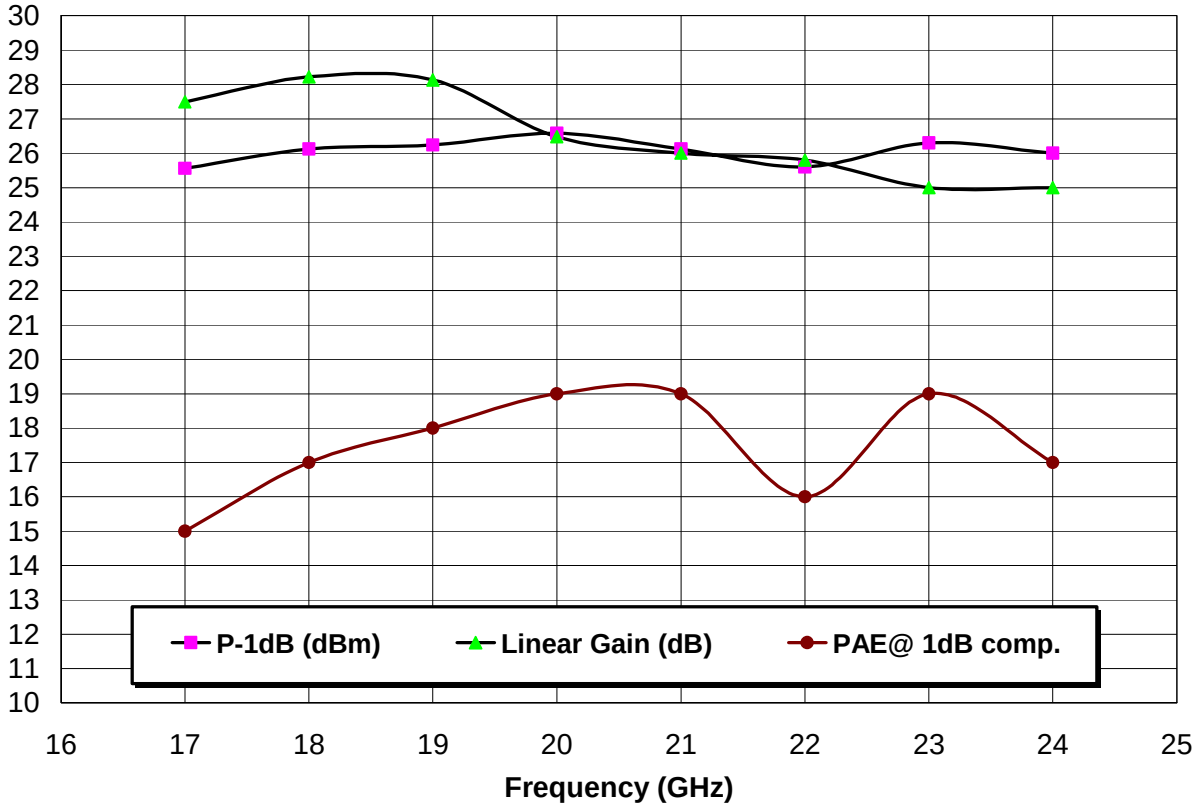
Typical on Jig Measurements

Bias conditions: Vd=6V, Vg tuned for Id = 400mA

Linear Gain & Return Losses versus frequency

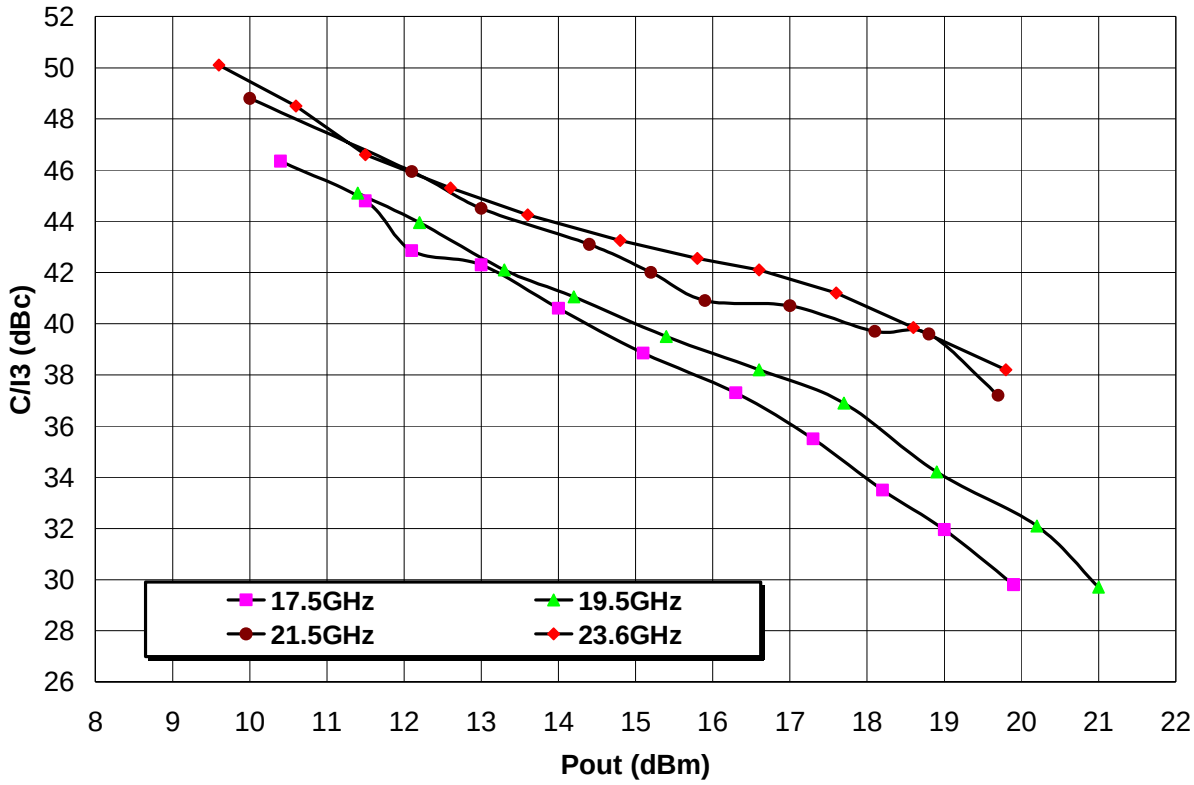


Linear Gain, Output power & associated PAE at 1dB compression versus frequency



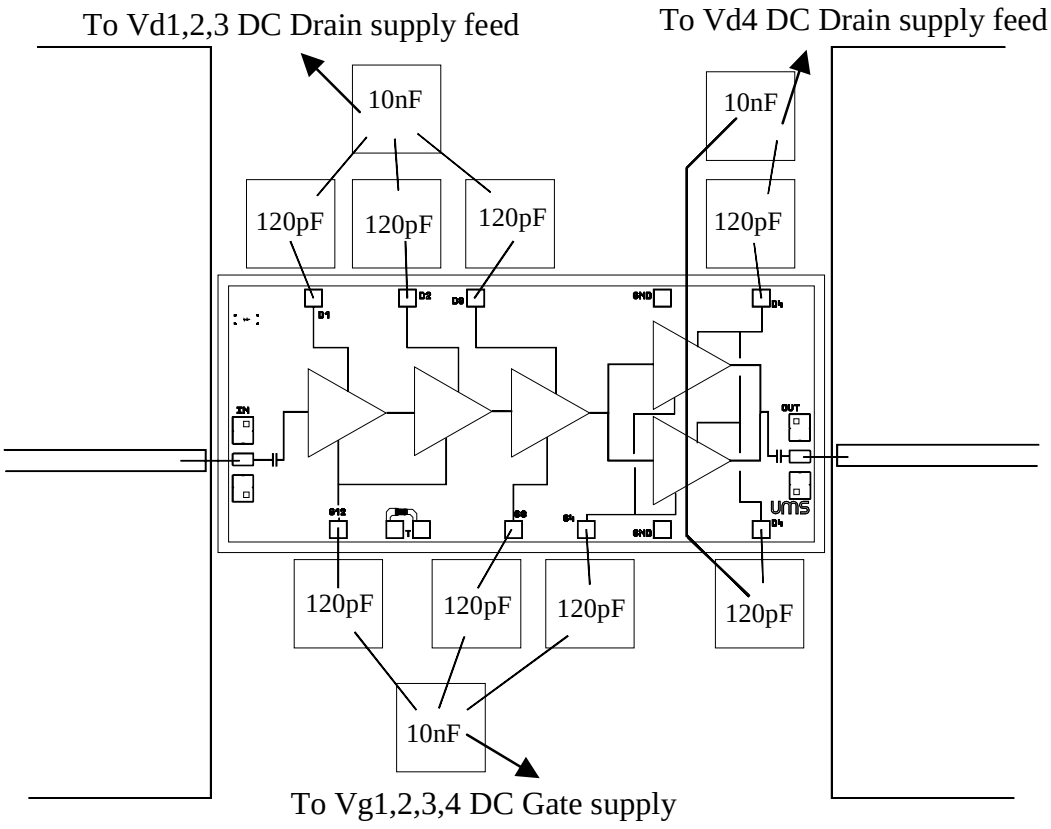
Route Départementale 128 , B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

C/I3 versus total output power (ΔF =10MHz)

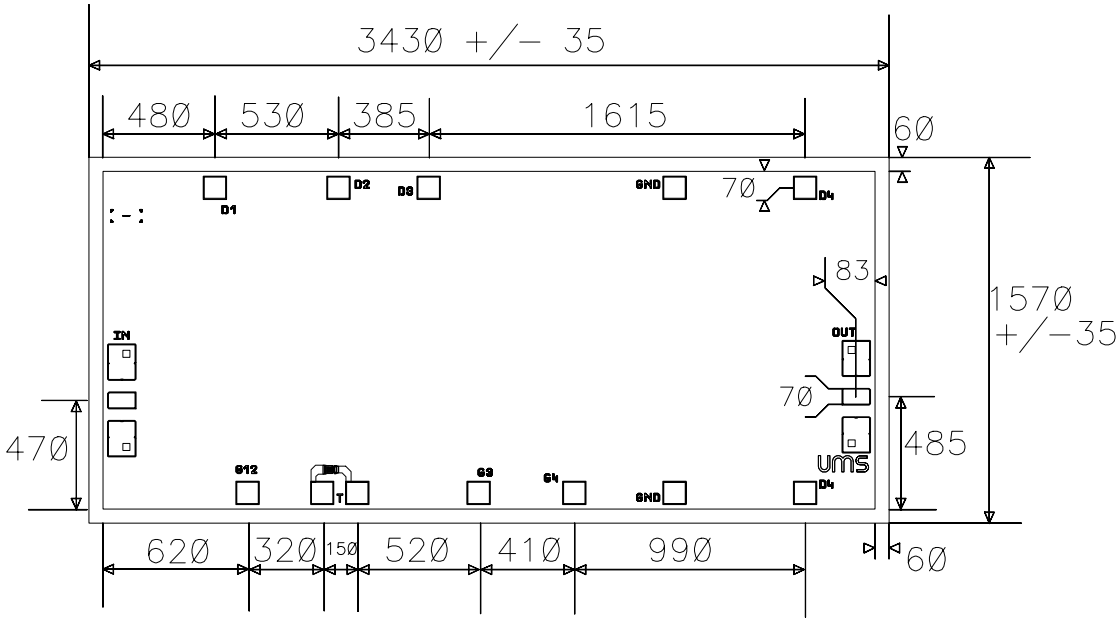


Route Départementale 128 , B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.



Bonding pad positions.

(Chip thickness : 50µm. All dimensions are in micrometers)

Route Départementale 128 , B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Application note

Bias operation sequence:

ON: Supply Gate voltage
Supply Drain voltage
OFF: Cut off Drain voltage
Cut off Gate voltage

Due to 50µm thickness, specific care is requested for the handling and assembly.

Ordering Information

Chip form : CHA5290-99F/00

Route Départementale 128 , B.P.46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09