

18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES094C – FEBRUARY 1997 – REVISED JUNE 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **A-Port Outputs Have Equivalent 50-Ω Series Resistors and B-Port Outputs Have Equivalent 20-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Very Small-Outline Package**

NOTE: For order entry:
The DBB package is abbreviated to G.

For tape and reel:
The DBBR package is abbreviated to GR.

description

The SN74ALVCHG162282 is an 18-bit to 36-bit registered bus exchanger. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select (SEL) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output-enable ($\overline{OE}$) and direction-control (DIR) input. DIR is registered to synchronize the bus direction changes with the clock.

DBB PACKAGE
(TOP VIEW)

V _{CC}	1	80	V _{CC}
GND	2	79	GND
2B9	3	78	1B10
1B9	4	77	2B10
2B8	5	76	1B11
GND	6	75	GND
1B8	7	74	2B11
2B7	8	73	1B12
1B7	9	72	2B12
V _{CC}	10	71	V _{CC}
2B6	11	70	1B13
1B6	12	69	2B13
2B5	13	68	1B14
1B5	14	67	2B14
GND	15	66	GND
2B4	16	65	1B15
1B4	17	64	2B15
2B3	18	63	1B16
1B3	19	62	2B16
V _{CC}	20	61	V _{CC}
GND	21	60	GND
2B2	22	59	1B17
1B2	23	58	2B17
2B1	24	57	1B18
1B1	25	56	2B18
V _{CC}	26	55	V _{CC}
A1	27	54	A18
A2	28	53	A17
A3	29	52	A16
GND	30	51	GND
A4	31	50	A15
A5	32	49	A14
A6	33	48	A13
V _{CC}	34	47	V _{CC}
A7	35	46	A12
A8	36	45	A11
A9	37	44	A10
GND	38	43	GND
CLK	39	42	$\overline{OE}$
SEL	40	41	DIR

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description (continued)

The A-port N-channel output transistors are sized at 450 μm and the P-channel output transistors are sized at 700 μm . All A-port outputs have equivalent 50- Ω series resistors. The B-port N-channel output transistors are sized at 225 μm , and the P-channel output transistors are sized at 560 μm . All B-port outputs have equivalent 20- Ω series resistors.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The switching characteristics are based on 25-pF (A port) and 80-pF (B port) loads, but are tested with the standard 50-pF load.

The SN74ALVCHG162282 is characterized for operation from 0°C to 70°C.

Function Tables

A-TO-B STORAGE
($\overline{\text{OE}} = \text{L}$, $\text{DIR} = \text{H}$)

INPUTS			OUTPUTS	
$\overline{\text{SEL}}$	CLK	A	1B	2B
H	X	X	1B ₀ [†]	2B ₀ [†]
L	↑	L	L [‡]	L
L	↑	H	H [‡]	H

[†] Output level before indicated steady-state input conditions were established

[‡] Two CLK edges are needed to propagate the data.

B-TO-A STORAGE
($\overline{\text{OE}} = \text{L}$, $\text{DIR} = \text{L}$)

INPUTS				OUTPUT A
CLK	$\overline{\text{SEL}}$	1B	2B	
↑	H	X	L	L [§]
↑	H	X	H	H [§]
↑	L	L	X	L
↑	L	H	X	H

[§] Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{\text{SEL}}$ is low and propagates to the second register when $\overline{\text{SEL}}$ is high.

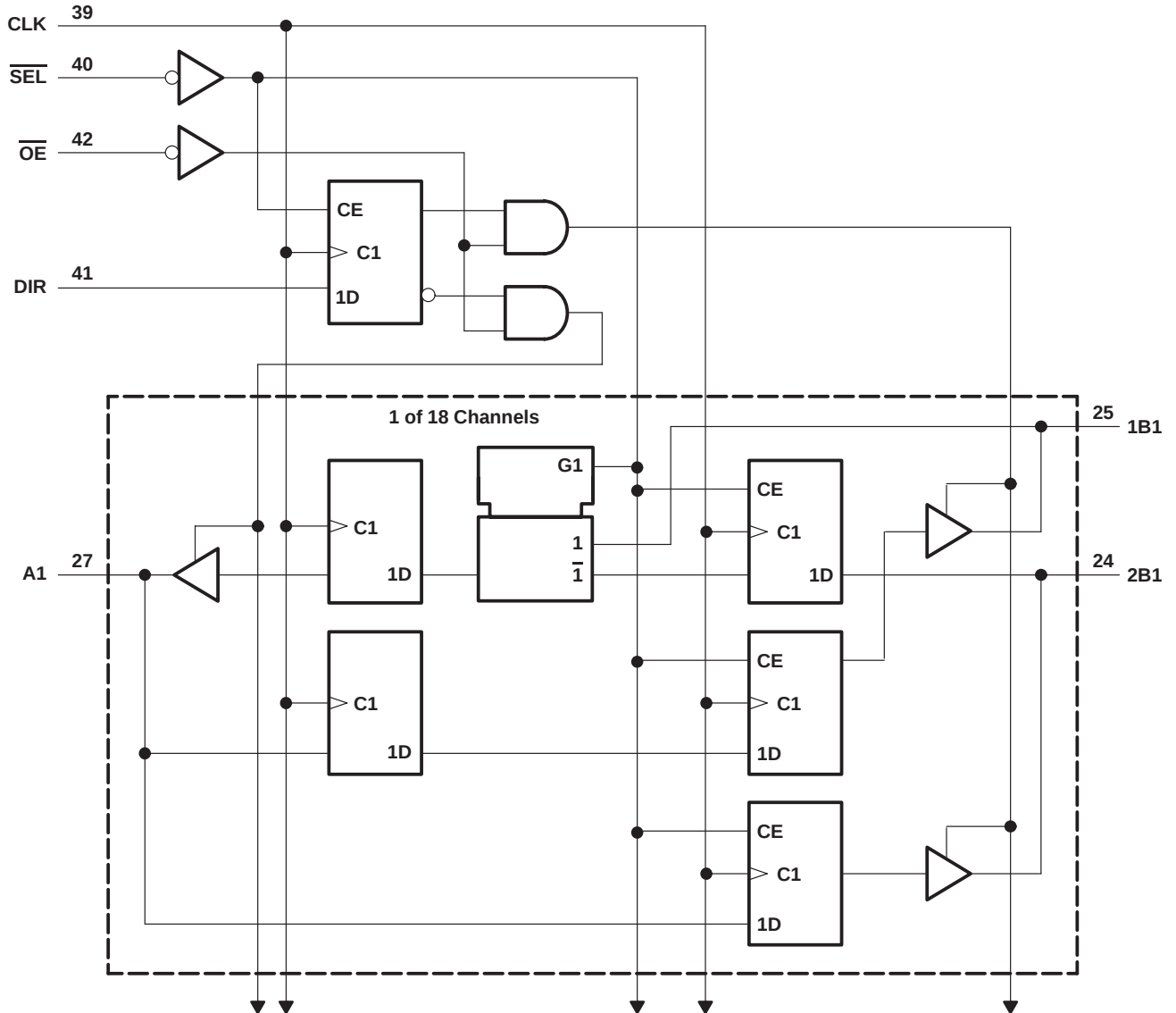
OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{\text{OE}}$	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	H	Z	Active
↑	L	L	Active	Z

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
 3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

				MIN	MAX	UNIT
V _{CC}	Supply voltage			3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V		2		V
V _{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V			0.8	V
V _I	Input voltage			0	V _{CC}	V
V _O	Output voltage			0	V _{CC}	V
I _{OH}	High-level output current	A to B	V _{CC} = 3 V	8		mA
		B to A	V _{CC} = 3 V	6		
I _{OL}	Low-level output current	A to B	V _{CC} = 3 V	8		mA
		B to A	V _{CC} = 3 V	6		
Δt/Δv	Input transition rise or fall rate			10		ns/V
T _A	Operating free-air temperature			0	70	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = –100 μA	3 V to 3.6 V	V _{CC} –0.2		V	
	A to B	I _{OH} = –8 mA	3 V	2			
	B to A	I _{OH} = –6 mA	3 V	2			
V _{OL}		I _{OL} = 100 μA	3 V to 3.6 V	0.2		V	
	A to B	I _{OL} = 8 mA	3 V	0.8			
	B to A	I _{OL} = 6 mA	3 V	0.8			
I _I		V _I = V _{CC} or GND	3.6 V	±5		μA	
I _I (hold)		V _I = 0.8 V	3 V	75		μA	
		V _I = 2 V	3 V	–75			
		V _I = 0 to 3.6 V [‡]	3.6 V	±500			
I _{OZ} [§]		V _O = V _{CC} or GND	3.6 V	±10		μA	
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	40		μA	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750		μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4		pF	
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	8.5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
f _{clock}	Clock frequency		160		MHz
t _w	Pulse duration, CLK high or low		2.3		ns
t _{su}	Setup time, high or low	A data before CLK↑	1.5		ns
		B data before CLK↑	2		
		DIR before CLK↑	2		
		$\overline{\text{SEL}}$ before CLK↑	2		
t _h	Hold time, high or low	A data after CLK↑	0.3		ns
		B data after CLK↑	0.3		
		DIR after CLK↑	0.3		
		$\overline{\text{SEL}}$ after CLK↑	0.3		

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switching characteristics over recommended operating free-air temperature range,
 $C_L = 25\text{ pF}$ (A port), 80 pF (B port) (unless otherwise noted) (see Figure 1)

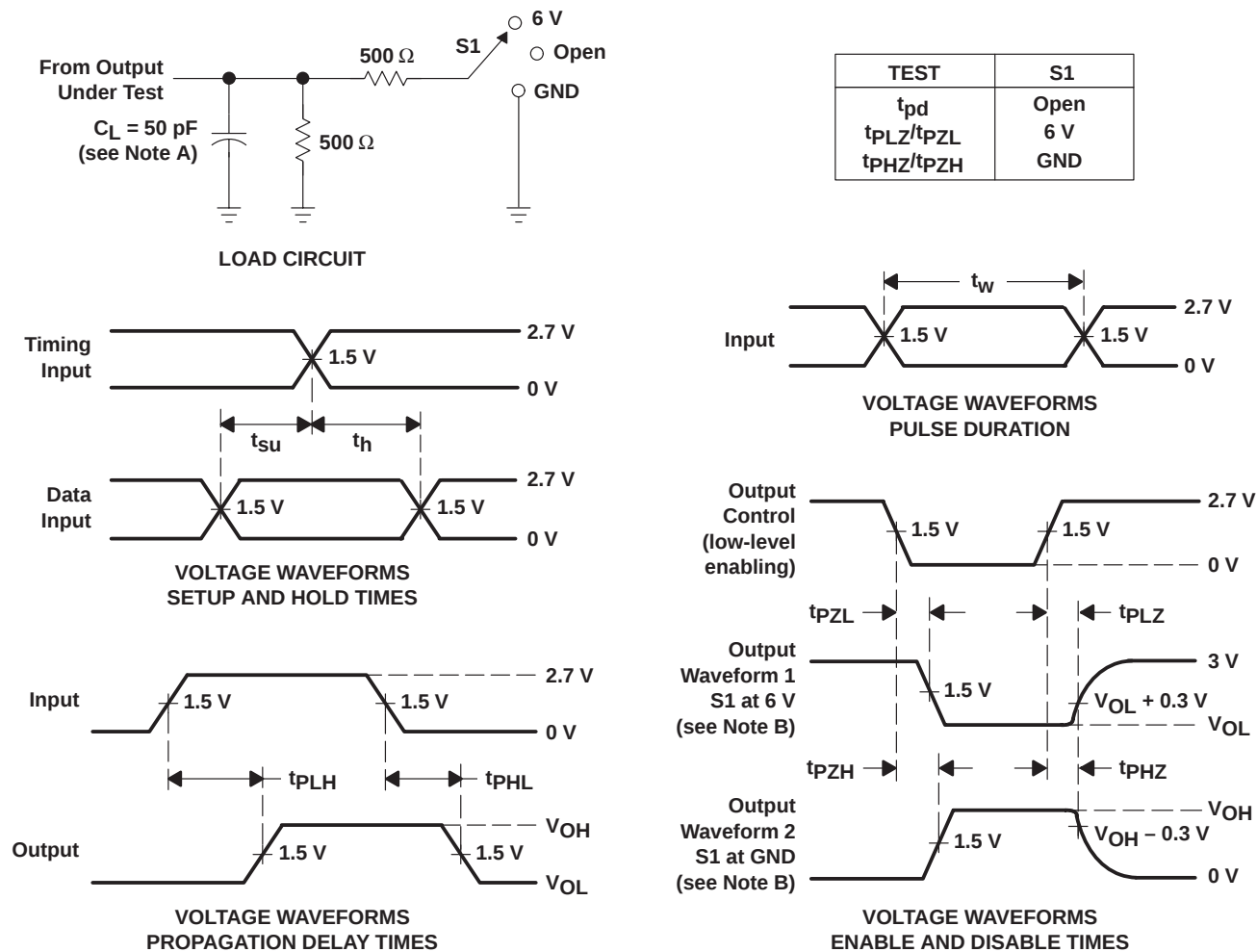
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	
f_{max}			160		MHz
t_{pd}	CLK	A	1.5	5	ns
		B	1.5	7.4	
t_{en}	CLK	A	1.5	6.3	ns
		B	1.5	9.4	
	$\overline{OE}$	A	1.5	6	
		B	1.5	9.5	
t_{dis}	CLK	A	1.5	6.4	ns
		B	1.5	7.8	
	$\overline{OE}$	A	1.5	5	
		B	1.5	7.6	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The output is measured with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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