PCI2060 Asynchronous PCI-to-PCI Bridge

Data Manual

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- **Fully Supports *Advanced Configuration Power Interface (ACPI) Specification***
- **Architecture Configurable for *PCI Bus Power Management Interface Specification*, Revision 1.0 and Revision 1.1**
- **Two 32-Bit, 66-MHz Asynchronous PCI Buses**
- **1.8-V Core Logic with Universal PCI Interface Compatible with 3.3-V and 5-V PCI Signaling Environments**
- **Provides Concurrent Primary and Secondary Bus Operations**
- **Independent Read and Write Buffers for Each Direction**
- **Burst Data Transfers With Pipeline Architecture To Maximize Data Throughput In Both Directions**
- **Up To Three Delayed Transactions For All PCI Configuration, I/O, and Memory Read Commands In Both Directions**
- **Provides 10 Secondary PCI Bus Clock Outputs**
- **Provides Internal Two-Tier Arbitration For Up To Nine Secondary Bus Masters**
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- **Provides an IEEE Standard 1149.1 Joint Test Action Group (JTAG) Interface**
- **Packaged in 257-Terminal PBGA Package**

2 Introduction

2.1 Description

The Texas Instruments PCI2060 is a 32-bit, asynchronous, PCI-to-PCI bridge that is fully compliant with the *PCI Local Bus Specification*, Revision 2.3 and the *PCI-to-PCI Bridge Specification*, Revision 1.1. The PCI2060 bridge makes it possible for the primary and secondary bus clocks to be completely asynchronous and supports the PCI clock frequency up to 66 MHz.

The PCI2060 bridge is architecture-configurable for the *PCI Bus Power Interface Specification*. It can be configured to support either revision 1.0 or revision 1.1. Power conservation is made possible by using 1.8-V core logic with a universal PCI interface compatible with 3.3-V and 5-V PCI signaling environments.

The PCI2060 bridge allows the primary and secondary buses to operate concurrently. It provides independent read and write buffers for each direction and utilizes pipeline architecture for burst data transfer.

The PCI2060 bridge makes it possible to overcome the electrical loading limit of ten devices per PCI bus and one PCI device per expansion slot by creating hierarchical buses. Each PCI2060 bridge that is added to the system creates a new PCI bus. The PCI2060 bridge provides a two-tier internal arbitration for up to nine secondary bus masters and may be implemented with an external arbiter.

The PCI2060 bridge provides CompactPCI hot-swap support that is compliant with the *PICMG CompactPCI Hot-Swap Specification,* Revision 1.0.

2.2 Related Documents

- *Advanced Configuration and Power Interface (ACPI) Specification,* Revision 2.0
- *PCI Local Bus Specification,* Revision 2.3
- *PCI-to-PCI Bridge Specification,* Revision 1.1
- *PCI Bus Power Management Interface Specification,* Revision 1.1
- *PICMG CompactPCI Hot-Swap Specification,* Revision 1.0
- *IEEE Standard Test Access Port and Boundary-Scan Architecture*

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- CompactPCI is a trademark of PICMG – PCI Industrial Computer Manufacturers Group, Inc.
- Intel is a trademark of Intel Corporation.
- TI and MicroStar BGA are trademarks of Texas Instruments
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2.4 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{P\_RST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. RSVD indicates that the referenced item is reserved.

2.5 Ordering Information

ORDERING NUMBER	VOLTAGE	TEMPERATURE	PACKAGE
PCI2060	3.3-V, 5-V tolerant I/Os	0^0C to 70^0C	257-terminal GHK
PCI2060I	3.3-V, 5-V tolerant I/Os	−40^0C to 85^0C	257-terminal GHK

2.6 Terminal Assignments

The PCI2060 bridge is packaged in a 257-terminal GHK MicroStar BGA™. Figure 2−1 is a GHK-package terminal diagram.

Table 2−1 lists the terminal assignments in terminal-number order with corresponding signal names for the GHK package. Table 2−2 lists the terminal assignments arranged in alphanumerical order by signal name with corresponding terminal numbers for the GHK package.

Terminal E5 on the GHK package is an identification ball used for device orientation.

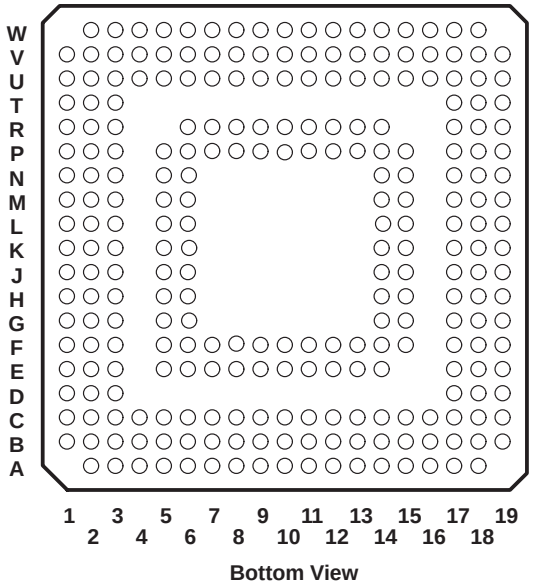


Figure 2−1. PCI2060 GHK-Package Terminal Diagram

Table 2−1. 257-Terminal GHK Signal Names Sorted by Terminal Number

GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME
A2	NC	C8	V_{CC}	F11	$\overline{\text{S\_FRAME}}$	K14	TMS
A3	V_{CC}	C9	S_AD18	F12	S_C/$\overline{\text{BE1}}$	K15	V_{CC}
A4	S_AD31	C10	NC	F13	GND	K17	TDO
A5	S_AD28	C11	$\overline{\text{S\_IRDY}}$	F14	S_AD9	K18	TDI
A6	S_AD25	C12	$\overline{\text{S\_LOCK}}$	F15	S_AD10	K19	NC
A7	GND	C13	S_PAR	F17	S_AD8	L1	S_CLKOUT0
A8	S_AD20	C14	V_{CC}	F18	GND	L2	S_CLKOUT1
A9	V_{CC}	C15	GND	F19	S_AD7	L3	NC
A10	S_C/$\overline{\text{BE2}}$	C16	NC	G1	$\overline{\text{S\_GNT3}}$	L5	S_CLKOUT2
A11	$\overline{\text{S\_DEVSEL}}$	C17	NC	G2	$\overline{\text{S\_GNT2}}$	L6	GND
A12	GND	C18	NC	G3	GND	L14	HSLED
A13	V_{CC}	C19	NC	G5	$\overline{\text{S\_REQ8}}$	L15	$\overline{\text{HSENUM}}$
A14	GND	D1	NC	G6	$\overline{\text{S\_REQ3}}$	L17	MASK_IN
A15	S_AD13	D2	V_{CC}	G14	S_AD6	L18	CONFIG66
A16	V_{CC}	D3	NC	G15	S_C/$\overline{\text{BE0}}$	L19	P_VIO
A17	NC	D17	NC	G17	V_{CC}	M1	S_CLKOUT3
A18	NC	D18	SEC_ASYNC_RATE	G18	S_AD5	M2	V_{CC}
B1	NC	D19	GND	G19	S_AD4	M3	S_CLKOUT4
B2	NC	E1	$\overline{\text{S\_REQ5}}$	H1	$\overline{\text{S\_GNT7}}$	M5	GND
B3	NC	E2	$\overline{\text{S\_REQ4}}$	H2	$\overline{\text{S\_GNT6}}$	M6	S_CLKOUT5
B4	$\overline{\text{S\_REQ0}}$	E3	$\overline{\text{S\_REQ1}}$	H3	$\overline{\text{S\_GNT5}}$	M14	P_AD4
B5	S_AD29	E5	NC	H5	$\overline{\text{S\_GNT4}}$	M15	V_{CC}
B6	S_AD26	E6	S_AD30	H6	$\overline{\text{S\_GNT1}}$	M17	P_AD1
B7	S_C/$\overline{\text{BE3}}$	E7	GND	H14	S_AD3	M18	P_AD0
B8	S_AD21	E8	S_AD23	H15	GND	M19	GND
B9	NC	E9	GND	H17	S_AD2	N1	S_CLKOUT6
B10	GND	E10	S_AD16	H18	V_{CC}	N2	S_CLKOUT7
B11	$\overline{\text{S\_TRDY}}$	E11	V_{CC}	H19	S_AD1	N3	V_{CC}
B12	$\overline{\text{S\_STOP}}$	E12	$\overline{\text{S\_PERR}}$	J1	$\overline{\text{S\_GNT8}}$	N5	BPCCE
B13	$\overline{\text{S\_SERR}}$	E13	S_AD15	J2	GND	N6	S_CLKOUT8
B14	S_AD14	E14	S_AD11	J3	S_CLK	N14	P_AD8
B15	S_AD12	E17	MS0	J5	$\overline{\text{S\_RST}}$	N15	V_{CC}
B16	NC	E18	S_M66ENA	J6	$\overline{\text{S\_CFN}}$	N17	GND
B17	NC	E19	V_{CC}	J14	GND	N18	P_AD3
B18	NC	F1	$\overline{\text{S\_GNT0}}$	J15	S_AD0	N19	P_AD2
B19	NC	F2	$\overline{\text{S\_REQ7}}$	J17	S_VIO	P1	S_CLKOUT9
C1	SEC_ASYNC_CLK	F3	$\overline{\text{S\_REQ6}}$	J18	$\overline{\text{TRST}}$	P2	$\overline{\text{P\_RST}}$
C2	NC	F5	$\overline{\text{S\_REQ2}}$	J19	TCK	P3	P_CLK
C3	NC	F6	V_{CC}	K1	GPIO3/$\overline{\text{HSSWITCH}}$	P5	GND
C4	SEC_ASYNC_SEL	F7	V_{CC}	K2	GPIO2	P6	$\overline{\text{P\_REQ}}$
C5	GND	F8	S_AD22	K3	V_{CC}	P7	V_{CC}
C6	S_AD27	F9	S_AD19	K5	GPIO1	P8	V_{CC}
C7	S_AD24	F10	S_AD17	K6	GPIO0	P9	P_AD18

Table 2−1. 257-Terminal GHK Signal Names Sorted by Terminal Number (Continued)

GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME
P10	P_C/$\overline{BE2}$	R18	P_C/$\overline{BE0}$	U15	P_AD10	V18	NC
P11	$\overline{P\_TRDY}$	R19	GND	U16	NC	V19	NC
P12	$\overline{P\_LOCK}$	T1	P_AD30	U17	NC	W2	NC
P13	P_C/$\overline{BE1}$	T2	V_{CC}	U18	NC	W3	NC
P14	P_AD12	T3	NC	U19	NC	W4	V_{CC}
P15	V_{CC}	T17	NC	V1	NC	W5	P_AD28
P17	P_AD7	T18	V_{CC}	V2	NC	W6	P_AD25
P18	P_AD6	T19	MS1	V3	NC	W7	P_IDSEL
P19	P_AD5	U1	GND	V4	NC	W8	V_{CC}
R1	$\overline{P\_GNT}$	U2	NC	V5	NC	W9	P_AD21
R2	NC	U3	NC	V6	GND	W10	V_{CC}
R3	P_AD31	U4	NC	V7	P_C/$\overline{BE3}$	W11	$\overline{P\_FRAME}$
R6	P_AD29	U5	GND	V8	P_AD22	W12	$\overline{P\_STOP}$
R7	P_AD26	U6	P_AD27	V9	P_AD20	W13	$\overline{P\_SERR}$
R8	GND	U7	P_AD24	V10	P_AD17	W14	P_AD15
R9	P_AD19	U8	P_AD23	V11	V_{CC}	W15	V_{CC}
R10	GND	U9	GND	V12	NC	W16	P_M66ENA
R11	$\overline{P\_DEVSEL}$	U10	P_AD16	V13	P_PAR	W17	GND
R12	$\overline{P\_PERR}$	U11	$\overline{P\_IRDY}$	V14	GND	W18	NC
R13	P_AD14	U12	GND	V15	P_AD11		
R14	GND	U13	V_{CC}	V16	V_{CC}		
R17	P_AD9	U14	P_AD13	V17	NC		

Table 2−2. 257-Terminal GHK Signal Names Sorted Alphabetically

SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER
BPCCE	N5	NC	A17	NC	W18	$\overline{\text{P\_IRDY}}$	U11
CONFIG66	L18	NC	A18	NC	W3	$\overline{\text{P\_LOCK}}$	P12
GND	A7	NC	B1	P_AD0	M18	P_M66ENA	W16
GND	A12	NC	B2	P_AD1	M17	P_PAR	V13
GND	A14	NC	B3	P_AD2	N19	$\overline{\text{P\_PERR}}$	R12
GND	B10	NC	B9	P_AD3	N18	$\overline{\text{P\_REQ}}$	P6
GND	C5	NC	B16	P_AD4	M14	$\overline{\text{P\_RST}}$	P2
GND	C15	NC	B17	P_AD5	P19	$\overline{\text{P\_SERR}}$	W13
GND	D19	NC	B18	P_AD6	P18	$\overline{\text{P\_STOP}}$	W12
GND	E7	NC	B19	P_AD7	P17	$\overline{\text{P\_TRDY}}$	P11
GND	E9	NC	C2	P_AD8	N14	P_VIO	L19
GND	F13	NC	C3	P_AD9	R17	S_AD0	J15
GND	F18	NC	C10	P_AD10	U15	S_AD1	H19
GND	G3	NC	C16	P_AD11	V15	S_AD2	H17
GND	H15	NC	C17	P_AD12	P14	S_AD3	H14
GND	J2	NC	C18	P_AD13	U14	S_AD4	G19
GND	J14	NC	C19	P_AD14	R13	S_AD5	G18
GND	L6	NC	D1	P_AD15	W14	S_AD6	G14
GND	M5	NC	D3	P_AD16	U10	S_AD7	F19
GND	M19	NC	D17	P_AD17	V10	S_AD8	F17
GND	N17	NC	E5	P_AD18	P9	S_AD9	F14
GND	P5	NC	K19	P_AD19	R9	S_AD10	F15
GND	R8	NC	L3	P_AD20	V9	S_AD11	E14
GND	R10	NC	R2	P_AD21	W9	S_AD12	B15
GND	R14	NC	T3	P_AD22	V8	S_AD13	A15
GND	R19	NC	T17	P_AD23	U8	S_AD14	B14
GND	U1	NC	U2	P_AD24	U7	S_AD15	E13
GND	U5	NC	U3	P_AD25	W6	S_AD16	E10
GND	U9	NC	U4	P_AD26	R7	S_AD17	F10
GND	U12	NC	U16	P_AD27	U6	S_AD18	C9
GND	V6	NC	U17	P_AD28	W5	S_AD19	F9
GND	V14	NC	U18	P_AD29	R6	S_AD20	A8
GND	W17	NC	U19	P_AD30	T1	S_AD21	B8
GPIO0	K6	NC	V1	P_AD31	R3	S_AD22	F8
GPIO1	K5	NC	V2	P_CLK	P3	S_AD23	E8
GPIO2	K2	NC	V3	P_C/$\overline{\text{BE0}}$	R18	S_AD24	C7
GPIO3/$\overline{\text{HSSWITCH}}$	K1	NC	V4	P_C/$\overline{\text{BE1}}$	P13	S_AD25	A6
$\overline{\text{HSENUM}}$	L15	NC	V5	P_C/$\overline{\text{BE2}}$	P10	S_AD26	B6
HSLED	L14	NC	V12	P_C/$\overline{\text{BE3}}$	V7	S_AD27	C6
MASK_IN	L17	NC	V17	$\overline{\text{P\_DEVSEL}}$	R11	S_AD28	A5
MS0	E17	NC	V18	$\overline{\text{P\_FRAME}}$	W11	S_AD29	B5
MS1	T19	NC	V19	$\overline{\text{P\_GNT}}$	R1	S_AD30	E6
NC	A2	NC	W2	P_IDSEL	W7	S_AD31	A4

Table 2−2. 257-Terminal GHK Signal Names Sorted Alphabetically (Continued)

SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER	SIGNAL NAME	GHK NUMBER
S_CFN	J6	S_GNT1	H6	S_RST	J5	V_{CC}	H18
S_CLK	J3	S_GNT2	G2	S_SERR	B13	V_{CC}	K3
S_CLKOUT0	L1	S_GNT3	G1	S_STOP	B12	V_{CC}	K15
S_CLKOUT1	L2	S_GNT4	H5	S_TRDY	B11	V_{CC}	M2
S_CLKOUT2	L5	S_GNT5	H3	S_VIO	J17	V_{CC}	M15
S_CLKOUT3	M1	S_GNT6	H2	TCK	J19	V_{CC}	N3
S_CLKOUT4	M3	S_GNT7	H1	TDI	K18	V_{CC}	N15
S_CLKOUT5	M6	S_GNT8	J1	TDO	K17	V_{CC}	P7
S_CLKOUT6	N1	S_IRDY	C11	TMS	K14	V_{CC}	P8
S_CLKOUT7	N2	S_LOCK	C12	TRST	J18	V_{CC}	P15
S_CLKOUT8	N6	S_M66ENA	E18	V_{CC}	A3	V_{CC}	T2
S_CLKOUT9	P1	S_PAR	C13	V_{CC}	A9	V_{CC}	T18
S_C/BE0	G15	S_PERR	E12	V_{CC}	A13	V_{CC}	U13
S_C/BE1	F12	S_REQ0	B4	V_{CC}	A16	V_{CC}	V11
S_C/BE2	A10	S_REQ1	E3	V_{CC}	C8	V_{CC}	V16
S_C/BE3	B7	S_REQ2	F5	V_{CC}	C14	V_{CC}	W4
SEC_ASYNC_CLK	C1	S_REQ3	G6	V_{CC}	D2	V_{CC}	W8
SEC_ASYNC_RATE	D18	S_REQ4	E2	V_{CC}	E11	V_{CC}	W10
SEC_ASYNC_SEL	C4	S_REQ5	E1	V_{CC}	E19	V_{CC}	W15
S_DEVSEL	A11	S_REQ6	F3	V_{CC}	F6		
S_FRAME	F11	S_REQ7	F2	V_{CC}	F7		
S_GNT0	F1	S_REQ8	G5	V_{CC}	G17		

2.7 Terminal Descriptions

Table 2−3 through Table 2−12 give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

Table 2−3. PCI Primary Bus Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
P_CLK	P3	I	Primary PCI bus clock. P_CLK provides timing for all transactions on the primary PCI bus. All primary PCI signals are sampled at the rising edge of P_CLK.
P_RST	P2	I	PCI reset. When the primary PCI bus reset is asserted, P_RST causes the bridge to place all output buffers in a high-impedance state and to reset all internal registers. When asserted, the secondary interface is driven low and the device is completely nonfunctional. After P_RST is deasserted, the bridge is in its default state.

Table 2−4. PCI Primary Bus Address and Data Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
P_AD31 P_AD30 P_AD29 P_AD28 P_AD27 P_AD26 P_AD25 P_AD24 P_AD23 P_AD22 P_AD21 P_AD20 P_AD19 P_AD18 P_AD17 P_AD16 P_AD15 P_AD14 P_AD13 P_AD12 P_AD11 P_AD10 P_AD9 P_AD8 P_AD7 P_AD6 P_AD5 P_AD4 P_AD3 P_AD2 P_AD1 P_AD0	R3 T1 R6 W5 U6 R7 W6 U7 U8 V8 W9 V9 R9 P9 V10 U10 W14 R13 U14 P14 V15 U15 R17 N14 P17 P18 P19 M14 N18 N19 M17 M18	I/O	Primary address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, P_AD31 through P_AD0 contain a 32-bit address or other destination information. During the data phase, P_AD31 through P_AD0 contain data.
P_C/$\overline{BE3}$ P_C/$\overline{BE2}$ P_C/$\overline{BE1}$ P_C/$\overline{BE0}$	V7 P10 P13 R18	I/O	Primary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, P_C/$\overline{BE3}$ through P_C/$\overline{BE0}$ define the bus command. During the data phase, this 4-bit bus is used as a byte enable. The byte enable determines which byte paths of the full 32-bit data bus carry meaningful data. P_C/$\overline{BE0}$ applies to byte 0 (P_AD7 through P_AD0), P_C/$\overline{BE1}$ applies to byte 1 (P_AD15 through P_AD8), P_C/$\overline{BE2}$ applies to byte 2 (P_AD23 through P_AD16), and P_C/$\overline{BE3}$ applies to byte 3 (P_AD31 through P_AD24).

Table 2−5. PCI Primary Bus Control Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
P_DEVSEL	R11	I/O	Primary device select. The bridge asserts P_DEVSEL to claim a PCI cycle as the target device. As a PCI master on the primary bus, the bridge monitors P_DEVSEL until a target responds. If no target responds before the time-out occurs, then the bridge terminates the cycle with a master abort.
P_FRAME	W11	I/O	Primary cycle frame. P_FRAME is driven by the master of a primary bus cycle. P_FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When P_FRAME is deasserted, the primary bus transaction is in the final data phase.
P_GNT	R1	I	Primary bus grant to bridge. P_GNT is driven by the primary PCI bus arbiter to grant the bridge access to the primary PCI bus after the current data transaction has completed. P_GNT may or may not follow a primary bus request, depending on the primary bus-arbitration algorithm.
P_IDSEL	W7	I	Primary initialization device select. P_IDSEL selects the bridge during configuration space accesses. P_IDSEL can be connected to 1 of the upper 24 PCI address lines on the primary PCI bus. **Note:** There is no IDSEL signal interfacing the secondary PCI bus; thus, the entire configuration space of the bridge can only be accessed from the primary bus.
P_IRDY	U11	I/O	Primary initiator ready. P_IRDY indicates the ability of the primary bus master to complete the current data phase of the transaction. A data phase is completed on a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until both P_IRDY and P_TRDY are sample-asserted, wait states are inserted.
P_LOCK	P12	I/O	Primary PCI bus lock. P_LOCK locks the primary bus and gains exclusive access as a bus master.
P_PAR	V13	I/O	Primary parity. In all primary bus read and write cycles, the bridge calculates even parity across the P_AD and P_C/BE buses. As a bus master during PCI write cycles, the bridge outputs this parity indicator with a one P_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the parity indicator of the master; a miscompare can result in a parity error assertion (P_PERR).
P_PERR	R12	I/O	Primary parity error indicator. P_PERR is driven by a primary-bus PCI device to indicate the calculated parity does not match P_PAR when P_PERR is enabled through the primary command register (offset 04h).
P_REQ	P6	O	Primary PCI bus request. Asserted by the bridge to request access to the primary PCI bus as a master.
P_SERR	W13	O	Primary system error. Output pulsed from the bridge when enabled through the primary command register (offset 04h) indicating a system error has occurred. The bridge need not be the target of the primary PCI cycle to assert this signal. When S_SERR is enabled in the bridge control register (offset 3Eh), this signal also pulses, indicating that a system error has occurred on one of the subordinate buses downstream from the bridge.
P_STOP	W12	I/O	Primary cycle stop signal. This signal is driven by a PCI target to request that the master stop the current primary bus transaction. This signal is used for target disconnects and is commonly asserted by target devices which do not support burst data transfers.
P_TRDY	P11	I/O	Primary target ready. P_TRDY indicates the ability of the primary bus target to complete the current data phase of the transaction. A data phase is completed upon a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until both P_IRDY and P_TRDY are asserted, wait states are inserted.

Table 2−6. PCI Secondary Bus System Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
S_CLKOUT9 S_CLKOUT8 S_CLKOUT7 S_CLKOUT6 S_CLKOUT5 S_CLKOUT4 S_CLKOUT3 S_CLKOUT2 S_CLKOUT1 S_CLKOUT0	P1 N6 N2 N1 M6 M3 M1 L5 L2 L1	O	Secondary PCI bus clocks. Provide timing for all transactions on the secondary PCI bus. Each secondary bus device samples all secondary PCI signals at the rising edge of the corresponding S_CLKOUT input.
S_CLK	J3	I	Secondary PCI bus clock input. This input synchronizes the PCI2060 bridge to the secondary bus clocks.
$\overline{\text{S\_CFN}}$	J6	I	Secondary external arbiter enable. When this signal is low, the secondary internal arbiter is enabled. When this signal is high, the secondary external arbiter is enabled. When the external arbiter is enabled, the $\overline{\text{S\_REQ0}}$ terminal is reconfigured as a secondary bus grant input to the bridge and $\overline{\text{S\_GNT0}}$ is reconfigured as a secondary bus master request to the external arbiter on the secondary bus.
$\overline{\text{S\_RST}}$	J5	O	Secondary PCI reset. $\overline{\text{S\_RST}}$ is the logical OR of $\overline{\text{P\_RST}}$ and the state of the secondary bus reset bit (bit 6) of the bridge-control register (offset 3Eh). $\overline{\text{S\_RST}}$ is asynchronous with respect to the state of the secondary interface CLK signal.

Table 2−7. PCI Secondary Bus Address and Data Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
S_AD31 S_AD30 S_AD29 S_AD28 S_AD27 S_AD26 S_AD25 S_AD24 S_AD23 S_AD22 S_AD21 S_AD20 S_AD19 S_AD18 S_AD17 S_AD16 S_AD15 S_AD14 S_AD13 S_AD12 S_AD11 S_AD10 S_AD9 S_AD8 S_AD7 S_AD6 S_AD5 S_AD4 S_AD3 S_AD2 S_AD1 S_AD0	A4 E6 B5 A5 C6 B6 A6 C7 E8 F8 B8 A8 F9 C9 F10 E10 E13 B14 A15 B15 E14 F15 F14 F17 F19 G14 G18 G19 H14 H17 H19 J15	I/O	Secondary address/data bus. These signals make up the multiplexed PCI address and data bus on the secondary interface. During the address phase of a secondary bus PCI cycle, S_AD31 through S_AD0 contain a 32-bit address or other destination information. During the data phase, S_AD31 through S_AD0 contain data.
S_C/$\overline{BE3}$ S_C/$\overline{BE2}$ S_C/$\overline{BE1}$ S_C/$\overline{BE0}$	B7 A10 F12 G15	I/O	Secondary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a secondary bus PCI cycle, S_C/$\overline{BE3}$ through S_C/$\overline{BE0}$ define the bus command. During the data phase, this 4-bit bus is used as a byte enable. The byte enable determines which byte paths of the full 32-bit data bus carry meaningful data. S_C/$\overline{BE0}$ applies to byte 0 (S_AD7 through S_AD0), S_C/$\overline{BE1}$ applies to byte 1 (S_AD15 through S_AD8), S_C/$\overline{BE2}$ applies to byte 2 (S_AD23 through S_AD16), and S_C/$\overline{BE3}$ applies to byte 3 (S_AD31 through S_AD24).

Table 2−8. PCI Secondary Bus Control Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
S_DEVSEL	A11	I/O	Secondary device select. The bridge asserts S_DEVSEL to claim a PCI cycle as the target device. As a PCI master on the secondary bus, the bridge monitors S_DEVSEL until a target responds. If no target responds before time-out occurs, then the bridge terminates the cycle with a master abort.
S_FRAME	F11	I/O	Secondary cycle frame. S_FRAME is driven by the master of a secondary bus cycle. S_FRAME is asserted to indicate that a bus transaction is beginning and data transfers continue while S_FRAME is asserted. When S_FRAME is deasserted, the secondary bus transaction is in the final data phase.
S_GNT8 S_GNT7 S_GNT6 S_GNT5 S_GNT4 S_GNT3 S_GNT2 S_GNT1 S_GNT0	J1 H1 H2 H3 H5 G1 G2 H6 F1	O	Secondary bus grant. The bridge provides internal arbitration and these signals grant potential secondary PCI bus masters access to the bus. Ten potential masters (including the bridge) can be located on the secondary PCI bus. When the internal arbiter is disabled, S_GNT0 is reconfigured as an external secondary bus request signal for the bridge.
S_IRDY	C11	I/O	Secondary initiator ready. S_IRDY indicates the ability of the secondary bus master to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both S_IRDY and S_TRDY are asserted. Until S_IRDY and S_TRDY are asserted, wait states are inserted.
S_LOCK	C12	I/O	Secondary PCI bus lock. S_LOCK locks the secondary bus and gains exclusive access as a master.
S_PAR	C13	I/O	Secondary parity. In all secondary bus read and write cycles, the bridge calculates even parity across the S_AD and S_C/BE buses. As a master during PCI write cycles, the bridge outputs this parity indicator with a one S_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the master parity indicator. A miscompare can result in a parity error assertion (S_PERR).
S_PERR	E12	I/O	Secondary parity error indicator. S_PERR is asserted when a data parity error is detected for data received on the secondary interface.
S_REQ8 S_REQ7 S_REQ6 S_REQ5 S_REQ4 S_REQ3 S_REQ2 S_REQ1 S_REQ0	G5 F2 F3 E1 E2 G6 F5 E3 B4	I	Secondary PCI request signals. The bridge provides internal arbitration, and these signals are used as inputs from secondary PCI bus masters requesting the bus. Ten potential masters (including the bridge) can be located on the secondary PCI bus. When the internal arbiter is disabled, the S_REQ0 signal is reconfigured as an external secondary bus grant for the bridge.
S_SERR	B13	I	Secondary system error. S_SERR is passed through the primary interface by the bridge if enabled through the bridge control register (offset 3Eh). S_SERR is never asserted by the bridge.
S_STOP	B12	I/O	Secondary-cycle stop signal. S_STOP is driven by a PCI target to request that the master stop the current secondary bus transaction. S_STOP is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
S_TRDY	B11	I/O	Secondary target ready. S_TRDY indicates the ability of the secondary bus target to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both S_IRDY and S_TRDY are asserted. Until S_IRDY and S_TRDY are asserted, wait states are inserted.

Table 2−9. Miscellaneous Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
BPCCE	N5	I	Bus/power clock-control management terminal. When the BPCCE signal is tied high and when the PCI2060 bridge is placed in the D3 power state, it enables the PCI2060 bridge to place the secondary bus in the B2 power state. The PCI2060 bridge disables the secondary clocks and drives them to 0. When tied low, placing the PCI2060 bridge in the D3 power state has no effect on the secondary bus clocks.
GPIO3/ $\overline{\text{HSSWITCH}}$ GPIO2 GPIO1 GPIO0	K1 K2 K5 K6	I/O	General-purpose I/O terminals GPIO3 is $\overline{\text{HSSWITCH}}$ in the compactPCI mode. $\overline{\text{HSSWITCH}}$ provides the status of the ejector handle switch to the compactPCI logic.
$\overline{\text{HSENUM}}$	L15	O	Hot-swap $\overline{\text{ENUM}}$. This signal notifies the host that a card insertion or removal event is pending.
HSLED	L14	O	Hot-swap LED output
MS0	E17	I	Mode select 0
MS1	T19	I	Mode select 1
P_M66ENA	W16	I	Primary interface 66-MHz enable. This input-only signal terminal designates the primary interface bus speed. This signal must be pulled low for 33-MHz operation on the primary bus. In this case, the S_M66ENA signal is driven low by the PCI2060 bridge, forcing the secondary bus to run at 33 MHz. For 66-MHz operation, this signal must be pulled high.
CONFIG66	L18	I	Configure 66-MHz operation. This input-only terminal specifies whether the PCI2060 bridge is capable of running at 66 MHz. If this terminal is tied high, then the device can be run at 66 MHz. If this terminal is tied low, then the PCI2060 bridge can only function under the 33-MHz PCI specification.
S_M66ENA	E18	I/O	Secondary 66-MHz enable. This signal designates the secondary bus speed. See Section 3.10.1 for more detail on the use of the S_M66ENA signal. Note that S_M66ENA is an open-drained output.
SEC_ASYNC_CLK	C1	I	Secondary asynchronous clock. This terminal is the secondary clock input when the SEC_ASYNC_SEL terminal is high.
SEC_ASYNC_SEL	C4	I	Secondary clock select. This terminal selects the clock that generates the secondary bus clock. If SEC_ASYNC_SEL is low, then the primary PCI clock (P_CLK) input generates the secondary bus clock. If SEC_ASYNC_SEL is high, then the SEC_ASYNC_CLK generates the secondary bus clock.
SEC_ASYNC_RATE	D18	I	Secondary clock rate. This terminal selects the clock speed of the secondary bus clock. If SEC_ASYNC_RATE is low, then the secondary clock outputs are one-half of the input clock frequency. If SEC_ASYNC_RATE is high, then the secondary clock outputs are the same as the input clock frequency.
MASK_IN	L17	I	Secondary clock disable serial input. This input-only signal is used by the hardware mechanism to disable secondary clock outputs. The serial stream is received by the MASK_IN, starting when $\overline{\text{P\_RST}}$ is detected as deasserted and $\overline{\text{S\_RST}}$ is detected as asserted. This serial data is used for selectively disabling the secondary clock outputs and is shifted into the secondary clock control register (offset 68h). This input can be tied low to enable all secondary clock outputs or tied high to drive all secondary clock outputs high.

Table 2−10. JTAG Terminals

TERMINAL		I/O	DESCRIPTION
NAME	GHK NUMBER		
TCK	J19	I	JTAG boundary scan clock. TCK is the clock controlling the JTAG logic.
TDI	K18	I	JTAG serial data in. TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on TDI is sampled on the rising edge of TCK.
TDO	K17	O	JTAG serial data out. TDO is the serial output through which test instructions and test data from the test logic leave the PCI2060 bridge.
TMS	K14	I	JTAG test mode select. TMS causes state transitions in the test-access port controller.
$\overline{\text{TRST}}$	J18	I	JTAG reset. When $\overline{\text{TRST}}$ is asserted low, the TAP controller is asynchronously forced to enter a reset state and initialize the test logic.

Table 2−11. Power Supply Terminals

TERMINAL		DESCRIPTION
NAME	GHK NUMBER	
V_{CC}	A3, A9, A13, A16, C8, C14, D2, E11, E19, F6, F7, G17, H18, K3, K15, M2, M15, N3, N15, P7, P8, P15, T2, T18, U13, V11, V16, W4, W8, W10, W15	3.3-V power terminals
GND	A7, A12, A14, B10, C5, C15, D19, E7, E9, F13, F18, G3, H15, J2, J14, L6, M5, M19, N17, P5, R8, R10, R14, R19, U1, U5, U9, U12, V6, V14, W17	Device ground terminals
P_VIO	L19	Primary interface I/O voltage. This signal must be tied to either 3.3 V or 5 V, corresponding to the signaling environment of the primary PCI bus as described in the *PCI Local Bus Specification*, Revision 2.3. When any device on the primary PCI bus uses 5-V signaling levels, tie P_VIO to 5 V. When all the devices on the primary bus use 3.3-V signaling levels, tie P_VIO to 3.3 V.
S_VIO	J17	Secondary interface I/O voltage. This signal must be tied to either 3.3 V or 5 V, corresponding to the signaling environment of the secondary PCI bus as described in the *PCI Local Bus Specification*, Revision 2.3. When any device on the secondary PCI bus uses 5-V signaling levels, tie S_VIO to 5 V. When all the devices on the secondary bus use 3.3-V signaling levels, tie S_VIO to 3.3 V.

Table 2−12. No Connect Terminals

TERMINAL		DESCRIPTION
NAME	GHK NUMBER	
NC	A2, A17, A18, B1, B2, B3, B9, B16, B17, B18, B19, C2, C3, C10, C16, C17, C18, C19, D1, D3, D17, E5, K19, L3, R2, T3, T17, U2, U3, U4, U16, U17, U18, U19, V1, V2, V3, V4,V5, V12, V17, V18, V19, W2, W3, W18	These terminals have no function on the PCI2060 bridge.

3 Principles of Operation

The PCI2060 is a bridge between two PCI buses and is compliant with both the *PCI Local Bus Specification* and the *PCI-to-PCI Bridge Specification*. The PCI2060 bridge makes it possible for both the primary and secondary bus clocks to be completely asynchronous and supports the PCI clock frequency up to 66 MHz. The primary and secondary buses operate independently in either 3.3-V or 5-V signaling environment. The core logic of the bridge, however, is powered at 1.8-V to reduce power consumption. Figure 3−1 shows a simplified block diagram of a typical system implementation using the PCI2060 bridge.

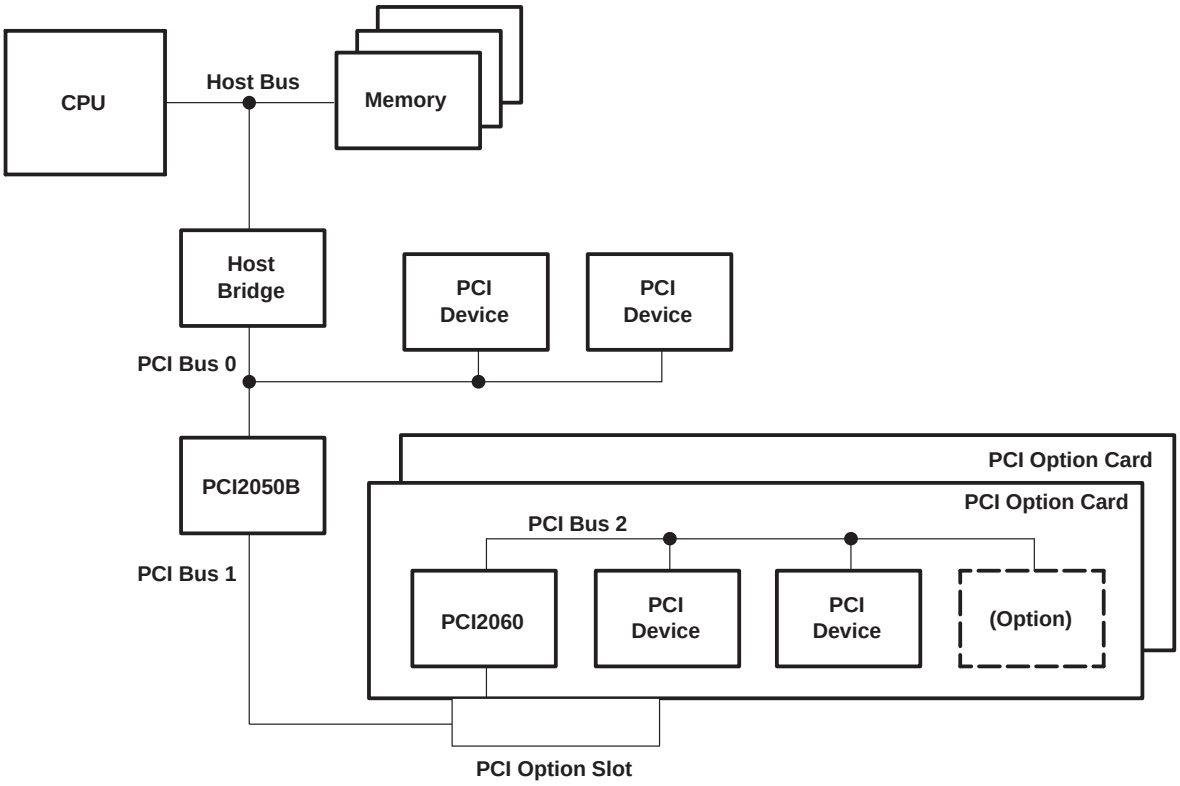


Figure 3−1. System Block Diagram

Host software interacts with the bridge through internal registers. These internal registers provide the standard PCI status and control for both the primary and secondary buses. Many vendor-specific features that exist in the TI extension register set are included in the bridge. The PCI configuration header of the bridge is only accessible from the primary PCI interface.

The bridge provides internal arbitration for the nine possible secondary bus masters, and provides each with a dedicated active low request/grant pair ($\overline{REQ}$/$\overline{GNT}$). The arbiter features a two-tier rotational scheme with the PCI2060 bridge defaulting to the highest priority tier. The PCI2060 bridge also supports external arbitration.

Upon system power up, power-on self-test (POST) software configures the bridge according to the devices that exist on subordinate buses, and enables performance-enhancing features of the PCI2060 bridge. In a typical system, this is the only communication with the bridge internal register set.

3.1 Types of Transactions

PCI bus commands indicate to the target the type of transaction the master is requesting. Table 3−1 lists the PCI command and name of each PCI transaction on the command/byte enable (C/$\overline{BE}$) bus during the address phase of a bus cycle. The master and target columns indicate PCI2060 support for each transaction when the PCI2060 bridge initiates transactions as a master, on the primary bus and on the secondary bus, and when the PCI2060 bridge responds to transactions as a target, on the primary bus and on the secondary bus.

Table 3−1. PCI2060 PCI Transactions

C/$\overline{BE3}$ − C/$\overline{BE0}$	PCI2060 AS THE MASTER		PCI2060 AS THE TARGET	
	PRIMARY	SECONDARY	PRIMARY	SECONDARY
0000 = Interrupt acknowledge	No	No	No	No
0001 = Special cycle	Yes	Yes	No	No
0010 = I/O read	Yes	Yes	Yes	Yes
0011 = I/O write	Yes	Yes	Yes	Yes
0100 = Reserved	Reserved	Reserved	Reserved	Reserved
0101 = Reserved	Reserved	Reserved	Reserved	Reserved
0110 = Memory read	Yes	Yes	Yes	Yes
0111 = Memory write	Yes	Yes	Yes	Yes
1000 = Reserved	Reserved	Reserved	Reserved	Reserved
1001 = Reserved	Reserved	Reserved	Reserved	Reserved
1010 = Configuration read	No	Yes	Yes	No
1011 = Configuration write	Type 1	Yes	Yes	Type 1
1100 = Memory read multiple	Yes	Yes	Yes	Yes
1101 = Memory write multiple	Yes	Yes	Yes	Yes
1110 = Memory read line	Yes	Yes	Yes	Yes
1111 = Memory write line	Yes	Yes	Yes	Yes

As a PCI master, the PCI2060 bridge never initiates the interrupt acknowledge and reserved commands. As a target, the PCI2060 bridge ignores the interrupt acknowledge and reserved commands.

The PCI2060 bridge never responds as a PCI target to the special cycle command. The bridge does, however, initiate special cycles on both interfaces when a type 1 configuration cycle issues the special cycle request.

The PCI2060 bridge never initiates a type 0 configuration transaction on the primary bus. The bridge never responds to a type 0 configuration transaction on the secondary bus.

The remaining PCI commands address memory, I/O, or configuration space. The bridge accepts PCI cycles by asserting $\overline{DEVSEL}$ as a medium-speed device; for example, $\overline{DEVSEL}$ is asserted two clock cycles after the address phase.

The PCI2060 bridge converts memory write-and-invalidate commands to memory write commands when forwarding transactions from either the primary or secondary side of the bridge, if the bridge cannot guarantee that an entire cache line will be delivered.

3.2 Decoding Options

The *PCI-to-PCI Bridge Architecture Specification* supports both positive and subtractive decoding. Positive decoding is a method of address decoding in which a device responds only to accesses within an assigned address range. Subtractive decoding is a method of address decoding in which a device responds only to accesses outside of an assigned address range. The PCI2060 bridge supports positive decoding on the primary bus and subtractive decoding on the secondary bus.

3.3 Configuration Cycles

The *PCI Local Bus Specification* defines two types of PCI configuration read and write transactions: type 0 and type 1. The bridge decodes each type differently. Type 0 configuration transactions are intended for devices on the primary bus, while type 1 configuration transactions are intended for devices on some hierarchically subordinate bus. The difference between these two types of transactions is the encoding of the primary PCI (P_AD) bus during the address phase of the transaction. Table 3−2 shows the P_AD bus encoding during the address phase of a type 0 configuration transaction. Table 3−3 shows the P_AD bus encoding during the address phase of a type 1 configuration transaction.

Table 3−2. PCI AD31−AD0 During Address Phase of a Type 0 Configuration Type

31 11	10 8	7 2	1	0
Reserved	Function Number	Register Number	0	0

Table 3−3. PCI AD31−AD0 During Address Phase of a Type 1 Configuration Type

31 24	23 16	15 11	10 8	7 2	1	0
Reserved	Bus Number	Device Number	Function Number	Register Number	0	1

The 6-bit register number field in both type 0 and type 1 configuration transactions represents an 8-bit address with the two lower bits masked to 00b, indicating a doubleword boundary. This results in a 256-byte configuration address space per function per device. Individual byte accesses may be selected within a doubleword by using the P_C/$\overline{BE}$ signals during the data phase of the cycle.

3.3.1 Type 0 Configuration Transaction

The PCI2060 configuration space is accessed by a type 0 configuration transaction on the primary bus. The bridge never responds to a type 0 configuration transaction on the secondary bus.

The PCI2060 bridge claims only type 0 configuration cycles when its P_IDSEL terminal is asserted during the address phase of the configuration cycle and the PCI function number encoded in the cycle is 0. If the function number is 1 or greater, then the bridge does not recognize the configuration command. In this case, the bridge does not assert P_$\overline{DEVSEL}$ and the configuration transaction results in a master abort. The bridge services a valid type 0 configuration read or write cycle by accessing internal registers from the bridge configuration header (see Table 4−1).

The PCI2060 bridge limits all configuration accesses to a single doubleword data transfer and returns a target disconnect with the first data transfer if additional data phases are requested. Read transactions to the bridge configuration space do not have side-effects; all bytes in the requested doubleword are returned regardless of the value of the byte-enable bits.

3.3.2 Type 1 to Type 0 Translation

The type 1 configuration transactions are intended for devices on some hierarchically subordinate bus. A bridge is the only device that is capable of responding to a type 1 configuration transaction.

When the PCI2060 bridge claims a type 1 configuration transaction that has a bus number equal to its secondary bus number, the PCI2060 bridge converts the type 1 configuration transaction to a type 0 configuration transaction and asserts the proper S_AD line as the IDSEL (see Table 3−4). The PCI2060 bridge can only generate a type 0 configuration on the secondary bus. It can never generate a type 1 configuration on the secondary bus.

When the PCI2060 bridge converts the type 1 transaction to a type 0 transaction on the secondary bus, it performs the following conversion:

- The two lower address bits on S_AD[1:0] are set to 00b.
- The device number is decoded and drives the bit pattern specified in Table 3−4 onto S_AD[31:16] for the purpose of asserting the device's IDSEL signal.
- The device number, function number, and register number fields are left unchanged.

The mapping of the secondary bus address lines depends on the device number in the type 1 address bits P_AD[15:11]. Table 3−4 presents the mapping of the address lines.

Table 3−4. Device Number to IDSEL S_AD Pin Mapping

DEVICE NUMBER	SECONDARY IDSEL S_AD31 − S_AD16	S_AD ASSERTED
0h	0000 0000 0000 0001	16
1h	0000 0000 0000 0010	17
2h	0000 0000 0000 0100	18
3h	0000 0000 0000 1000	19
4h	0000 0000 0001 0000	20
5h	0000 0000 0010 0000	21
6h	0000 0000 0100 0000	22
7h	0000 0000 1000 0000	23
8h	0000 0001 0000 0000	24
9h	0000 0010 0000 0000	25
Ah	0000 0100 0000 0000	26
Bh	0000 1000 0000 0000	27
Ch	0001 0000 0000 0000	28
Dh	0010 0000 0000 0000	29
Eh	0100 0000 0000 0000	30
Fh	1000 0000 0000 0000	31
10h – 1Eh	0000 0000 0000 0000	−

3.3.3 Type 1 to Type 1 Forwarding

When a type 1 transaction accesses a bus number greater than the bridge secondary bus number but less than or equal to its subordinate bus number, the PCI2060 bridge forwards the type 1 transaction as a type 1 transaction on the secondary bus.

3.3.4 Special Cycle

The PCI2060 bridge is required to generate special cycles on both buses through a type 1 configuration transaction conversion. During a type 1 configuration transaction on the primary bus, if the bus number field matches the bridge secondary bus number, the device number field is 1Fh, and the function number field is 07h, then the bridge generates a special cycle transaction on the secondary bus with a message that matches the data in the type 1 configuration transaction. If the bus number is a subordinate bus and not the secondary bus, then the bridge passes the type 1 special cycle request through to the secondary bus along with the proper message.

During a type 1 configuration transaction on the secondary bus, if the bus number field matches the bridge primary bus number, the device number field is 1Fh, and the function number field is 07h, then the bridge generates a special cycle transaction on the primary bus with a message that matches the data in the type 1 configuration transaction.

Special cycle transactions are never passed through the bridge. Type 1 configuration transactions with a special cycle request can propagate in both directions.

3.4 Write Transaction

A write transaction is treated as either a posted write or delayed write transaction. Table 3−5 shows the method of forwarding used for each type of write operation.

Table 3−5. Write Transaction Forwarding

TYPE OF TRANSACTION	TYPE OF FORWARDING
Memory write	Posted
Memory write-and-invalidate	Posted
I/O write	Delayed
Type 1 configuration write	Delayed

3.4.1 Posted Write Transaction

All memory write and memory write-and-invalidate transactions are handled as posted write transactions and must be completed on the destination bus. The PCI2060 bridge has two 64-doubleword posted write FIFOs; one for upstream transaction and the other for downstream transactions (these FIFOs are shared with delayed request transactions).

When a posted write transaction is to be forwarded across the bridge, the PCI2060 bridge asserts the $\overline{\text{DEVSEL}}$ with medium timing and the $\overline{\text{TRDY}}$ in the same cycle. Due to the asynchronous clock implementation, the PCI2060 bridge requires eight doublewords of free space in the FIFO before it accepts any posted write transactions.

The PCI2060 bridge continues to accept write data until one of the following events occurs:

- The initiator terminates the transaction by deasserting $\overline{\text{FRAME}}$ and $\overline{\text{IRDY}}$.
- An internal write address boundary is reached, such as a cache line boundary or an aligned 4-KB boundary, depending on the transaction type.
- The posted write data buffer fills up.

When one of the last two events occurs, the PCI2060 bridge returns a target disconnect to the requesting initiator to terminate the transaction.

Once the PCI2060 bridge makes a request for the target bus and receives the grant for the target bus, the PCI2060 bridge asserts $\overline{\text{FRAME}}$ and drives the stored write address out on the target bus when the target bus is idle. On the next cycle, the PCI2060 bridge drives the first doubleword of the write data and continues to transfer write data until all write data corresponding to that transaction is delivered.

The PCI2060 bridge ends the transaction on the target bus when one of the following conditions is met:

- All posted write data has been delivered to the target.
- The target returns a target disconnect or a target retry (the PCI2060 bridge then starts another transaction to deliver the rest of the write data).
- The target returns a target abort (the PCI2060 bridge discards remaining write data).
- The master latency timer expires and the PCI2060 bridge no longer has the target bus grant (the PCI2060 then starts another transaction to deliver remaining write data).

The PCI2060 bridge handles memory write-and-invalidate transactions in two different ways:

- If bit 1 (MWI_MW_CONVERSION) in the TI diagnostic register (offset F0h) is cleared to 0b, and the PCI2060 bridge has FIFO space for a full cache line, then the PCI2060 bridge accepts the memory write-and-invalidate transaction. If the PCI2060 bridge does not have enough FIFO space for a full cache line, then the bridge converts the memory write-and-invalidate transaction to the memory transaction. The PCI2060 bridge waits until a full cache line of data is in the FIFO before initiating a memory write-and-invalidate transaction on the destination bus.
- If the MWI_MW_CONVERSION bit is set to 1b, then the bridge converts all memory write-and-invalidate transactions to memory write transactions before putting them in the FIFO.

3.4.2 Delayed Write Transaction

A delayed write transaction is used for I/O write transactions and for type 1 configuration write transactions. A delayed write transaction assures that the actual target response is returned back to the initiator without holding the initiating bus in wait states. A delayed write transaction is limited to a single doubleword data transfer. The PCI2060 bridge is capable of supporting up to three delayed transactions in each direction at any given time.

A delayed write transaction consists of three phases:

- An initiator issues the write request. The PCI2060 bridge claims the access by asserting the $\overline{\text{DEVSEL}}$ and returns a target retry to the initiator.
- The PCI2060 bridge initiates the write request on the target bus and writes data to the target. If a target retry is received in response to the write transaction on the target bus, the bridge continues to repeat the write transaction until the data transfer is completed, or until an error condition is encountered. If the PCI2060 bridge is unable to write the data to the target after 2^{24} attempts, then the PCI2060 bridge stops further write attempts, discards the write request, returns a target abort to the initiator, and conditionally sets the SERR signal.
- The initiator repeats the same write request. If the data has been written to the target, then the PCI2060 bridge claims the access by asserting $\overline{\text{DEVSEL}}$ and returns $\overline{\text{TRDY}}$ to the initiator to indicate the completion of the write data process. If the data have not been written to the target, then the PCI2060 bridge returns a target retry to the initiator. The PCI2060 bridge continues to return a target retry to the initiator until either the write data is delivered to the target or until an error condition is encountered. If the initiator requests multiple doublewords, then the PCI2060 bridge asserts the $\overline{\text{STOP}}$ in conjunction with $\overline{\text{TRDY}}$ to signal a target disconnect.

3.4.3 Discard Timer

A discard timer starts counting when the delayed write completion is at the head of the delayed transaction queue. The initial value of this timer can be set to one of two values: 2^{10} or 2^{15} PCI clocks. The value of this timer is selectable through bits 8 and 9 (PRI_DIS and SEC_DT) in the bridge control register (offset 3Eh). If the initiator does not repeat the write request before the discard timer expires, then the PCI2060 bridge discards the data or the status of the delayed transaction that was completed and conditionally sets the SERR signal.

3.4.4 Write Transaction Address Boundaries

The PCI2060 bridge uses the internal address boundaries when accepting write data. When the address boundaries are reached, the PCI2060 bridge returns a target disconnect to the initiator. Table 3−6 lists the disconnect address boundaries for the write transaction.

Table 3−6. Write Transaction Disconnect Address Boundaries

TYPE OF TRANSACTION	CONDITION	ALIGNED ADDRESS BOUNDARY
Delayer write	All	Single doubleword
Posted memory write	Memory write disconnect bit = 0b	Queue full or 4-KB boundary
Posted memory write	Memory write disconnect bit = 1b	Queue full, 4-KB boundary, cache line
Posted memory write-and-invalidate	Cache line size ≠ 1, 2, 4, 8, 16	4-KB boundary
Posted memory write-and-invalidate	Cache line size = 1, 2, 4, 8	nth cache line boundary, where a cache line boundary is reached and less than 8 free doublewords of posted write buffer space remain
Posted memory write-and-invalidate	Cache line size = 16	16-doubleword aligned address boundary

3.4.5 Fast Back-to-Back Write Transactions

The PCI2060 bridge can recognize and post fast back-to-back write transactions. When the PCI2060 bridge cannot accept the second transaction because of buffer space limitations, it returns a target retry to the initiator.

When the PCI2060 bridge has posted multiple write transactions, it can initiate fast back-to-back write transactions if bit 9 (FBB_ENB) in the primary command register (offset 04h) is set to 1b for upstream write transactions and if bit 7 (FBB_EN) in the bridge control register (offset 3Eh) is set to 1b for downstream write transactions.

3.4.6 Write Combining

The PCI2060 bridge supports write combining for upstream and downstream transactions. This feature combines separate sequential memory write transactions into a single burst transaction. This feature can only be used if the address of the next memory write transaction is the next sequential address after the address of the last doubleword of the previous memory transaction. For example, if the current memory transaction ends at address X and the next memory transaction starts at address X+1, then the PCI2060 bridge combines both transactions into a single transaction.

The write combining feature of the PCI2060 bridge is enabled by default on power-on reset. This feature can be disabled by setting bit 0 (PW_COMBINING_DIS) in the TI diagnostics register (offset F0h) to 1b.

3.5 Read Transactions

Read transactions are treated as either prefetchable or nonprefetchable. Table 3−7 shows the read behavior for each type of read transaction.

Table 3−7. Read Behavior

TYPE OF TRANSACTION	READ BEHAVIOR	CONDITION
I/O read	Nonprefetchable	
Configuration read	Nonprefetchable	
Memory read	Nonprefetchable	Nonprefetchable address space
Memory read	Prefetchable	Prefetchable address space
Memory read line	Prefetchable	
Memory read multiple	Prefetchable	

3.5.1 Prefetchable Read Transactions

A prefetchable read transaction is a read transaction where the bridge reads data from the target before it is requested by the initiator. Memory that is prefetchable has the attribute that it returns the same data when read multiple times and does not alter any other device state when it is read. The bridge is required to discard any prefetched read data not consumed when the initiator concludes the read transaction.

Prefetchable behavior is used for memory read line and memory read multiple transactions, as well as for memory read transactions that fall into prefetchable memory space.

3.5.2 Prefetch Optimization

The PCI2060 bridge incorporates a memory read prefetch optimization method that is intended to improve the performance of an initiating PCI master. The prefetch optimization method is used only on read burst transactions (memory read, memory read line, and memory read multiple). The prefetch optimization method is not implemented in the nonburst read transactions. When the target of a read burst transaction is on the opposite side of the PCI2060 bridge, the chances of the read being broken up on the initiating bus into multiple transactions increase as the latency between the primary and secondary buses becomes greater.

In an effort to reduce the impact on system performance, the PCI2060 bridge contains two independent threshold levels. One is called the primary connect threshold level (PCTL) and the other is called the secondary connect threshold level (SCTL). The PCTL is used for transactions that originate from the primary bus and target the secondary bus, while the SCTL is used for transactions that originate from the secondary bus and target the primary bus. Table 3−8 lists the value used for each threshold level.

Table 3−8. Read Connect Threshold Level

Ratio (Pri:Sec)	PCTL (DW)	SCTL (DW)
> 2:1	8	1
2:1 thru 1:2	1	1
<1:2	1	8

The PCI2060 bridge uses these threshold levels to know when to provide data to a master. For example, a master initiates a memory-read burst transaction that targets a device on the opposite side of the PCI2060 bridge. The PCI2060 bridge immediately retries this transaction until the PCI2060 bridge has one complete connect threshold level in its FIFO. Once the level has been reached, the PCI2060 bridge provides the data to the master.

3.5.3 Nonprefetchable Read Transactions

A nonprefetchable read transaction is a read transaction during which the PCI2060 bridge requests only one doubleword from the target and disconnects the initiator after delivery of the first doubleword of the read data.

Nonprefetchable behavior is used for I/O and configuration read transactions, as well as for memory read transactions that fall into nonprefetchable memory address space.

3.5.4 Delayed Read Transaction

All read transactions are delayed read transactions.

A delayed read transaction assures that the actual target response is returned back to the initiator without holding the initiating bus in a wait state. The PCI2060 bridge is capable of supporting up to three delayed transactions in each direction at any given time.

A delayed read transaction consists of three phases:

1. An initiator issues the read request. The PCI2060 bridge claims the access by asserting the $\overline{\text{DEVSEL}}$ and returns a target retry to the initiator.
2. The PCI2060 bridge initiates the read request on the target bus. If a target retry is received in response to the read transaction on the target bus, then the bridge continues to repeat the write transaction until the data transfer is completed, or until an error condition is encountered. If the PCI2060 bridge is unable to read the data from the target after 2^{24} attempts, then the PCI2060 bridge stops further read attempts, returns a target abort to the initiator, and conditionally sets the SERR signal. If the read transaction is terminated via normal master termination or a target disconnect after at least one data transfer has been completed, then the PCI2060 bridge does not initiate any further attempts to read more data.
3. The initiator repeats the same read request, the PCI2060 bridge claims the access by asserting $\overline{\text{DEVSEL}}$, and returns $\overline{\text{TRDY}}$ and read data to the initiator. The PCI2060 bridge returns a target disconnect along with the transfer of the last doubleword of read data to the initiator. If the initiator terminates the transaction before all read data has been transferred, then the remaining read data left in the bridge data buffers is discarded.

3.5.5 Discard Timer

A discard timer starts counting when the delayed read completion is at the head of the delayed transaction queue. The initial value of this timer can be set to one of two values: 2^{10} or 2^{15} PCI clocks. The value of this timer is selectable through bits 8 and 9 (PRI_DIS and SEC_DT) in the bridge control register (offset 3Eh). If the initiator does not repeat the read request before the discard timer expires, then the PCI2060 bridge discards the read data and the read transaction from its buffer and conditionally sets the SERR signal.

3.6 Transaction Termination

Either the master or the target may initiate the termination of a PCI transaction. An idle state is achieved when the $\overline{\text{FRAME}}$ and $\overline{\text{IRDY}}$ signals are deasserted.

3.6.1 Termination Initiated by the Master

A termination initiated by the master occurs when $\overline{\text{FRAME}}$ is deasserted and $\overline{\text{IRDY}}$ is still asserted. This condition signals to the target that the final data phase is in progress. The final data transfer occurs when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted. The transaction is completed when both $\overline{\text{FRAME}}$ and $\overline{\text{IRDY}}$ are deasserted.

The master terminates a transaction under following conditions:

- The master has completed the intended transaction to the target.
- With the exception of the memory write-and-invalidate transaction, the master latency timer may have expired and the master $\overline{\text{GNT}}$ line is deasserted. The intended transaction is not necessarily concluded. The timer may have expired because of target-induced access latency or because the intended operation was very long.
- The target terminates the transaction with a retry, a disconnect, or a target abort event.

If the master is delivering posted write data when it terminates the transaction because the master latency timer expires, then it initiates another transaction to deliver the remaining write data. The address of the transaction is updated to reflect the address of the current doubleword to be delivered.

If the master is prefetching read data when it terminates the transaction because the master latency timer expires, then it does not repeat the transaction to obtain more data.

3.6.2 Termination Initiated by the Target

When a target is unable to complete a request initiated by the master, it uses the $\overline{\text{STOP}}$ signal to initiate termination of the transaction.

The three types of target-initiated terminations are:

- The target returns a target retry to the initiator when it cannot accept write data or return read data because the target is busy and temporarily unable to process the transaction. This can happen if:
  - The target is unable to meet the initial latency requirement.
  - The target is currently locked by another initiator.
  - There is an internal resource conflict.

  The target signals retry by asserting $\overline{\text{STOP}}$ and not asserting $\overline{\text{TRDY}}$ on the initial data phase of the transaction. When the target uses retry, no data is transferred.
- The target returns a target disconnect to an initiator when one of the following conditions is met:
  - The target hits an internal address boundary.
  - The target cannot accept any more write data.
  - The target has no more read data to deliver.

  Disconnect with data may be signaled on any data phase by asserting $\overline{\text{TRDY}}$ and $\overline{\text{STOP}}$ together. This termination is used when the target is only willing to complete the current data phase and no more. Disconnect without data may be signaled on any subsequent data phase (meaning data was transferred on the previous data phase) by deasserting $\overline{\text{TRDY}}$ and asserting $\overline{\text{STOP}}$.
- The target returns a target abort to an initiator when one of the following conditions is met:
  - The target detects a fatal error.
  - The target is unable to obtain delayed read data from the target or to deliver delayed write data to the target after 2^{24} attempts.

  The target signals target-abort by deasserting $\overline{\text{DEVSEL}}$ and asserting $\overline{\text{STOP}}$ at the same time.

3.7 Bus Arbitrations

The PCI2060 bridge implements bus request (P_REQ) and bus grant (P_GNT) terminals for primary PCI bus arbitration. Nine secondary bus requests and nine secondary bus grants are provided on the secondary bus of the PCI2060 bridge. Ten potential initiators, including the bridge, can be located on the secondary bus. The PCI2060 bridge provides a two-tier arbitration scheme on the secondary bus for priority bus-master handling.

The two-tier arbitration scheme improves performance in systems in which master devices do not all require the same bandwidth. Any master that requires frequent use of the bus can be programmed to be in the higher priority tier.

3.7.1 Primary Bus Arbitration

The PCI2060 bridge, acting as an initiator on the primary bus, asserts P_REQ when forwarding transactions upstream to the primary bus. If a target disconnect, a target retry, or a target abort is received in response to a transaction initiated on the primary bus by the PCI2060 bridge, then the bridge deasserts P_REQ for two PCI clock cycles.

When the primary bus arbiter asserts P_GNT in response to a P_REQ from the PCI2060 bridge, the bridge initiates a transaction on the primary bus during the next PCI clock cycle after the primary bus is sampled idle.

When P_REQ is not asserted and the primary bus arbiter asserts P_GNT to the PCI2060 bridge, the bridge responds by parking the P_AD31–P_AD0 bus, the C/BE3−C/BE0 bus, and primary parity (P_PAR) by driving them to valid logic levels. If the PCI2060 bridge is parking the primary bus and wants to initiate a transaction on the bus, then it can start the transaction on the next PCI clock by asserting the primary cycle frame (P_FRAME) while P_GNT is still asserted. If P_GNT is deasserted, then the bridge must re-arbitrate for the bus to initiate a transaction.

3.7.2 Internal Secondary Bus Arbitration

The S_CFN terminal controls the state of the secondary internal arbiter. When S_CFN is low, the secondary internal arbiter is enabled. When S_CFN is high, the secondary external arbiter function is enabled. The PCI2060 bridge provides nine secondary bus request terminals and nine secondary bus grant terminals. Including the bridge, there are total of ten potential secondary bus masters.

When an external arbiter is implemented, S_REQ8 through S_REQ1 and S_GNT8 through S_GNT1 are placed in a high-impedance mode.

3.7.3 External Secondary Bus Arbitration

An external secondary bus arbiter can be used instead of the PCI2060 internal bus arbiter. When using an external arbiter, the PCI2050B internal arbiter must be disabled by pulling S_CFN high.

When an external secondary bus arbiter is used, the PCI2050B bridge internally reconfigures the S_REQ0 and S_GNT0 signals so that S_REQ0 becomes the secondary bus grant for the bridge and S_GNT0 becomes the secondary bus request for the bridge. This is done because S_REQ0 is an input and can thus provide the grant input to the bridge, and S_GNT0 is an output and can thus provide the request output from the bridge.

When an external arbiter is used, all unused secondary bus grant outputs (S_GNT8 through S_GNT1) are placed in a high-impedance mode. Any unused secondary bus request inputs (S_REQ8 through S_REQ1) must be pulled high to prevent the inputs from oscillating.

3.8 Parity Error Handling

When forwarding transactions, the PCI2060 bridge attempts to pass the parity condition from one interface to the other unchanged, whenever possible, to allow the master and target devices to handle the error condition.

3.8.1 Address Parity Error

The PCI2060 bridge checks address parity for all transactions on both buses, for all addresses and all bus commands.

When the PCI2060 bridge detects an address parity error on the primary bus, the following events occur:

- If bit 6 (PERR_ENB) in the primary command register (offset 04h) is set to 1b, then the PCI2060 bridge does not claim the transaction with P_DEVSEL; this allows the transaction to terminate in a master abort.
- If bit 6 (PERR_ENB) is not set, then the PCI2060 bridge proceeds normally and accepts the transaction if it is directed to or across the PCI2060 bridge.
- The PCI2060 bridge sets bit 15 (PAR_ERR) in the primary status register (offset 06h).
- The PCI2060 bridge asserts P_SERR and sets bit 14 (SYS_P_SERR) in the primary status register (offset 06h), if both of the following conditions are met:
  - Bit 8 (SERR_ENB) is set in the primary command register (offset 04h).
  - Bit 6 (PERR_ENB) is set in the primary command register (offset 04h).

When the PCI2060 bridge detects an address parity error on the secondary bus, the following events occur:

- If bit 0 (PERR_EN) in the bridge control register (offset 3Eh) is set to 1b, then the PCI2060 bridge does not claim the transaction with S_DEVSEL; this allows the transaction to terminate in a master abort.
- If the PERR_EN bit is not set, then the PCI2060 bridge proceeds normally and accepts the transaction if it is directed to or across the PCI2060 bridge.
- The PCI2060 bridge sets bit 15 (PAR_ERR) in the secondary status register (offset 1Eh).
- The PCI2060 bridge asserts P_SERR and sets bit 14 (SYS_P_SERR) in the primary status register (offset 06h), if the following conditions are met:
  - Bit 8 (SERR_ENB) is set in the primary command register (offset 04h).
  - Bit 0 (PERR_EN) is set in the bridge-control register (offset 3Eh).

3.8.2 Data Parity Error

If bit 6 (PERR_ENB) in the primary command register (offset 04h) is set, then the PCI2060 bridge signals PERR when it receives bad data. When the bridge detects bad parity, bit 15 (PAR_ERR) in the primary status register (offset 06h) is set.

If the PCI2060 bridge is configured to respond to parity errors via the PERR_ENB bit in the primary command register (offset 04h), then bit 8 (DATAPAR) in the primary status register (offset 06h) is set when the bridge detects bad parity. The DATAPAR bit is also set when the bridge, as a bus master, asserts PERR or detects PERR.

3.9 System Error Handling

The PCI2060 bridge can be configured to signal a system error (SERR) on the primary bus for a variety of conditions. The P_SERR event disable register (offset 64h) and the P_SERR status register (offset 6Ah) provide control and status bits for each condition for which the bridge can signal P_SERR.

By default, the PCI2060 bridge does not signal P_SERR. If bit 8 (SERR_ENB) in the primary command register (offset 04h) is set, then the bridge signals SERR if any of the error conditions in the P_SERR event disable register occur and that condition is enabled. By default, all error conditions are enabled in the P_SERR event disable register. When the bridge signals SERR on the primary bus, bit 14 (SYS_P_SERR) in the primary status register (offset 06h) is also set.

When the PCI2060 bridge detects the assertion of the SERR on the secondary bus, bit 14 (SYS_S_SERR) in the secondary status register (offset 1Eh) is also set. If bit 1 (SERR_EN) in the bridge control register (offset 3Eh) and bit 8 (SERR_ENB) in the primary command register (offset 04h) are set, then the PCI2060 bridge signals SERR on the primary bus.

The PCI2060 bridge conditionally asserts $\overline{\text{P\_SERR}}$ for any of the following reasons:

- Target abort detected during posted write transaction
- Master abort detected during posted write transaction
- Posted write data discarded after 2^{24} attempts to deliver
- Parity error reported on target bus during posted write transaction
- Delayed write data discarded after 2^{24} attempts to deliver
- Delayed read data cannot be transferred from target after 2^{24} attempts
- Master timeout on delayed transaction

3.10 Clocks

3.10.1 Secondary Bus Clock Behavior

The PCI2060 bridge has ten secondary clock outputs: S_CLKOUT [9:0]. Nine secondary clock outputs can be used as clock inputs for up to nine external secondary bus devices. One secondary clock output has to be used for the PCI2060 secondary clock input (S_CLK) for internal state-machine synchronization purposes. Figure 3−2 shows a block diagram of the secondary clock function.

The PCI2060 bridge is designed to use either the primary PCI clock input (P_CLK) or the new SEC_ASYNC_CLK clock input to generate the secondary bus clocks. The maximum clock frequency that the P_CLK and the SEC_ASYNC_CLK inputs support is 66 MHz.

When using the primary PCI clock (P_CLK) as the clock input to generate the secondary bus clocks, the primary and secondary clocks must be synchronized to each other. The PCI2060 bridge is capable of supporting the following frequency combinations when using the primary PCI clock (P_CLK) as the clock input:

- 66-MHz primary bus, 66-MHz secondary bus
- 66-MHz primary bus, 33-MHz secondary bus
- 33-MHz primary bus, 33-MHz secondary bus

When using the primary PCI clock (P_CLK) as the clock input to generate the secondary bus clocks, the PCI2060 bridge does not support 33-MHz primary bus/66-MHz secondary bus operation, where the secondary bus is operating at twice the frequency of the primary bus.

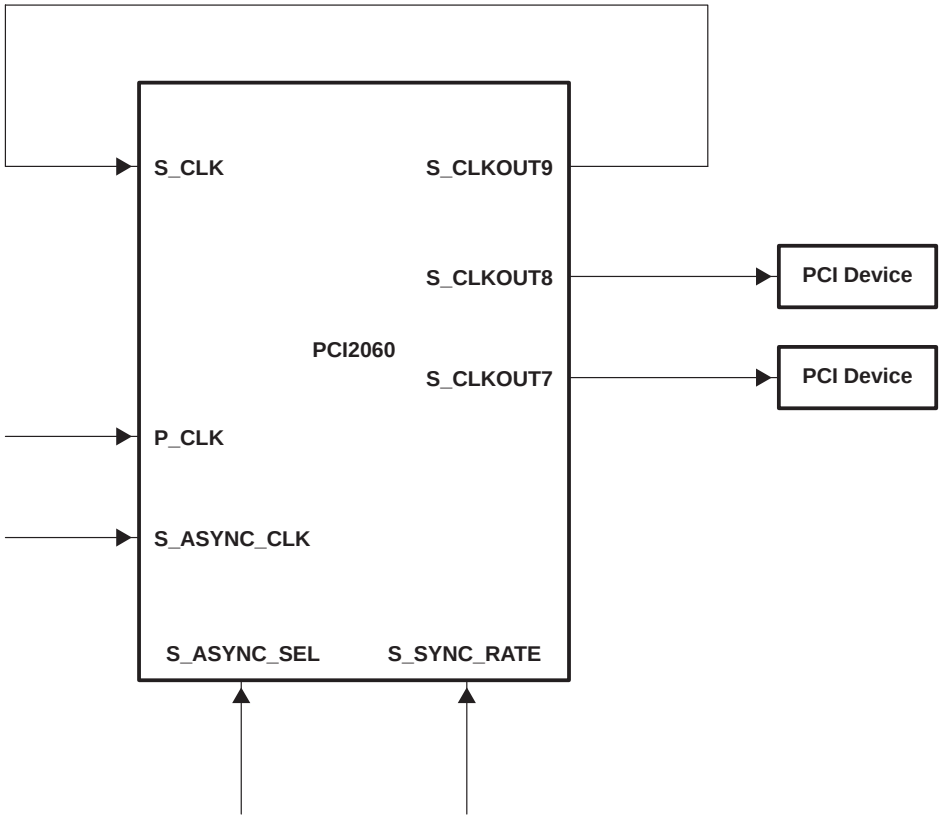


Figure 3−2. Secondary Clock Block Diagram

When using the SEC_ASYNC_CLK as the clock input to generate the secondary bus clocks, the secondary bus clocks do not need to be synchronized to the primary clock input. The PCI2060 bridge is capable of supporting operations in which the secondary bus clock frequencies can be greater than the primary clock frequency.

The SEC_ASYNC_SEL selects the clock that generates the secondary bus clock. If SEC_ASYNC_SEL is low, then the primary PCI clock (P_CLK) input generates the secondary bus clock. If SEC_ASYNC_SEL is high, then the SEC_ASYNC_CLK generates the secondary bus clock.

The SEC_ASYNC_RATE input determines if the secondary reference clock is directly output on the secondary clock terminals or if the secondary reference clock is divided by two before being output on the secondary clock terminals. If SEC_ASYNC_RATE is 0, then the clock outputs are divided by two. If SEC_ASYNC_RATE is 1, then the clock outputs are the same frequency as the secondary reference clock.

Table 3−9 illustrates the relationship between the CONFIG66, P_M66ENA, and S_M66ENA signals.

Table 3−9. CONFIG66, P_M66ENA, and S_M66ENA Configuration

CONFIG66	P_M66ENA	S_M66ENA	PRIMARY PCI INTERFACE TIME SPECIFICATION	SECONDARY PCI INTERFACE TIME SPECIFICATION
1	1	1	66 MHz	66 MHz
1	1	0	66 MHz	33 MHz
1	0	1	33 MHz	66 MHz
1	0	0	33 MHz	33 MHz
0	X	X	33 MHz	33 MHz

Table 3−10 illustrates the relationship between the SEC_ASYNC_SEL and the SEC_ASYNC_RATE signals.

Table 3−10. SEC_ASYNC_SEL and SEC_ASYNC_RATE Configuration

SEC_ASYNC_SEL	SEC_ASYNC_RATE	SECONDARY CLOCK SOURCE	CLOCK FREQUENCY RATIO
1	1	SEC_ASYNC_CLK	1
1	0	SEC_ASYNC_CLK	1/2
0	1	P_CLK	1
0	0	P_CLK	1/2

Table 3−11 illustrates the configuration of the CONFIG66, P_M66ENA, S_M66ENA, SEC_ASYNC_SEL, and SEC_ASYNC_RATE signals using some common frequencies as examples.

Table 3−11. CONFIG66, P_M66ENA, S_M66ENA, SEC_ASYNC_SEL, and SEC_ASYNC_RATE Configuration

P_CLK	SEC_ASYNC_CLK	CONFIG66	P_M66ENA	S_M66ENA	SEC_ASYNC_SEL	SEC_CL_RATE	S_CLK
66 MHz	X	1	1	1	0	1	66 MHz
66 MHz	50 MHz	1	1	1	1	1	50 MHz
66 MHz	X	1	1	0	0	0	33 MHz
66 MHz	50 MHz	1	1	0	1	0	25 MHz
33 MHz	66 MHz	1	0	1	1	1	66 MHz
33 MHz	50 MHz	1	0	1	1	1	50 MHz
33 MHz	X	0	X	X	0	1	33 MHz
33 MHz	50 MHz	0	X	X	1	0	25 MHz

The rules for using secondary clocks are:

- Each secondary clock output is limited to one load.
- One of the secondary clock outputs must be used for the PCI2060 S_CLK input. The clock line used for S_CLK must match the length of the longest secondary output trace.
- Use an equivalent amount of etch on the board for all secondary clocks, to minimize skew between them, and use a maximum etch delay of 2 ns.
- Route clock signals on the top layer and avoid vias for these signals.
- Terminate or disable unused secondary clock outputs using the secondary clock control register to reduce power dissipation and noise in the system.

3.11 Interrupt Routing

All parallel PCI interrupts on the secondary bus interface must be routed as sideband signals to the PCI interrupts on the primary interface. TI suggests that the board designer implement the interrupt routing scheme outlined in section 2.2.6 of the *PCI Local Bus Specification* Revision 2.2. Table 3−12 summarizes Section 2.2.6.

Table 3−12. Interrupt Routing Scheme

DEVICE NUMBER ON SECONDARY BUS	INTERRUPT TERMINAL ON DEVICE	INTERRUPT TERMINAL ON CONNECTOR
0, 4, 8, 12, 16, 20, 24, 28	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$
1, 5, 9, 13, 17, 21, 25, 29	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$
2, 6, 10, 14, 18, 22, 26, 30	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$
3, 7, 11, 15, 19, 23, 27, 31	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$

3.12 Mode Selection

The PCI2060 bridge supports three modes of operation: Intel-compatible mode, PCI power-management 1.1 mode, and CompactPCI hot-swap mode. Table 3−13 shows how each mode is selected using the MS0 and MS1 terminals. MS0 and MS1 can only be configured while the PCI2060 bridge is in reset.

Table 3−13. Mode Selections

MS0	MS1	MODE
0	0	Compact PCI Hot-Swap Mode GPIO3 functions as $\overline{\text{HSSWITCH}}$ *PCI Bus Power Management Interface Specification,* Revision 1.1
0	1	PCI Power-Management 1.1 Mode GPIO3 functions as GPIO3 *PCI Bus Power Management Interface Specification,* Revision 1.1
1	X	Intel-Compatible Mode *PCI Bus Power Management Interface Specification,* Revision 1.0

3.12.1 CompactPCI Hot-Swap Support

The PCI2060 bridge is designed to support the requirements for *Hot Swap Friendly* silicon in the CompactPCI 2.1 R1 specification. To be *Hot Swap Friendly* the PCI2060 bridge supports the following:

- Compliance with the *PCI Local Bus Specification*
- Tolerance of V_{CC} from early power
- Asynchronous reset
- Tolerance of precharge voltage
- I/O buffers meet the CompactPCI modified V/I requirements
- Limited I/O terminal current at precharge voltage
- Hot-swap control and status programming via an extended PCI capabilities linked list
- Hot-swap terminals: $\overline{\text{HSENUM}}$, $\overline{\text{HSSWITCH}}$, and HSLED

The PCI2060 bridge provides this functionality when configured into CompactPCI mode.

3.12.2 PCI Power Management

The *PCI Bus Power Management Interface Specification* establishes the infrastructure required to let the operating system control the power of PCI functions. This is accomplished by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI bus and the PCI functions can be assigned one of four software-visible power-management states, which result in varying levels of power savings.

The four power-management states of the PCI functions are: D0—fully on state, D1 and D2—intermediate states, and D3—off state. Similarly, bus power states of the PCI bus are B0 through B3. The bus power states B0 through B3 are derived from the device power state of the originating PCI2060 device.

For the operating system to manage the device power states on the PCI bus, the PCI function supports four power-management operations:

- Capabilities reporting
- Power status reporting
- Setting the power state
- System wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of the new capabilities list is indicated by bit 4 (CAPLIST) in the primary status register (offset 06h).

3.12.2.1 Behavior in Low-Power States

The PCI2060 bridge supports D0, D1, D2, and $D3_{HOT}$ power states when in the TI mode. The PCI2060 bridge only supports D0 and D3 power states when in the Intel mode. The PCI2060 bridge is fully functional only in D0 state. In the lower power state, the PCI2060 bridge does not accept any memory or I/O transactions. These transactions are aborted by the master. The bridge accepts type 0 configuration transactions in all power states except $D3_{COLD}$. The bridge also accepts type 1 configuration transactions but does not pass these cycles to the secondary bus in any of the lower power states. Type 1 configuration writes are discarded and reads return all 1s. All error reporting is done in the low power states. When in D2 and $D3_{HOT}$ states, the bridge turns off all secondary clocks for further power savings. When going from $D3_{HOT}$ to D0, an internal reset is generated. This reset initializes all PCI configuration registers to their default values except the TI specific registers (40h – FFh) and power-management registers.

3.13 JTAG Support

The PCI2060 bridge implements a JTAG test port based on the IEEE Standard 1149.1 *Standard Test Access Port and Boundary-Scan Architecture*. The JTAG port consists of the following:

- A 5-wire test access port
- A test access port controller
- An instruction register
- A bypass register
- A boundary-scan register

3.13.1 Test Port Instructions

The PCI2060 bridge supports the following JTAG instructions:

- EXTEST, BYPASS, and SAMPLE
- HIGHZ and CLAMP
- Private (various private instructions used by TI for test purposes)

3.13.2 Instruction Register

Table 3−14 lists and describes the different test port instructions, and gives the op code of each one. The instruction register selects and controls the operation of the boundary-scan and bypass registers.

Table 3−14. JTAG Instructions and Op Codes

INSTRUCTION	OP CODE	DESCRIPTION
EXTEST	00000	Drives terminals from the boundary scan register
SAMPLE	00001	Samples I/O terminals
CLAMP	00100	Drives terminals from the boundary scan register and selects the bypass register for shifts.
HIGHZ	00101	Puts all outputs and I/O terminals except for the TDO terminal into a high-impedance state.
BYPASS	11111	Selects the bypass register for shifts

3.13.3 1-Bit Bypass Register

The 1-bit bypass register is a 1-bit shift register that provides a means for effectively bypassing the JTAG test logic through a single-bit serial connection through the chip from TDI to TDO. At board-level testing, this helps reduce overall length of the scan ring.

3.13.4 Boundary Scan Register

The boundary-scan register is a single-shift register-based path formed by boundary-scan cells placed at the chip's signal terminals. The register is accessed through the JTAG port's TDI and TDO terminals.

3.13.4.1 Boundary-Scan Register Cells

Each boundary-scan cell operates in conjunction with the current instruction and the current state in the test access port controller state machine. The function of the boundary-scan register cells is determined by the associated terminals, as follows:

- Input-only terminals—The boundary-scan cell is basically a 1-bit shift register. The cell supports sample and shift functions.
- Output-only terminals—The boundary-scan cell comprises a 1-bit shift register and an output multiplexer. The cell supports the sample, shift, and drive output functions.
- Bidirectional terminals—The boundary-scan cell is identical to the output-only terminal cell, but it captures test data from the incoming data line. The cell supports sample, shift, drive output, and hold output functions. It is used at all I/O terminals.

The information in Table 3−15 is for implementation of boundary scan interface signals to permit in-circuit testing.

Table 3−15. Boundary Scan Terminal Order

BOUNDARY SCAN REGISTER NO.	GHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
0	J15	S_AD0	19	Bidirectional
1	H19	S_AD1	19	Bidirectional
2	H17	S_AD2	19	Bidirectional
3	H14	S_AD3	19	Bidirectional
4	G19	S_AD4	19	Bidirectional
5	G18	S_AD5	19	Bidirectional
6	G14	S_AD6	19	Bidirectional
7	F19	S_AD7	19	Bidirectional
8	G15	S_C/$\overline{\text{BE0}}$	19	Bidirectional
9	F17	S_AD8	19	Bidirectional
10	F14	S_AD9	19	Bidirectional
11	E18	S_M66ENA	19	Bidirectional
12	F15	S_AD10	19	Bidirectional
13	E17	MS0	−	Input
14	D18	SEC_ASYNC_RATE	−	Bidirectional
15	E14	S_AD11	19	Bidirectional
16	B15	S_AD12	19	Bidirectional
17	A15	S_AD13	19	Bidirectional
18	B14	S_AD14	19	Bidirectional
19	E13	S_AD15	19	Bidirectional
20	−	−	−	−
21	F12	S_C/$\overline{\text{BE1}}$	19	Bidirectional
22	C13	S_PAR	19	Bidirectional
23	B13	$\overline{\text{S\_SERR}}$	−	Input
24	E12	$\overline{\text{S\_PERR}}$	26	Bidirectional
25	C12	$\overline{\text{S\_LOCK}}$	26	Bidirectional
26	B12	$\overline{\text{S\_STOP}}$	26	Bidirectional
27	−	−	−	−
28	A11	$\overline{\text{S\_DEVSEL}}$	26	Bidirectional
29	B11	$\overline{\text{S\_TRDY}}$	26	Bidirectional
30	C11	$\overline{\text{S\_IRDY}}$	26	Bidirectional
31	F11	$\overline{\text{S\_FRAME}}$	26	Bidirectional
32	A10	S_C/$\overline{\text{BE2}}$	48	Bidirectional
33	E10	S_AD16	48	Bidirectional
34	F10	S_AD17	48	Bidirectional
35	C9	S_AD18	48	Bidirectional
36	F9	S_AD19	48	Bidirectional
37	A8	S_AD20	48	Bidirectional
38	B8	S_AD21	48	Bidirectional
39	F8	S_AD22	48	Bidirectional
40	E8	S_AD23	48	Bidirectional
41	B7	S_C/$\overline{\text{BE3}}$	48	Bidirectional
42	C7	S_AD24	48	Bidirectional

Table 3−15. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NO.	GHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
43	A6	S_AD25	48	Bidirectional
44	B6	S_AD26	48	Bidirectional
45	C6	S_AD27	48	Bidirectional
46	A5	S_AD28	48	Bidirectional
47	B5	S_AD29	48	Bidirectional
48	E6	S_AD30	48	Bidirectional
49	–	–	–	–
50	A4	S_AD31	48	Bidirectional
51	B4	$\overline{\text{S\_REQ0}}$	–	Input
52	E3	$\overline{\text{S\_REQ1}}$	–	Input
53	C4	SEC_ASYNC_SEL	–	Input
54	C1	SEC_ASYNC_CLK	–	Input
55	F5	$\overline{\text{S\_REQ2}}$	–	Input
56	G6	$\overline{\text{S\_REQ3}}$	–	Input
57	E2	$\overline{\text{S\_REQ4}}$	–	Input
58	E1	$\overline{\text{S\_REQ5}}$	–	Input
59	F3	$\overline{\text{S\_REQ6}}$	–	Input
60	F2	$\overline{\text{S\_REQ7}}$	–	Input
61	G5	$\overline{\text{S\_REQ8}}$	–	Input
62	F1	$\overline{\text{S\_GNT0}}$	61	Output
63	H6	$\overline{\text{S\_GNT1}}$	61	Output
64	–	–	–	Control
65	G2	$\overline{\text{S\_GNT2}}$	61	Output
66	G1	$\overline{\text{S\_GNT3}}$	61	Output
67	H5	$\overline{\text{S\_GNT4}}$	61	Output
68	H3	$\overline{\text{S\_GNT5}}$	61	Output
69	H2	$\overline{\text{S\_GNT6}}$	61	Output
70	H1	$\overline{\text{S\_GNT7}}$	61	Output
71	J1	$\overline{\text{S\_GNT8}}$	61	Output
72	J3	S_CLK	–	Input
73	J5	$\overline{\text{S\_RST}}$	78	Output
74	J6	$\overline{\text{S\_CFN}}$	–	Input
75	K1	GPIO3	78	Bidirectional
76	K2	GPIO2	78	Bidirectional
77	K5	GPIO1	78	Bidirectional
78	K6	GPIO0	78	Bidirectional
79	L1	S_CLKOUT0	–	Output
80	L2	S_CLKOUT1	–	Output
81	–	–	–	–
82	L5	S_CLKOUT2	–	Output
83	M1	S_CLKOUT3	–	Output
84	M3	S_CLKOUT4	–	Output
85	M6	S_CLKOUT5	–	Output

Table 3−15. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NO.	GHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
86	N1	S_CLKOUT6	−	Output
87	N2	S_CLKOUT7	−	Output
88	N6	S_CLKOUT8	−	Output
89	P1	S_CLKOUT9	−	Output
90	P2	$\overline{\text{P\_RST}}$	−	Input
91	N5	BPCCE	−	Input
92	P3	P_CLK	−	Input
93	R1	$\overline{\text{P\_GNT}}$	−	Input
94	P6	$\overline{\text{P\_REQ}}$	92	Output
95	−	−	−	−
96	R3	P_AD31	111	Bidirectional
97	T1	P_AD30	111	Bidirectional
98	R6	P_AD29	111	Bidirectional
99	W5	P_AD28	111	Bidirectional
100	U6	P_AD27	111	Bidirectional
101	R7	P_AD26	111	Bidirectional
102	W6	P_AD25	111	Bidirectional
103	U7	P_AD24	111	Bidirectional
104	V7	P_C/$\overline{\text{BE3}}$	111	Bidirectional
105	W7	P_IDSEL	−	Input
106	U8	P_AD23	111	Bidirectional
107	V8	P_AD22	111	Bidirectional
108	W9	P_AD21	111	Bidirectional
109	V9	P_AD20	111	Bidirectional
110	R9	P_AD19	111	Bidirectional
111	P9	P_AD18	111	Bidirectional
112	V10	P_AD17	111	Bidirectional
113	U10	P_AD16	111	Bidirectional
114	−	−	−	−
115	P10	P_C/$\overline{\text{BE2}}$	111	Bidirectional
116	W11	$\overline{\text{P\_FRAME}}$	118	Bidirectional
117	U11	$\overline{\text{P\_IRDY}}$	118	Bidirectional
118	P11	$\overline{\text{P\_TRDY}}$	118	Bidirectional
119	R11	$\overline{\text{P\_DEVSEL}}$	118	Bidirectional
120	W12	$\overline{\text{P\_STOP}}$	118	Bidirectional
121	−	−	−	−
122	P12	$\overline{\text{P\_LOCK}}$	118	Input
123	R12	$\overline{\text{P\_PERR}}$	118	Bidirectional
124	W13	$\overline{\text{P\_SERR}}$	142	Output
125	V13	P_PAR	142	Bidirectional
126	P13	P_C/$\overline{\text{BE1}}$	142	Bidirectional
127	W14	P_AD15	142	Bidirectional

Table 3−15. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NO.	GHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
128	R13	P_AD14	142	Bidirectional
129	U14	P_AD13	142	Bidirectional
130	P14	P_AD12	142	Bidirectional
131	V15	P_AD11	142	Bidirectional
132	U15	P_AD10	142	Bidirectional
133	T19	MS1	–	Input
134	R17	P_AD9	142	Bidirectional
135	N14	P_AD8	142	Bidirectional
136	R18	P_C/$\overline{BE0}$	142	Bidirectional
137	P17	P_AD7	142	Bidirectional
138	P18	P_AD6	142	Bidirectional
139	P19	P_AD5	142	Bidirectional
140	M14	P_AD4	142	Bidirectional
141	N18	P_AD3	142	Bidirectional
142	N19	P_AD2	142	Bidirectional
143	M17	P_AD1	142	Bidirectional
144	M18	P_AD0	142	Bidirectional
145	–	–	–	–
146	L17	MASK_IN	–	Input
147	–	–	–	–
148	L15	$\overline{HS\_ENUM}$	144	Output
149	L14	HS_LED	144	Output

3.14 GPIO INTERFACE

The PCI2060 bridge implements a four-terminal general-purpose I/O (GPIO) interface. Besides functioning as a GPIO interface, the GPIO terminals can read the secondary clock mask and stop the bridge from accepting I/O and memory transactions.

3.14.1 Secondary Clock Mask

The PCI2060 bridge uses GPIO0, GPIO2 and MSK_IN to shift the secondary clock mask from an external shift register. A secondary mask timing diagram is shown in Figure 3−3. Table 3−16 lists the format for clock mask data.

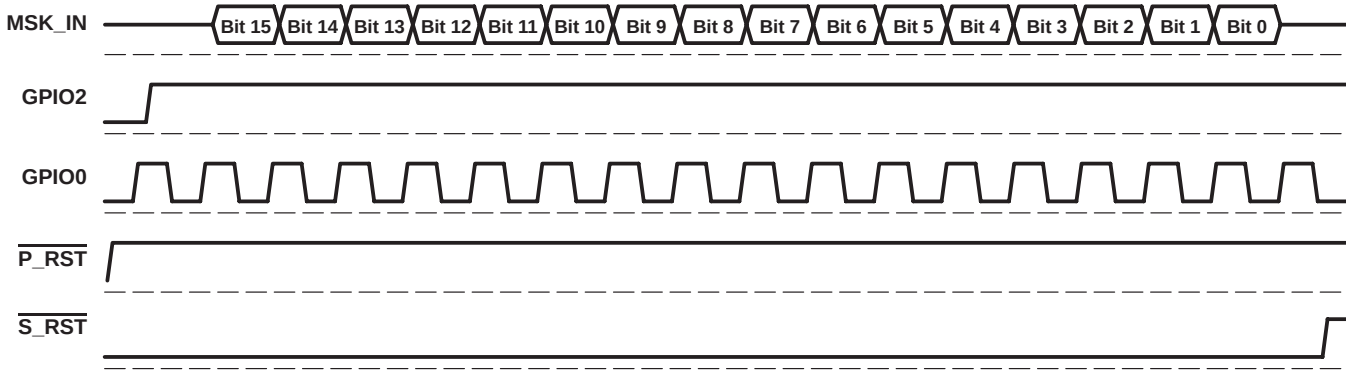


Figure 3−3. Clock Mask Read Timing After Reset

Table 3−16. Clock Mask Data Format

BIT	CLOCK
[0:1]	S_CLKOUT0
[2:3]	S_CLKOUT1
[4:5]	S_CLKOUT2
[6:7]	S_CLKOUT3
8	S_CLKOUT4
9	S_CLKOUT5
10	S_CLKOUT6
11	S_CLKOUT7
12	S_CLKOUT8
13	S_CLKOUT9
[14:15]	Reserved

3.14.2 Transaction Forwarding Control

The PCI2060 bridge stops forwarding I/O and memory transactions if bit 5 in the chip control register (offset 40h) is set to 1b and GPIO3 is driven high. The bridge completes all queued posted writes and delayed requests, but delayed completions are not returned until GPIO3 is driven low. This feature is not available in CompactPCI Hot-Swap mode because GPIO3 is used as the HS_SWITCH in this mode.

4 Configuration Header Space

This chapter describes the configuration header space of the PCI2060 bridge. The configuration head space is in compliance with the *PCI Local Bus Specification (*Revision 1.1). Table 4−1 shows the PCI configuration head space, which includes predefined portion of the bridge configuration space. Address spaces starting at offset 40h are device-specific registers. The PCI configuration offset is shown in the right column under the OFFSET heading.

Table 4−1. PCI Configuration Header Space

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Primary status		Primary command		04h
Class code			Revision ID	08h
BIST	Header type	Latency timer	Cache line size	0Ch
Reserved				10h
Reserved				14h
Secondary latency timer	Subordinate bus number	Secondary bus number	Primary bus number	18h
Secondary status		I/O Limit	I/O base	1Ch
Memory limit		Memory base		20h
Prefetchable memory limit		Prefetchable memory base		24h
Prefetchable base upper 32 bits				28h
Prefetchable limit upper 32 bits				2Ch
I/O limit upper 16 bits		I/O base upper 16 bits		30h
Reserved			Capabilities pointer	34h
Reserved				38h
Bridge control		Interrupt pin	Interrupt line	3Ch
Arbiter control		Extended diagnostic	Chip control	40h
Reserved				44h−60h
GPIO input data	GPIO output enable	GPIO output data	P_SER event disable	64h
Reserved	P_SER status	Secondary clock control		68h
Reserved				6Ch−D8hh
Power-management capabilities		PM next item pointer	PM capability ID	DCh
Data (Reserved)	PMCSR bridge support	Power-management control and status		E0h
Reserved	Hot-swap control and status	HS next item pointer	HS capability ID	E4h
Reserved				E8h−ECh
Reserved		TI diagnostic		F0h
Reserved				F4h−FCh

4.1 Vendor ID Register (00h)

The value in this 16-bit read-only register is allocated by the PCI special interest group (SIG) and identifies the manufacturer of the device. This register contains the value 104Ch, which identifies Texas Instruments as the manufacturer of this device.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2 Device ID Register (02h)

The value in this 16-bit read-only register is assigned by the device manufacturer and identifies the type of device. The device ID for the PCI2060 asynchronous bridge is AC2Ch.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	1	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0

4.3 Primary Command Register (04h)

The primary command register provides basic control over the PCI2060's ability to respond to and/or perform PCI accesses. Bits [15:11] are reserved for future use and must return 00000b. See Table 4−2 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−2. Primary Command Register

BIT	FIELD NAME	DESCRIPTION
15:11	RSVD	Reserved. Returns 00000b when read.
10	INT_DISABLE	$\overline{\text{INTx}}$ disable. This bit enables or disables device-specific interrupts. The PCI2060 bridge does not generate any interrupts internally. This bit is read-only and returns 0b when it is read.
9	FBB_ENB	Fast back-to-back enable 0 = The PCI2060 bridge does not generate back-to-back transactions on the primary bus. 1 = The PCI2060 bridge generates back-to-back transactions on the primary bus.
8	SERR_ENB	$\overline{\text{P\_SERR}}$ enable 0 = Disables the signaling of $\overline{\text{P\_SERR}}$ by PCI2060 bridge 1 = Enables the signaling of $\overline{\text{P\_SERR}}$ by PCI2060 bridge
7	STEP_ENB	Address/data stepping control. The PCI2060 bridge does not support address/data stepping. This bit is read-only and returns 0b when it is read.
6	PERR_ENB	Parity error response enable 0 = The PCI2060 bridge must ignore any address or data parity errors that it detects on the primary bus and continue normal operation. 1 = The PCI2060 bridge must take the appropriate action when any address or data parity errors are detected on the primary bus.
5	VGA_ENB	VGA palette snoop enable. When set, the PCI2060 bridge passes I/O writes on the primary PCI bus with addresses 3C6h, 3C8h, and 3C9h inclusive of ISA aliases (that is, only P_AD[9:0] are included in the decode).
4	MWI_ENB	Memory write-and-invalidate enable. The PCI2060 bridge generates memory write-and-invalidate transactions only when operating on behalf of another master whose memory write-and-invalidate transaction is crossing the PCI2060 bridge. This bit is read-only and returns 0b when it is read.
3	SPECIAL	Special cycle enable. The PCI2060 bridge does not respond to special cycle transactions. This bit is read-only and returns 0b when it is read.
2	MASTER_ENB	Bus master enable 0 = The PCI2060 bridge does not initiate I/O or memory transactions on the primary bus and does not respond to I/O or memory transactions on the secondary bus. 1 = The PCI2060 bridge is enabled to be an initiator on the primary bus and responds to I/O or memory transactions on the secondary bus.
1	MEMORY_ENB	Memory space enable 0 = The PCI2060 bridge does not respond to the memory transactions on the primary bus. 1 = The PCI2060 bridge responds to the memory transactions on the primary bus.
0	IO_ENB	I/O space enable 0 = The PCI2060 bridge does not respond to the I/O transactions on the primary bus. 1 = The PCI2060 bridge responds to the I/O transactions on the primary bus.

4.4 Primary Status Register (06h)

The status register provides status of the primary bus of the PCI2060 bridge. Bits in this register are cleared by writing a 1b to the respective bit; writing a 0b to a bit location has no effect. Bits 6 and [2:0] are reserved for future use and must return 0s. See Table 4−3 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	1	0	0	0	X†	1	0	0	0	0

† The default state of this bit is controlled by the CONFIG66 terminal.

Table 4−3. Primary Status Register

BIT	FIELD NAME	DESCRIPTION
15	PAR_ERR	Detected parity error. This bit is set when the PCI2060 bridge detects an address or data parity error on the primary bus. This bit is set regardless of the state of bit 6 (PERR_ENB) in the primary command register (offset 04h). 0 = No parity error detected 1 = Parity error detected
14	SYS_P_SERR	Signaled system error. This bit is set when the PCI2060 bridge signals $\overline{\text{P\_SERR}}$ on the primary bus. 0 = $\overline{\text{P\_SERR}}$ is not signaled 1 = $\overline{\text{P\_SERR}}$ is signaled
13	MABORT	Received master abort. This bit is set when the PCI2060 bridge is acting as a master on the primary bus and receives a master abort. 0 = Master abort not received on the primary bus 1 = Master abort received on the primary bus
12	TABORT_REC	Received target abort. This bit is set when the PCI2060 bridge is acting as a master on the primary bus and receives a target abort from the primary target. 0 = Target abort not received on the primary bus 1 = Target abort received on the primary bus
11	TABORT_SIG	Signaled target abort. This bit is set when the PCI2060 bridge is acting as a target on the primary bus and returns a target abort to the primary master. 0 = Target abort not signaled on the primary bus 1 = Target abort signaled on the primary bus
10:9	DEVSEL TIMING	DEVSEL timing. These two bits indicate the slowest response to a nonconfiguration command on the primary bus. These two bits are read-only and read 01b to indicate the PCI2060 bridge responds no slower than with medium timing.
8	DATAPAR	Master data parity error. This bit is set when the following conditions are met: • The PCI2060 device is the bus master on the primary bus during the data parity error. • $\overline{\text{P\_PERR}}$ was asserted by any PCI device on the primary bus including the PCI2060 device. • Bit 6 (PERR_ENB) is set in the primary command register (offset 04h). 0 = No data parity error detected on the primary bus 1 = Data parity error detected on the primary bus
7	FBB_CAP	Fast back-to-back capable. The PCI2060 bridge is able to accept fast back-to-back transactions; thus, this bit is hardwired to 1b.
6	RSVD	Reserved. Returns 0b when read.
5	66MHZ	66-MHz capable. This bit indicates whether the primary interface is 66 MHz capable. It reads 0b when CONFIG66 is tied low to indicate that PCI2060 bridge is not 66 MHz capable. It reads 1b when CONFIG66 is tied high to indicate that the primary bus is 66 MHz capable.
4	CAPLIST	Capabilities list. This read-only bit indicates whether or not a device implements the pointer for a new capabilities linked list at offset 34h. This bit returns 1b when read, indicating that the PCI2060 bridge supports additional PCI capabilities.
3	INT_STATUS	Interrupt status. This read-only bit reflects the state of the interrupt in the device. Since the PCI2060 bridge does not generate an interrupt internally, this bit returns 0b when it is read.
2:0	RSVD	Reserved. Returns 000b when read.

4.5 Revision ID Register (08h)

The value in this 8-bit read-only register specifies a device-specific revision identifier. The revision ID register returns 00h when it is read.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.6 Programming Interface Register (09h)

The value in this 8-bit read-only register specifies a register-level programming interface so that device-independent software can interface with the device. The programming interface register returns 00h when it is read.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.7 Subclass Code Register (0Ah)

The value in this 8-bit read-only register returns 04h when it is read, classifies the PCI2060 as a PCI-to-PCI bridge.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

4.8 Base Class Code Register (0Bh)

The value in this 8-bit read-only register returns 06h when it is read, classifies the PCI2060 as a bridge device.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	1	0

4.9 Cache Line Size Register (0Ch)

This read/write register is programmed by host software to indicate the system-cache line size needed by the bridge for memory read line, memory read multiple, and memory write-and-invalidate transactions. The PCI2060 bridge supports cache line sizes up to and including 16 doublewords for memory write-and-invalidate. If the cache line size is larger than 16 doublewords, then the command is converted to a memory write command.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.10 Primary Latency Timer Register (0Dh)

This read/write register defines the minimum period of time (in PCI clock cycles since $\overline{\text{P\_FRAME}}$ is asserted) that the PCI2060 bridge may continue a burst transaction even if it is preempted ($\overline{\text{P\_GNT}}$ is deasserted). When this register is set to 00h, the PCI2060 bridge relinquishes the bus after the first data transfer when $\overline{\text{P\_GNT}}$ is deasserted.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.11 Header Type Register (0Eh)

The header type register is read-only and returns 01h when read, indicating that the PCI2060 configuration space adheres to the PCI-to-PCI bridge configuration. Only the layout for bytes 10h–3Fh of the configuration space is considered.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

4.12 BIST Register (0Fh)

The PCI2060 bridge does not support built-in self-test (BIST). The BIST register is read-only and returns the value 00h when read.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.13 Primary Bus Number Register (18h)

The primary bus number register indicates the primary bus number to which the PCI2060 bridge is connected. The bridge uses this register, in conjunction with the secondary bus number and subordinate bus number registers, to decode type 1 configuration transactions on the secondary interface that must be either converted to special cycle transactions on the primary interface or passed upstream unaltered.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.14 Secondary Bus Number Register (19h)

This read/write register specifies the bus number of the PCI bus segment that the secondary interface is connected to. The PCI2060 bridge uses this register to determine when to respond to and forward type 1 configuration transactions on the primary interface, and to determine when to convert them to type 0 or special cycle transactions on the secondary interface.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.15 Subordinate Bus Number Register (1Ah)

This read/write register specifies the bus number of the highest number PCI bus segment that is subordinate to the PCI2060 bridge. In conjunction with the secondary bus number register, the PCI2060 bridge uses this register to determine when to respond to type 1 configuration transactions on the primary interface and pass them to the secondary interface as a type 1 configuration transaction.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.16 Secondary Latency Timer Register (1Bh)

This read/write register defines the minimum period of time (in PCI clock cycles since $\overline{\text{S\_FRAME}}$ is asserted) that the PCI2060 bridge may continue a burst transaction even if it is preempted (the PCI2060 secondary bus grant is deasserted). When this register is set to 00h, the PCI2060 bridge relinquishes the bus after the first data transfer when its secondary bus grant is deasserted.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.17 I/O Base Address Register (1Ch)

The I/O base address register defines the lower limit of the I/O address range that is used by the PCI2060 bridge to determine when to forward I/O transactions from one interface to the other. Bits [3:0] are read-only and default to 1h to indicate that the PCI2060 bridge supports 32-bit I/O addressing. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 address bits of the I/O base address are assumed to be 000h. Thus, the bottom of the defined I/O address range is aligned on a 4K-byte boundary. The upper 16 address bits of the 32-bit I/O base address correspond to the contents of the I/O base address upper 16 bits register (offset 30h). See Table 4−4 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

Table 4−4. I/O Base Register

BIT	FIELD NAME	DESCRIPTION
7:4	IOBASE [15:12]	I/O base. Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O base address upper 16 bits register.
3:0	IOTYPE	I/O type. This field is read-only. It reads 1h indicating that the PCI2060 bridge supports 32-bit I/O addressing.

4.18 I/O Limit Address Register (1Dh)

This read/write register defines the upper limit of the I/O addresses range that is used by the PCI2060 bridge to determine when to forward I/O transactions from one interface to the other. Bits [3:0] are read-only and default to 1h to indicate that the PCI2060 bridge supports 32-bit I/O addressing. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 address bits of the I/O limit address are considered FFFh. Thus, the top of the defined I/O address range is aligned on a 4K-byte boundary. The upper 16 address bits of the 32-bit I/O limit address correspond to the contents of the I/O limit address upper 16 bits register (offset 32h). See Table 4−5 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

Table 4−5. I/O Limit Address Register

BIT	FIELD NAME	DESCRIPTION
7:4	IOLIMIT [15:12]	I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writeable and correspond to address bits [15:12]. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit address upper 16 bits register.
3:0	IOTYPE	I/O type. This field is read-only. It reads 1h indicating that the PCI2060 bridge supports 32-bit I/O addressing.

4.19 Secondary Status Register (1Eh)

The status register provides status of the primary bus of the PCI2060 bridge. Writing a 1b to the respective bit clears bits in this register; writing a 0b to a bit location has no effect. See Table 4−6 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	1	0	0	0	X†	0	0	0	0	0

† The default state of this bit is dependent on the state of the CONFIG66 terminal.

Table 4−6. Secondary Status Register

BIT	FIELD NAME	DESCRIPTION
15	PAR_ERR	Detected parity error. This bit is set when an address or data parity error is detected on the secondary bus. This bit is set regardless of the state of bit 0 (PERR_EN) in the bridge control register (offset 3Eh). 0 = Parity error is not detected 1 = Parity error is detected
14	SYS_S_SERR	Received system error. This bit reports the detection of the assertion of $\overline{\text{S\_SERR}}$ on the secondary bus. 0 = $\overline{\text{S\_SERR}}$ assertion is not detected on the secondary bus 1 = $\overline{\text{S\_SERR}}$ assertion is detected on the secondary bus
13	MABORT	Received master abort. This bit reports the detection of a master-abort termination by the PCI2060 bridge when it is the master of a transaction on its secondary bus. 0 = Master abort is not detected by the PCI2060 bridge on its secondary bus 1 = Unsupported request or master abort is detected by the PCI2060 bridge on its secondary bus
12	TABORT_REC	Received target abort. This bit reports the detection of a target-abortion termination by the PCI2060 bridge when it is the master of a transaction on its secondary bus. 0 = Target abort is not detected by the PCI2060 bridge on its secondary bus 1 = Target abort is detected by the PCI2060 bridge on its secondary bus
11	TABORT_SIG	Signaled target abort. This bit reports the signaling of a target-abort termination by the PCI2060 bridge when it responds as the target of a transaction on its secondary bus. 0 = Target abort is not signaled by the PCI2060 bridge on its secondary bus 1 = Target abort is signaled by the PCI2060 bridge on its secondary bus
10:9	PCI_SPEED	DEVSEL timing. These bits indicate the slowest response time to a command on the secondary bus. These bits return 01b, indicating that the PCI2060 bridge responds no slower than with medium timing.
8	DATAPAR	Master data parity error. This bit is set to 1b when the following conditions have been met: • The PCI2060 bridge is the bus master. • $\overline{\text{S\_PERR}}$ was asserted by any PCI device on the secondary bus, including the PCI2060 bridge. • Bit 0 (PERR_EN) is set in the bridge control register (offset 3Eh). 0 = Data parity error is not detected on the secondary interface 1 = Data parity error is detected on the secondary interface
7	FBB_CAP	Fast back-to-back capable. This bit reads 1b to indicate PCI2060 bridge is able to respond to fast back-to-back transaction on the secondary bus.
6	RSVD	Reserved. Returns 0b when read.
5	66MHZ	66-MHz capable. This bit indicates whether the secondary interface is 66-MHz capable. It reads 0b when CONFIG66 is tied low to indicate that PCI2060 bridge is not 66-MHz capable. It reads 1b when CONFIG66 is tied high to indicate that the secondary bus is 66-MHz capable.
4:0	RSVD	Reserved. Returns 00000b when read.

4.20 Memory Base Address Register (20h)

The memory base address register defines the bottom address of a memory-mapped I/O address range used by the bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits [31:20]. The lower 20 address bits are assumed to be 00000h; thus, the address range is aligned to a 1M-byte boundary. The bottom four bits are reserved and return 0h when read. See Table 4−7 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−7. Memory Base Address Register

BIT	FIELD NAME	DESCRIPTION
15:4	MEMBASE	Memory base. Defines the bottom address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h.
3:0	RSVD	Reserved. Returns 0h when read.

4.21 Memory Limit Address Register (22h)

The memory limit address register defines the upper-limit address of a memory-mapped I/O address range used by the PCI2060 bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits [31:20]. The lower 20 address bits are assumed to be FFFFFh; thus, the address range is aligned to a 1M-byte boundary. The bottom 4 bits are reserved and return 0h when read. See Table 4−8 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−8. Memory Limit Address Register

BIT	FIELD NAME	DESCRIPTION
15:4	MEMLIMIT	Memory limit. Defines the top address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	Reserved. Returns 0h when read.

4.22 Prefetchable Memory Base Address Register (24h)

The prefetchable memory base address register defines the bottom address of a prefetchable memory address range used by the PCI2060 bridge to determine when to forward memory transactions from one interface to the other. Bits [3:0] are read-only and default to 1h to indicate that the PCI2060 bridge supports 64-bit memory addressing. The upper 12 bits of this register are read/write and correspond to the address bits [31:20]. The lower 20 address bits are assumed to be 00000h; thus, the address range is aligned to a 1M-byte boundary. See Table 4−9 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4−9. Prefetchable Memory Base Address Register

BIT	FIELD NAME	DESCRIPTION
15:4	PREBASE	Prefetchable memory base. Defines the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base-address upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	64-bit memory indicator. This field is read-only. It reads 1h indicating that the PCI2060 bridge supports 64-bit memory addressing.

4.23 Prefetchable Memory Limit Address Register (26h)

The prefetchable memory-limit address register defines the upper-limit address of a prefetchable memory address range that determines when to forward memory transactions from one interface to the other. Bits [3:0] are read-only and default to 1h to indicate the PCI2060 bridge supports 64-bit memory addressing. The upper 12 bits of this register are read/write and correspond to the address bits [31:20]. The lower 20 address bits are considered FFFFFh; thus, the address range is aligned to a 1M-byte boundary. See Table 4−10 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4−10. Prefetchable Memory Limit Address Register

BIT	FIELD NAME	DESCRIPTION
15:4	PRELIMIT	Prefetchable memory limit. Defines the top address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable-limit upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	64-bit memory Indicator. This field is read-only. It reads 1h indicating that the PCI2060 bridge supports 64-bit memory addressing.

4.24 Prefetchable Memory Base Address Upper 32-Bit Register (28h)

The prefetchable memory-base address upper 32-bit register and the prefetchable memory-base address register define the base address of the 64-bit prefetchable memory address range used by the PCI2060 bridge to determine when to forward memory transactions from one interface to the other. The prefetchable memory base address upper 32-bit register must be programmed to 0000 0000h when 32-bit addressing is being used. See Table 4−11 for a complete description of the register contents.

Bit Number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−11. Prefetchable Memory Base Address Upper 32-Bit Register

BIT	FIELD NAME	DESCRIPTION
31:0	PREBASE	Prefetchable memory-base upper 32 bits. Defines the upper 32 bits of the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

4.25 Prefetchable Memory Limit Address Upper 32-Bit Register (2Ch)

The prefetchable memory-limit address upper 32-bit register and prefetchable memory-limit address register define the upper-limit address of the 64-bit prefetchable memory address range used by the PCI2060 bridge to determine when to forward memory transactions from one interface to the other. The prefetchable memory-limit address upper 32-bit register must be programmed to 0000 0000h when 32-bit addressing is being used. See Table 4−12 for a complete description of the register contents.

Bit Number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Number	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−12. Prefetchable Memory Limit Address Upper 32-Bit Register

BIT	FIELD NAME	DESCRIPTION
31:0	PRELIMIT	Prefetchable memory-limit upper 32 bits. Defines the upper-limit of the 64-bit prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

4.26 I/O Base-Address Upper 16-Bit Register (30h)

The I/O base-address upper 16-bit register and the I/O base-address register define the base address of the 32-bit I/O memory-address range that determines when to forward I/O transactions from one interface to the other. The I/O base-address upper 16-bit register must be programmed to 0000h when 16-bit addressing is being used. See Table 4−13 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−13. I/O Base-Address Upper 16-Bit Register

BIT	FIELD NAME	DESCRIPTION
15:0	IOBASE	I/O base upper 16 bits. Defines the upper 16 bits of the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other.

4.27 I/O Limit-Address Upper 16-Bit Register (32h)

The I/O limit-address upper 16-bit register and I/O limit-address register define the upper-limit address of the 32-bit I/O memory-address range used by the PCI2060 bridge to determine when to forward I/O transactions from one interface to the other. The I/O limit-address upper 16-bit register must be programmed to 0000h when 16-bit addressing is being used. See Table 4−14 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−14. I/O Limit-Address Upper 16-Bit Register

BIT	FIELD NAME	DESCRIPTION
15:0	IOLIMIT	I/O limit upper 16 bits. Defines the upper-limit address of the 32-bit I/O memory address range used by the PCI2060 bridge to determine when to forward I/O transactions from one interface to the other.

4.28 Capabilities Pointer Register (34h)

The capabilities pointer register points to a linked list of additional capabilities implemented by a device. For the PCI2060 bridge, the capabilities pointer register provides the pointer to the PCI configuration header where the PCI power-management register block resides. The capabilities pointer register is read-only and returns DCh when read, indicating the power-management registers are located at PCI header offset DCh.

Bit Number	7	6	5	4	3	2	1	0
Reset State	1	1	0	1	1	1	0	0

4.29 Interrupt Line Register (3Ch)

The interrupt line register is read/write and communicates interrupt-line routing information. Since the bridge does not implement an interrupt signal terminal, this register defaults to 00h.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.30 Interrupt Pin Register (3Dh)

This register returns 00h when it is read, indicating the PCI2060 bridge does not implement an interrupt pin.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.31 Bridge Control Register (3Eh)

The bridge control register provides extensions to the command register that are specific to a bridge. The bridge control register provides many of the same controls for the secondary interface that are provided by the command register for the primary interface. See Table 4−15 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−15. Bridge Control Register

BIT	FIELD NAME	DESCRIPTION
15:12	RSVD	Reserved. Returns 0h when read.
11	DTSERR	Discard timer $\overline{\text{SERR}}$ enable. This bit controls the assertion of $\overline{\text{P\_SERR}}$ on the primary interface when either the primary discard timer or the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. 0 = Do not assert $\overline{\text{P\_SERR}}$ on the primary bus as a result of expiration of either the primary discard timer or the secondary discard timer 1 = Assert $\overline{\text{P\_SERR}}$ on the primary bus if either the primary discard timer or the secondary discard timer expires and a delayed transaction is discarded
10	DTSTATUS	Discard timer status. This bit is set to a 1b when either the primary discard timer or the secondary discard timer expires and a delayed completion is discarded from a queue in the bridge. 0 = No discard timer error 1 = Discard timer error
9	SEC_DT	Secondary discard timer. Selects the number of PCI clocks that the PCI2060 bridge will wait for a master on the secondary bus to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary bus) has reached the head of the downstream queue of the bridge (that is, all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = The secondary discard timer counts 2^{15} PCI clock cycles 1 = The secondary discard timer counts 2^{10} PCI clock cycles
8	PRI_DIS	Primary discard timer. Selects the number of PCI clocks that the bridge will wait for a master on the primary bus to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the secondary interface) has reached the head of the upstream queue of the bridge (that is, all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the primary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = The primary discard timer counts 2^{15} PCI clock cycles 1 = The primary discard timer counts 2^{10} PCI clock cycles
7	FBB_EN	Fast back-to-back enable. This bit controls the ability of the PCI2060 bridge to generate fast back-to-back transactions to different devices on the secondary interface. 0 = The PCI2060 bridge is disabled to generate fast back-to-back transactions on the secondary PCI bus 1 = The PCI2060 bridge is enabled to generate fast back-to-back transactions on the secondary PCI bus
6	SRST	Secondary bus reset. Setting this bit to 1b forces the assertion of $\overline{\text{S\_RST}}$ on the secondary interface. The $\overline{\text{S\_RST}}$ is asserted by the bridge whenever this bit is set or the $\overline{\text{P\_RST}}$ terminal on the primary bus is asserted. When this bit is cleared, $\overline{\text{S\_RST}}$ on the secondary bus is asserted whenever the primary interface $\overline{\text{RST}}$ is asserted. 0 = Do not force the assertion of the $\overline{\text{S\_RST}}$ 1 = Force the assertion of the $\overline{\text{S\_RST}}$

Table 4−15. Bridge Control Register (Continued)

BIT	FIELD NAME	DESCRIPTION
5	MAM	Master abort mode. Controls how the bridge responds to a master abort that occurs on either interface when the bridge is the master. If this bit is set, the posted write transaction has completed on the requesting interface, and SERR enable (bit 8) of the primary command register (offset 04h) is 1b, then P_SERR is asserted when a master abort occurs. If the transaction has not completed, then a target abort is signaled. If the bit is cleared, then all 1s are returned on reads and write data is accepted and discarded when a transaction that crosses the bridge is terminated with master abort. 0 = Do not report master aborts (returns FFFF FFFFh on reads and discards data on writes) 1 = The PCI2060 bridge returns a target abort on the initiator bus for delayed transactions. For posted write transactions, the bridge asserts P_SERR if bit 8 (SERR_ENB) is set in the primary command register
4	RSVD	Reserved. Returns 0b when read.
3	VGA	VGA enable. This bit modifies the response by the PCI2060 bridge to VGA-compatible addresses. If this bit is set, then the PCI2060 bridge positively decodes and forwards the following accesses on the primary to the secondary bus (and, conversely, blocks the forwarding of these addresses from the secondary to primary bus): • Memory accesses in the range 000A 0000h to 000B FFFFh • I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases—address bits [15:10] may possess any value and are not used in the decoding) If the VGA enable bit is set, then forwarding of VGA addresses is independent of: the value of bit 2 (ISA), the I/O address range and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the primary command register (offset 04h). 0 = Do not forward VGA-compatible memory and I/O addresses from the primary to secondary bus (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges 1 = Forward VGA-compatible memory and I/O addresses (addresses defined above) from the primary to the secondary bus (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of bit 2 (ISA)
2	ISA	ISA enable. This bit modifies the response by the PCI2060 bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, then the PCI2060 bridge blocks forwarding I/O transactions from primary to secondary that address the last 768 bytes in each 1 KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1 KB block. 0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers 1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1 KB block)
1	SERR_EN	SERR enable. Controls the forwarding of S_SERR assertion to the primary bus. The bridge asserts P_SERR on the primary bus when all of the following are true: • S_SERR is asserted on the secondary interface. • This bit is set. • Bit 8 (SERR_ENB) is set in the primary command register (offset 04h). 0 = The PCI2060 bridge does not assert P_SERR on the primary bus in response to the assertion of S_SERR on the secondary bus 1 = The PCI2060 bridge asserts P_SERR on the primary bus in response to the assertion of S_SERR on the secondary bus
0	PERR_EN	Parity error response enable. Controls the bridge response to address and data parity errors on the secondary bus. 0 = The PCI2060 bridge does not assert S_PERR. Bit 8 (DATAPAR) in the secondary status register (offset 1Eh) is not set. The PCI2060 bridge also does not report any parity errors by asserting P_SERR on the primary bus 1 = The PCI2060 bridge asserts S_PERR and conditionally sets bit 8 (DATAPAR) in the secondary status register (offset 1Eh) when a data parity error is detected on the secondary bus. This bit must be set to 1b in order for the PCI2060 bridge to assert the P_SERR assertion when parity errors are detected on the secondary interface

5 Extension Registers

The TI extension registers are those registers that lie outside the standard PCI-to-PCI bridge device configuration space (that is, registers 40h−FFh in the PCI configuration space in the PCI2060 bridge). These registers can be accessed through configuration reads and writes. The TI extension registers add flexibility and performance benefits to the standard PCI-to-PCI bridge. Mapping of the extension registers is contained in Table 4−1.

5.1 Chip Control Register (40h)

The chip control register controls the functionality of certain PCI transactions. See Table 5−1 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−1. Chip Control Register

BIT	FIELD NAME	DESCRIPTION
7:6	RSVD	Reserved. Returns 00b when read.
5	TRANS_CTRL	Transaction forwarding control for I/O and memory cycles. 0 = Transaction forwarding is enabled and controlled by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the primary command register (offset 04h) 1 = Transaction forwarding is disabled if GPIO3 is driven high. Bits 0 (IO_ENB), 1 (MEMORY_ENB), and 2 (MASTER_ENB) in the primary command register (offset 04h) are set to 000b
4	READ_PREFETCH_DIS	Memory read prefetch disable. When set, bit 4 disables read prefetching on upstream memory read commands. 0 = Upstream memory read prefetch is enabled 1 = Upstream memory reads prefetch is disabled
3:2	RSVD	Reserved. Returns 00b when read.
1	MW_DISCONNECT_CRTL	Memory write disconnect control. This bit does not affect memory write-and-invalidate transactions. 0 = Disconnects on queue full or 4-KB boundaries 1 = Disconnects on queue full, 4-KB boundaries, and cache line boundaries
0	RSVD	Reserved. Returns 0b when read.

5.2 Extended Diagnostic Register (41h)

Bit 0 of the extended diagnostic register resets both the PCI2060 bridge and the secondary bus. See Table 5−2 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−2. Extended Diagnostic Register

BIT	FIELD NAME	DESCRIPTION
7:1	RSVD	Reserved. Returns 000 0000b when read.
0	CHIP_RESET	Chip and secondary bus reset control. Setting this bit to 1b causes the PCI2060 bridge to perform a chip reset. Data buffers, configuration registers, and both the primary and secondary interfaces are reset to their initial state. This bit is self-clearing.

5.3 Arbiter Control Register (42h)

The arbiter control register is used for the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The PCI2060 bridge is the only secondary bus initiator that defaults to the higher priority arbitration tier. See Table 5−3 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Table 5−3. Arbiter Control Register

BIT	FIELD NAME	DESCRIPTION
15:10	RSVD	Reserved. Returns 00 0000b when read.
9	BRIDGE_TIER_SEL	Bridge tier select. This bit determines in which tier the PCI2060 bridge is placed in the two-tier arbitration scheme. 0 = Low priority tier 1 = High priority tier
8	GNT8_TIER_SEL	$\overline{\text{S\_GNT8}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT8}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
7	GNT7_TIER_SEL	$\overline{\text{S\_GNT7}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT7}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
6	GNT6_TIER_SEL	$\overline{\text{S\_GNT6}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT6}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
5	GNT5_TIER_SEL	$\overline{\text{S\_GNT5}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT5}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
4	GNT4_TIER_SEL	$\overline{\text{S\_GNT4}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT4}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
3	GNT3_TIER_SEL	$\overline{\text{S\_GNT3}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT3}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
2	GNT2_TIER_SEL	$\overline{\text{S\_GNT2}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT2}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
1	GNT1_TIER_SEL	$\overline{\text{S\_GNT1}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT1}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier
0	GNT0_TIER_SEL	$\overline{\text{S\_GNT0}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT0}}$ is placed in the arbitration scheme. 0 = Low priority tier 1 = High priority tier

5.4 P_SERR Event Disable Register (64h)

The P_SERR event disable register enables/disables the SERR event on the primary interface. All events are enabled by default. See Table 5−4 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−4. P_SERR Event Disable Register

BIT	FIELD NAME	DESCRIPTION
7	RSVD	Reserved. Returns 0b when read.
6	DELAYED_READ_TO	Master delayed read time-out. This bit controls the assertion of the $\overline{\text{P\_SERR}}$ when the PCI2060 bridge is unable to transfer any read data from the target after 2^{24} attempts. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
5	DELAYED_WRITE_TO	Master delayed write time-out. The bit controls the assertion of the $\overline{\text{P\_SERR}}$ when the PCI2060 bridge is unable to deliver delayed write data after 2^{24} attempts. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
4	MASTER_ABORT_PW	Master abort on posted write transactions. This bit controls the assertion of the $\overline{\text{P\_SERR}}$ when the PCI2060 bridge receives a master abort when attempting to deliver posted write data. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
3	TARGET_ABORT_PW	Target abort on posted write transactions. This bit controls the assertion of $\overline{\text{P\_SERR}}$ when it receives a target abort when attempting to deliver posted write data. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
2	POSTED_WRITE_TO	Posted write time out. This bit controls the assertion of the $\overline{\text{P\_SERR}}$ when the PCI2060 bridge is unable to deliver posted write data after 2^{24} attempts. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
1	POSTED_WRITE_PERR	Posted write parity error. This bit controls the assertion of the $\overline{\text{P\_SERR}}$ when a parity error is detected on the target bus during a posted write transaction. 0 = $\overline{\text{P\_SERR}}$ is asserted if this event occurs and bit 8 (SERR_ENB) in the primary command register (offset 04h) is set 1 = $\overline{\text{P\_SERR}}$ is not asserted if this event occurs
0	RSVD	Reserved. Returns 0b when read.

5.5 GPIO Output Data Register (65h)

The GPIO output data register controls the data driven on the GPIO terminals configured as outputs. If both an output-high bit and an output-low bit are set for the same GPIO terminal, then the output-low bit takes precedence. The output data bits have no effect on a GPIO terminal that is programmed as an input. See Table 5−5 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−5. GPIO Output Data Register

BIT	FIELD NAME	DESCRIPTION
7:4	GPIO OUTPUT WRITE_1_TO_SET	The GPIO [3:0] pin output data write 1 to set. Writing a 1b to any of these bits drives the corresponding bit high on the GPIO [3:0] bus if it is programmed as bidirectional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Writing 0b to these bits has no effect.
3:0	GPIO OUTPUT WRITE_1_TO_CLEAR	The GPIO [3:0] pin output data write 1 to clear. Writing a 1b to any of these bits drives the corresponding bit low on the GPIO [3:0] bus if it is programmed as bidirectional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Writing 0b to these bits has no effect.

5.6 GPIO Output Enable Register (66h)

The GPIO output enable register controls the direction of the GPIO signal. By default, all GPIO terminals are inputs. If both an output-enable bit and an input-enable bit are set for the same GPIO terminal, then the input-enable bit takes precedence. See Table 5−6 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−6. GPIO Output Enable Register

BIT	FIELD NAME	DESCRIPTION
7:4	GPIO OUTPUT ENABLE WRITE_1_TO_SET	The GPIO [3:0] output enable write 1 to set. Writing a 1b to any of these bits configures the corresponding GPIO [3:0] terminal, enables the output driver, and drives the value set in the output data register (65h). Writing 0b to this register has no effect.
3:0	GPIO OUTPUT ENABLE WRITE_1_TO_CLEAR	The GPIO [3:0] output enable write 1 to clear. Writing 1b to any of these bits configures the corresponding GPIO [3:0] terminal as an input only. Writing 0b to this register has no effect.

5.7 GPIO Input Data Register (67h)

This register reads the current state of the GPIO terminals. Each GPIO field in this register is updated on the rising edge of the PCI clock following the change in the GPIO terminals. See Table 5−7 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−7. GPIO Input Data Register

BIT	FIELD NAME	DESCRIPTION
7	GPIO [3:0] INPUT DATA	GPIO3−GPIO0 input data. These four bits return the current state of the GPIO terminals. Each GPIO field in this register is updated on the rising edge of the PCI clock following the change in the GPIO terminals.
3:0	RSVD	Reserved. Returns 0h when read.

5.8 Secondary Clock Control Register (68h)

The secondary clock control register controls the secondary clock outputs. See Table 5−8 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−8. Secondary Clock Control Register

BIT	FIELD NAME	DESCRIPTION
15:14	RSVD	Reserved. Returns 00b when read.
13	CLKOUT9_DISABLE	S_CLKOUT9 disable 0 = S_CLKOUT9 enabled 1 = S_CLKOUT9 disabled and driven low
12	CLKOUT8_DISABLE	S_CLKOUT8 disable 0 = S_CLKOUT8 enabled 1 = S_CLKOUT8 disabled and driven low
11	CLKOUT7_DISABLE	S_CLKOUT7 disable 0 = S_CLKOUT7 enabled 1 = S_CLKOUT7 disabled and driven low
10	CLKOUT6_DISABLE	S_CLKOUT6 disable 0 = S_CLKOUT6 enabled 1 = S_CLKOUT6 disabled and driven low
9	CLKOUT5_DISABLE	S_CLKOUT5 disable 0 = S_CLKOUT5 enabled 1 = S_CLKOUT6 disabled and driven low
8	CLKOUT4_DISABLE	S_CLKOUT4 disable 0 = S_CLKOUT4 enabled 1 = S_CLKOUT4 disabled and driven low
7:6	CLKOUT3_DISABLE	S_CLKOUT3 disable 00, 01, 10 = S_CLKOUT3 enabled 11 = S_CLKOUT3 disabled and driven low
5:4	CLKOUT2_DISABLE	S_CLKOUT2 disable 00, 01, 10 = S_CLKOUT2 enabled 11 = S_CLKOUT2 disabled and driven low
3:2	CLKOUT1_DISABLE	S_CLKOUT1 disable 00, 01, 10 = S_CLKOUT1 enabled 11 = S_CLKOUT1 disabled and driven low
1:0	CLKOUT0_DISABLE	S_CLKOUT0 disable 00, 01, 10 = S_CLKOUT0 enabled 11 = S_CLKOUT0 disabled and driven low

5.9 P_SERR Status Register (6Ah)

The P_SERR status register indicates the cause of $\overline{\text{P\_SERR}}$ assertion. See Table 5−9 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−9. P_SERR Status Register

BIT	FIELD NAME	DESCRIPTION
7	RSVD	Reserved. Returns 0b when read.
6	DELAYED_READ_TO	Master delayed read time-out. $\overline{\text{P\_SERR}}$ is asserted since the PCI2060 bridge was unable to read data from the target after 2^{24} attempts.
5	DELAYED_WRITE_TO	Master delayed write time-out. $\overline{\text{P\_SERR}}$ is asserted since the PCI2060 bridge was unable to deliver delayed write data after 2^{24} attempts.
4	MASTER_ABORT_PW	Master abort on posted write transactions. $\overline{\text{P\_SERR}}$ is asserted since the PCI2060 bridge received a master abort when attempting to deliver posted write data.
3	TARGET_ABORT_PW	Target abort on posted writes. $\overline{\text{P\_SERR}}$ is asserted since the PCI2060 bridge received a target abort when delivering posted write data.
2	POSTED_WRITE_TO	Master posted write time-out. $\overline{\text{P\_SERR}}$ is asserted since the PCI2060 bridge was unable to deliver posted write data to the target after 2^{24} attempts.
1	POSTED_WRITE_PERR	Posted write parity error. $\overline{\text{P\_SERR}}$ is asserted since a posted write data parity error was detected on the target bus.
0	RSVD	Reserved. Returns 0b when read.

5.10 Capability ID Register (DCh)

The capability ID register identifies the linked list item as the register for PCI power management. The capability ID register is read-only and returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

5.11 Next Item Pointer Register (DDh)

The next item pointer register indicates the next item in the linked list of PCI power-management capabilities. The next-item pointer returns E4h in CompactPCI mode, indicating that the PCI206 bridge supports more than one extended capability, but in all other modes returns 00h, indicating that only one extended capability is provided.

Bit Number	7	6	5	4	3	2	1	0
Reset State	1	1	1	0	0	1	0	0

5.12 Power-Management Capabilities Register (DEh)

The power-management capabilities register contains information on the capabilities of the PCI2060 functions related to power management. The PCI2060 function supports D0, D1, D2, and D3 power states when MS1 is low. The PCI2060 bridge does not support any power states when MS1 is high. See Table 5−10 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	x	x	0	0	0	0	0	0	0	x	x

Table 5−10. Power-Management Capabilities Register

BIT	FIELD NAME	DESCRIPTION
15:11	PME_SUPPORT	$\overline{\text{PME}}$ support. This five-bit field is read-only and returns 00000b when read, indicating that the PCI2060 bridge does not support the $\overline{\text{PME}}$ terminal.
10	D2_SUPPORT	D2 support. This bit returns 1b when MS0 is 0b, indicating that the bridge function supports the D2 device power state. This bit returns 0b when MS0 is 1b, indicating that the bridge function does not support the D2 device power state.
9	D1_SUPPORT	D1 support. This bit returns 1b when MS0 is 0b, indicating that the bridge function supports the D1 device power state. This bit returns 0b when MS0 is 1b, indicating that the bridge function does not support the D1 device power state.
8:6	AUX_CURRENT	3.3 V_{AUX} auxiliary current requirements. This requirement is design-dependent.
5	DSI	Device specific initialization. This bit returns 0b when read, indicating that the PCI2060 bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	Reserved. Returns 0b when read.
3	PME_CLK	$\overline{\text{PME}}$ clock. This bit returns 0b indicating that the PCI2060 bridge does not support the $\overline{\text{PME}}$ terminal.
2:0	PM_VERSION	Version. This three-bit field returns the *PCI Bus Power Management Interface Specification* revision number. This three-bit field returns 001b when MS0 is 1b, indicating that the PCI2060 bridge supports *PCI Bus Power Management Interface Specification*, Revision 1.0. This three-bit field returns 010b when MS0 is 0b, indicating that the PCI2060 bridge supports *PCI Bus Power Management Interface Specification*, Revision 1.1.

5.13 Power-Management Control/Status Register (E0h)

This register determines and changes the current power state of the PCI2060 bridge. The contents of this register are not affected by the internally generated reset caused by the transition from the $D3_{hot}$ to D0 state in reverse mode. In forward mode, no internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 5−11 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−11. Power-Management Control/Status Register

BIT	FIELD NAME	DESCRIPTION
15	PME_STAT	$\overline{\text{PME}}$ status. This bit returns 0b when read since the PCI2060 bridge does not support $\overline{\text{PME}}$ signaling.
14:13	DATA_SCALE	Data scale. This 2-bit field returns 00b when read since the data register is not implemented.
12:9	DATA_SEL	Data select. This 4-bit field returns 0h when read since the data register is not implemented.
8	PME_EN	$\overline{\text{PME}}$ enable. This bit returns 0b when read since the PCI2060 bridge does not support $\overline{\text{PME}}$ signaling.
7:2	RSVD	Reserved. Returns 000000b when read.
1:0	PWR_STATE	Power state. This 2-bit field determines the current power state of the function and sets the function to a new power state. This field is encoded as follows: 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$

5.14 Power-Management Bridge-Support Extension Register (E2h)

The power-management bridge-support extension register indicates to the host software the state of the secondary bus when the PCI2060 bridge is placed in D3. See Table 5−12 for a complete description of the register contents.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5−12. Power-Management Bridge-Support Extension Register

BIT	FIELD NAME	DESCRIPTION
7	BPCCE	Bus power/clock control enable. When the BPCCE terminal is tied high, this bit reads 1b to indicate that the bus power/clock control mechanism is enabled, as described in BSTATE (bit 6). When the BPCCE terminal is tied low, this bit reads 0b to indicate that the bus power/clock control mechanism is disabled (secondary clocks are not disabled when this device is placed in $D3_{HOT}$).
6	BSTATE	B2_B3 support for $D3_{HOT}$. When the BPCCE bit (bit 7) reads 1b, this bit reads 1b to indicate that the secondary bus clock outputs are stopped and driven low when this device is placed in $D3_{HOT}$. This bit is not defined when the BPCCE bit reads 0b.
5:0	RSVD	Reserved

5.15 Power-Management Data Register (E3h)

The data register is an optional, 8-bit, read-only register that provides a mechanism for the function to report state-dependent operating data such as power consumption or heat dissipation. The PCI2060 bridge does not implement the power-management data register. This register returns 00h when read.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

5.16 Hot-Swap Capability ID Register (E4h)

The hot-swap capability ID register identifies the linked list item as the register for cPCI hot-swap capabilities. The register returns 06h when read, which is the unique ID assigned by the PICMG for PCI location of the capabilities pointer and the value. In Intel™-compatible mode, this register is read-only and defaults to 00h.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	1	0

5.17 Hot-Swap Next-Item Pointer Register (E5h)

The hot-swap next-item pointer register indicates the next item in the linked list of the PCI extended capabilities. This register returns 00h indicating no additional capabilities are supported.

Bit Number	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

5.18 Hot-Swap Control and Status Register (E6h)

The CompactPCI hot-swap control and status register provides the control and status information about the Compact PCI hot-swap resources. See Table 5−13 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−13. Hot-Swap Control and Status Register (E6h)

BIT	FIELD NAME	DESCRIPTION
7	INS	$\overline{\text{HS\_ENUM}}$ insertion status. When set, the $\overline{\text{HS\_ENUM}}$ output is driven by the PCI2060 device. This bit defaults to 0b, and is set after a PCI reset occurs, the preload of serial ROM is complete, the ejector handle is closed ($\overline{\text{HS\_SWITCH}}$ low), and the EXT bit is 0b. Thus, this bit is set following an insertion when the board implementing the PCI2060 bridge is ready for configuration. This bit cannot be set by software.
6	EXT	$\overline{\text{HS\_ENUM}}$ extraction status. When set, the $\overline{\text{HS\_ENUM}}$ output is driven by the PCI2060 device. This bit defaults to 0b, and is set when the ejector handle is opened ($\overline{\text{HS\_SWITCH}}$ high) and INS bit is 0b. Thus, this bit is set when the board implementing the PCI2060 bridge is about to be removed. This bit cannot be set by software.
5:4	RSVD	Reserved. Returns 00b when read.
3	LOO	LED on/off. This bit defaults to 0b, and controls the external LED indicator (HS_LED) under normal conditions. However, for a duration following a $\overline{\text{PCI\_RST}}$, the HSLED output is driven high by the PCI2060 bridge and this bit is ignored. 0 = LED off (HS_LED low) 1 = LED on (HS_LED high) Following $\overline{\text{PCI\_RST}}$, the HS_LED output is driven high by the PCI2060 bridge until both the secondary clock control register is loaded and the ejector handle is closed ($\overline{\text{HS\_SWITCH}}$ low). When these conditions are met, the HSLED is under software control via the LOO bit.
2	RSVD	Reserved. Returns 0b when read.
1	EIM	$\overline{\text{HS\_ENUM}}$ interrupt mask. This bit allows the $\overline{\text{HS\_ENUM}}$ output to be masked by software. The INS and EXT bits are set independently from the EIM bit. 0 = Enable $\overline{\text{HS\_ENUM}}$ output 1 = Mask $\overline{\text{HS\_ENUM}}$ output
0	RSVD	Reserved. Returns 0b when read.

5.19 TI Diagnostic Register (F0h)

This register controls the behavior of write combining and memory write-and-invalidate commands. This register also limits burst size for both upstream and downstream transactions to 32 doublewords. See Table 5−14 for a complete description of the register contents.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−14. TI Diagnostic Register

BIT	FIELD NAME	DESCRIPTION
15:5	RSVD	Reserved. Returns 000 0000 0000b when read.
4	DOWN_FLOW_CONTROL	Downstream flow control. Setting this bit to 1b causes the PCI2060 bridge to limit all burst transactions (memory read, memory read line, memory read multiple, memory write, and memory write-and-invalidate) that are targeting the secondary bus to 32 doublewords. 0 = Disable upstream flow control 1 = Enable upstream flow control
3	RSVD	Reserved. Returns 0b when read.
2	UP_FLOW_CONTROL	Upstream flow control. Setting this bit to 1b causes PCI2060 bridge to limit all burst transactions (memory read, memory read line, memory read multiple, memory write, and memory write-and-invalidate) that are targeting the primary bus to 32 doublewords. 0 = Disable upstream flow control 1 = Enable upstream flow control
1	MWI_MW_CONVERSION	MWI/MW conversion. This bit causes all memory write-and-invalidate transactions to be converted to memory write transactions. 0 = MWI transactions are only converted to MW transactions if there is not enough space in the FIFO for a cache line or data. 1 = All MWI transactions are converted to MW transactions.
0	PW_COMBINING_DIS	Disable posted write combining. 0 = Enable posted write combining 1 = Disable posted write combining

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Operating Temperature Ranges †

Supply voltage range:	V_{CC}	−0.5 V to 3.6 V
	P_V_{CCP}	−0.5 V to 6 V
	S_V_{CCP}	−0.5 V to 6 V
Input voltage range, V_I: CMOS‡		−0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: PCI§		−0.5 V to 6 V
Output voltage range, V_O: CMOS‡		−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O: PCI§		−0.5 V to 6 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2)		±20 mA
Storage temperature range, T_{stg}		−65°C to 150°C
Virtual junction temperature, T_J		150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ CMOS terminals are J6, J18, J19, K1, K2, K5, K6. K14, K17, K18, L1, L2, L5, L14, L15, L17, M1, M3, M6, N1, N2, N6, P1 for the GHK-packaged device.

§ All signal terminals other than CMOS terminals are PCI terminals.

NOTES: 1. Applies for external input and bidirectional buffers. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. The limit is specified for a dc condition.

2. Applies for external input and bidirectional buffers. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. The limit is specified for a dc condition.

6.2 Recommended Operating Conditions (see Note 3)

			OPERATION	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (core)	Commercial	3.3 V	3	3.3	3.6	V
P_V_{CCP}	PCI primary bus I/O clamping rail voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
S_V_{CCP}	PCI secondary bus I/O clamping rail voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_{IH}†	High-level input voltage	PCI	3.3 V	0.5 V_{CCP}		V_{CCP}	V
			5 V	2		V_{CCP}	
		CMOS		0.7 V_{CC}		V_{CC}	
		CLK¶		0.57V_{CCP}		V_{CCP}	
		P_RST_L		0.77V_{CCP}		V_{CCP}	
		TRST_L		0.9 V_{CC}		V_{CC}	
V_{IL}†	Low-level input voltage	PCI	3.3 V	0		0.3 V_{CCP}	V
			5 V	0		0.8	
		CMOS		0		0.2 V_{CC}	
		CLK¶		0		0.2 V_{CCP}	
V_I	Input voltage	PCI		0		V_{CCP}	V
		CMOS		0		V_{CCP}	
V_O‡	Output voltage	Output voltage		0		V_{CC}	V
t_t	Input transition time (t_r and t_f)	PCI		1		4	ns
		CMOS		0		6	
T_A	Operating ambient temperature range	PCI2060		0	25	70	°C
		PCI2060I		−40	25	85	
T_J§	Virtual junction temperature			0	25	115	°C

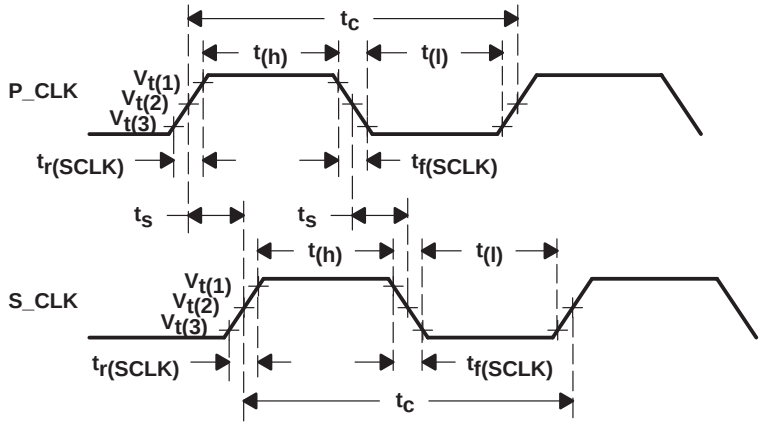
NOTES: 3. Unused terminals (input or I/O) must be held high or low to prevent them from floating.
† Applies to external input and bidirectional buffers without hysteresis
‡ Applies to external output buffers
§ These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.
¶ CLK includes P_CLK and S_CLK terminals.

6.3 Electrical Characteristics Over Recommended Operating Conditions

PARAMETER		TERMINALS	OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI	3.3 V	I_{OH} = −0.5 mA	0.9 V_{CC}		V
			5 V	I_{OH} = −2 mA	2.4		
		CMOS1†		I_{OH} = −4 mA	2.1		
		CMOS2‡		I_{OH} = −8 mA	2.1		
V_{OL}	Low-level output voltage	PCI	3.3 V	I_{OL} = 1.5 mA		0.1 V_{CC}	V
			5 V	I_{OH} = −2 mA		0.55	
		CMOS1†		I_{OH} = 4 mA		0.5	
		CMOS2‡		I_{OH} = 8 mA		0.5	
I_{IH}	High-level input current	Input terminals		$V_I = V_{CCP}$		10	µA
		I/O terminals§		$V_I = V_{CCP}$		10	
I_{IL}	Low-level input current	Input terminals		V_I = GND		−1	µA
		I/O terminals§		V_I = GND		−10	
		Pu terminals¶		V_I = GND		−60	
I_{OZ}	High-impedance output current	Output terminals		$V_O = V_{CCP}$ or GND		±10	µA

† CMOS1 includes terminals K1, K2, K5, K6 for the GHK-packaged device.
‡ CMOS2 includes terminals K17, L1, L2, L5, L14, M1, M3, M6, N1, N2, N6, P1 for the GHK-packaged device.
§ For I/O terminals, the input leakage current (I_{IL} and I_{IH}) includes the I_{OZ} leakage of the disabled output.
¶ Pu terminals include TDI, TMS, and TRST_L. These are pulled up with internal resistors.

6.4 66-MHz PCI Clock Signal AC Parameters

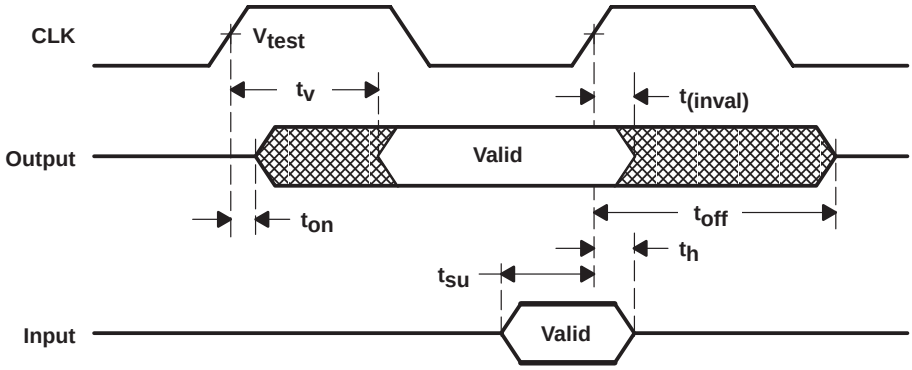


NOTE: $V_{t(1)}$ = 2.0 V for 5-V clocks; 0.5 V_{CC} for 3.3-V clocks
$V_{t(2)}$ = 1.5 V for 5-V clocks; 0.4 V_{CC} for 3.3-V clocks
$V_{t(3)}$ = 0.8 V for 5-V clocks; 0.3 V_{CC} for 3.3-V clocks

Figure 6−1. PCI Clock Signal AC Parameter Measurements

PARAMETER		MIN	MAX	UNIT
t_c	P_CLK, S_CLK cycle time	15	30	ns
$t_{(h)}$	P_CLK, S_CLK high time	6		ns
$t_{(l)}$	P_CLK, S_CLK low time	6		ns
$t_{(PSS)}$	P_CLK, S_CLK slew rate (0.2 V_{CC} to 0.6 V_{CC})	1.5	4	V/ns
$t_{d(SCLK)}$	Delay from P_CLK to S_CLK	0	7	ns
$t_{r(SCLK)}$	P_CLK rising to S_CLK rising	0	7	ns
$t_{f(SCLK)}$	P_CLK falling to S_CLK falling	0	7	ns
$t_{d(skew)}$	S_CLK0 duty cycle skew from P_CLK duty cycle		0.750	ns
t_{sk}	S_CLKx to SCLKy		0.500	ns

6.5 66-MHz PCI Signal Timing



NOTE: V_{test} = 1.5 V for 5-V signals; 0.4 V_{CC} for 3.3-V signals

Figure 6−2. PCI Signal Timing Measurement Conditions

PARAMETER		MIN	MAX	UNIT
$t_{v(bus)}$	CLK to signal valid delay—bused signals (see Notes 4, 5, and 6)	2	6	ns
$t_{v(ptp)}$	CLK to signal valid delay—point-to-point (see Notes 4, 5, and 6)	2	6	ns
t_{on}	Float to active delay (see Notes 4, 5, and 6)	2		ns
t_{off}	Active to float delay (see Notes 4, 5, and 6)		14	ns
$t_{su(bus)}$	Input setup time to CLK—bused signal (see Notes 4, 5, and 6)	3		ns
$t_{su(ptp)}$	Input setup time to CLK—point-to-point (see Notes 4, 5, and 6)	5		ns
t_h	Input signal hold time from CLK (see Notes 4 and 5)	0		ns

NOTES: 4. See Figure 6−2
5. All primary interface signals are synchronized to P_CLK and all secondary interface signals are synchronized to S_CLK.
6. Bused signals are as follows:
P_AD, P_C/BE, P_PAR, P_PERR, P_SERR, P_FRAME, P_IRDY, P_TRDY, P_LOCK, P_DEVSEL, P_STOP, P_IDSEL, S_AD, S_C/BE, S_PAR, S_PERR, S_SERR, S_FRAME, S_IRDY, S_TRDY, S_LOCK, S_DEVSEL, S_STOP

Point-to-point signals are as follows:
P_REQ, S_REQx, P_GNT, S_GNTx

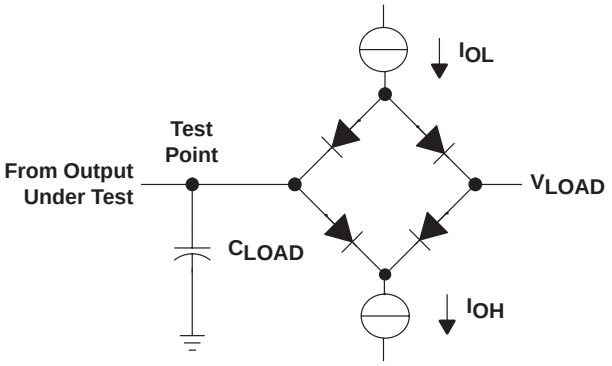
6.6 Parameter Measurement Information

LOAD CIRCUIT PARAMETERS

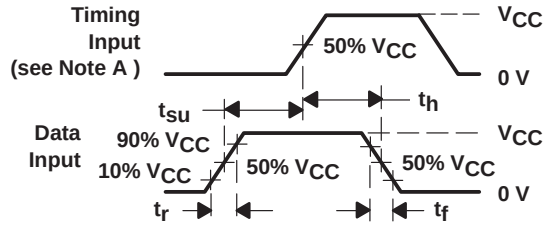
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	−8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	−8	1.5
	t_{PLZ}				
t_{pd}		50	8	−8	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

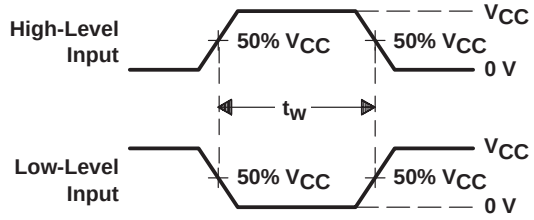
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where V_{OL} = 0.6 V, I_{OL} = 8 mA



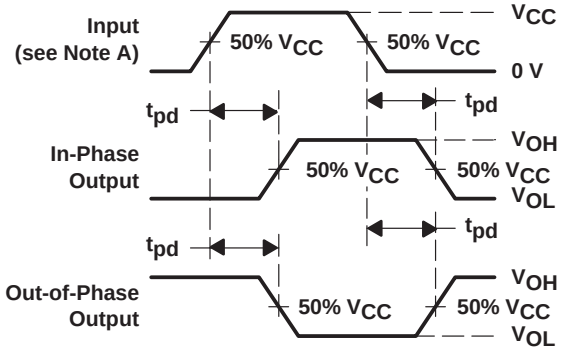
LOAD CIRCUIT



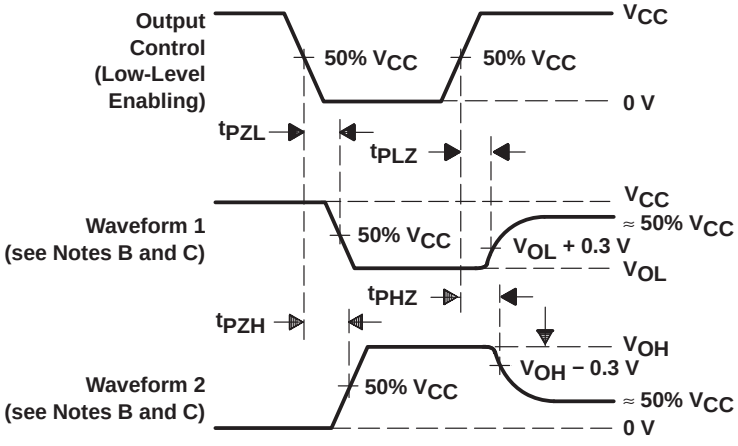
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 6−3. Load Circuit and Voltage Waveforms

6.7 PCI Bus Parameter Measurement Information

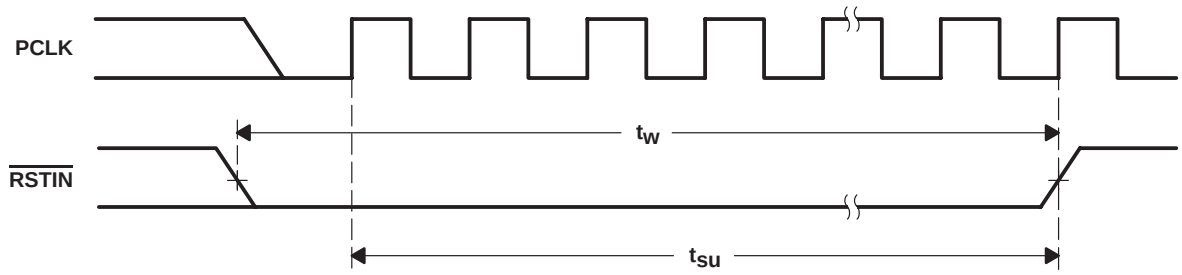
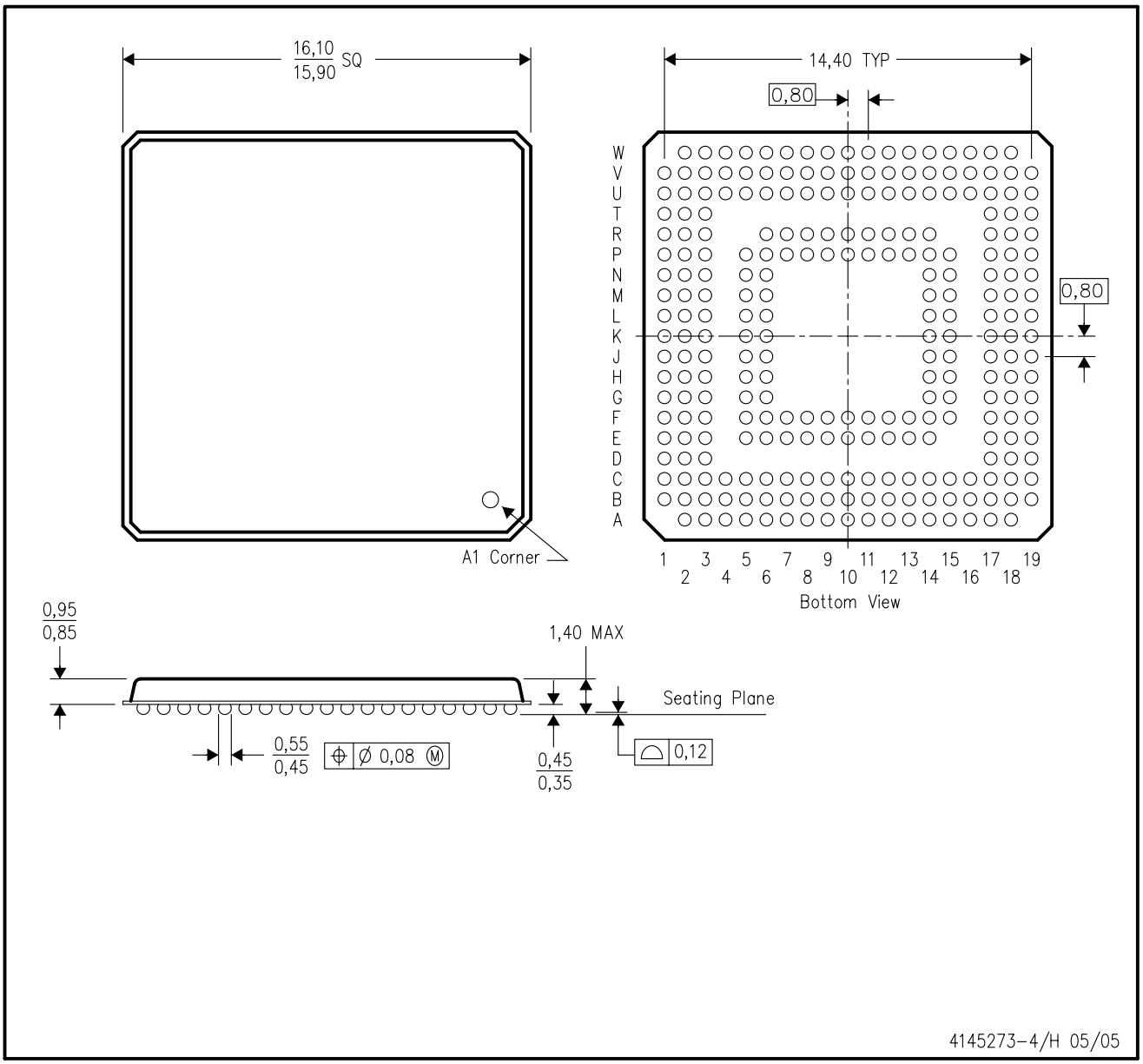


Figure 6−4. $\overline{\text{RSTIN}}$ Timing Waveforms

7 Mechanical Data

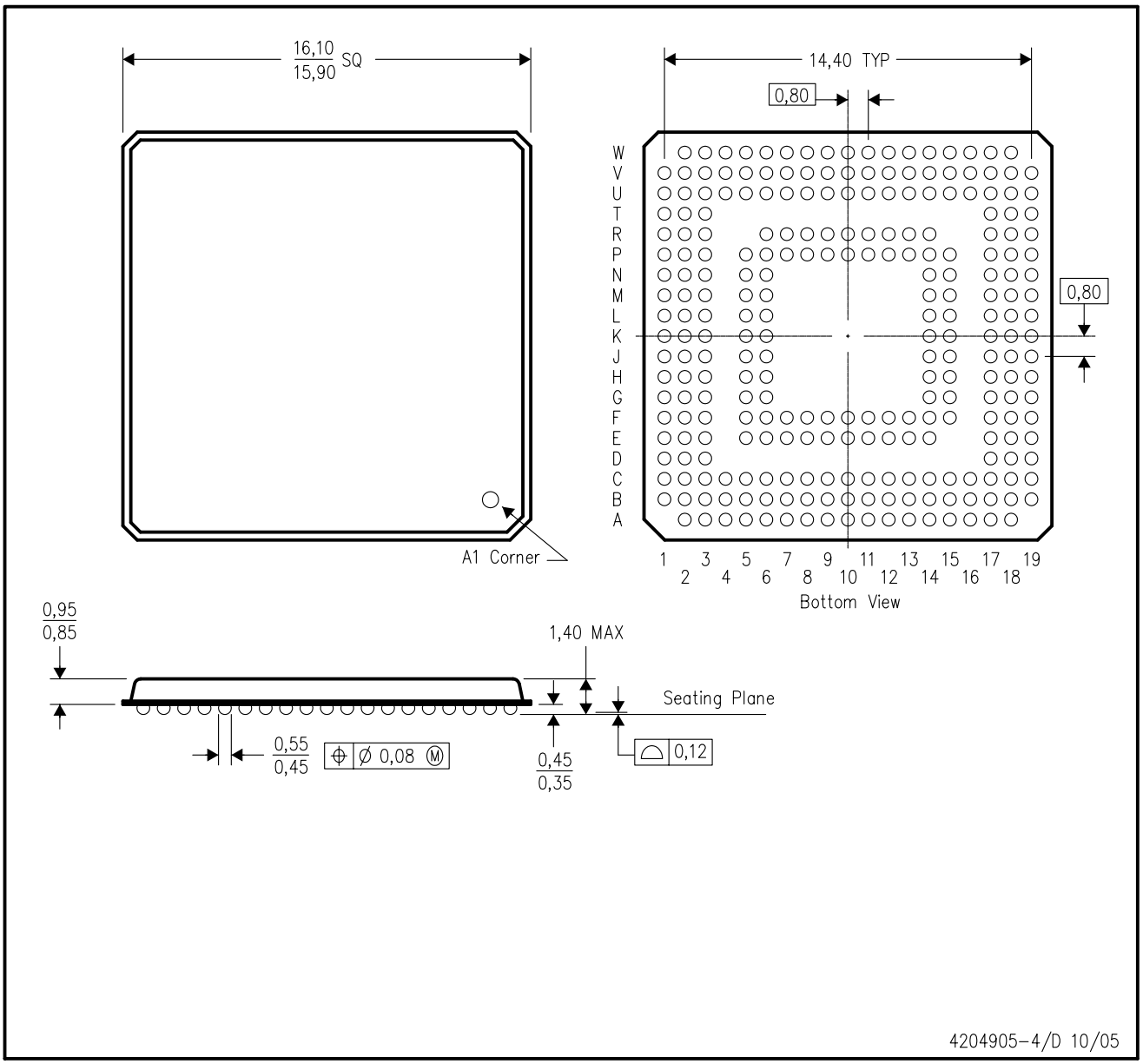
The PCI2060 device is available in the 257-terminal MicroStar BGA™ package (GHK). The following figure shows the mechanical dimensions for the GHK package.

GHK (S–PBGA–N257) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

ZHK (S–PBGA–N257) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.