National Semiconductor

February 2004

ADC78H90
8-Channel, 500 kSPS, 12-Bit A/D Converter

General Description

The ADC78H90 is a low-power, eight-channel CMOS 12-bit analog-to-digital converter with a conversion throughput of 500 kSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to eight input signals at inputs AIN1 through AIN8.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE™, and many common DSP serial interfaces.

The ADC78H90 may be operated with independent analog and digital supplies. The analog supply (AV_{DD}) can range from +2.7V to +5.25V, and the digital supply (DV_{DD}) can range from +2.7V to AV_{DD}. Normal power consumption using a +3V or +5V supply is 1.5 mW and 8.3 mW, respectively. The power-down feature reduces the power consumption to just 0.3 µW using a +3V supply, or 0.5 µW using a +5V supply.

The ADC78H90 is packaged in a 16-lead TSSOP package. Operation over the industrial temperature range of −40˚C to +85˚C is guaranteed.

Features

- Eight input channels
- Variable power management
- Independent analog and digital supplies
- SPI™/QSPI™/MICROWIRE™/DSP compatible
- Packaged in 16-lead TSSOP

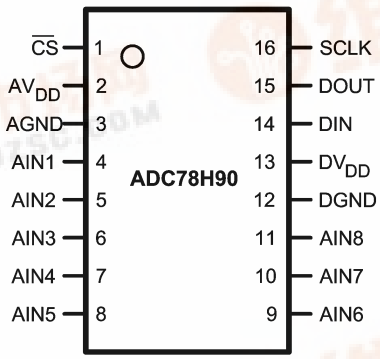
Key Specifications

- Conversion Rate 500 kSPS
- DNL ± 1 LSB (max)
- INL ± 1 LSB (max)
- Power Consumption
  - — 3V Supply 1.5 mW (typ)
  - — 5V Supply 8.3 mW (typ)

Applications

- Automotive Navigation
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

Connection Diagram



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Ordering Information

Order Code	Temperature Range	Description
ADC78H90CIMT	−40˚C to +85˚C	16-Lead TSSOP Package
ADC78H90CIMTX	−40˚C to +85˚C	16-Lead TSSOP Package, Tape & Reel
ADC78H90EVAL		Evaluation Board

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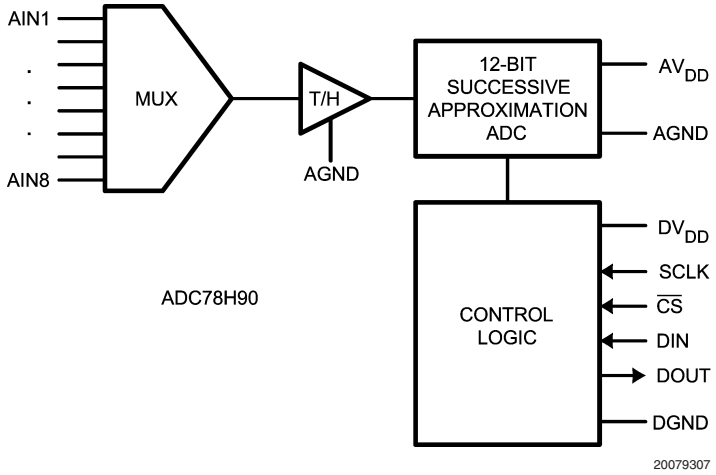
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
4 - 11	AIN1 to AIN8		Analog inputs. These signals can range from 0V to AV_{DD}.
DIGITAL I/O			
16	SCLK		Digital clock input. The range of frequencies for this input is 50 kHz to 8 MHz, with guaranteed performance at 8 MHz. This clock directly controls the conversion and readout processes.
15	DOUT		Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
14	DIN		Digital data input. The ADC78H90's Control Register is loaded through this pin on rising edges of the SCLK pin.
1	$\overline{CS}$		Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
POWER SUPPLY			
2	AV_{DD}		Positive analog supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 µF tantalum capacitor and a 0.1 µF ceramic monolithic capacitor located within 1 cm of the power pin.
13	DV_{DD}		Positive digital supply pin. This pin should be connected to a +2.7V to AV_{DD} supply, and bypassed to GND with a 0.1 µF ceramic monolithic capacitor located within 1 cm of the power pin.
3	AGND		The ground return for the analog supply and signals.
12	DGND		The ground return for the digital supply and signals.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Analog Supply Voltage AV_{DD}	−0.3V to 6.5V
Digital Supply Voltage DV_{DD}	−0.3V to AV_{DD} + 0.3V, max 6.5V
Voltage on Any Pin to GND	−0.3V to AV_{DD} +0.3V
Input Current at Any Pin (Note 3)	±10 mA
Package Input Current(Note 3)	±20 mA
Power Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature, Infrared, 10 seconds (Note 6)	260˚C
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40˚C ≤ T_A ≤ +85˚C
AV_{DD} Supply Voltage	+2.7V to +5.25V
DV_{DD} Supply Voltage	+2.7V to AV_{DD}
Digital Input Pins Voltage Range	-0.3V to AV_{DD}
Clock Frequency	50 kHz to 8 MHz
Analog Input Voltage	0V to AV_{DD}

Package Thermal Resistance

Package	θ_{JA}
16-lead TSSOP on 4-layer, 2 oz. PCB	96˚C / W

ADC78H90 Converter Electrical Characteristics (Note 8)

The following specifications apply for AV_{DD} = DV_{DD} = +2.7V to 5.25V, AGND = DGND = 0V, f_{SCLK} = 8 MHz, f_{SAMPLE} = 500 KSPS, unless otherwise noted. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25˚C.

Symbol	Parameter	Conditions	Typical	Limits (Note 7)	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12**	Bits
INL	Integral Non-Linearity	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±1**	LSB (max)
DNL	Differential Non-Linearity	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±1**	LSB (max)
V_{OFF}	Offset Error	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±2**	LSB (max)
OEM	Offset Error Match	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±2**	LSB (max)
GE	Gain Error	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±3**	LSB (max)
GEM	Gain Error Match	AV_{DD} = +5.0V, DV_{DD} = +3.0V		**±3**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70**	dB (min)
SNR	Signal-to-Noise Ratio	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70.8**	dB (min)
THD	Total Harmonic Distortion	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	−86	**−74**	dB (max)
SFDR	Spurious-Free Dynamic Range	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	88	**75.6**	dB (min)
ENOB	Effective Number of Bits	AV_{DD} = +5.0V, DV_{DD} = +3.0V,	11.8	**11.3**	Bits (min)
	Channel-to-Channel Crosstalk	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_{IN} = 40.2 kHz	-82		dB
IMD	Intermodulation Distortion, Second Order Terms	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_a = 40.161 kHz, f_b = 41.015 kHz	-93		dB
	Intermodulation Distortion, Third Order Terms	AV_{DD} = +5.0V, DV_{DD} = +3.0V, f_a = 40.161 kHz, f_b = 41.015 kHz	-90		dB
FPBW	-3 dB Full Power Bandwidth	AV_{DD} = +5V	11		MHz
		AV_{DD} = +3V	8		MHz

ADC78H90 Converter Electrical Characteristics (Note 8) (Continued)

The following specifications apply for AV_{DD} = DV_{DD} = +2.7V to 5.25V, AGND = DGND = 0V, f_{SCLK} = 8 MHz, f_{SAMPLE} = 500 KSPS, unless otherwise noted. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25˚C.

Symbol	Parameter	Conditions	Typical	Limits (Note 7)	Units
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to AV_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Input Capacitance	Track Mode	33		pF
		Hold Mode	3		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage	DV_{DD} = +4.75Vto +5.25V		**2.4**	V (min)
		DV_{DD} = +2.7V to +3.6V		**2.1**	V (min)
V_{IL}	Input Low Voltage	DV_{DD} = +2.7V to +5.25V		**0.8**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or DV_{DD}	±0.01	**±1**	µA (max)
C_{IND}	Digital Input Capacitance		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, DV_{DD} = +2.7V to +5.25V		**DV_{DD} –0.5**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OZH}, I_{OZL}	TRI-STATE® Leakage Current			**±1**	µA (max)
C_{OUT}	TRI-STATE® Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)					
AV_{DD}, DV_{DD}	Analog and Digital Supply Voltages	$AV_{DD} \geq DV_{DD}$		**2.7**	V (min)
				5.25	V (max)
$I_A + I_D$	Total Supply Current, Normal Mode (Operational, $\overline{CS}$ low)	AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz	1.65	**2.3**	mA (max)
		AV_{DD} = DV_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 500 kSPS, f_{IN} = 40 kHz	0.5	**2.3**	mA (max)
	Total Supply Current, Shutdown ($\overline{CS}$ high)	AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 0 kSPS	200		nA
		AV_{DD} = DV_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 0 kSPS	200		nA
P_D	Power Consumption, Normal Mode (Operational, $\overline{CS}$ low)	\AV_{DD} = DV_{DD} = +4.75V to +5.25V	8.3	**12**	mW (max)
		AV_{DD} = DV_{DD} = +2.7V to +3.6V	1.5	**8.3**	mW (max)
	Power Consumption, Shutdown ($\overline{CS}$ high)	AV_{DD} = DV_{DD} = +4.75V to +5.25V	0.5		µW
		AV_{DD} = DV_{DD} = +2.7V to +3.6V	0.3		µW
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Maximum Clock Frequency			**8**	MHz (min)
f_{SMIN}	Minimum Clock Frequency		50		kHz
f_S	Maximum Sample Rate			**500**	KSPS (min)
t_{CONV}	Conversion Time			**13**	SCLK cycles
DC	SCLK Duty Cycle		50	**40**	% (min)
				60	% (max)
t_{ACQ}	Track/Hold Acquisition Time	Full-Scale Step Input		**3**	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time		**16**	SCLK cycles
f_{RATE}	Throughput Rate			**500**	kSPS (min)
t_{AD}	Aperture Delay		4		ns

ADC78H90 Timing Specifications

The following specifications apply for AV_{DD} = DV_{DD} = +2.7V to 5.25V, AGND = DGND = 0V, f_{SCLK} = 8 MHz, f_{SAMPLE} = 500 KSPS, C_L = 50 pF, **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25˚C.

Symbol	Parameter	Conditions	Typical	Limits (Note 7)	Units
t_{1a}	Setup Time SCLK High to $\overline{CS}$ Falling Edge	(Note 9)		**10**	ns (min)
t_{1b}	Hold time SCLK Low to $\overline{CS}$ Falling Edge	(Note 9)		**10**	ns (min)
t_2	Delay from $\overline{CS}$ Until DOUT active			**30**	ns (max)
t_3	Data Access Time after SCLK Falling Edge			**30**	ns (max)
t_4	Data Setup Time Prior to SCLK Rising Edge			**10**	ns (min)
t_5	Data Valid SCLK Hold Time			**10**	ns (min)
t_6	SCLK High Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_7	SCLK Low Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_8	$\overline{CS}$ Rising Edge to DOUT High-Impedance			**20**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 16-pin TSSOP, θ_{JA} is 96˚C/W, so P_DMAX = 1,200 mW at 25˚C and 625 mW at the maximum operating ambient temperature of 85˚C. Note that the power consumption of this device under normal operation is a maximum of 12 mW. The values for maximum power dissipation listed above will be reached only when the ADC78H90 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms

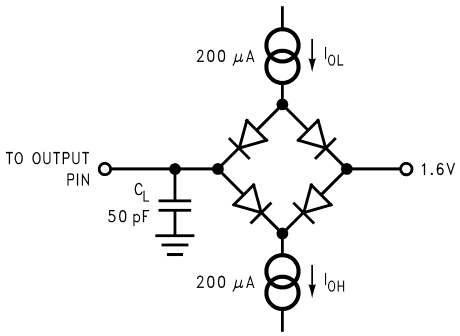
Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: Tested limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

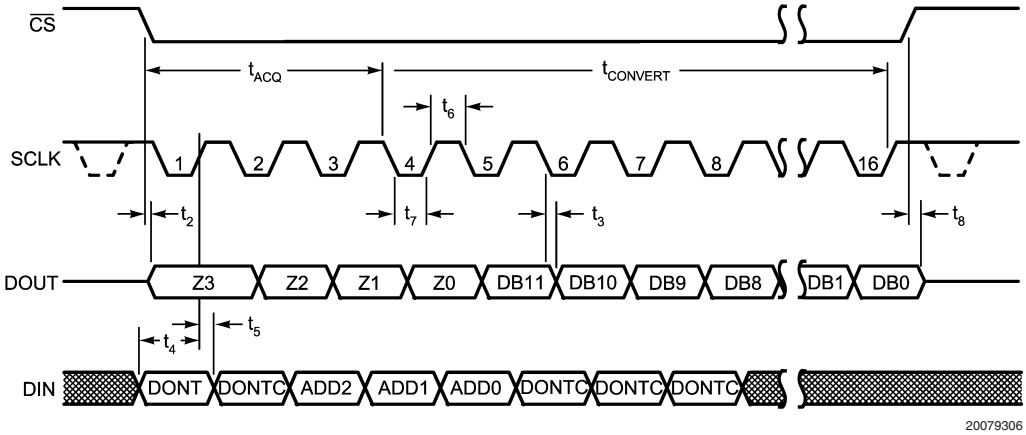
Note 8: Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Clock may be in any state (high or low) when $\overline{CS}$ is asserted, with the restrictions on setup and hold time given by t_{1a} and t_{1b}.

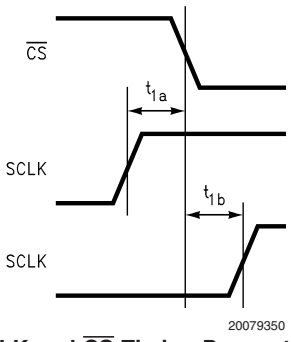
Timing Diagrams



Timing Test Circuit



ADC78H90 Serial Timing Diagram



SCLK and $\overline{CS}$ Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage. This is 4 clock cycles for the ADC78H90.

APERTURE DELAY is the time between the fourth falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word. This is 13 clock cycles for the ADC78H90.

CROSSTALK is the coupling of energy from one channel into the other channel, or the amount of signal energy from one analog input that appears at the measured analog input.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC78H90 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_6^2}{f_1^2}}$$

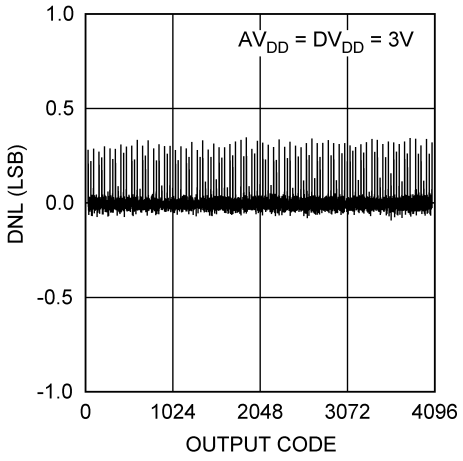
where f_1 is the RMS power of the input frequency at the output and f_2 through f_6 are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion time. In the case of the ADC78H90, this is 16 SCLK periods.

Typical Performance Characteristics

T_A = +25˚C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

DNL



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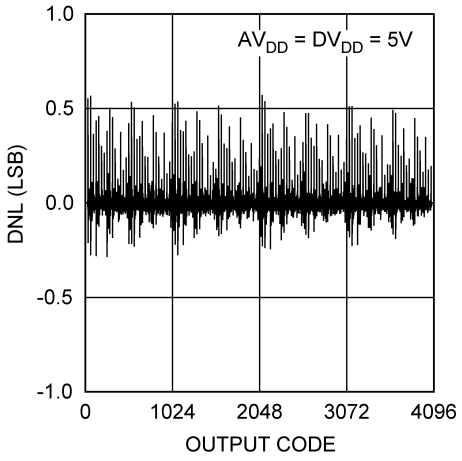
DNL



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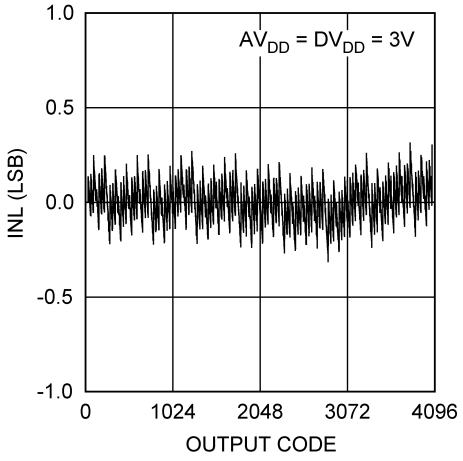
INL



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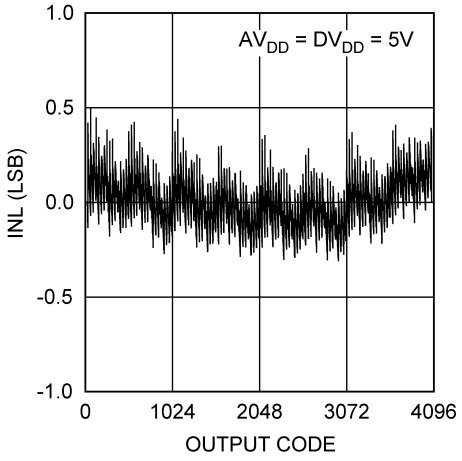
INL



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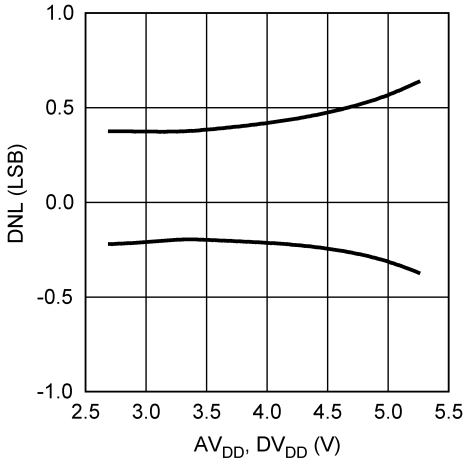
DNL vs. Supply



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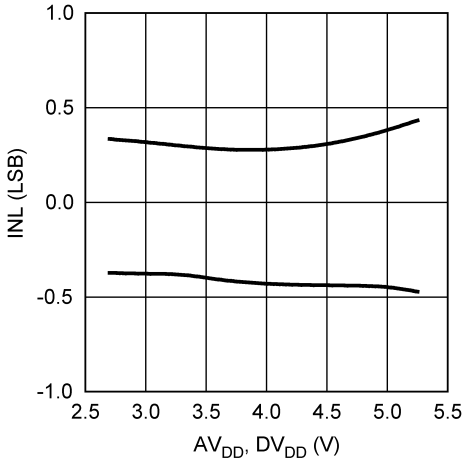
INL vs. Supply



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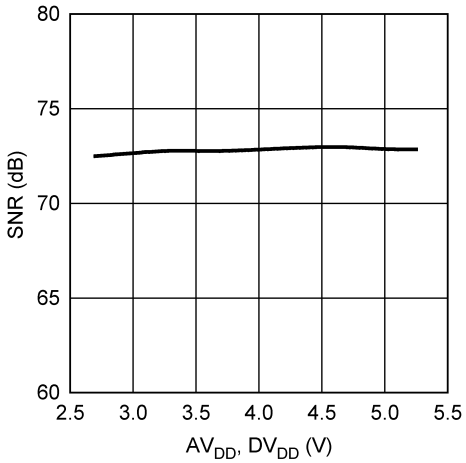
Typical Performance Characteristics T_A = +25˚C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated. (Continued)

SNR vs. Supply



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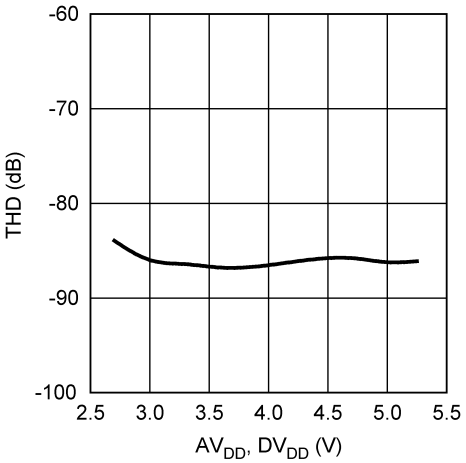
THD vs. Supply



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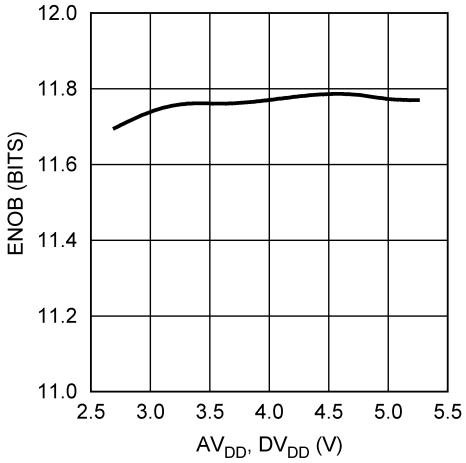
ENOB vs. Supply



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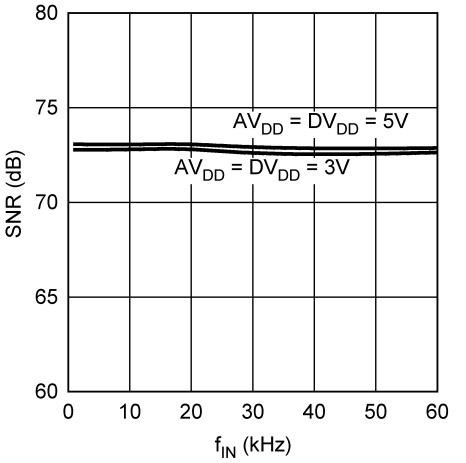
SNR vs. Input Frequency



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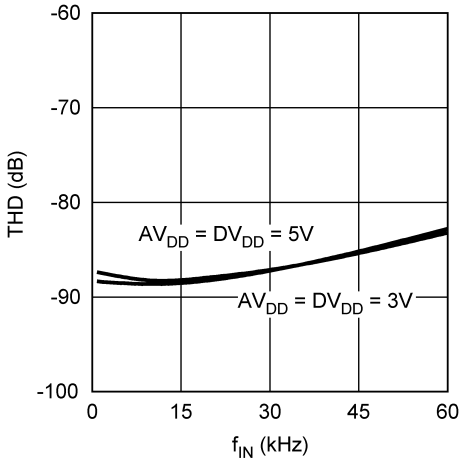
THD vs. Input Frequency



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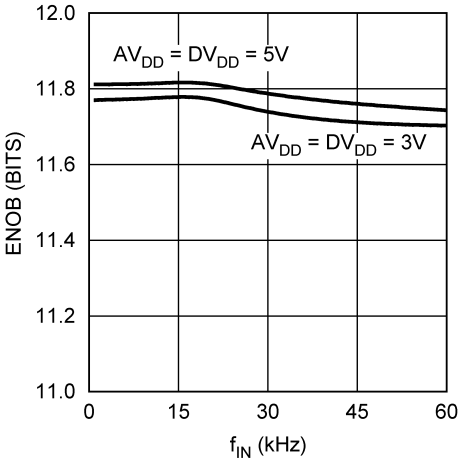
ENOB vs. Input Frequency



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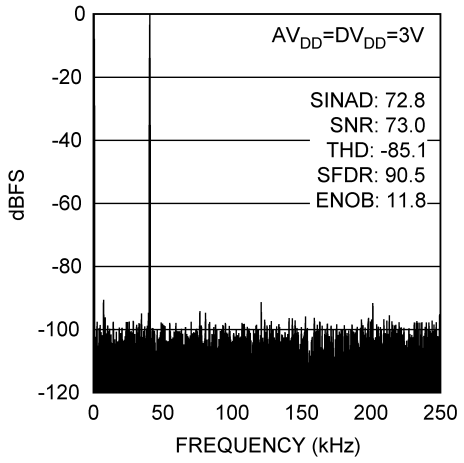
Typical Performance Characteristics T_A = +25˚C, f_{SAMPLE} = 500 kSPS, f_{SCLK} = 8 MHz, f_{IN} = 40.2 kHz unless otherwise stated. (Continued)

Spectral Response



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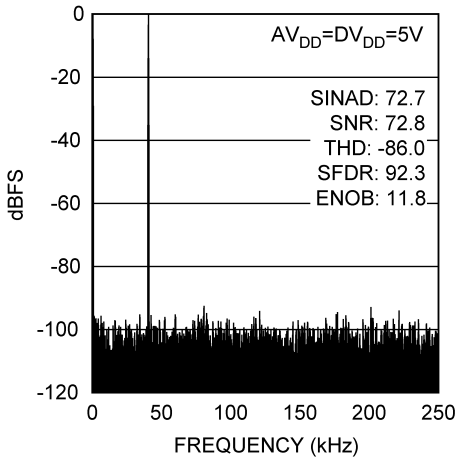
Spectral Response



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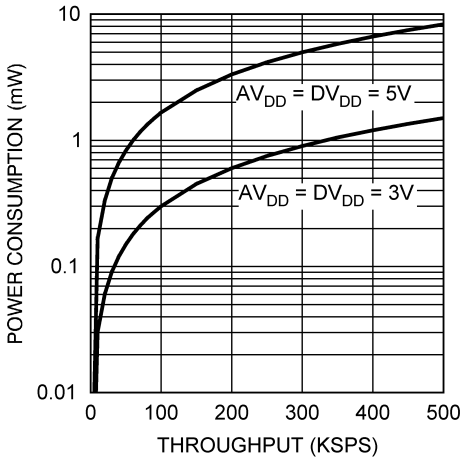
Power Consumption vs. Throughput



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Applications Information

1.0 ADC78H90 OPERATION

The ADC78H90 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADC78H90 in both track and hold operation are shown in *Figures 1, 2*, respectively. In *Figure 1*, the ADC78H90 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC78H90 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 2 shows the ADC78H90 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC78H90 is in this state for the last thirteen SCLK cycles after $\overline{CS}$ is brought low.

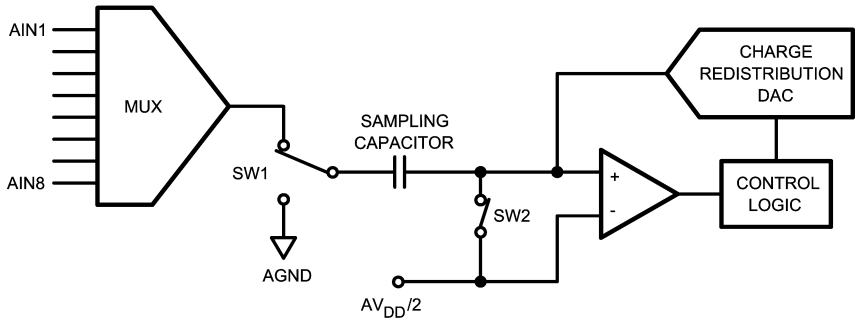


FIGURE 1. ADC78H90 in Track Mode

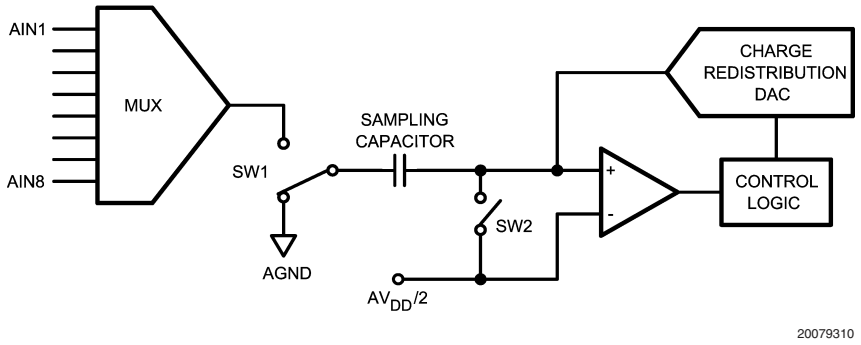


FIGURE 2. ADC78H90 in Hold Mode

The time when $\overline{CS}$ is low is considered a serial frame. Each of these frames should contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

2.0 USING THE ADC78H90

A ADC78H90 timing diagram is shown in *Figure 3*. A serial interface timing diagram for the ADC78H90 is shown in the Timing Diagrams section. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC78H90's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

Applications Information (Continued)

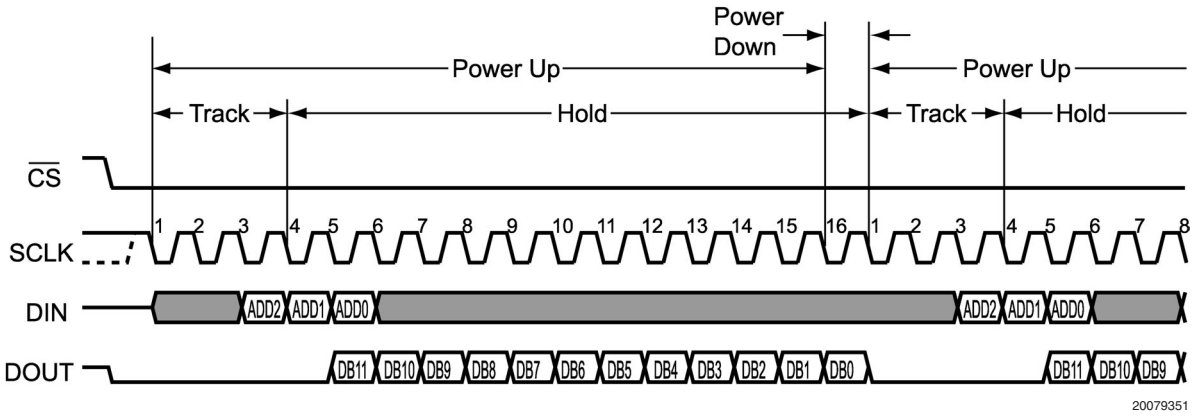


FIGURE 3. ADC78H90 Timing Diagram

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Additionally, the device goes into a power down state when $\overline{CS}$ is high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first. That is, for rising edges 1 through 3 after the fall of $\overline{CS}$, the ADC is in the track mode and for rising edges 4 through 16 a conversion is performed and the data is clocked out. If there are more than one conversion in a frame, the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode on the N*16+4th rising edge of SCLK, where "N" must be an integer.

When $\overline{CS}$ is brought high, SCLK is internally gated off. If SCLK is stopped in the low state while $\overline{CS}$ is high, the subsequent fall of $\overline{CS}$ will generate a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode on the first falling edge of SCLK after the falling edge of $\overline{CS}$.

During each conversion, data is clocked into the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. For each conversion, it is necessary to clock in the data indicating the input that is selected for the conversion after the current one. See *Tables 1, 2, 3*

The first conversion after power up is meaningless information and should be ignored.

If $\overline{CS}$ and SCLK go low simultaneously, it is the following rising edge of SCLK that is considered the first rising edge for clocking data into DIN.

TABLE 1. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

TABLE 2. Control Register Bit Descriptions

Bit #:	Symbol:	Description
7, 6, 2, 1, 0	DONTC	Don't care. The value of these bit do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted on the next falling edge of $\overline{CS}$. The mapping between codes and channels is shown in *Table 3*.
4	ADD1	
3	ADD0	

Applications Information (Continued)

TABLE 3. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
0	0	0	AIN1 (Default)
0	0	1	AIN2
0	1	0	AIN3
0	1	1	AIN4
1	0	0	AIN5
1	0	1	AIN6
1	1	0	AIN7
1	1	1	AIN8

3.0 ADC78H90 TRANSFER FUNCTION

The output format of the ADC89H90 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC78H90 is AV_{DD} / 4096. The ideal transfer characteristic is shown in *Figure 4*. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of AV_{DD} / 8192. Other code transitions occur at steps of one LSB.

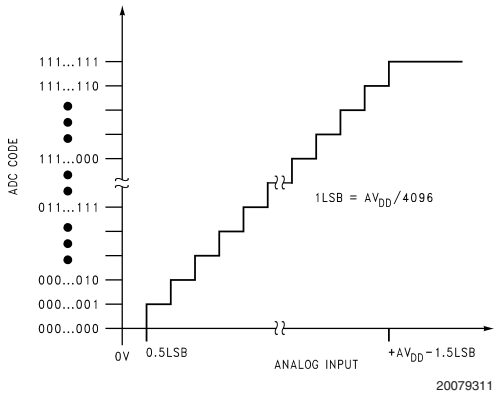


FIGURE 4. Ideal Transfer Characteristic

4.0 TYPICAL APPLICATION CIRCUIT

A typical application of the ADC78H90 is shown in *Figure 5*. The split analog and digital supplies are both provided in this example by the National LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The analog supply is bypassed with a capacitor network located close to the ADC78H90. The digital supply is separated from the analog supply by an isolation resistor and conditioned with additional bypass capacitors. The ADC78H90 uses the analog supply (AV_{DD}) as its reference voltage, so it is very important that AV_{DD} be kept as clean as possible. Because of the ADC78H90's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is also shown connected to a microprocessor or DSP.

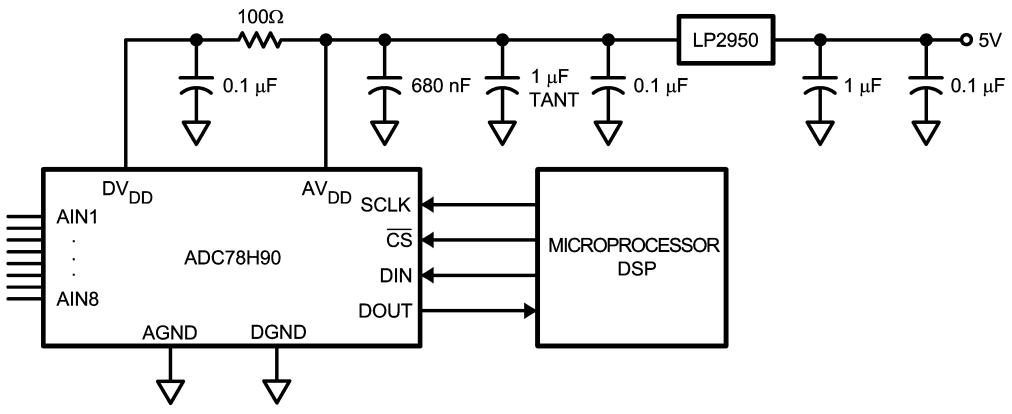


FIGURE 5. Typical Application Circuit

Applications Information (Continued)

5.0 ANALOG INPUTS

An equivalent circuit for one of the ADC78H90's input channels is shown in *Figure 6*. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input go beyond (AV_{DD} + 300 mV) or (GND - 300 mV), as these ESD diodes will begin conducting, which could result in erratic operation.

The capacitor C1 in *Figure 6* has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch, and is typically 500 ohms. Capacitor C2 is the ADC78H90 sampling capacitor, and is typically 30 pF. The ADC78H90 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC78H90 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

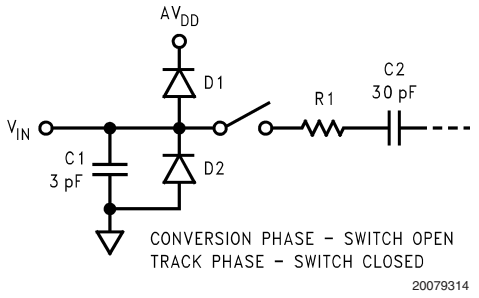


FIGURE 6. Equivalent Input Circuit

6.0 DIGITAL INPUTS AND OUTPUTS

The ADC78H90's digital inputs (SCLK, $\overline{CS}$, and DIN) are limited by and cannot exceed the analog supply voltage AV_{DD}. The digital input pins are not prone to latch-up; SCLK, $\overline{CS}$, and DIN may be asserted before DV_{DD} without any risk.

7.0 POWER SUPPLY CONSIDERATIONS

The ADC78H90 has two supplies, although they could both have the same potential. There are two major power supply concerns with this product. They are relative power supply levels, including power on sequencing, and the effect of digital supply noise on the analog supply.

7.1 Power Management

The ADC78H90 is a dual-supply device. These two supplies share ESD resources, and thus care must be exercised to ensure that the power supplies are applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (DV_{DD}) cannot exceed the analog supply (AV_{DD}) by more than 300 mV. The ADC78H90's analog power supply must, therefore, be applied before (or concurrently with) the digital power supply.

The ADC78H90 is fully powered-up whenever $\overline{CS}$ is low, and fully powered-down whenever $\overline{CS}$ is high, with one exception: the ADC78H90 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see *Figure 3*).

The user does not need to worry about any kind of power-up delays or dummy conversions with the ADC78H90. The part is able to acquire input to full resolution in the first conversion immediately following power-up.

The ADC78H90 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC78H90 will perform conversions continuously as long as $\overline{CS}$ is held low.

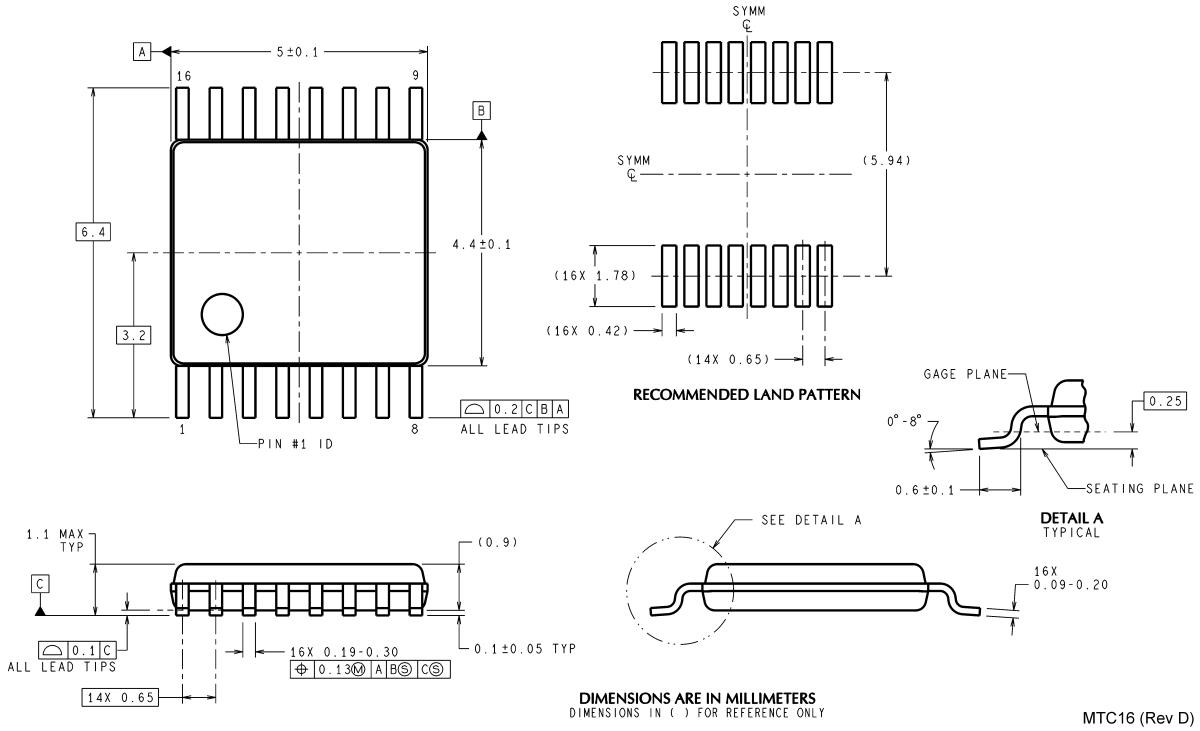
The user may trade off throughput for power consumption by simply performing fewer conversions per unit time. The Power Consumption vs. Sample Rate curve in the Typical Performance Curves section shows the typical power consumption of the ADC78H90 versus throughput. To calculate the power consumption, simply multiply the fraction of time spent in the normal mode by the normal mode power consumption (8.3 mW with $AV_{DD} = DV_{DD}$ = +3.6V, for example), and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power dissipation (0.3 mW with $AV_{DD} = DV_{DD}$ = +3.6V).

7.2 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, DV_{DD}. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could cause degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than noise on the digital supply. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

The first solution is to decouple the analog and digital supplies from each other, or use separate supplies for them, to keep digital noise out of the analog supply. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 25 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead TSSOP
Order Number ADC78H90CIMT, ADC78H90CIMTX
NS Package Number MTC16

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