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June 1999

National Semiconductor

CLC5612
Dual, High Output, Programmable Gain Buffer

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Dual, High Output, Programmable Gain Buffer

General Description

The CLC5612 is a dual, low-cost, high-speed (90MHz) buffer which features user-programmable gains of +2, +1, and -1V/V. The CLC5612 also has a new output stage that delivers high output drive current (130mA), but consumes minimal quiescent supply current (1.5mA/ch) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3dB frequency.

The CLC5612 offers 0.1dB gain flatness to 18MHz and differential gain and phase errors of 0.15% and 0.02°. These features are ideal for professional and consumer video applications.

The CLC5612 offers superior dynamic performance with a 90MHz small-signal bandwidth, 290V/µs slew rate and 6.2ns rise/fall times ($2V_{step}$). The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5612 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC5612 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5612 will drive a 100Ω load with only -74/-86dBc second/third harmonic distortion (A_V = +2, V_{out} = $2V_{pp}$, f = 1MHz). With a 25Ω load, and the same conditions, it produces only -70/-67dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution A/D converters, the CLC5612 provides excellent -87/-93dBc second/third harmonic distortion (A_V = +2, V_{out} = $2V_{pp}$, f = 1MHz, R_L = 1kΩ) and fast settling time.

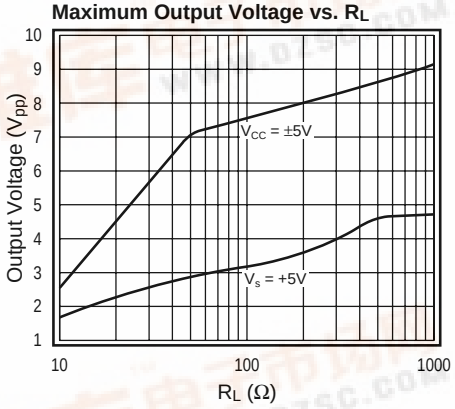
Features

- 130mA output current
- 0.15%, 0.02° differential gain, phase
- 1.5mA/ch supply current
- 90MHz bandwidth (A_V = +2)
- -87/-93dBc HD2/HD3 (1MHz)
- 17ns settling to 0.05%
- 290V/µs slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V to ±5V supplies

Applications

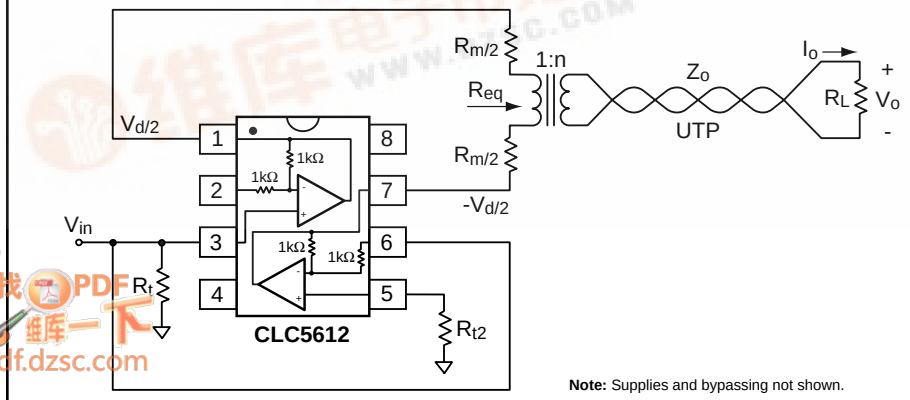
- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/coil driver
- High capacitive load driver
- Portable/battery-powered applications
- A/D driver

Maximum Output Voltage vs. R_L



Typical Application

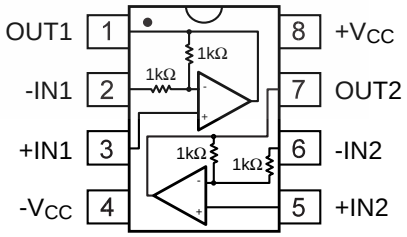
Differential Line Driver with Load Impedance Conversion



Note: Supplies and bypassing not shown.

Pinout

DIP & SOIC



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+5V Electrical Characteristics (A_v = +2, R_L = 100Ω, V_s = +5V[1], V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC5612IN/IM	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_o = 0.5V_{pp}	75	50	50	50	MHz	
	V_o = 2.0V_{pp}	62	57	54	52	MHz	
-0.1dB bandwidth	V_o = 0.5V_{pp}	18	13	11	11	MHz	
gain peaking	<200MHz, V_o = 0.5V_{pp}	0	0.5	0.9	1.2	dB	
gain rolloff	<30MHz, V_o = 0.5V_{pp}	0.2	0.9	1.0	1.0	dB	
linear phase deviation	<30MHz, V_o = 0.5V_{pp}	0.1	0.4	0.5	0.5	deg	
differential gain	NTSC, R_L = 150Ω to -1V	0.09	–	–	–	%	
differential phase	NTSC, R_L = 150Ω to -1V	0.14	–	–	–	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5.5	9.0	9.7	10.5	ns	
settling time to 0.05%	1V step	20	28	45	70	ns	
overshoot	2V step	3	6.5	14	14	%	
slew rate	2V step	185	150	130	120	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-74	-70	-67	-67	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-79	-77	-72	-72	dBc	
	2V_{pp}, 5MHz	-65	-58	-58	-58	dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-86	-82	-79	-79	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-81	-79	-76	-76	dBc	
	2V_{pp}, 5MHz	-60	-55	-53	-53	dBc	
equivalent input noise							
voltage (e_{ni})	>1MHz	3.4	4.4	4.9	4.9	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	6.3	8.2	9.0	9.0	pA/√Hz	
inverting current (i_{bi})	>1MHz	8.7	11.3	12.4	12.4	pA/√Hz	
crosstalk (input referred)	10MHz, 1V_{pp}	-80	–	–	–	dB	
STATIC DC PERFORMANCE							
input offset voltage		8	30	35	35	mV	A
average drift		80	–	–	–	µV/°C	
input bias current (non-inverting)		3	14	18	18	µA	A
average drift		25	–	–	–	nA/°C	
gain accuracy		±0.3	±1.5	±2.0	±2.0	%	A
internal resistors (R_f, R_g)		1000	±20%	±26%	±30%	Ω	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	47	45	43	43	dB	
supply current (per amplifier)	R_L= ∞	1.5	1.7	1.8	1.8	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.41	0.29	0.26	0.26	MΩ	
input capacitance (non-inverting)		2.2	3.3	3.3	3.3	pF	
input voltage range, High		4.2	4.1	4.0	4.0	V	
input voltage range, Low		0.8	0.9	1.0	1.0	V	
output voltage range, High	R_L = 100Ω	4.0	3.9	3.8	3.8	V	
output voltage range, Low	R_L = 100Ω	1.0	1.1	1.2	1.2	V	
output voltage range, High	R_L = ∞	4.1	4.0	4.0	3.9	V	
output voltage range, Low	R_L = ∞	0.9	1.0	1.0	1.1	V	
output current		100	80	65	40	mA	
output resistance, closed loop	DC	400	600	600	600	mΩ	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

A) J-level: spec is 100% tested at +25°C.
B) The short circuit current can exceed the maximum safe output current.
1) V_s = V_{CC} - V_{EE}

Absolute Maximum Ratings

supply voltage (V_{CC} - V_{EE})	+14V
output current (see note C)	140mA
common-mode input voltage	V_{EE} to V_{CC}
maximum junction temperature	+150°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Reliability Information

Transistor Count	98
MTBF (based on limited test data)	285Mhr

±5V Electrical Characteristics (A_v = +2, R_L = 100Ω, V_{CC} = ±5V, unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC5612IN/IM	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_o = 1.0V_{pp}	90	75	65	65	MHz	
	V_o = 4.0V_{pp}	49	43	40	38	MHz	
-0.1dB bandwidth	V_o = 1.0V_{pp}	17	12	10	10	MHz	
gain peaking	<200MHz, V_o = 1.0V_{pp}	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, V_o = 1.0V_{pp}	0.2	0.5	0.7	0.7	dB	
linear phase deviation	<30MHz, V_o = 1.0V_{pp}	0.2	0.4	0.5	0.5	deg	
differential gain	NTSC, R_L=150Ω	0.15	0.4	–	–	%	
differential phase	NTSC, R_L=150Ω	0.02	0.06	–	–	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	6.2	6.9	7.3	7.7	ns	
settling time to 0.05%	2V step	17	19	35	55	ns	
overshoot	2V step	10	16	18	18	%	
slew rate	2V step	290	250	220	200	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-74	-70	-67	-67	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-87	-80	-77	-77	dBc	
	2V_{pp}, 5MHz	-67	-61	-59	-59	dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-86	-82	-79	-79	dBc	
	2V_{pp}, 1MHz; R_L = 1kΩ	-93	-88	-85	-85	dBc	
	2V_{pp}, 5MHz	-63	-59	-56	-56	dBc	
equivalent input noise							
voltage (e_{ni})	>1MHz	3.4	4.4	4.9	4.9	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	6.3	8.2	9.0	9.0	pA/√Hz	
inverting current (i_{bi})	>1MHz	8.7	11.3	12.4	12.4	pA/√Hz	
crosstalk (input referred)	10MHz, 1V_{pp}	-80	–	–	–	dB	
STATIC DC PERFORMANCE							
output offset voltage		3	30	35	35	mV	
average drift		80	–	–	–	µV/°C	
input bias current (non-inverting)		5	12	16	17	µA	
average drift		40	–	–	–	nA/°C	
gain accuracy		±0.3	±1.5	±2.0	±2.0	%	
internal resistors (R_f, R_g)		1000	±20%	±26%	±30%	Ω	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	48	46	44	44	dB	
supply current (per amplifier)	R_L= ∞	1.6	1.9	2.0	2.0	mA	
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.52	0.38	0.34	0.34	MΩ	
input capacitance (non-inverting)		1.9	2.85	2.85	2.85	pF	
common-mode input range		±4.2	±4.1	±4.1	±4.0	V	
output voltage range	R_L = 100Ω	±3.8	±3.6	±3.6	±3.5	V	
output voltage range	R_L = ∞	±4.0	±3.8	±3.8	±3.7	V	
output current		130	100	80	50	mA	B
output resistance, closed loop	DC	400	600	600	600	mΩ	

Notes

B) The short circuit current can exceed the maximum safe output current.

Package Thermal Resistance

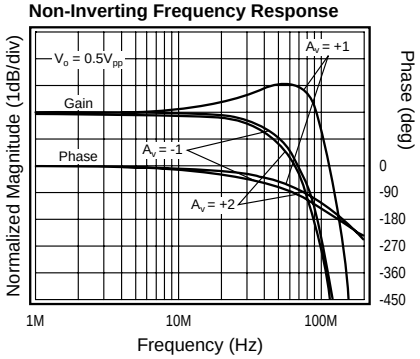
Package	θ_{JC}	θ_{JA}
Plastic (IN)	65°C/W	130°C/W
Surface Mount (IM)	50°C/W	145°C/W

Ordering Information

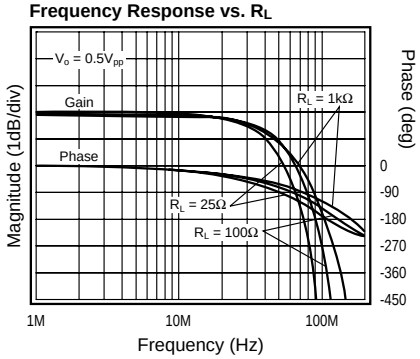
Model	Temperature Range	Description
CLC5612IN	-40°C to +85°C	8-pin PDIP
CLC5612IM	-40°C to +85°C	8-pin SOIC
CLC5612IMX	-40°C to +85°C	8-pin SOIC tape and reel

+5V Typical Performance (A_V = +2, R_L = 100Ω, V_S = +5V[1], V_{CM} = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified)

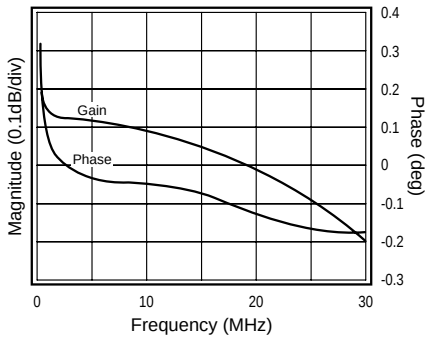
Non-Inverting Frequency Response



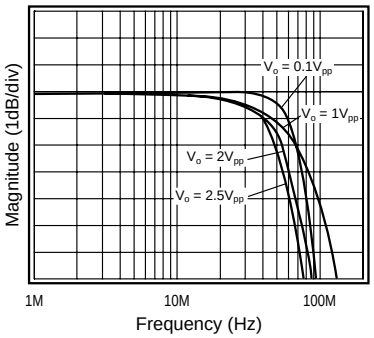
Frequency Response vs. R_L



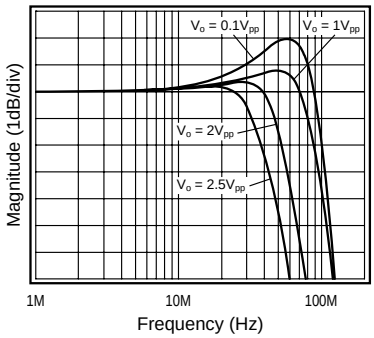
Gain Flatness & Linear Phase



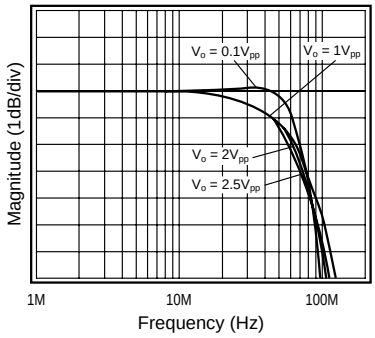
Frequency Response vs. V_o (A_V = 2)



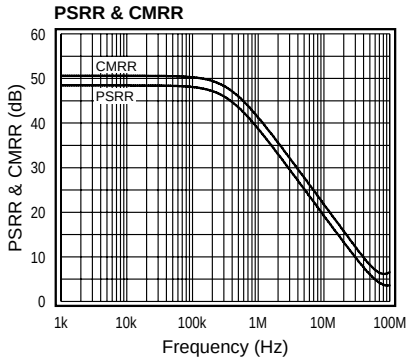
Frequency Response vs. V_o (A_V = 1)



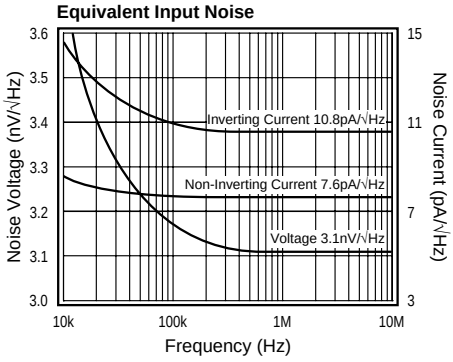
Frequency Response vs. V_o (A_V = -1)



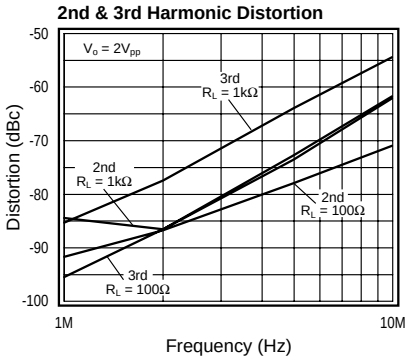
PSRR & CMRR



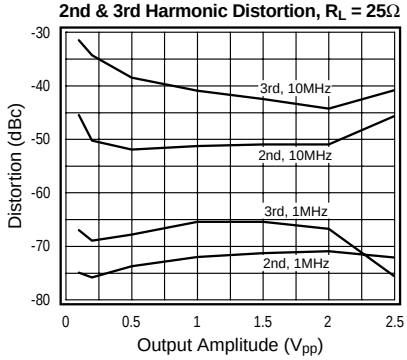
Equivalent Input Noise



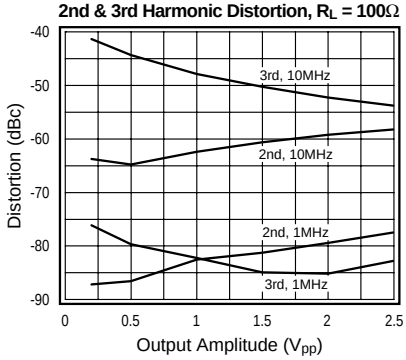
2nd & 3rd Harmonic Distortion



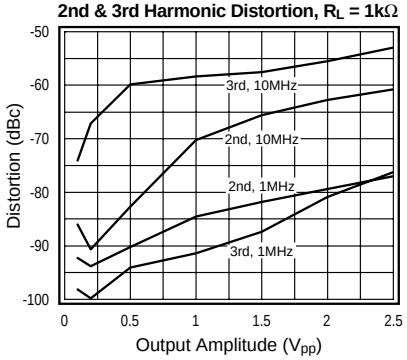
2nd & 3rd Harmonic Distortion, R_L = 25Ω



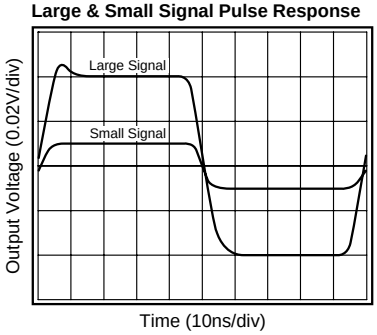
2nd & 3rd Harmonic Distortion, R_L = 100Ω



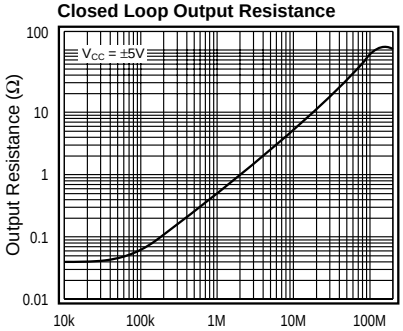
2nd & 3rd Harmonic Distortion, R_L = 1kΩ



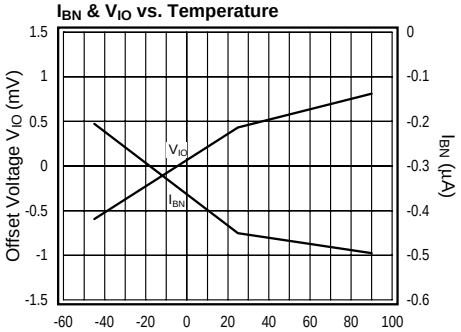
Large & Small Signal Pulse Response



Closed Loop Output Resistance

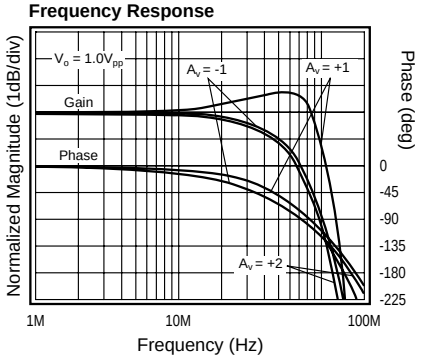


I_{BN} & V_{IO} vs. Temperature

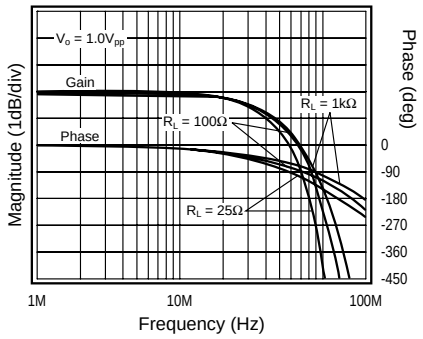


±5V Typical Performance (A_v = +2, R_L = 100Ω, V_{CC} = ± 5V, unless specified)

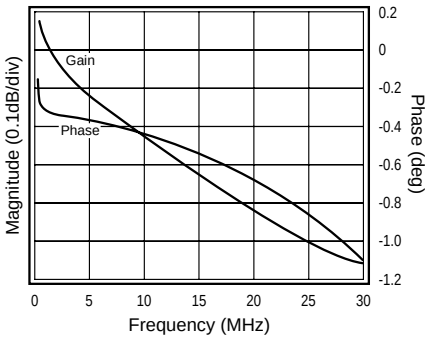
Frequency Response



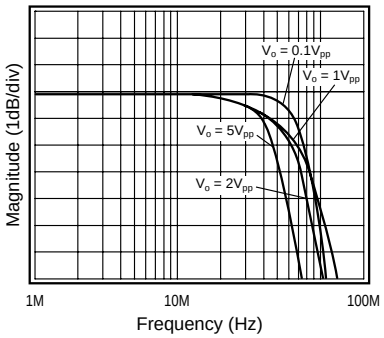
Frequency Response vs. R_L



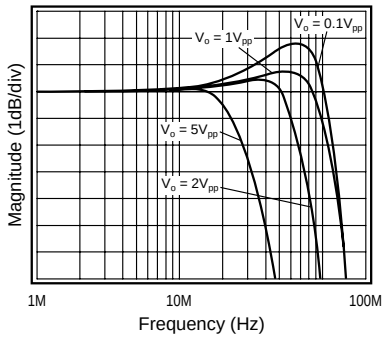
Gain Flatness & Linear Phase



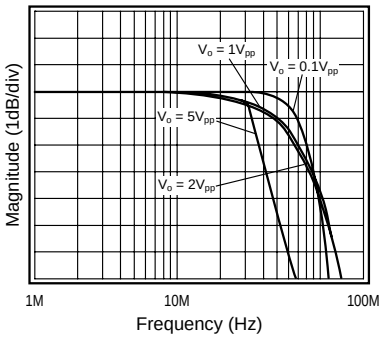
Frequency Response vs. V_o (A_v = 2)



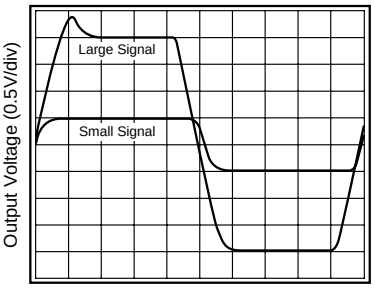
Frequency Response vs. V_o (A_v = 1)



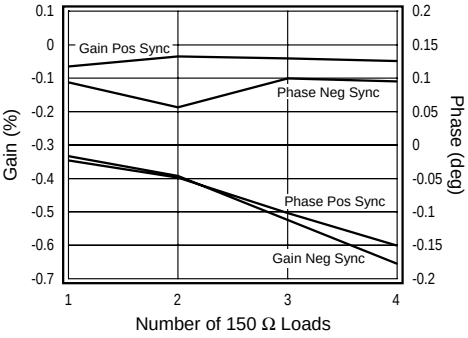
Frequency Response vs. V_o (A_v = -1)



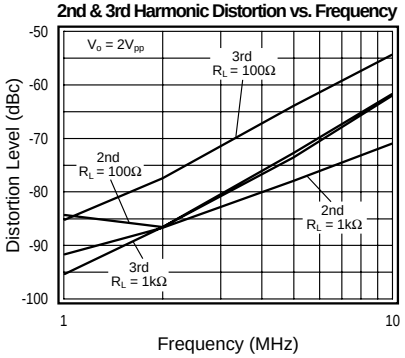
Large & Small Signal Pulse Response



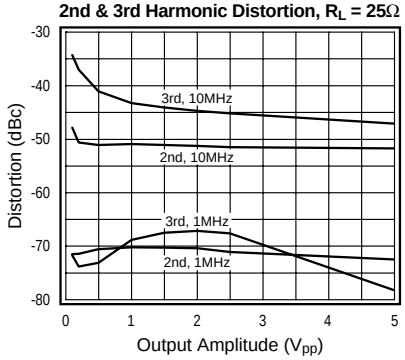
Differential Gain & Phase



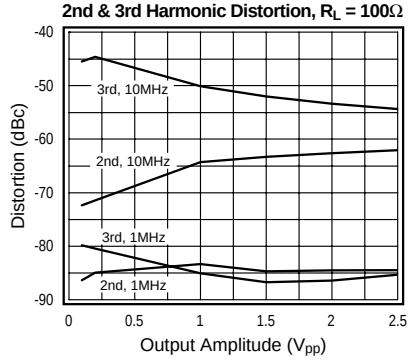
2nd & 3rd Harmonic Distortion vs. Frequency



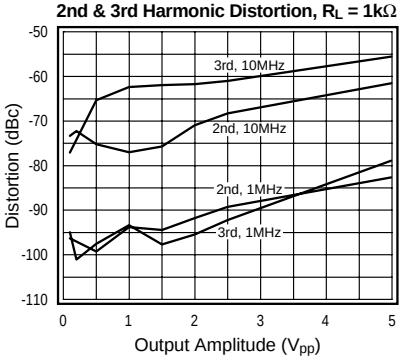
2nd & 3rd Harmonic Distortion, R_L = 25Ω



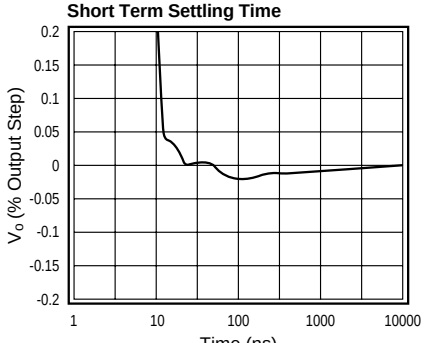
2nd & 3rd Harmonic Distortion, R_L = 100Ω



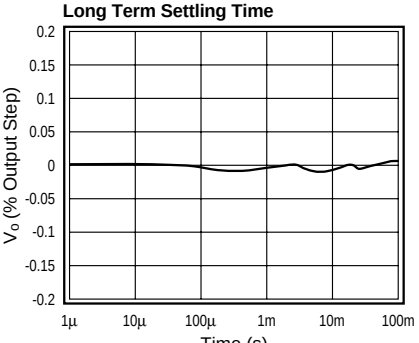
2nd & 3rd Harmonic Distortion, R_L = 1kΩ



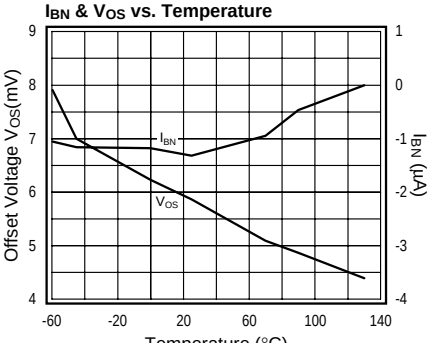
Short Term Settling Time



Long Term Settling Time

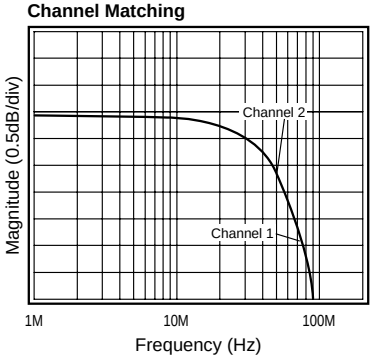


I_{BN} & V_{OS} vs. Temperature

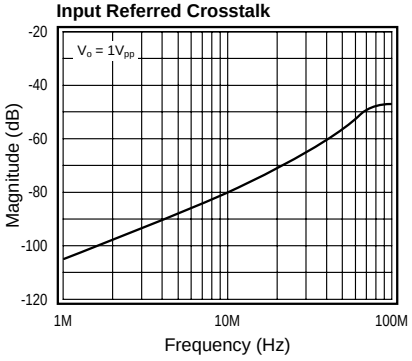


±5V Typical Channel Matching Performance (A_v = +2, R_L = 100Ω, V_{CC} = ± 5V, unless specified)

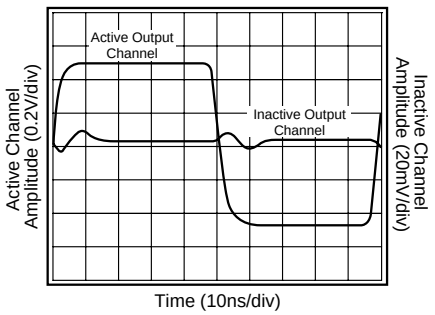
Channel Matching



Input Referred Crosstalk



Pulse Crosstalk



CLC5612 Operation

The CLC5612 is a current feedback buffer built in an advanced complementary bipolar process. The CLC5612 operates from a single 5V supply or dual ±5V supplies. Operating from a single 5V supply, the CLC5612 has the following features:

- Gains of +1, -1, and 2V/V are achievable without external resistors
- Provides 100mA of output current while consuming only 7.5mW of power
- Offers low -79/-81dBc 2nd and 3rd harmonic distortion
- Provides BW > 50MHz and 1MHz distortion < -75dBc at $V_o = 2V_{pp}$

The CLC5612 performance is further enhanced in ±5V supply applications as indicated in the ***±5V Electrical Characteristics*** table and ***±5V Typical Performance*** plots.

If gains other than +1, -1, or +2V/V are required, then the CLC5602 can be used. The CLC5602 is a current feedback amplifier with near identical performance and allows for external feedback and gain setting resistors.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \qquad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC5612's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

CLC5612 Design Information

Closed Loop Gain Selection

The CLC5612 is a current feedback op amp with $R_f = R_g$ = 1kΩ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of +2, +1, and -1V/V by connecting pins 2 and 3 (or 5 and 6) as described in the chart below.

Gain A_v	Input Connections	
	Non-Inverting (pins 3,5)	Inverting (pins 2,6)
-1V/V	ground	input signal
+1V/V	input signal	NC (open)
+2V/V	input signal	ground

The gain accuracy of the CLC5612 is excellent and stable over temperature change. The internal gain setting resistors, R_f and R_g are diffused silicon resistors with a process variation of ± 20% and a temperature coefficient of ~ 2000ppm/°C. Although their absolute values change with processing and temperature, their ratio (R_f/R_g) remains constant. If an external resistor is used in series with R_g, gain accuracy over temperature will suffer.

Single Supply Operation (V_{CC} = +5V, V_{EE} = GND)

The specifications given in the ***+5V Electrical Characteristics*** table for single supply operation are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC5612 is typically +0.8V to +4.2V. The typical output range with R_L=100Ω is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figures 1, 2, and 3 on the following page, show the recommended configurations for input signals that remain above 0.8V DC.

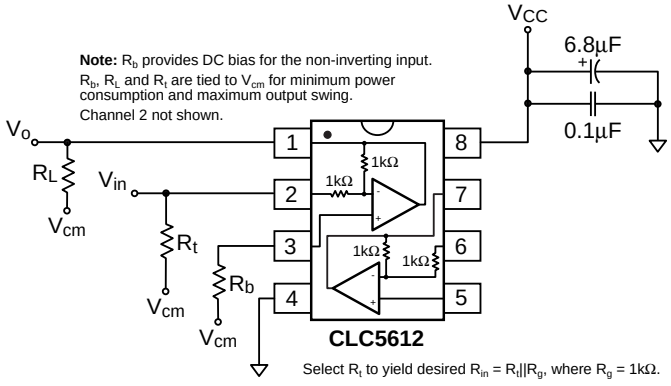


Figure 1: DC Coupled, A_V = -1V/V Configuration

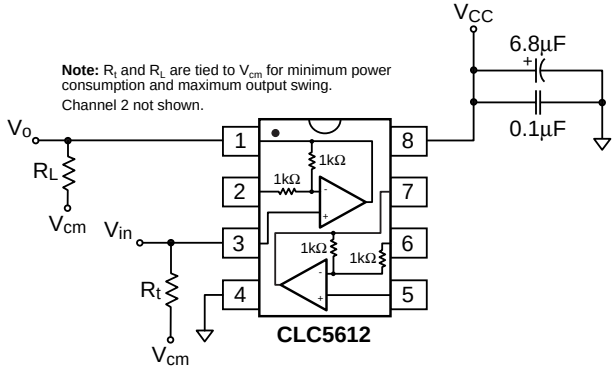


Figure 2: DC Coupled, A_V = +1V/V Configuration

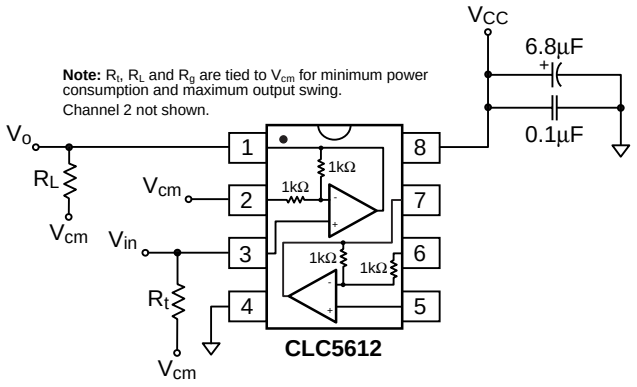


Figure 3: DC Coupled, A_V = +2V/V Configuration

AC Coupled Single Supply Operation

Figures 4, 5, and 6 show possible non-inverting and inverting configurations for input signals that go below 0.8V DC.

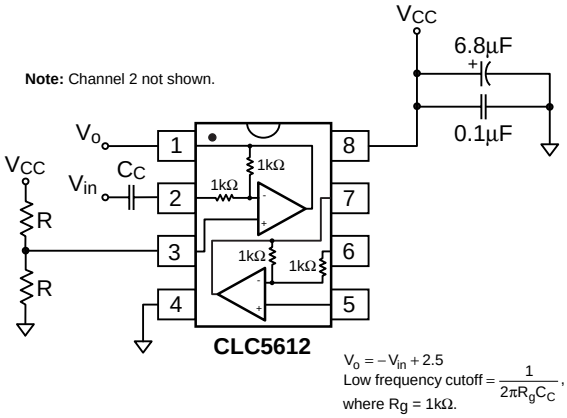


Figure 4: AC Coupled, A_V = -1V/V Configuration

The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2$ = 2.5V (For V_{CC} = +5V).

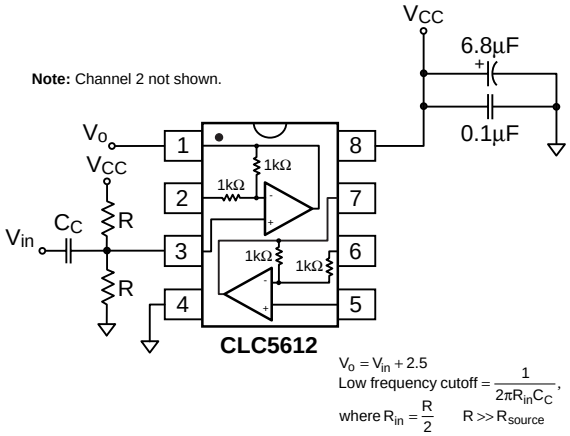


Figure 5: AC Coupled, A_V = +1V/V Configuration

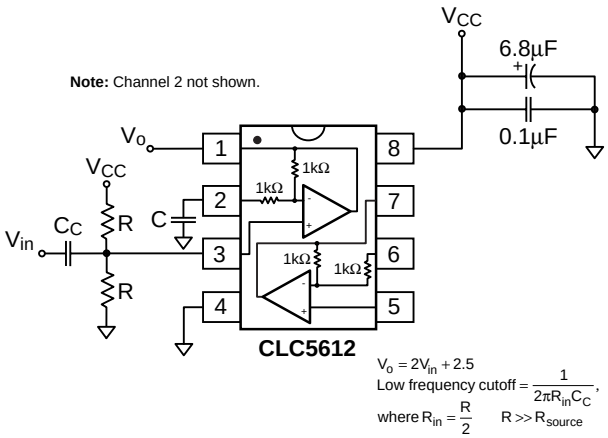


Figure 6: AC Coupled, A_V = +2V/V Configuration

Dual Supply Operation

The CLC5612 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 7, 8 and 9.

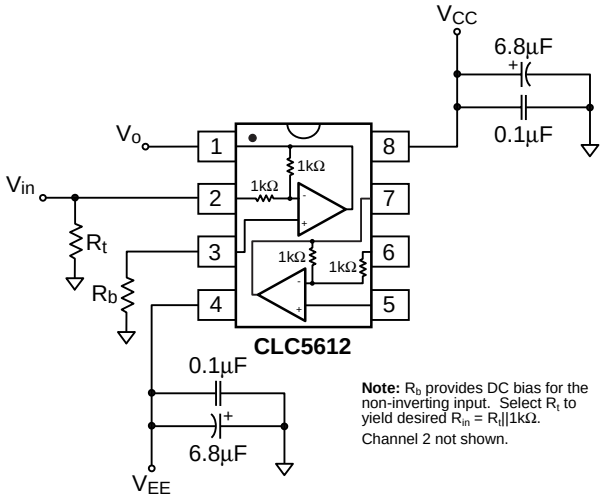


Figure 7: Dual Supply, A_V = -1V/V Configuration

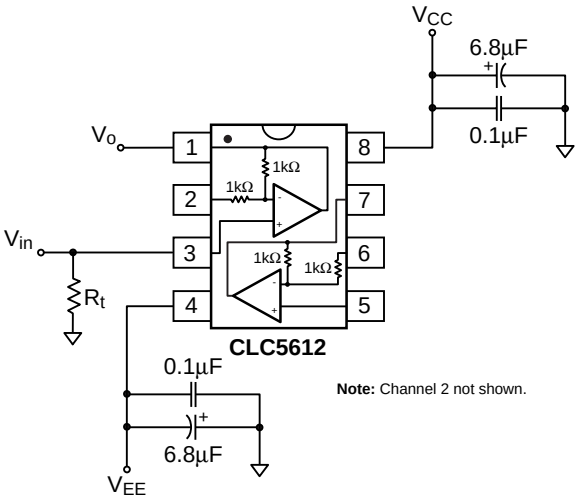


Figure 8: Dual Supply, A_V = +1V/V Configuration

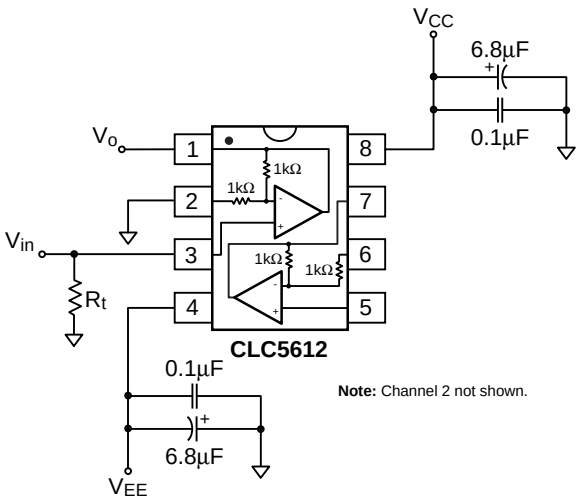


Figure 9: Dual Supply, A_V = +2V/V Configuration

Load Termination

The CLC5612 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm}.

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC5612 will improve stability and settling performance. The ***Frequency Response vs. C_L*** plot, shown below in Figure 10, gives the recommended series resistance value for optimum flatness at various capacitive loads.

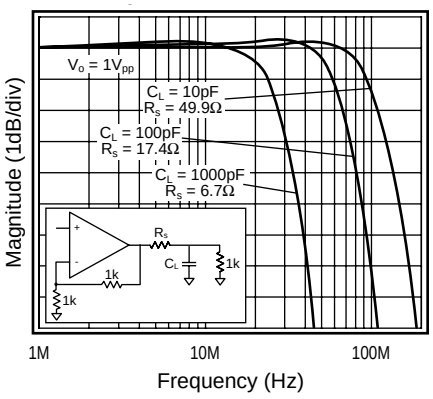


Figure 10: Frequency Response vs. C_L

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 11 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-inverting gain applications:

- Connect pin 2 as indicated in the table in the ***Closed Loop Gain Selection*** section.
- Make R_1, R_2, R_6, and R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_o.
- Make R_5 II $R_g = Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

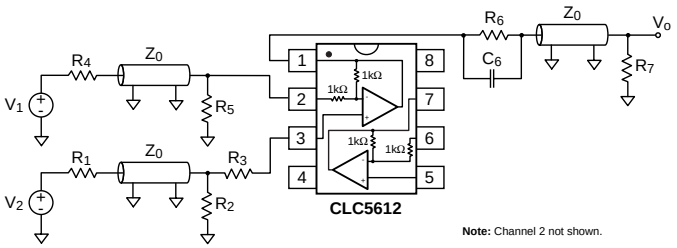


Figure 11: Transmission Line Matching

Power Dissipation
Follow these steps to determine the power consumption of the CLC5612:

1. Calculate the quiescent (no-load) power: $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage: $P_o = (V_{CC} - V_{load}) (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power: $P_t = P_{amp} + P_o$

The maximum power that the DIP and SOIC, packages can dissipate at a given temperature is illustrated in Figure 12. The power derating curve for any CLC5612 package can be derived by utilizing the following equation:

$$\frac{(175° - T_{amb})}{\theta_{JA}}$$

where

T_{amb} = Ambient temperature (°C)
θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

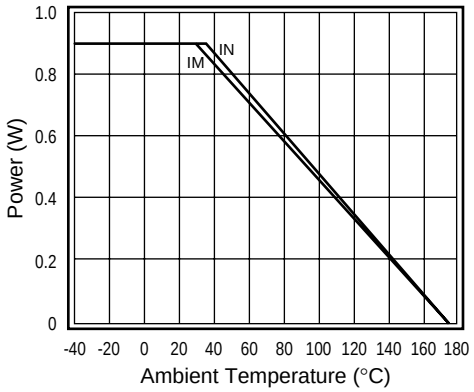


Figure 12: Power Derating Curve

Layout Considerations
A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC5612 (CLC730038-DIP, CLC730036-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information
A data sheet is available for the CLC730038/ CLC730036 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

Special Evaluation Board Considerations for the CLC5612

To optimize off-isolation of the CLC5612, cut the R_f trace on both the CLC730038 and the CLC730036 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. Figure 13 shows where to cut both evaluation boards for improved off-isolation.

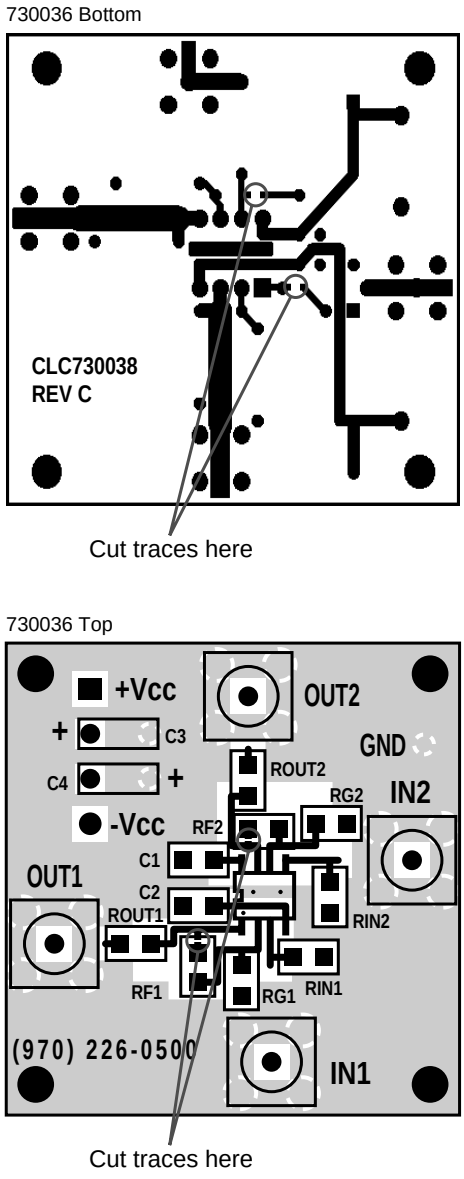


Figure 13: Evaluation Board Changes

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

Single Supply Cable Driver

Figure 14 below shows the CLC5612 driving 10m of 75Ω coaxial cable. The CLC5612 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o. The response after 10m of cable is illustrated in Figure 15.

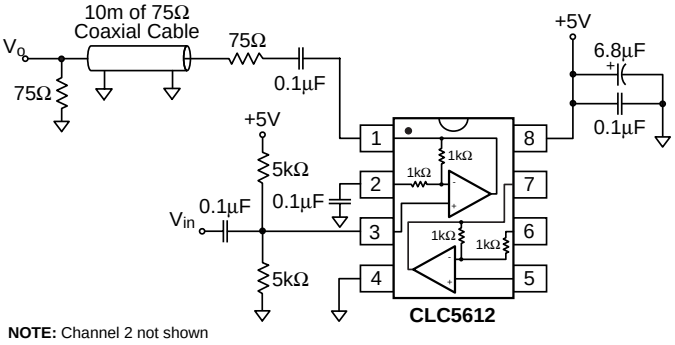


Figure 14: Single Supply Cable Driver

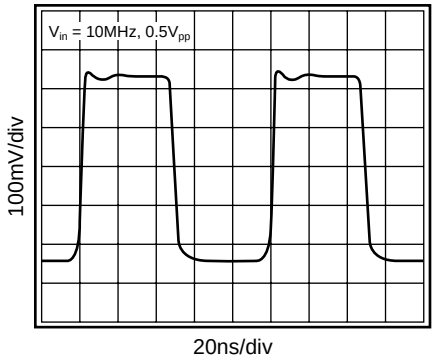


Figure 15: Response After 10m of Cable

Differential Line Driver With Load Impedance Conversion

The circuit shown in the ***Typical Application*** schematic on the front page and in Figure 16, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC5612's output capabilities. The single-ended input signal is converted to a differential signal by the CLC5612. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.

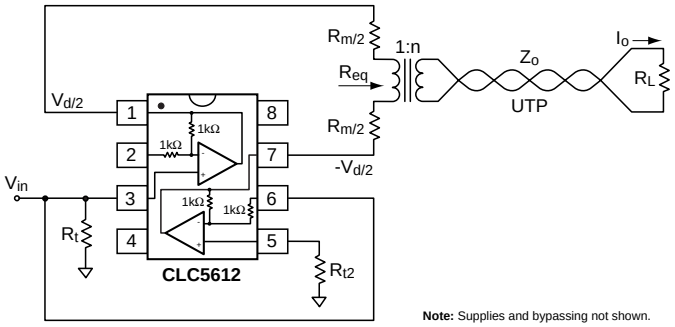


Figure 16: Differential Line Driver with Load Impedance Conversion

Set up the CLC5612 as a difference amplifier:

- Set the Channel 1 amplifier to a gain of +1V/V
- Set the Channel 2 amplifier to a gain of -1V/V

Make the best use of the CLC5612's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where R_{eq} is the transformed value of the load impedance, V_{max} is the Output Voltage Range, and I_{max} is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_o$$
$$R_m = R_{eq}$$
$$n = \sqrt{\frac{R_L}{R_{eq}}}$$

Select the transformer so that it loads the line with a value very near Z_o over frequency range. The output impedance of the CLC5612 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{o(5612)}(j\omega)}{Z_o} \right|, \text{dB}$$

where $Z_{o(5612)}(j\omega)$ is the output impedance of the CLC5612 and $|Z_{o(5612)}(j\omega)| << R_m$.

The load voltage and current will fall in the ranges:

$$|V_o| \leq n \cdot V_{max}$$
$$|I_o| \leq \frac{I_{max}}{n}$$

The CLC5612's high output drive current and low distortion make it a good choice for this application.

Differential Input/Differential Output Amplifier

Figure 17 below illustrates a differential input/differential output configuration. The bypass capacitors are the only external components required.

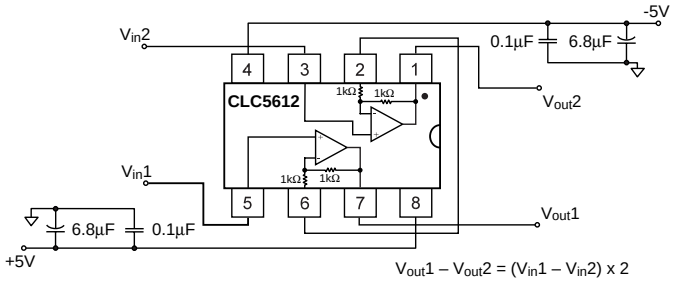


Figure 17: Differential Input/Differential Output Amplifier

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