MICROPOWER RRO Operational Amplifier with Shutdown

Features

- Tiny SOT23-6 Package
- Guaranteed specs at 1.8V, 2.2V, 2.7V, 3V and 5V
- Less than 1µA idle current.
- Very Low operating Supply current typically 85µA@3V
- Rail-to-Rail Output
- Simple shutdown mode (with logic level control)
- Typical Total Harmonic Distortion of 0.02% at 3V
- 1.66MHz Typical Gain Bandwidth Product
- 1V/µS Typical Slew Rate

Applications

- Mobile Communications
- Cellular Phones
- Portable Equipment
- Notebooks and PDAs
- Electronic Toys

Product Description

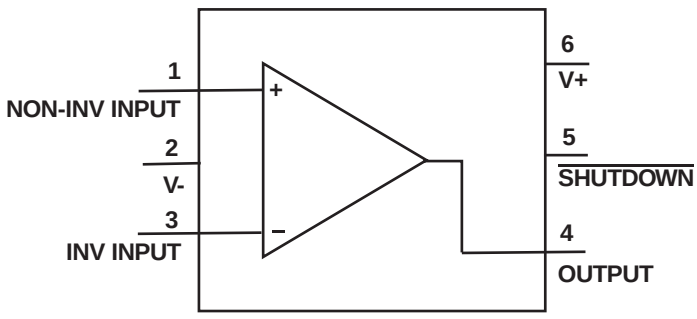
The CMV1026 is a high performance CMOS operational amplifier available in a small SOT23-6 package. Operating with very low supply current, it is ideal for battery operated applications where power, space and weight are critical.

Performance is similar to CAMD's CMV1020 SOT Amp, with the addition of a shutdown pin to greatly reduce supply current when idle. The shutdown mode is controlled by an extra pin, and is compatible with most logic family signal levels.

Ideal for use in personal electronics such as cellular handsets, pagers, cordless telephones and other products with limited space and battery power.

PIN DIAGRAM

6-Pin SOT23-6



STANDARD PART ORDERING INFORMATION

Package		Ordering Part Number	
Pins	Style	Tape & Reel	Part Marking
6	SOT23-6	CMV1026Y/R	1016

ABSOLUTE MAXIMUM RATINGS (NOTE 1)		
Parameter	**Rating**	**Unit**
ESD Protection (HBM, Note 2)	2000	V
Differential Input Voltage	+/– Supply Voltage	V
Voltage at input/output Pin	(V+) +0.3, (V–) –0.3	V
Temperature: Storage Operating Junction (Note 4) Lead (Soldering, 10s)	–65 to 150 125 260	°C
Supply Voltage (V+ to V–)	7.5	V
Current at Input Pin	5	mA
Current at Output Pin (Note 3)	15	mA
Current at Power Supply Pins	15	mA

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	**Rating**	**Unit**
Supply Voltage	1.8 to 7	V
Junction Temperature	–40 to 85	°C
Thermal Resistance	325	°C / W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate ratings for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Operating Characteristics.

Note 2: Human Body Model, 1.5KΩ in series with 100pF.

Note 3 : Applies to both single-supply and split-supply operation. Continuous short ckt operation at elevated ambient temperatures can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4 : The maximum power dissipation is a function of $T_{J\ (MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J\ (MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly to a PC board.

1.8V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified Tj = 25°C, V+ = 1.8V, V- = 0V, RL > 1MΩ)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Limit**	**Unit**
V_{OS}	Input Offset Voltage	V_{OUT} = 0.9V		9	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
I_S	Supply Current	Amplifier ON V_{SD} = 1.8V	75	150	µA
I_S	Supply Current	Amplifier OFF V_{SD} = 0V	0.01	1	µA
GBW	Gain Bandwidth Product		1.35		MHz
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2V to 1.6V	80	60	dB
SR	Slew Rate	A_V = –1, RL = 100K	0.8	0.2	V/µs
PSRR	Power Supply Rejection Ratio	V+ = 0.9V t0 1.2V V– = –0.9V to –1.2V VCM = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < VCM < 0.8V	60	40	dB
V_{CM}	Common Mode Input Range		0 1.1		V
THD	Total Harmonic Distortion	A_V = –1, f = 1KHz, V_{OUT} = 1Vp-p RL = 100K	0.026		%
I_{SC}	Output Short Circuit Current	Source/Sink	5		mA
V_O	Output Swing from either rail	RL = 10K	20	150	mV
V_{SDIH}	Amplifier ON Logic level	Amplifier ON		1.2	V
V_{SDIL}	Amplifier OFF Logic level	Amplifier OFF		0.6	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1	µA
T_{ON}	Turn On Time		22		µs
T_{OFF}	Turn Off Time		1		µs

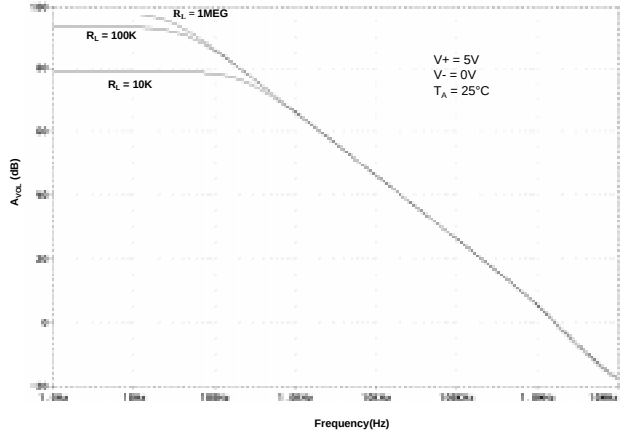
2.2V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified Tj = 25°C, V+ = 2.2V, V- = 0V, RL > 1MΩ)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Limit**	**Unit**
V_{OS}	Input Offset Voltage	V_{OUT} = 1.1V		9	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
I_S	Supply Current	Amplifier ON V_{SD} = 2.2V	80	160	µA
I_S	Supply Current	Amplifier OFF V_{SD} = 0V	0.01	1	µA
GBW	Gain Bandwidth Product		1.5		MHz
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2V to 2V	80	60	dB
SR	Slew Rate	A_V = –1, RL = 100K	0.9	0.2	V/µs
PSRR	Power Supply Rejection Ratio	V+ = 1.1V t0 1.4V V– = –1.1V to –1.4V VCM = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < VCM < 1.2V	60	40	dB
V_{CM}	Common Mode Input Range		0 1.5		V
THD	Total Harmonic Distortion	A_V = –1, f = 1KHz, V_{OUT} = 1.4Vp-p RL = 100K	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	7		mA
V_O	Output Swing from either rail	RL = 10K	20	150	mV
V_{SDIH}	Amplifier ON Logic level	Amplifier ON		1.6	V
V_{SDIL}	Amplifier OFF Logic level	Amplifier OFF		0.6	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1	µA
T_{ON}	Turn On Time		18		µs
T_{OFF}	Turn Off Time		1		µs

2.7V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified Tj = 25°C, V+ = 2.7V, V- = 0V, RL > 1MΩ)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Limit**	**Unit**
V_{OS}	Input Offset Voltage	V_{OUT} = 1.35V		6	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
I_S	Supply Current	Amplifier ON V_{SD} = 2.7V	85	170	µA
I_S	Supply Current	Amplifier OFF V_{SD} = 2.7V	0.01	1	µA
GBW	Gain Bandwidth Product		1.6		MHz
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2V to 2.5V	85	65	dB
SR	Slew Rate	A_V = –1, RL = 100K	1	0.25	V/µs
PSRR	Power Supply Rejection Ratio	V+ = 1.35V to 1.65V V– = –1.35V to 1.65V VCM = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < VCM < 1.7V	60	45	dB
V_{CM}	Common Mode Input Range		0 2		V
THD	Total Harmonic Distortion	A_V = –1, f = 1KHz, V_{OUT} = 1.9Vp-p RL = 100K	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	12		mA
V_O	Output Swing from either rail	RL = 10K	20	150	mV
V_{SDIH}	Amplifier ON Logic Level	Amplifier ON		2	V
V_{SDIL}	Amplifier OFF Logic Level	Amplifier OFF		0.8	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1	µA
T_{ON}	Turn On Time		15		µs
T_{ON}	Tun Off Time		1		µs

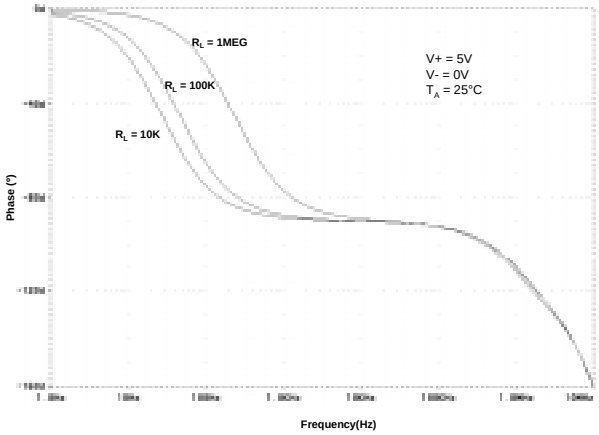
3V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified Tj = 25°C, V+ = 3V, V- = 0V, RL > 1MΩ)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Limit**	**Unit**
V_{OS}	Input Offset Voltage	V_{OUT} = 1.5V		5	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
I_S	Supply Current	Amplifier ON V_{SD} = 5V	85	170	µA
I_S	Supply Current	Amplifier OFF V_{SD} = 0V	0.01	1	µA
GBW	Gain Bandwidth Product		1.66		MHz
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2V to 4.8V	85	65	dB
SR	Slew Rate	A_V = –1, RL = 100K	1	0.25	V/µs
PSRR	Power Supply Rejection Ratio	V+ = 2.5V to 2.8V V– = –2.5V to –2.8V VCM = 0V	80	55	dB
CMRR	Common Mode Rejection Ratio	0V < VCM < 4V	70	50	dB
V_{CM}	Common Mode Input Range		0 4.3		V
THD	Total Harmonic Distortion	A_V = –1, f = 1KHz, V_{OUT} = 4Vp-p RL = 100K	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	15		mA
V_O	Output Swing from either rail	RL = 10K	20	150	mV
V_{SDIH}	Amplifier ON Logic Level	Amplifier ON		2.2	V
V_{SDIL}	Amplifier OFF Logic Level	Amplifier OFF		1	V
I_{IN}	Logic Pin Current	V_{SD} + V+ or GND		1	µA
T_{ON}	Turn On Time		13		µs
T_{OFF}	Turn Off Time		1		µs

5V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified Tj = 25°C, V+ = 5V, V- = 0V, RL > 1MΩ)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Limit**	**Unit**
V_{OS}	Input Offset Voltage	V_{OUT} = 1.5V		5	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		TΩ
I_S	Supply Current	Amplifier ON V_{SD} = 5V	100	200	µA
I_S	Supply Current	Amplifier OFF V_{SD} = 0V	0.01	1	µA
GBW	Gain Bandwidth Product		1.8		MHz
A_V	Large Signal Voltage Gain	V_{OUT} = 0.2V to 2.8V	90	70	dB
SR	Slew Rate	A_V = –1, RL = 100K	1.2	0.3	V/µs
PSRR	Power Supply Rejection Ratio	V+ = 1.5V to 1.8V V– = –1.5V to –1.8V VCM = 0V	80	55	dB
CMRR	Common Mode Rejection Ratio	0V < VCM < 2V	70	50	dB
V_{CM}	Common Mode Input Range		0 4.3		V
THD	Total Harmonic Distortion	A_V = –1, f = 1KHz, V_{OUT} = 2Vp-p RL = 100K	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	25		mA
V_O	Output Swing from either rail	RL = 10K	20	150	mV
V_{SDIH}	Amplifier ON Logic Level	Amplifier ON		4	V
V_{SDIL}	Amplifier OFF Logic Level	Amplifier OFF		1	V
I_{IN}	Logic Pin Current	V_{SD} + V+ or GND		1	µA
T_{ON}	Turn On Time		7.5		µs
T_{OFF}	Turn Off Time		1		µs

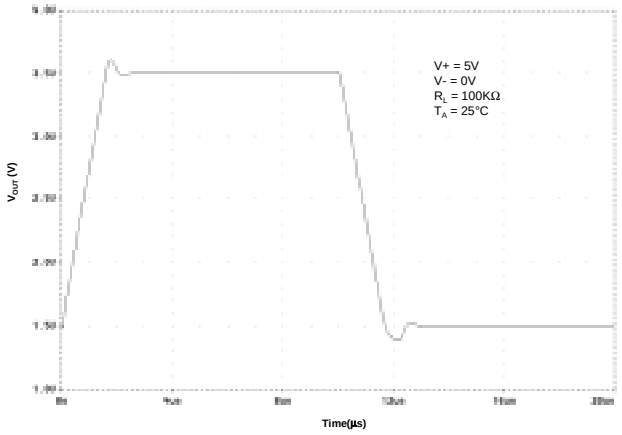
Open Loop Voltage Gain Response



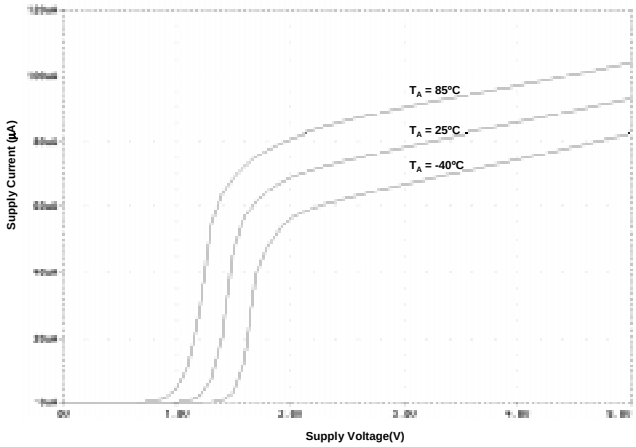
Open Loop Phase Response



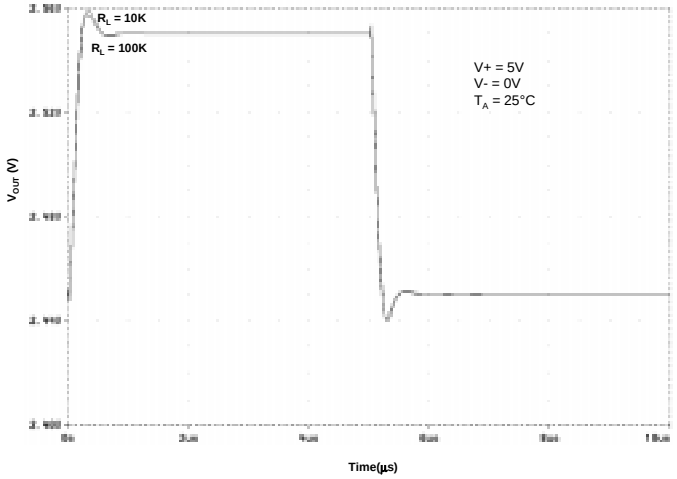
Large Signal Pulse Response



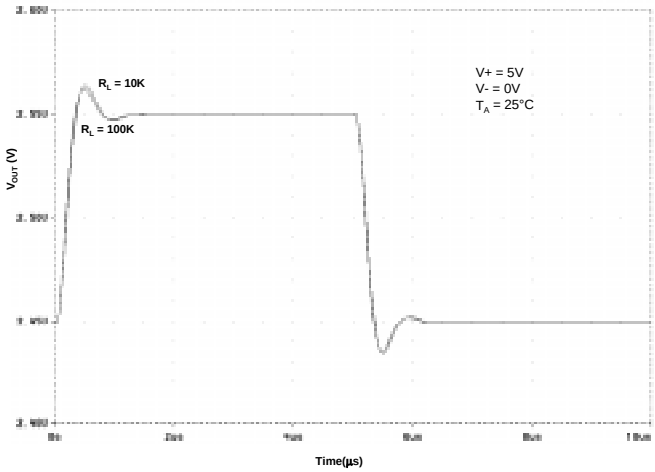
Supply Current Versus Supply Voltage



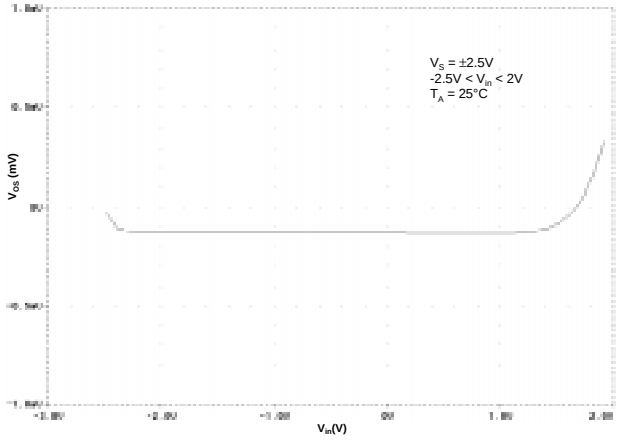
Non Inverting Small Signal Response



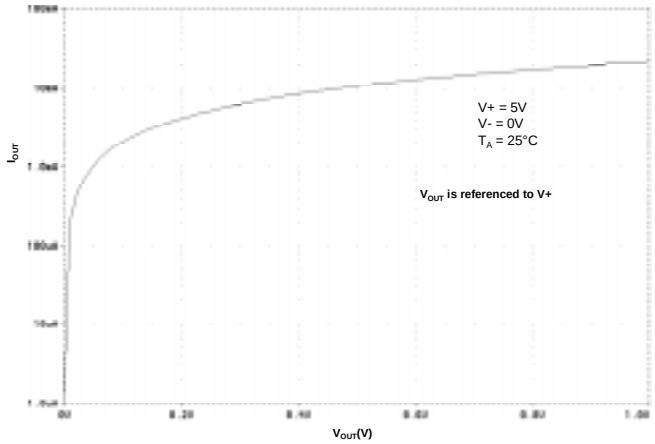
Inverting Small Signal Response



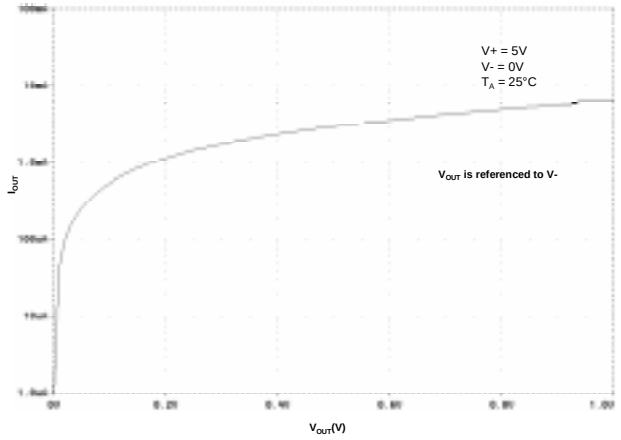
Common Mode Rejection Ratio



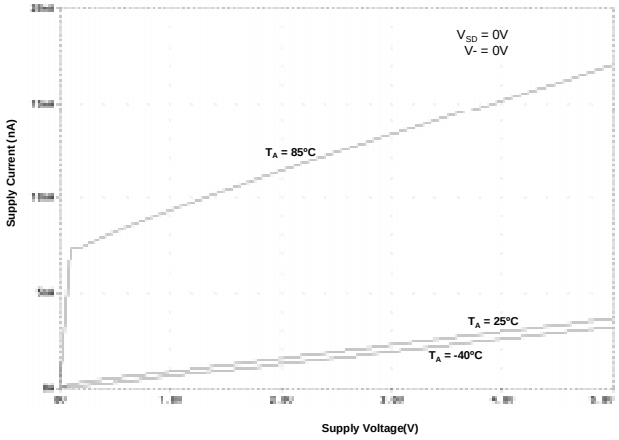
Current Sourcing Versus V_{OUT}



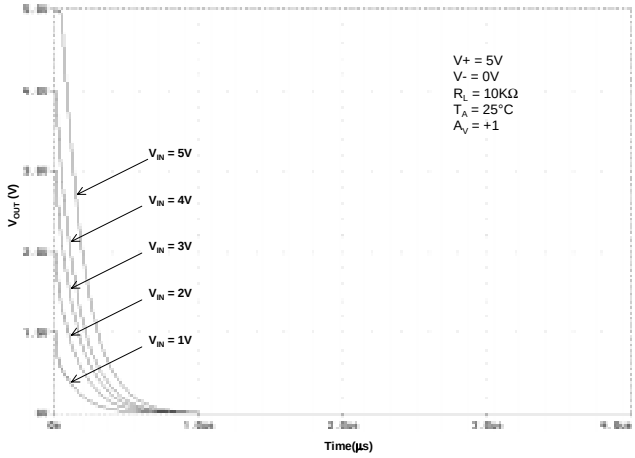
Current Sinking Versus V_{OUT}



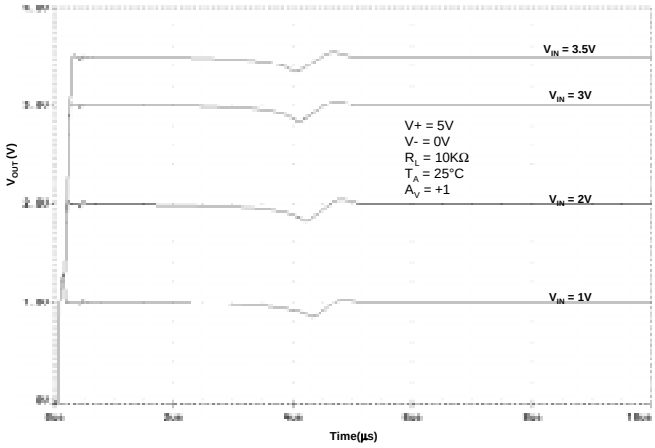
Disabled Supply Current Versus Supply Voltage



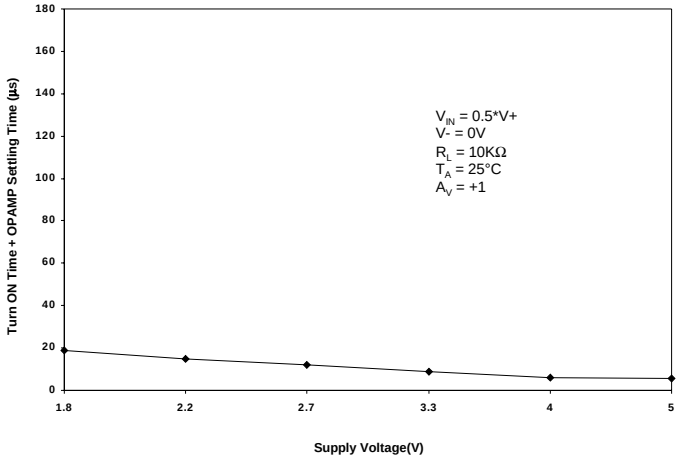
5V Disable Response for a family of DC Inputs



5V Enable Response for a family of DC Inputs



Turn ON Time Versus Supply Voltage



Applications Information

1. Input Common Mode Range and Output Voltage Considerations

The CMV1026 is capable of accommodating an input common mode voltage equal to one volt below the positive rail and all the way to the negative rail. It is also capable of output voltages equal to both power supply rails. Voltages that exceed the supply voltages will not cause phase inversion of the output, however, ESD diode clamps are provided at the inputs that can be damaged if static currents in excess of ±5mA are allowed to flow in them. This can occur when the magnitude of input voltage exceeds the rail by more than 0.3 volt. To preclude damage, an applications resistor, Rs, in series with the input is recommended as illustrated in Figure 1 whose value for R_S is given by:

$$R_S > \frac{V_{IN} - (V+ + 0.3V)}{5\ mA}$$

For V+ (or V–) equal to 2.2 volts and V_{IN} equal to 10 volts, R_S should be chosen for a value of 2.5KΩ or greater.

The Shutdown pin also provides ESD clamp diodes that will be damaged if the signal exceeds the rail by 0.3 volts and should also be limited to <5mA by inserting the appropriate resistor between the input signal or logic gate and the Shutdown input.

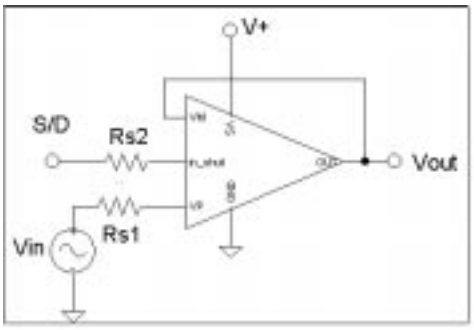


Figure 1.

2. Output Current and Power Dissipation Considerations

The CMV1026 is capable of sinking and sourcing output currents in excess of 7mA (V+ = 2.2 volts) at voltages very nearly equal to the rails. As such, it does not have any internal short circuit protection (which would in any event detract from its rail to rail capability). Although the power dissipation and junction temperature rise are small, a short analysis is worth investigating.

Obviously, the worst case from a power dissipation point of view is when the output is shorted to either ground in a single rail application or to the opposite supply voltage in split rail applications. Since device only draws 60μA supply current (100μA maximum), its contribution to the junction temperature, T_J, is negligible. As an example, let us analyze a situation in which the CMV1026 is operated from a 5 volt supply and ground, the output is "programmed" to positive saturation, and the output pin is indefinitely shorted to ground. In general:

$$P_{DISS} = (V+ - V_{OUT})*I_{OUT} + I_S*V+$$

Where: P_{DISS} = Power dissipated by the chip
V+ = Supply voltage
V_{OUT} = The output voltage
I_S = Supply Current

The contribution to power dissipation due to supply current is 500μW and is indeed negligible as stated above.

The primary contribution to power dissipation occurs in the output stage. $V+ - V_{OUT}$ would equal 5V – 0V = 5 V while the short circuit current would be 25mA. The power dissipation would be equal to 125mW.

$$T_J = T_A + \theta_{JA} * P_{DISS}$$

Where: T_A = The ambient temperature
θ_{JA} = The thermal impedance of the package junction to ambient

The SOT23 exhibits a θ_{JA} equal to 325°C/W. Thus for our example the junction rise would be about 41°C which is clearly not a destructive situation even under an ambient temperature of 85°C.

3. Input Impedance Considerations

The CMV1026 exhibits an input impedance typically in excess of 1 Tera Ω (1 X 10^{12} ohms) making it very appropriate for applications involving high source impedance such as photodiodes and high output impedance transducers or long time constant integrators. High source impedances usually dictate large feedback resistors. But, the output capacitance of the source in parallel with the input capacitance of the CMV1026 (which is typically 3pF) create a parasitic pole with the feedback resistor which erodes the phase margin of the amplifier. The usual fix is to bypass, R_F, as shown in Figure 2 with a small capacitor to cancel the input pole. The usual formula for

calculating C_F always results in a value larger than that is required:

$$\frac{1}{2\Pi R_S C_S} \geq \frac{1}{2\Pi R_F C_F}$$

Since the parasitic capacitance can change between the breadboard and the production printed circuit board, we favor the use of a “gimmick”, a technique perfected by TV technicians in the 1950’s. A gimmick is made by taking two lengths (typically about a foot) of small gauge wire such as AWG 24, twisting them together, and then after baring all ends soldering the gimmick across R_F. With the circuit operating, C_F is “adjusted” by clipping short lengths of the gimmick off until the compensation is nominal. Then simply remove the gimmick, take it to an impedance bridge, and select the capacitor accordingly.

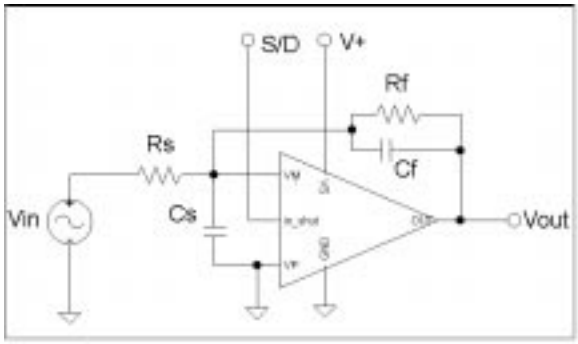


Figure 2.

4. Capacitive Load Considerations

The CMV1026 is capable of driving capacitate loads in excess of 100pF without oscillation. However, significant peaking will result. Probably the easiest way minimize this problem is to use an isolation resistor as shown in Figure 3.

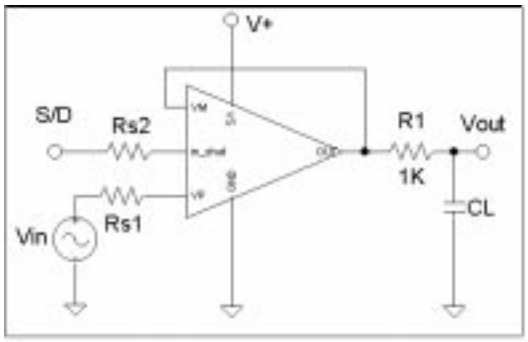


Figure 3

5. Power Supply Decoupling

The CMV1026 is not prone to oscillation without the use of power supply decoupling capacitors, however to minimize hum and noise pick-up, it is recommended that the rails be bypassed with 0.01mF capacitors.

6. Turn On and Turn Off (Shut Down) Characteristics

The turn off delay (Disable Response), t_{OFF}, is defined as the time between the shut down signal crossing the disable threshold (typically V+ – 1 volt) and the time for the amplifier’s output to come within 10% of zero. It is largely governed by a propagation delay within the CMV1026 of few hundred nanoseconds followed by an exponential decay determined by the load resistance in parallel with the load capacitance.

The turn on delay (Enable Response), t_{ON}, is defined as the time between the shutdown signal crossing the threshold and the time the output reaches to within 10% of its final value. t_{ON} is largely independent of supply voltage and input level.

7. Typical Applications

Illustrated in Figure 4 is a Sample and Hold Amplifier capable of operating from a single rail, but it will work equally well with split rails The circuit will accommodate input voltages (common mode) from zero volts to V+ – 1 volt. The Shut Down feature of the CMV1026 is used to disable A_1 whose output acts like a very high impedance in this mode. The high slew rate of the CMV1026 and large output current minimize Acquisition Time. A_2 presents a very high input impedance and very low bias current. A Logic “1”, a voltage > V+ – 1 volt, will put the circuit into “Sample” mode. A Logic “0” will put the circuit in “Hold” mode. For the values shown, Acquisition Time to 0.1% is typically 10 μS for a zero to 4 volt input, the hold step is typically 400 μV, and the droop rate at 85 °C is 0.1μV/μS. Overall accuracy is better than 0.01%. For minimum droop, C_1 should be of polystyrene construction.

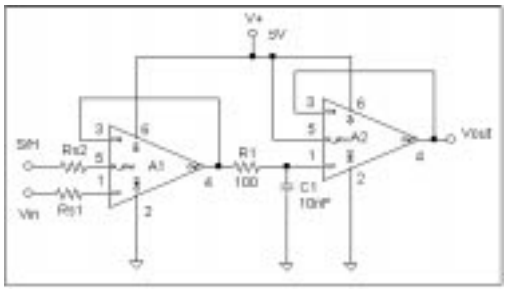


Figure 4

The circuit illustrated in Figure 5 provides a simple analog switch capable of operating from supply voltages as low as 2.2 volts. The circuit takes advantage of the CMV1026's shutdown feature which places the output stage in a high impedance mode. The outputs are simply "wire OR'd", and as configured, a Logic "1" (Logic In voltage > V+ – 1 volt), $V_{IN}2$ is selected.

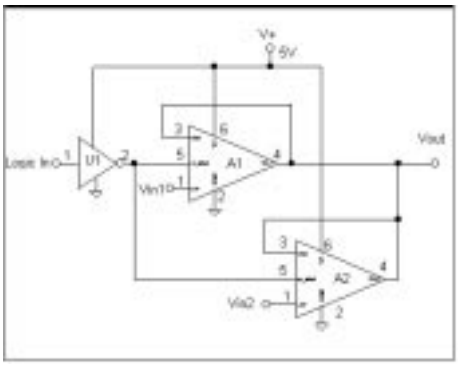


Figure 5