

[查询PM10CNJ060供应商](#)

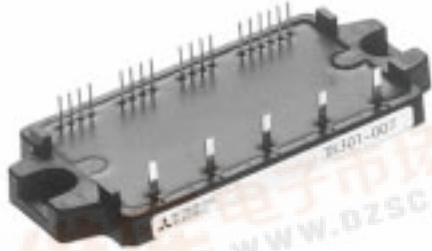
[捷多邦, 专业PCB打样工厂, 24小时加急出货](#)

MITSUBISHI <INTELLIGENT POWER MODULES>

PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

PM10CNJ060



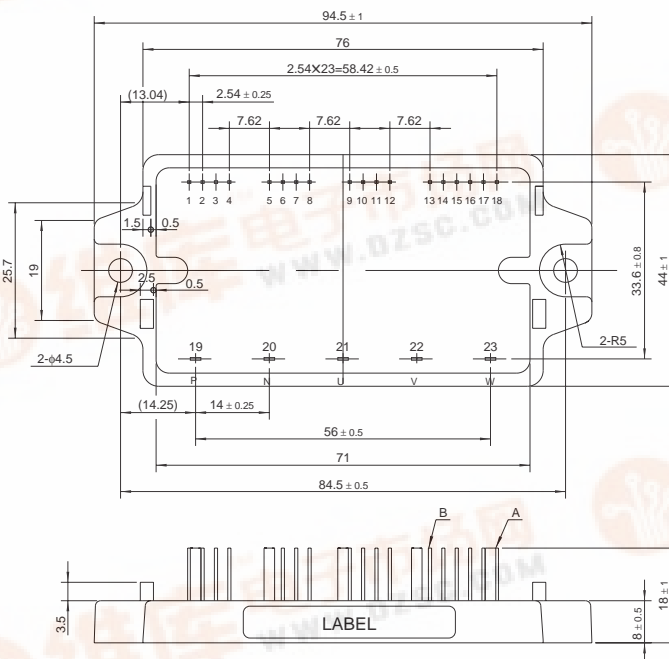
- 3 phase IGBT (10A/600V) inverter output
- Monolithic gate drive & protection logic circuit
- Protection logic
 - Over circuit (OC)
 - Short circuit (SC)
 - Over temperature (OT)
 - Under voltage lock-out (UV)
- UL Recognized File No. E80271
Yellow Card No. E80276

APPLICATION

General purpose inverter, servo drives and other motor controllers

PACKAGE OUTLINES

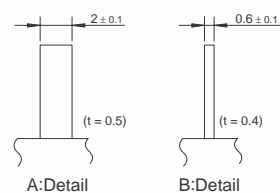
Dimensions in mm



Terminal code

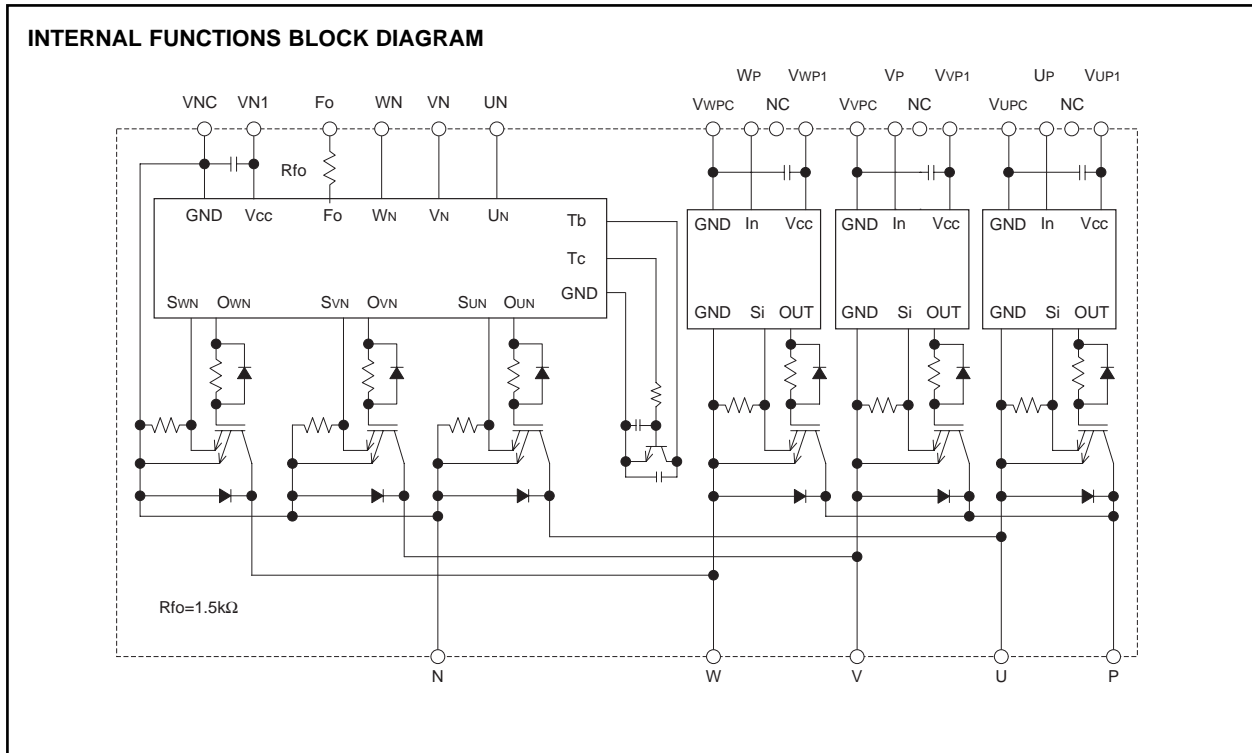
- | | |
|----------|---------|
| 1. VUPC | 13. VNC |
| 2. NC | 14. VN1 |
| 3. UP | 15. UN |
| 4. VUP1 | 16. VN |
| 5. VVPC | 17. WN |
| 6. NC | 18. FO |
| 7. VP | 19. P |
| 8. VVP1 | 20. N |
| 9. VVPC | 21. U |
| 10. NC | 22. V |
| 11. WP | 23. W |
| 12. VWP1 | |

NC : No Connect



PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CEs}	Collector-Emitter Voltage	V _D = 15V, V _{CIN} = 15V	600	V
±I _C	Collector Current	T _C = 25°C	10	A
±I _{CP}	Collector Current (Peak)	T _C = 25°C	20	A
P _C	Collector Dissipation	T _C = 25°C	39	W
T _j	Junction Temperature		-20 ~ +125*	°C

*The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the IPM to ensure safe operation. However, these power elements can endure junction temperature as high as 150°C instantaneously. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is requested to be provided before use.

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Supply Voltage	Applied between : V _{UP1} -V _{UVC} V _{VPC1} -V _{VPC} , V _{WP1} -V _{WPC} , V _{N1} -V _{NVC}	20	V
V _{CIN}	Input Voltage	Applied between : U _P -V _{UVC} , V _P -V _{VPC} W _P -V _{WPC} , U _N • V _N • W _N -V _{NVC}	20	V
V _{FO}	Fault Output Supply Voltage	Applied between : F _O -V _{NVC}	20	V
I _{FO}	Fault Output Current	Sink current at F _O terminals	20	mA

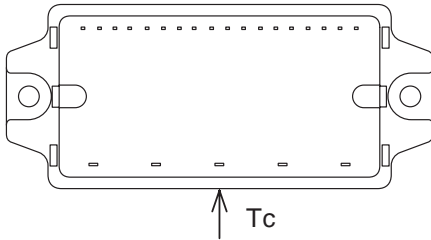
PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = 125°C Start	400	V
VCC(surge)	Supply Voltage	Applied between : P-N, Surge value	500	V
T _C	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V _{rms}

(Note-1) T_C measurement point



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 10A V _{CIN} = 0V, Pulsed (Fig. 1)	T _j = 25°C	—	1.8	2.5	V
			T _j = 125°C	—	1.9	2.6	
V _{EC}	FWDi Forward Voltage	-I _C = 10A, V _D = 15V, V _{CIN} = 15V (Fig. 2)	—	1.8	3.0	V	
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 300V, I _C = 10A T _j = 125°C, Inductive Load (Upper-Lower Arm) (Fig. 3)	—	0.3	0.7	1.6	μs
t _{tr}			—	0.15	0.5	μs	
t _{c(on)}			—	0.3	1.0	μs	
t _{off}			—	1.5	2.3	μs	
t _{c(off)}			—	0.4	1.2	μs	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 4)	T _j = 25°C	—	—	1	mA
			T _j = 125°C	—	—	10	

PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

CONTROL PART

Symbol	Parameter	Test Condition	Limits			Unit	
			Min.	Typ.	Max.		
Id	Circuit Current	V _D = 15V, V _{CIN} = 15V	VN1-VNC	—	18	25	mA
			VXP1-VXPC	—	7	10	
V _{th(ON)}	Input ON Voltage	Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN-VNC	1.2	1.5	1.8	V	
V _{th(OFF)}	Input OFF Voltage		1.7	2.0	2.3	V	
OC	Over Current Trip Level	-20 ≤ T _j ≤ 125°C, V _D = 15V (Fig. 5,6)	12	18	—	A	
SC	Short Circuit Trip Level	-20 ≤ T _j ≤ 125°C, V _D = 15V (Fig. 5,6)	—	27	—	A	
t _{off(OC)}	Over Current Delay Time	V _D = 15V (Fig. 5,6)	—	10	—	μs	
OT	Over Temperature protection	V _D = 15V	Trip level	100	110	120	°C
			Reset level	—	90	—	°C
UV	Supply Circuit Under-Voltage Protection	-20 ≤ T _j ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV _r			Reset level	—	12.5	—	V
I _{FO(H)}	Fault Output Current	V _D = 15V, V _{CIN} = 15V (Note-2)	—	—	0.01	mA	
I _{FO(L)}			—	10	15	mA	
t _{FO}	Minimum Fault Output Pulse Width	V _D = 15V (Note-2)	1.0	1.8	—	ms	

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1/6 module)	—	—	3.2	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/6 module)	—	—	4.5	°C/W
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.5	°C/W

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M4	0.98	1.18	1.47	N • m
			10	12	15	kg • cm
—	Weight	—	60	—	g	

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals (Fig. 3)	≤ 400	V
V _D	Control Supply Voltage	Applied between : V _{UP1} -V _{U_{PC}} , V _{VP1} -V _{V_{PC}} V _{WP1} -V _{W_{PC}} , V _{N1} -V _{N_C} (Note-3)	15 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-V _{U_{PC}} , VP-V _{V_{PC}} , WP-V _{W_{PC}} UN • VN • WN-VNC	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 4.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 15	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2	μs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input signals should be low level.
After this, each input signal should be set to the specified ON and OFF level.
2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above $V_{CC(surge)}$ rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

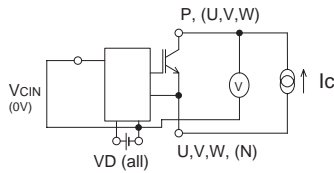


Fig. 1 $V_{CE(sat)}$ Test

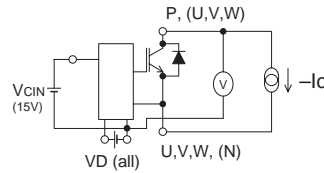
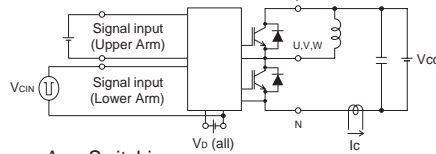


Fig. 2 V_{ec} Test

a) Lower Arm Switching



b) Upper Arm Switching

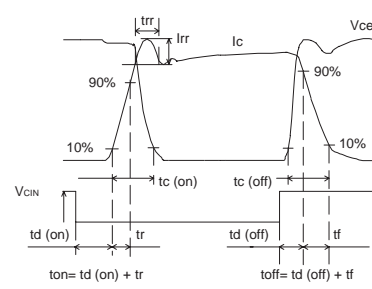
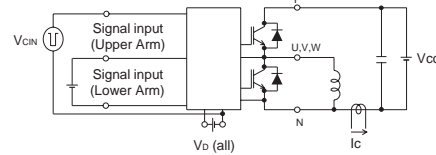


Fig. 3 Switching time Test circuit and waveform

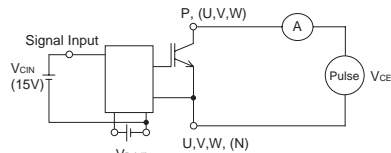


Fig. 4 I_{CES} Test

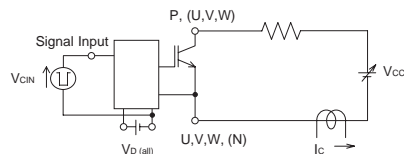
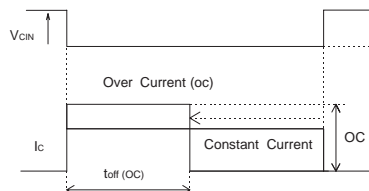


Fig. 5 OC and SC Test

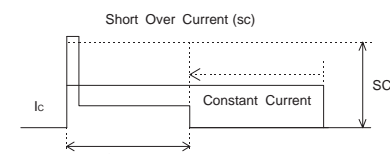


Fig. 6 OC and SC Test waveform

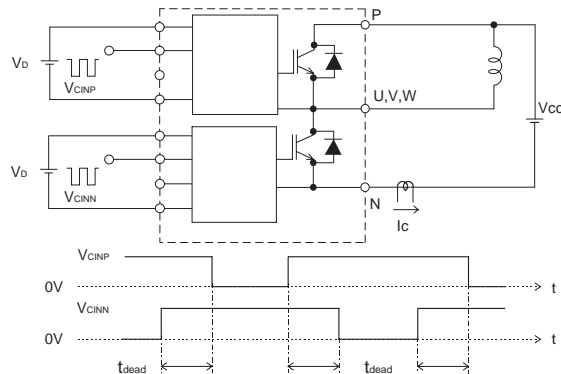


Fig. 7 Dead time measurement point example

PM10CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

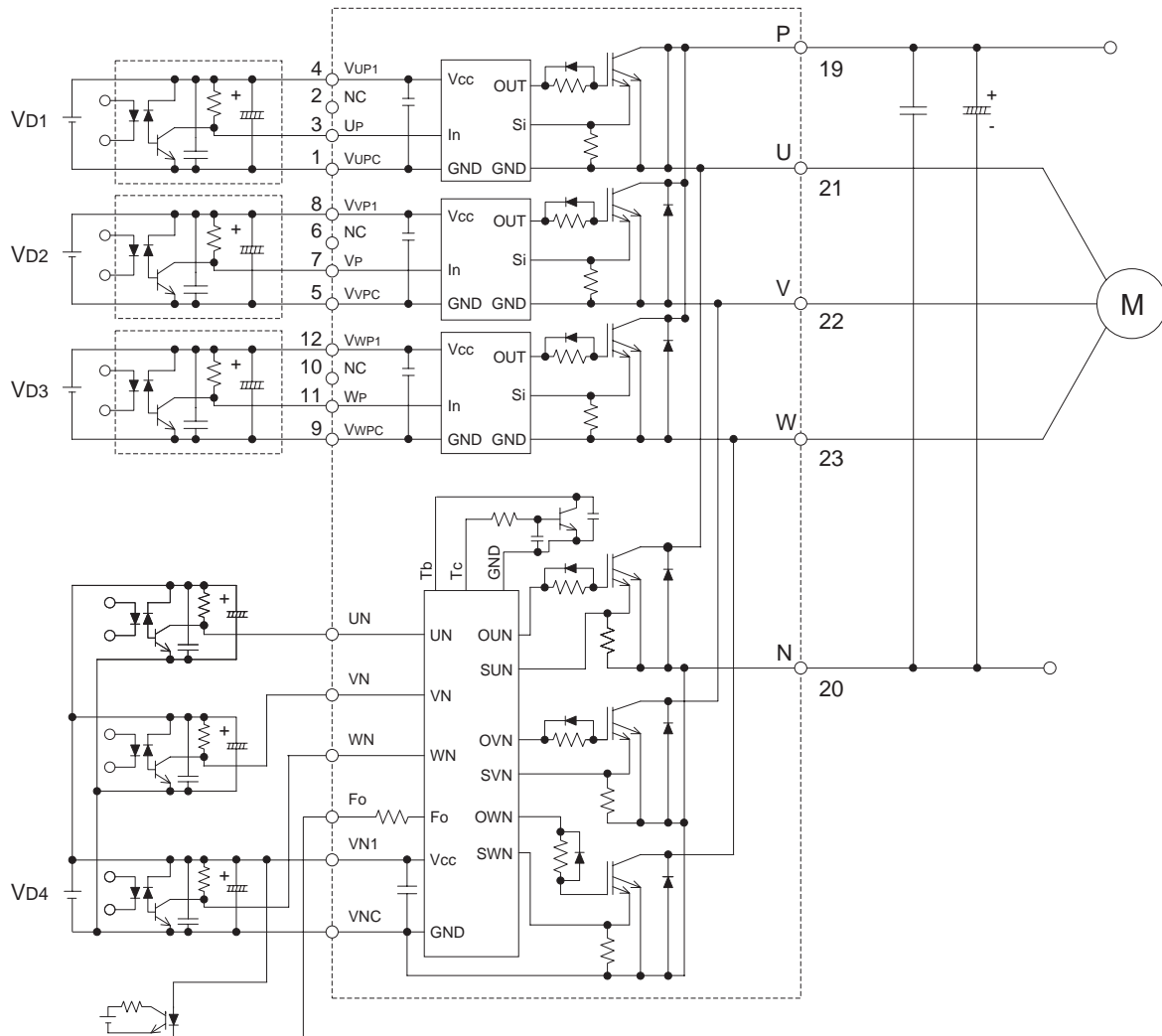


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.