HEWLETT® PACKARD

VDE 0884 Approved, Ultra High CMR, High Speed Optocoupler

Technical Data

CNW4504

Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  UL1577 (File No. E55361)
  CSA Certified-Component Acceptance Notice #5 (File CA88324)
  VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  FIMKO/SETI-SEMKO-NEMKO DEMKO according to IEC 65/950/335 (Pending)
  BSI According to BS 415/BS EN60950 (BS 7002)/BS EN41003
- **Short Propagation Delays for TTL and IPM Applications**
- **Ultra High Common Mode Transient Immunity: 15 kV/µs at V_{CM} = 1500 V Specified for TTL Load/Drive**
- **High CTR >23% at 25°C, I_F = 16 mA**
- **Electrical Specifications for Common IPM Applications**
- **TTL Compatible**
- **AC and DC Performance Specified Over Temperature: 0°C to 70°C**
- **Open Collector Output**

Applications

- **High Voltage Insulation**
- **Inverter Circuits and Intelligent Power Module (IPM) Interfacing -**
  High common mode transient immunity (>10 kV/µs for an IPM load/drive) and (t_{PLH} - t_{PHL}) specificied. (See Power Inverter Dead Time section)
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL**
- **Line Receivers -**
  Short propagation delays and low input-output capacitance (0.5 pF).
- **Replace Pulse Transformers -**
  Save board space and weight.
- **Analog Signal Ground Isolation -**
  Integrated photodetector provides improved linearity over phototransistors.

Description

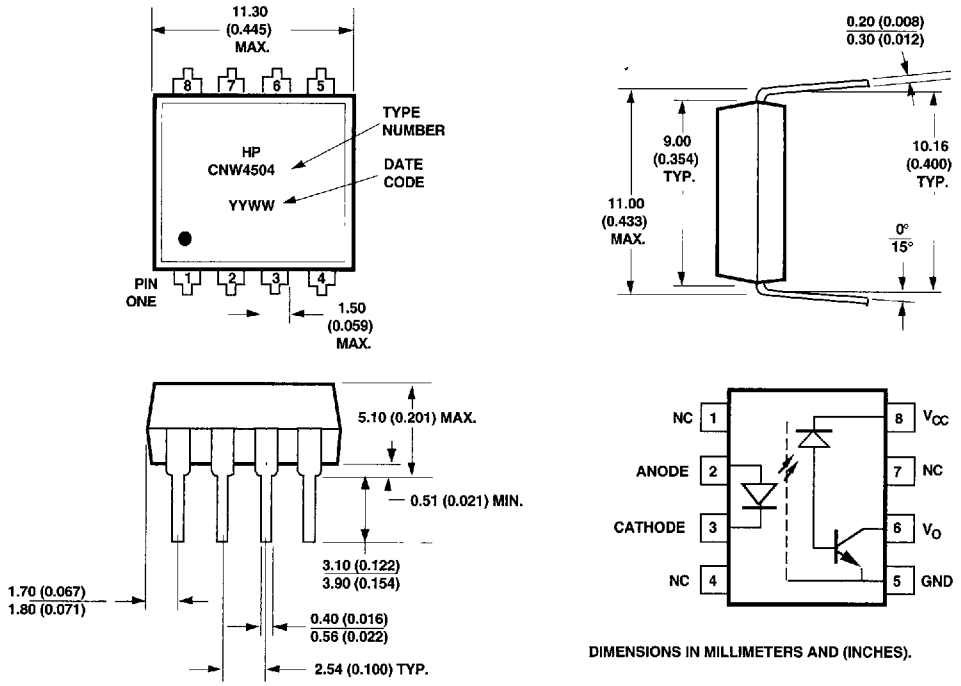
The CNW4504 is a high voltage and fast switching optocoupler consisting of an AlGaAs LED and a silicon photodetector. A wide body encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW4504 is similar to HP's other high speed transistor output optocouplers, but with shorter propagation delays and higher CTR. The CNW4504 also has propagation delay difference (t_{PLH} - t_{PHL}) specified. These features make the CNW4504 an excellent solution to IPM inverter dead time and other switching problems.

The CNW4504 CTR, propagation delays, and CMR are specified both for TTL load and drive conditions and for IPM load and drive conditions. Specifications and typical performance plots for both TTL and IPM conditions are provided for ease of application.

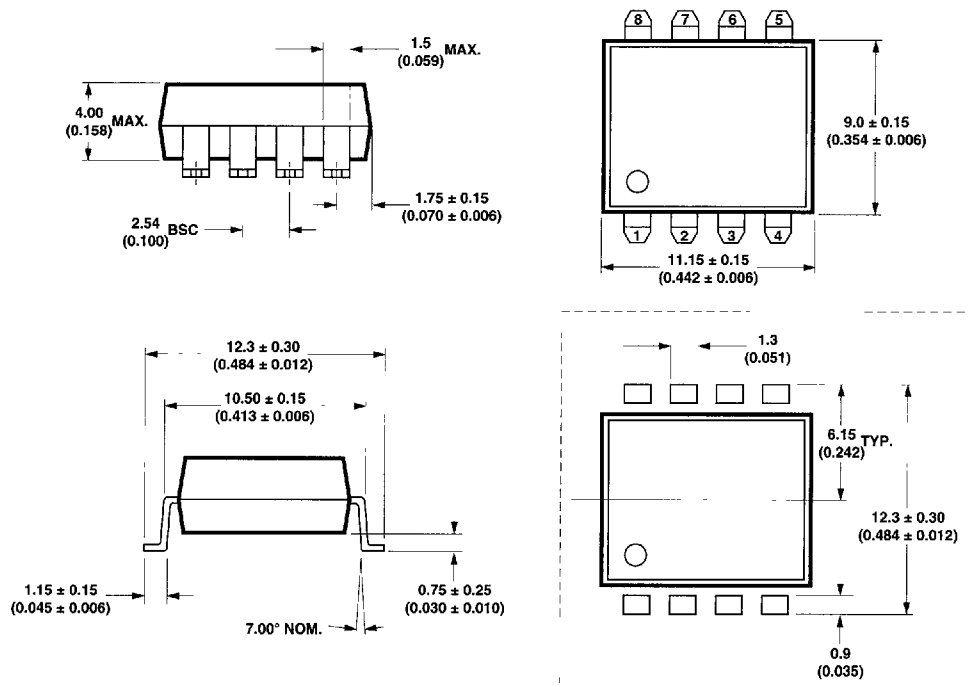
CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

Gull Wing Surface Mount Option #300

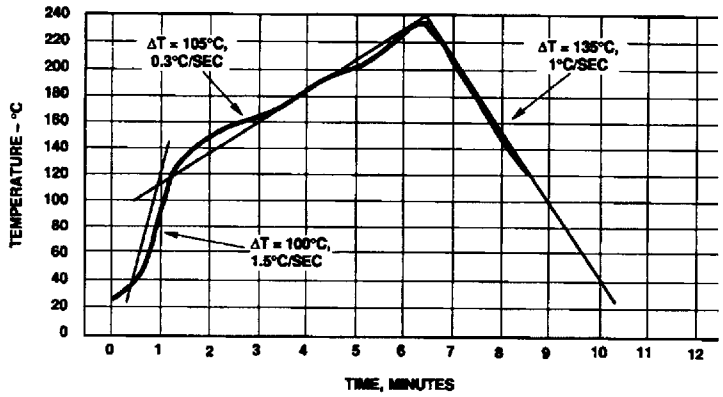


LEAD COPLANARITY = 0.102 (0.004").

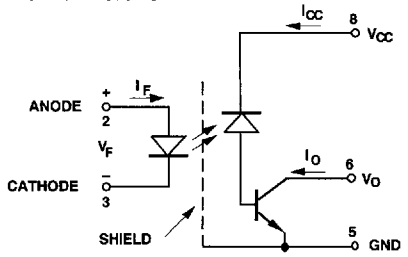
DIMENSIONS IN MILLIMETERS (INCHES).

PAD LOCATION (FOR REFERENCE ONLY)

Temperature Profile



Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	L
L	H

Regulatory Information

The CNW4504 optocoupler features a 10.16 mm (0.400 inch) wide, eight pin DIP package. This package was specifically designed to meet worldwide regulatory requirements. The CNW4504 is approved by the following organizations:

UL	Covered under UL 1577, component recognition, FILE E55361
CSA	Certified according to Component Acceptance Notice #5 (File CA 88324)
VDE	Approved according to VDE 0884/06.92
NORDIC	Tested for application (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution. FIMKO/SETI-SEMKO-NEMKO-DEMKO-according to IEC65/IEC950/IEC335 (SEMKO and DEMKO pending).
BSI	Certification according to BS 415:1990, BS EN60950:1992 (BS 7002:1992), and EN41003:1993 for class II applications.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Clearance (External Air Gap)	L (IO1)	9.6	mm	Measured from input terminals to output terminals, through air, shortest distance
Minimum External Creepage (External Tracking Path)	L (IO2)	10.0	mm	Measured from input terminals to output terminals, along body of optocoupler, shortest distance
Minimum Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance, conductor to conductor, emitter to detector
Minimum Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from emitter to detector, along internal cavity wall
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group DIN VDE 0110

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/01.89, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/01.89)		2	
Maximum Working Insulation Voltage	V_{IOWM}	1414	V_{PEAK}
	V_{IORM}	1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.875 x V_{IORM}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V_{PEAK}
		1875	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.5 x V_{IORM}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V_{PEAK}
		1500	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature Current (Input Current I_F, P_S = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7,6,5 = ground)	 T_S I_S $P_{S, OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_{IO}	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the HP Optoelectronics Designer's Catalog, under Product Safety Regulations Section, (VDE 0884) for a detailed description.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Ambient Operating Temperature ..... -55°C to +85°C
Reflow Temperature Profile ..... See Temperature Profile (page 3)
Lead Solder Temperature (up to seating plane) ..... 260°C for 10 s
Average Input Current - I_F ..... 25 mA
Peak Input Current I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current I_F ..... 100 mA
(< 1 µs pulse width, 300 pps)
Reverse Input Voltage - V_R (Pin 3-2) ..... 3 V
Input Power Dissipation ..... 40 mW
Average Output Current I_O (Pin 6) ..... 8 mA
Peak Output Current ..... 16 mA
Output Voltage - V_O (Pin 6-5) ..... -0.5 V to 20 V
Supply Voltage - V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Output Power Dissipation ..... 100 mW

DC Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 7.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	23	29	60	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA	1,2,4	1
		19	31	63			V_O = 0.5 V	V_{CC} = 4.5 V		
Current Transfer Ratio	CTR	25	33	65	%	T_A = 25°C	V_O = 0.4 V	I_F = 12 mA	1,2,4	1
		21	35	68			V_O = 0.5 V	V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}		0.2	0.4	V	T_A = 25°C	I_O = 3.6 mA	I_F = 16 mA		
			0.2	0.5			I_O = 3.0 mA	V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	5	
			0.01	1.0		T_A = 25°C	V_O = V_{CC} = 15 V			
				50						
Logic Low Supply Current	I_{CCL}		50	200	µA	I_F = 16 mA, V_{CC} = 15 V, V_O = open				
Logic High Supply Current	I_{CCH}		0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_{CC} = 15 V, V_O = open			
			0.02	2						
Input Forward Voltage	V_F	1.45	1.59	1.85	V	T_A = 25°C	I_F = 16 mA		3	
		1.35		1.95						
Input Reverse Breakdown Voltage	BV_R	3			V	I_R = 100 µA, T_A = 25°C				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.4		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}		70		pF	f = 1 Mhz, V_F = 0 V				
Input-Output Insulation Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min, T_A = 25°C				2, 8
Resistance (Input-Output)	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 V_{dc}			2
		10^{11}				T_A = 100°C				
Capacitance (Input-Output)	C_{I-O}		0.5	0.6	pF	f = 1 MHz				2

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz Duty Cycle = 10% I_F = 16 mA V_{CC} = 5.0 V R_L = 1.9 kΩ C_L = 15 pF V_{THHL} = 1.5 V	6, 8, 9	5
			0.2	0.5					
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50% I_F = 12 mA V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF V_{THHL} = 1.5 V	6, 10-14	6
		0.1	0.5	1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}		0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz Duty Cycle = 10% I_F = 16 mA V_{CC} = 5.0 V R_L = 1.9 kΩ C_L = 15 pF V_{THLH} = 1.5 V	6, 8, 9	5
			0.3	0.7					
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50% I_F = 12 mA V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF V_{THLH} = 2.0 V	6, 10-14	6
		0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50% I_F = 12 mA V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF V_{THHL} = 1.5 V V_{THLH} = 2.0 V	6, 10-14	9
		-0.7	0.3	1.3					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V R_L = 1.9 kΩ C_L = 15 pF I_F = 0 mA	7	3, 5
		15	30			V_{CM} = 1500 V_{p-p}	V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF I_F = 0 mA	7	4, 6
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V R_L = 1.9 kΩ C_L = 15 pF I_F = 16 mA	7	3, 5
		10	30			V_{CM} = 1500 V_{p-p}	V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF I_F = 12 mA	7	4, 6
		15	30				V_{CC} = 15.0 V R_L = 20 kΩ C_L = 100 pF I_F = 16 mA	7	4, 6

*All typicals at T_A = 25°C.

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O), to the forward LED input current (I_F), times 100.
2. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
3. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
4. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0$ V).
5. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and a 5.6 kΩ pull-up resistor.
6. The R_L=15 kΩ, C_L=100 pF load represents an IPM (Intelligent Power Module) load.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Characteristics Table.
9. The difference between t_{PLH} and t_{PHL} between any two CNW4504 parts under the same operating condition. (See Power Inverter Dead Time and Propagation Delay Specifications section).

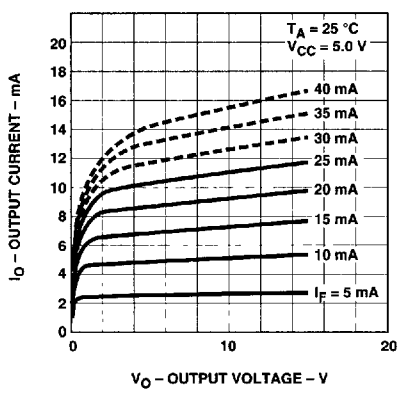


Figure 1. DC and Pulsed Transfer Characteristics.

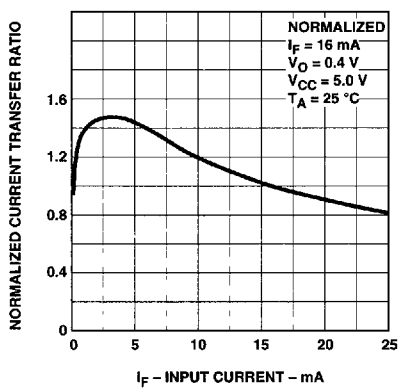


Figure 2. Current Transfer Ratio vs. Input Current.

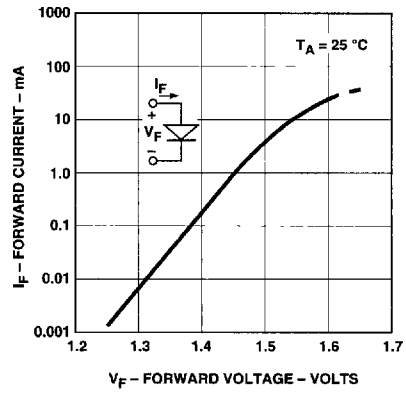


Figure 3. Input Current vs. Forward Voltage.

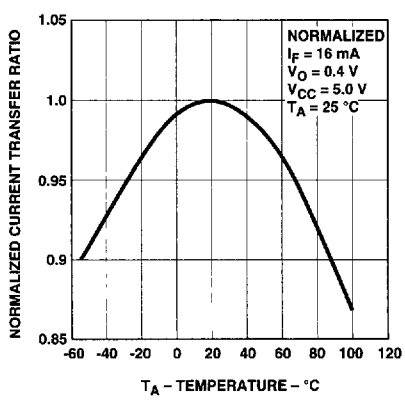


Figure 4. Current Transfer Ratio vs. Temperature.

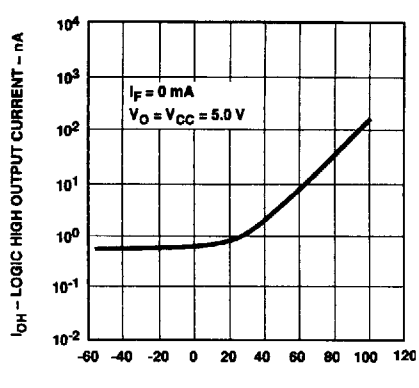


Figure 5. Logic High Output Current vs. Temperature.

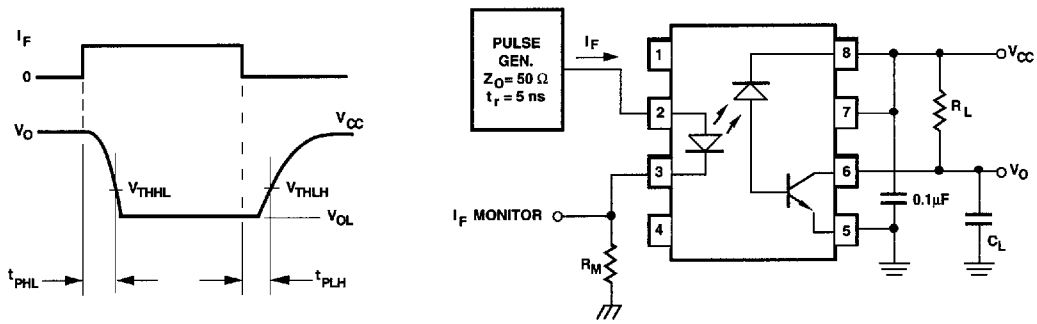


Figure 6. Switching Test Circuit.*

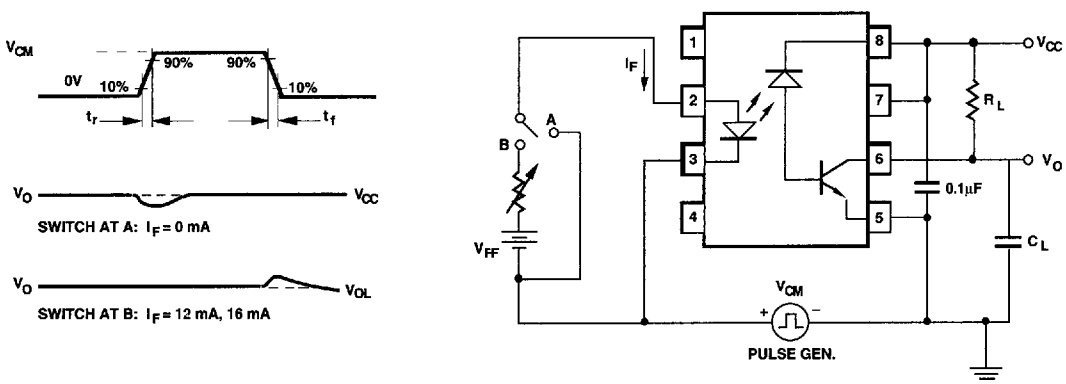


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

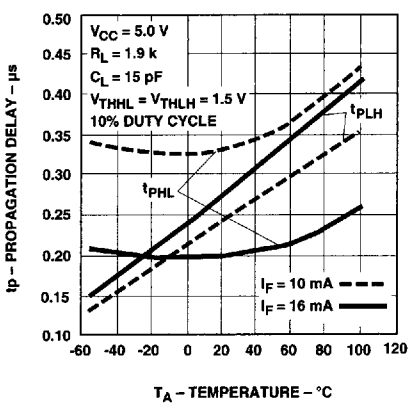


Figure 8. Propagation Delay Time vs. Temperature.

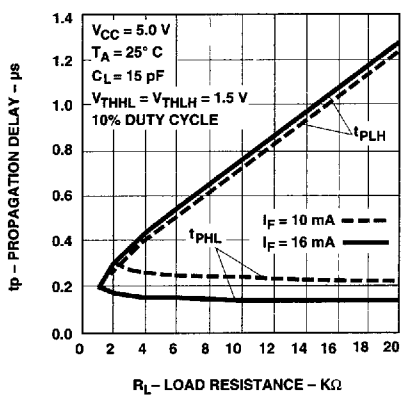


Figure 9. Propagation Delay Time vs. Load Resistance.

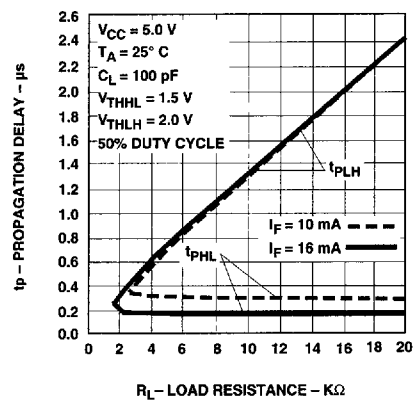


Figure 10. Propagation Delay Time vs. Load Resistance.

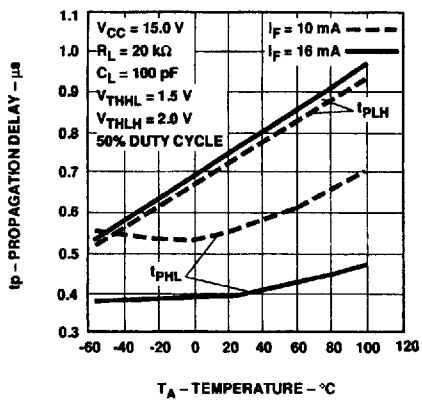


Figure 11. Propagation Delay Time vs. Temperature.

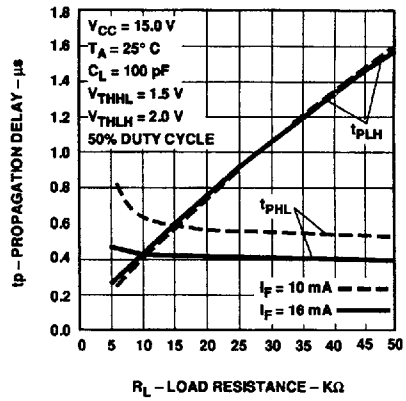


Figure 12. Propagation Delay Time vs. Load Resistance.

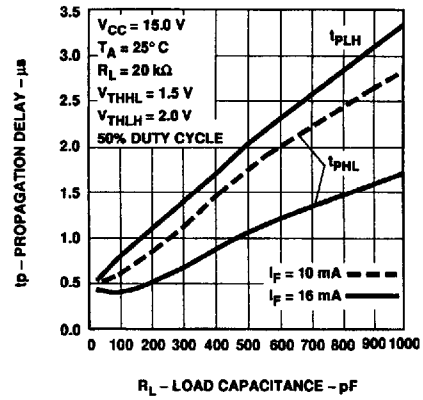


Figure 13. Propagation Delay Time vs. Load Capacitance.

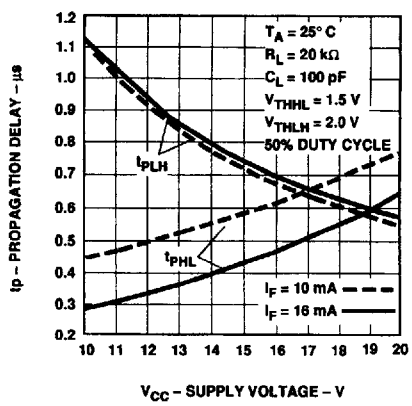


Figure 14. Propagation Delay Time vs. Supply Voltage.

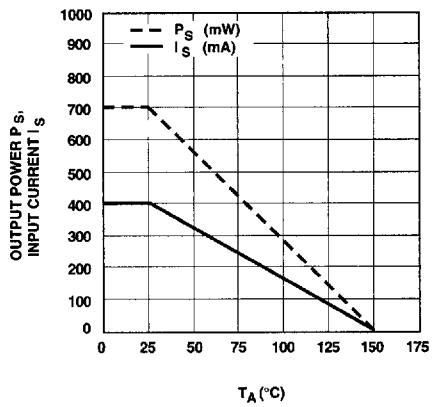


Figure 15. Dependence of Safety Maximum Ratings with Ambient Temperature.

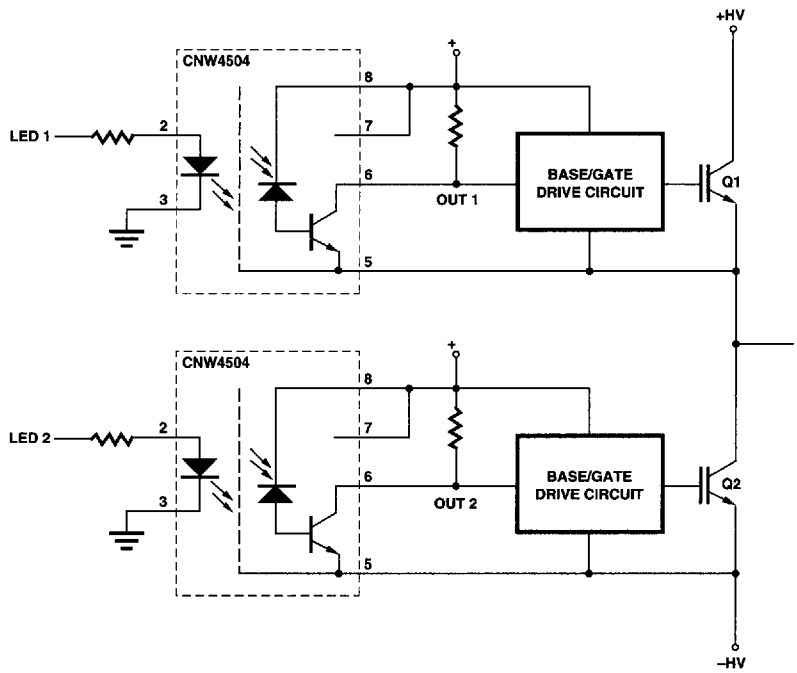


Figure 16. Typical Power Inverter.

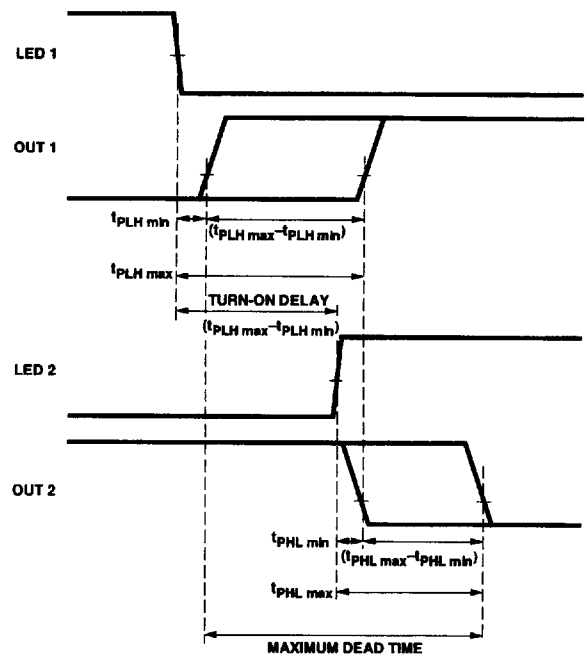


Figure 17. LED Delay and Dead Time Diagram.

Power Inverter Dead Time and Propagation Delay Specifications

The CNW4504 includes a specification intended to help designers minimize "dead time" in their power inverter designs. The new "propagation delay difference" specification (t_{PLH} - t_{PHL}) is useful for determining not only how much optocoupler switching delay is needed to prevent "shoot-through" current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 16), it is essential that they never conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled "LED1", "LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) will never turn on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than (t_{PLHmax} - t_{PHLmin}), which also happens to be the maximum data sheet value for the propagation delay difference specification, (t_{PLH} - t_{PHL}). The CNW4504 specifies a maximum (t_{PLH} - t_{PHL}) of 1.3 µs over an operating temperature range of 0-70°C.

Although $(t_{PLH}-t_{PHL})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PLH} - t_{PHL})_{max}$, the minimum dead time is zero (i.e., there is zero time between the turn-off of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PLH} - t_{PHL})_{max}$, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turn-off delay,

$$[(t_{PLHmax}-t_{PLHmin})+(t_{PHLmax}-t_{PHLmin})].$$

This expression can be rearranged to obtain

$$[(t_{PLHmax}-t_{PHLmin})-(t_{PHLmin}-t_{PHLmax})],$$

and further rearranged to obtain

$$[(t_{PLH}-t_{PHL})_{max}-(t_{PLH}-t_{PHL})_{min}],$$

which is the maximum minus the minimum data sheet values of (t_{PLH}-t_{PHL}). The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not

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just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The CNW4504 specifies a minimum (t_{PLH} - t_{PHL}) of -0.7 µs over an operating temperature range of 0-70°C, resulting in a maximum dead time of 2.0 µs when the LED turn-on delay is equal to $(t_{PLH}-t_{PHL})_{max}$, or 1.3 µs.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PLH} - t_{PHL})_{max}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.

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