TelCom Semiconductor, Inc.

MICROPROCESSOR MONITOR

FEATURES

- **Precision Voltage Monitor ..... Adjustable +4.5V or +4.75V**
- **Reset Pulse Width ..... 250msec Min**
- **No External Components**
- **Adjustable Watchdog Timer ..... 150msec, 600msec or 1.2sec**
- **Debounced Manual Reset Input for External Override**

APPLICATIONS

- **Computers**
- **Controllers**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical µP Power Monitoring**

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1232COA	8-Pin SOIC	0°C to +70°C
TC1232COE	16-Pin SOIC (Wide)	0°C to +70°C
TC1232CPA	8-Pin PDIP	0°C to +70°C
TC1232EOA	8-Pin SOIC	– 40°C to +85°C
TC1232EOE	16-Pin SOIC (Wide)	– 40°C to +85°C
TC1232EPA	8-Pin PDIP	– 40°C to +85°C

GENERAL DESCRIPTION

The TC1232 is a fully-integrated processor supervisor. It provides three important functions to safeguard processor sanity: precision power on/off reset control, watchdog timer and external reset override.

On power-up, the TC1232 holds the processor in the reset state for a minimum of 250msec after V_{CC} is within tolerance to ensure a stable system start-up.

Microprocessor sanity is monitored by the on-board watchdog circuit. The microprocessor must provide a periodic low-going signal on the $\overline{ST}$ input. Should the processor fail to supply this signal within the selected time-out period (150msec, 600msec or 1200msec), an out-of-control processor is indicated and the TC1232 issues a processor reset as a result.

The outputs of the TC1232 are immediately driven active when the PB input is brought low by an external push-button switch or other electronic signal. When connected to a push-button switch, the TC1232 provides contact debounce.

The TC1232 is packaged in a space-saving 8-pin plastic DIP or SOIC package and requires no external components.

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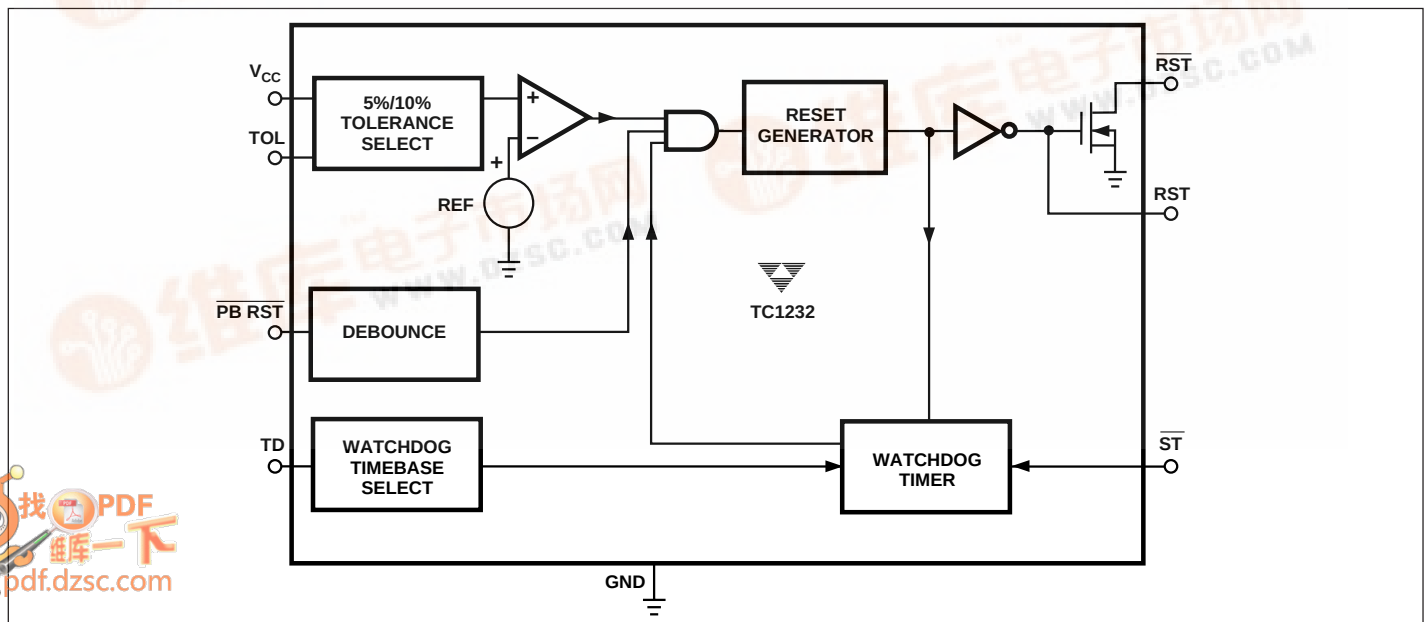
FUNCTIONAL BLOCK DIAGRAM



TC1232

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin (With Respect to GND) – 0.3V to +5.8V
Operating Temperature Range:
TC1232C ..... 0°C to +70°C
TC1232E ..... – 40°C to + 85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS: $T_A = T_{MIN}$ to $T_{MAX;}$ V_{CC} = +4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level	Note 1	2.0	—	V_{CC} +0.3	V
V_{IL}	$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level		– 0.3	—	+0.8	V
I_L	Input Leakage $\overline{ST}$, TOL		– 1.0	—	+1.0	µA
I_{OH}	Output Current RST	V_{OH} = 2.4V	– 1.0	–12	—	mA
I_{OL}	Current RST, $\overline{RST}$	V_{OL} = 0.4V	2.0	10	—	mA
I_{CC}	Operating Current	Note 2	—	50	200	µA
V_{CCTP}	V_{CC} 5% Trip Point (Note 3)	TOL = GND	4.50	4.62	4.74	V
V_{CCTP}	V_{CC} 10% Trip Point (Note 3)	TOL = V_{CC}	4.25	4.37	4.49	V

CAPACITANCE (Note 4): T_A = +25°C

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance $\overline{ST}$, TOL		—	—	5	pF
C_{OUT}	Output Capacitance RST, $\overline{RST}$		—	—	7	pF

AC ELECTRICAL CHARACTERISTICS: $T_A = T_{MIN}$ to $T_{MAX;}$ V_{CC} = +5V to ±10%, unless otherwise specified.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
t_{PB}	$\overline{PB\ RST}$ (Note 5)	Figure 3	20	—	—	msec
t_{PBD}	$\overline{PB\ RST}$ Delay	Figure 3	1	4	20	msec
t_{RST}	Reset Active Time		250	610	1000	msec
t_{ST}	$\overline{ST}$ Pulse Width	Figure 4	75	—	—	nsec
t_{TD}	$\overline{ST}$ Time-out Period	Figure 4				
		TD Pin = 0V	62.5	150	250	msec
		TD Pin = Open	250	600	1000	msec
		TD Pin = V_{CC}	500	1200	2000	msec
t_F	V_{CC} Fall Time (Note 4)	Figure 5	10	—	—	µsec

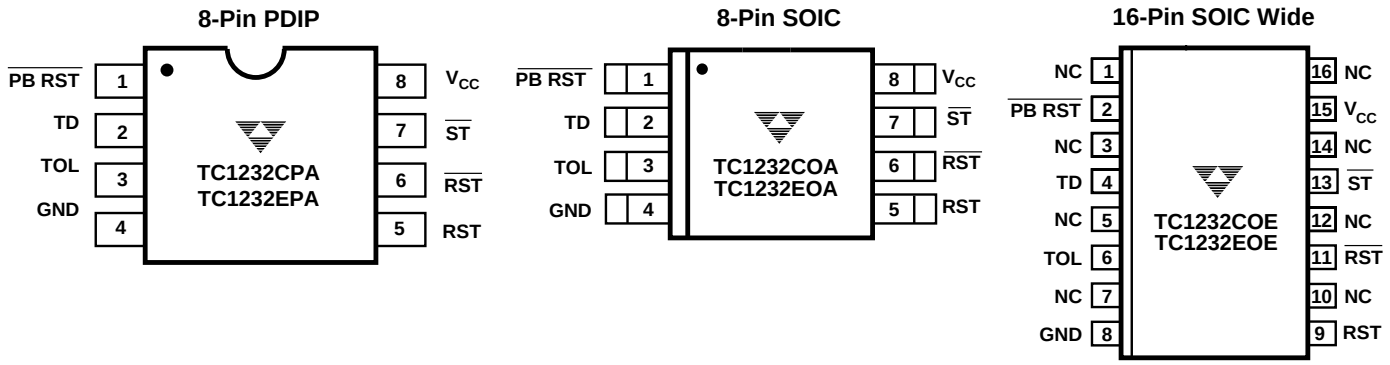
AC ELECTRICAL CHARACTERISTICS: (Cont.)

$T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +5V to ±10%, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_R	V_{CC} Rise Time (Note 4)	Figure 6	0	—	—	µsec
t_{RPD}	V_{CC} Detect to RST High and RST Low	Figure 7, V_{CC} Falling	—	—	100	nsec
t_{RPU}	V_{CC} Detect to RST High and $\overline{RST}$ Open (Note 6)	Figure 8, V_{CC} Rising	250	610	1000	msec

NOTES: 1. $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40kΩ.
2. Measured with outputs open.
3. All voltages referenced to GND.
4. Guaranteed by design.
5. $\overline{PB\ RST}$ must be held low for a minimum of 20msec to guarantee a reset.
6. t_R = 5µsec.

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin No. (8-Pin PDIP)	Pin No. (8-Pin SOIC)	Pin No. (16-Pin SOIC)	Symbol	Description
1	1	2	$\overline{PB\ RST}$	Push-button Reset Input. A debounced active-low input that ignores pulses less than 1msec in duration and is guaranteed to recognize inputs of 20msec or greater.
2	2	4	TD	Time Delay Set. The watchdog time-out select input (t_{TD} = 150msec for TD = 0V, t_{TD} = 600msec for TD = open, t_{TD} = 1.2sec for TD = V_{CC}).
3	3	6	TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
4	4	8	GND	Ground.
5	5	9	RST	Reset Output (Active High) - goes active: 1. If V_{CC} falls below the selected reset voltage threshold 2. If $\overline{PB\ RST}$ is forced low 3. If $\overline{ST}$ is not strobed within the minimum time-out period 4. During power-up
6	6	11	$\overline{RST}$	Reset Output (Active Low, Open Drain) - see RST.
7	7	13	$\overline{ST}$	Strobe Input. Input for watchdog timer.
8	8	15	V_{CC}	The +5V Power-Supply Input.
		1, 3, 5, 7, 10, 12, 14, 16	NC	No Internal Connection.

DETAILED DESCRIPTION

Power Monitor

The TC1232 detects out-of-tolerance power supply conditions and warns a processor-based system of an impending power failure. When V_{CC} is detected as below the preset level defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. If TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. If TOL is connected to V_{CC}, the RST and $\overline{RST}$ become active as V_{CC} falls below 4.5 volts. Because the processing is stopped at the last possible moment of valid $V_{CC,}$ the RST and $\overline{RST}$ are excellent control signals for a µP. The reset outputs will remain in their active states until V_{CC} has been continuously in-tolerance for a minimum of 250msec allowing the power supply and µP to stabilize before $\overline{RST}$ is released.

Push-button Reset Input

The debounced manual reset input ($\overline{PB\ RST}$) manually forces the reset outputs into their active states. Once $\overline{PB\ RST}$ has been low for a time $t_{PBD,}$ the push-button delay time, the reset outputs go active. The reset outputs remain in their active states for a minimum of 250msec after $\overline{PB\ RST}$ rises above V_{IH} (Figure 3).

A mechanical push-button or active logic signal can drive the $\overline{PB\ RST}$ input. The debounced input ignores input pulses less than 1msec and is guaranteed to recognize pulses of 20msec or greater. No external pull-up resistor is required because the $\overline{PB\ RST}$ input has an internal pull-up to V_{CC} of approximately 100µA.

Watchdog Timer

When the $\overline{ST}$ input is not stimulated for a preset time period, the watchdog timer function forces RST and $\overline{RST}$ signals to the active state. The preset time period is determined by the $\overline{TD}$ inputs to be 150msec with TD connected to ground, 600msec with TD floating, or 1200msec with TD connected to $V_{CC,}$ typical. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250msec minimum (Figure 2).

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that is executed frequently enough so the time between toggles is less than the watchdog time-out period. One common technique controls the µP I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

Supply Monitor Noise Sensitivity

The TC1232 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays), may require a 0.01µF or 0.1µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC1232 as possible to keep the capacitor lead length short.

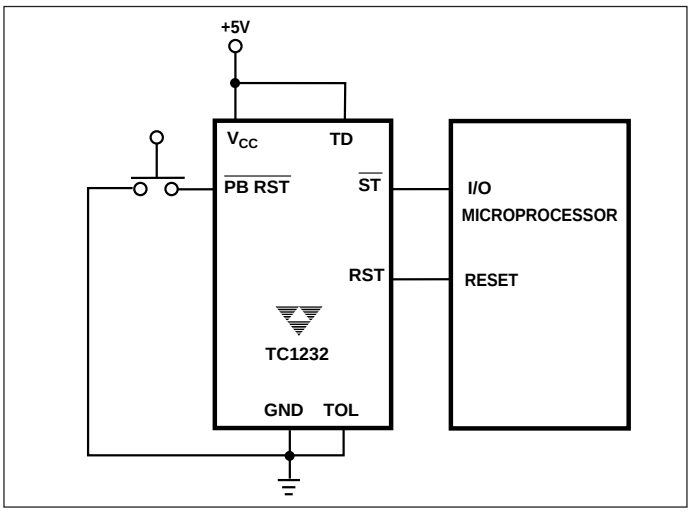


Figure 1. Push-button Reset

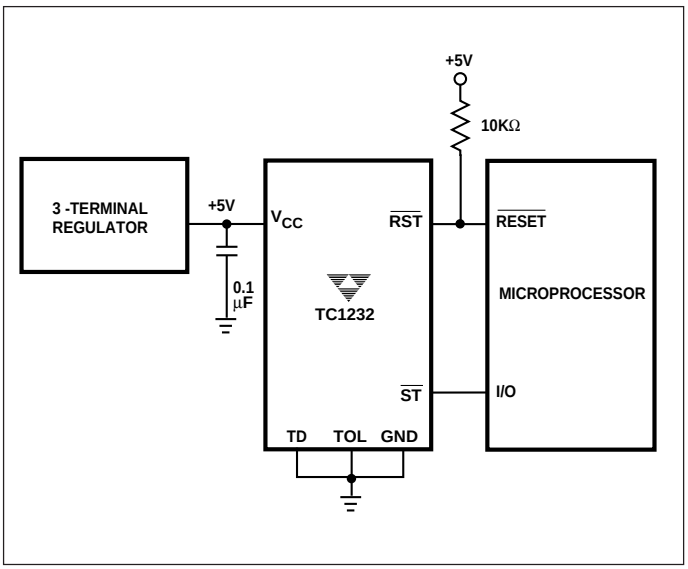


Figure 2. Watchdog Timer

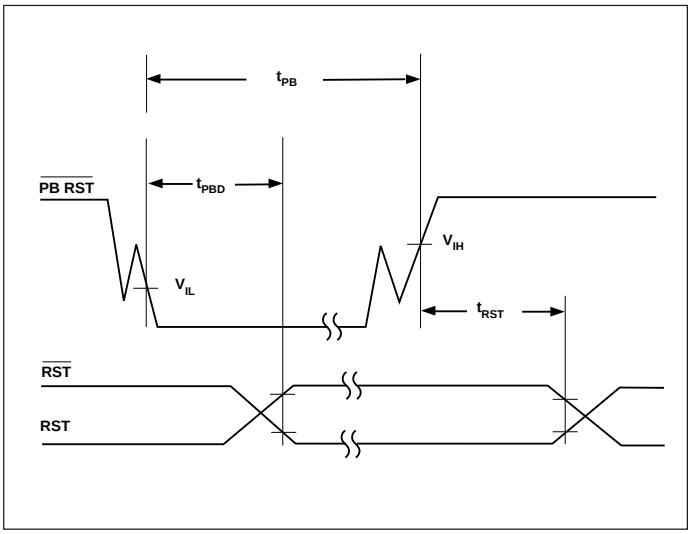


Figure 3. Push-button Reset. The debounced $\overline{PB\ RST}$ input ignores input pulses less than 1msec and is guaranteed to recognize pulses of 20msec or greater

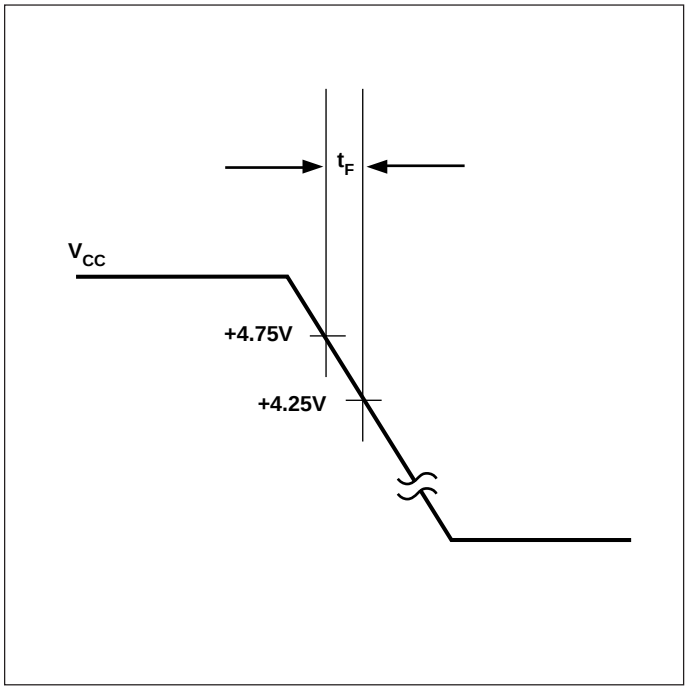
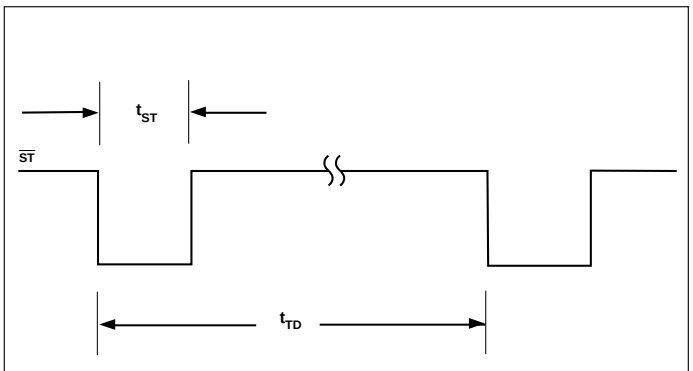


Figure 5. Power-Down Slew Rate

PUSH-BUTTON RESET



NOTE: t_{TD} IS THE MAXIMUM ELAPSED TIME BETWEEN $\overline{ST}$ HIGH-TO-LOW TRANSITIONS ($\overline{ST}$ IS ACTIVATED BY FALLING EDGES ONLY) WHICH WILL KEEP THE WATCHDOG TIMER FROM FORCING THE RESET OUTPUTS ACTIVE FOR A TIME OF t_{RST}. t_{TD} IS A FUNCTION OF THE VOLTAGE AT THE TD PIN, AS TABULATED BELOW.

	t_{TD}		
CONDITON	MIN	TYP	MAX
TD PIN = 0V	62.5msec	150msec	250msec
TD PIN = OPEN	250msec	600msec	1000msec
TD PIN = V_{CC}	500msec	1200msec	2000msec

Figure 4. Strobe Input

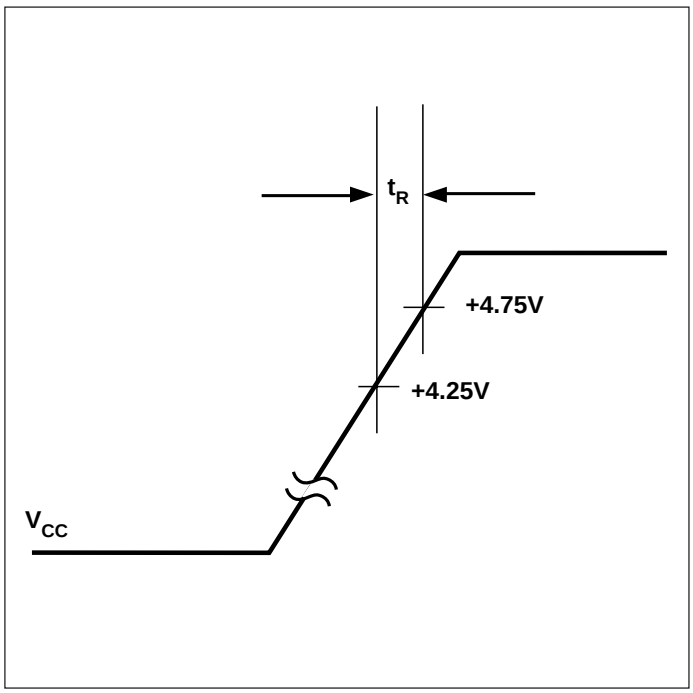


Figure 6. Power-Up Slew Rate

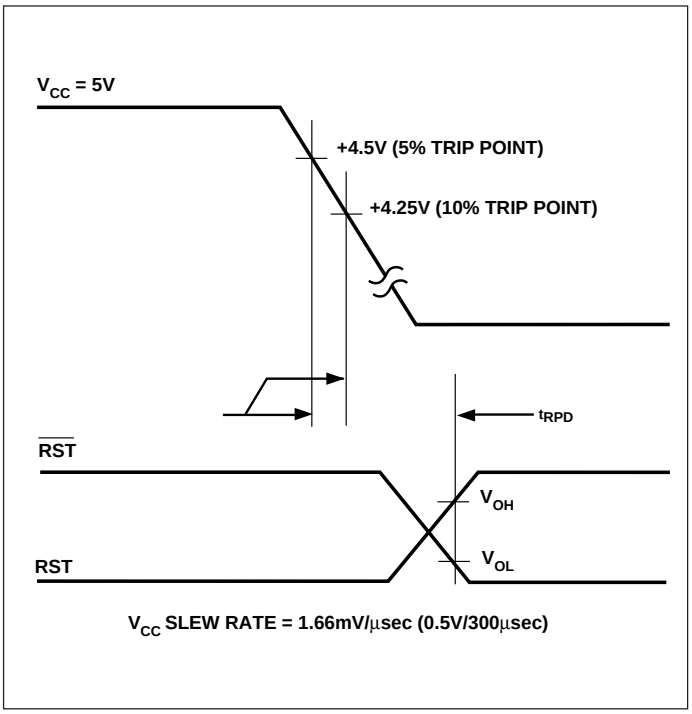


Figure 7. V_{CC} Detect Reset Output Delay (Power-Down)

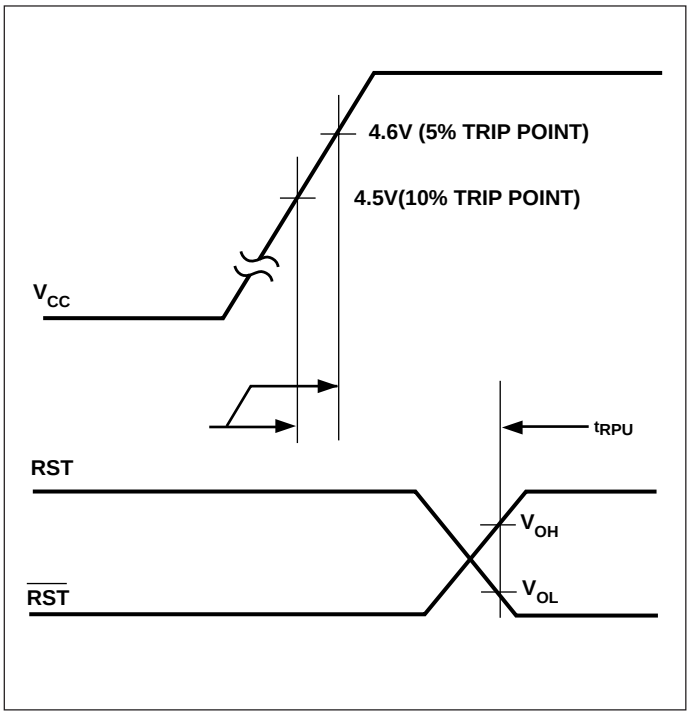


Figure 8. V_{CC} Detect Reset Output Delay (Power-Up)