

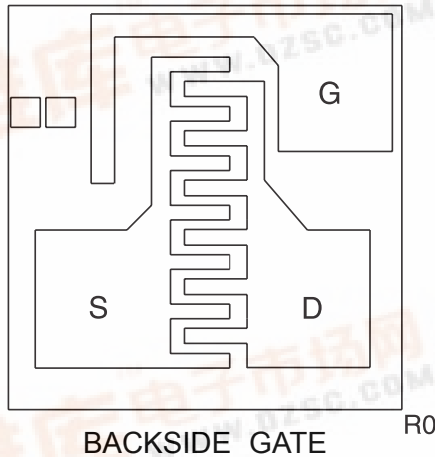
查询CP210供应商
PROCESS CP210
Small Signal Transistors
N - Channel Silicon Amplifer J FET Chip

捷多邦, 专业PCB打样工厂, 24小时加急出货™
Central
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Area	3.2 X 4.0 MILS
Source Bonding Pad Area	3.2 X 4.0 MILS
Gate Bonding Pad Area	3.2 X 4.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 6,000Å

GEOMETRY

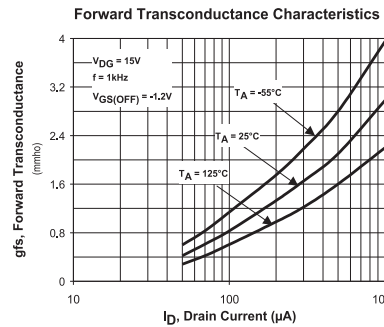
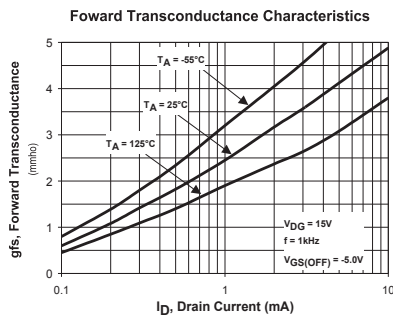
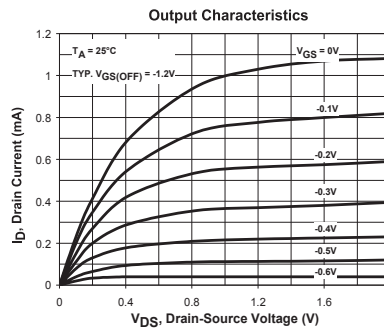
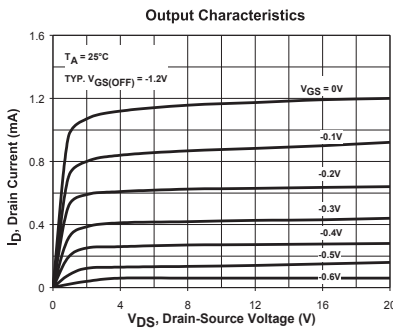
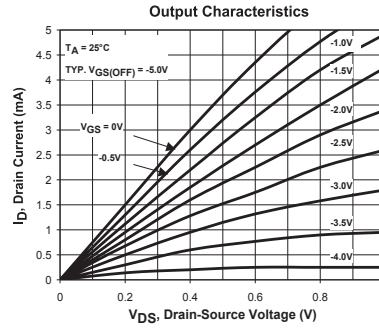
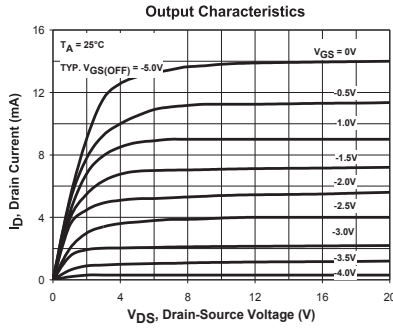


GROSS DIE PER 4 INCH WAFER
53,730

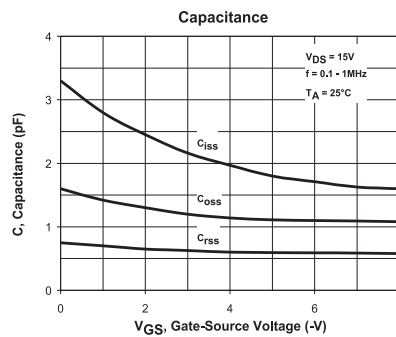
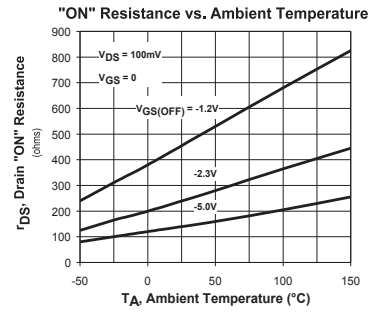
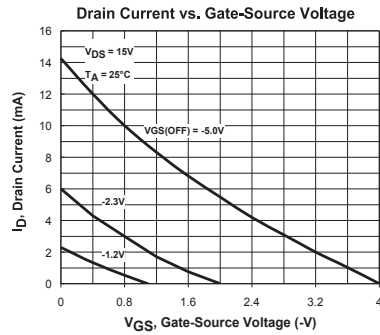
PRINCIPAL DEVICE TYPES
2N4416A
CMPF4416A

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R3 (9 -September 2003)



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