

PROCESS **CP709**
Power Transistor
PNP - Low Saturation Transistor Chip

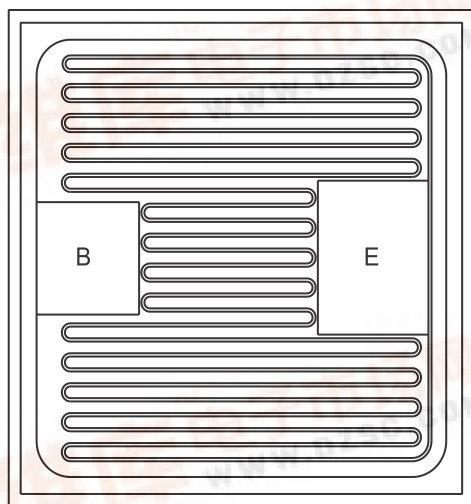
捷多邦，专业PCB打样工厂，24小时加急出货™

Central
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	41.3 x 41.3 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	9.5 x 9.2 MILS
Emitter Bonding Pad Area	12.8 x 10.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

R0

GROSS DIE PER 4 INCH WAFER

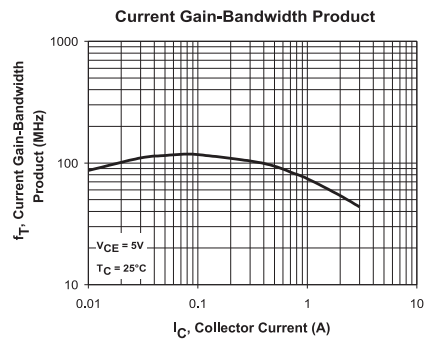
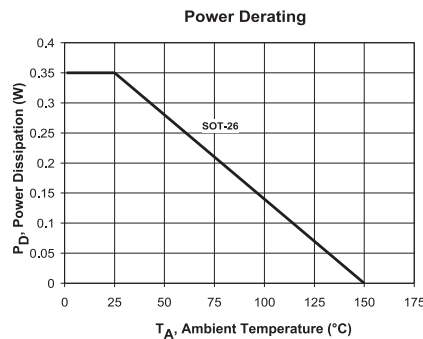
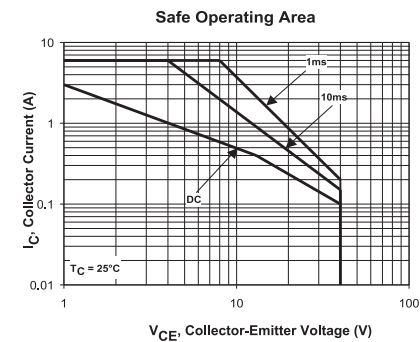
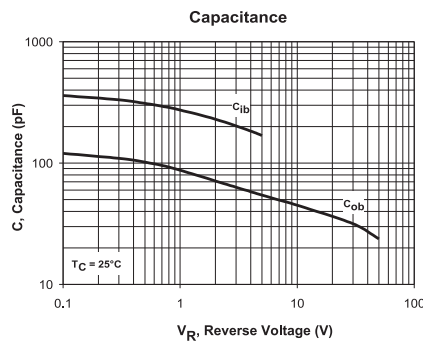
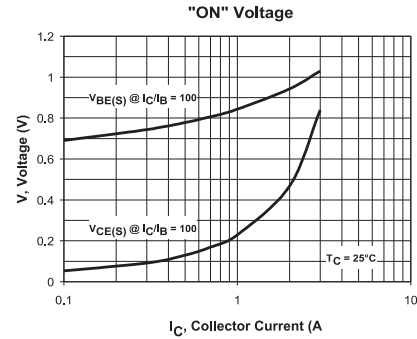
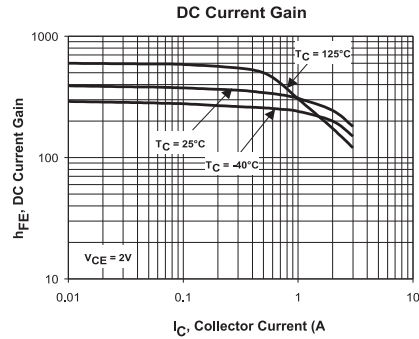
6,670

PRINCIPAL DEVICE TYPES

CMPT7090L
CXT7090L
CZT7090L
CMXT7090L

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R2 (12- September 2003)



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