19-1162; Rev 0; 12/96

MAXIM

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

General Description

The MAX4530/MAX4531/MAX4532 are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (mux) (MAX4530), two 4-channel muxes (MAX4531), and three single-pole/double-throw switches (MAX4532). These devices are pin compatible with the industry-standard 74HC4351/74HC4352/74HC4353. All devices have two complementary switch-enable inputs and address latching.

The MAX4530/MAX4531/MAX4532 operate from a single supply of +2V to +12V, or from dual supplies of ±2V to ±6V. On-resistance (150Ω max) is matched between switches to 8Ω max. Each switch can handle rail-to-rail analog signals. Off-leakage current is only 1nA at T_A = +25°C and 50nA at T_A = +85°C.

All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
Networking
ATE Equipment
Audio-Signal Routing

Features

- **Pin Compatible with 74HC4351/74HC4352/74HC4353**
- **±2.0V to ±6V Dual Supplies +2.0V to +12V Single Supply**
- **75Ω Signal Paths with ±5V Supplies 150Ω Signal Paths with +5V Supply**
- **Rail-to-Rail Signal Handling**
- **t_{ON} and t_{OFF} = 150ns and 120ns at ±4.5V**
- **<1µW Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Small, 20-Pin SSOP/SO/DIP Packages**

Ordering Information

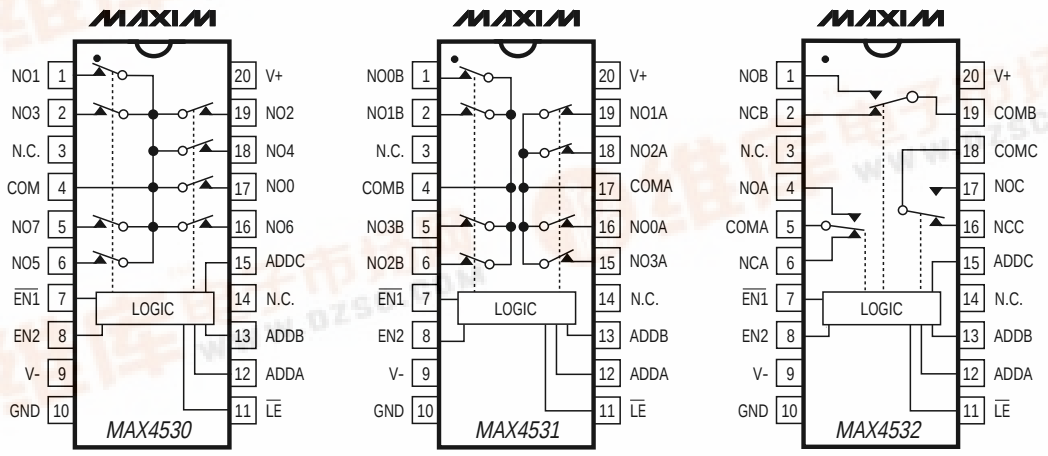
PART	TEMP. RANGE	PIN-PACKAGE
MAX4530CPP	0°C to +70°C	20 Plastic DIP
MAX4530CWP	0°C to +70°C	20 SO
MAX4530CAP	0°C to +70°C	20 SSOP
MAX4530C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

**Contact factory for availability.*

Pin Configurations

TOP VIEW



NARROW DIP/WIDE SO **NARROW DIP/WIDE SO** **NARROW DIP/WIDE SO**

N.C. = NOT CONNECTED

Truth Table appears at end of data sheet.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ .....-0.3 to +13V
Voltage into Any Terminal (Note 1)
or ±20mA (whichever occurs first) .....-0.3 to (V+ + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current, NO, NC, or COM_
(pulsed at 1ms, 10% duty cycle).....±40mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C).....800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX453_C_P .....0°C to +70°C
MAX453_E_P .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{\overline{LE}}$ = 2.4V, $V_{ADD\_L} = V_{EN\_L}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog-Signal Range	V_{COM}, V_{NO}, $V_{NC\_}$	(Note 3)			V-		V+	V
Channel On-Resistance	R_{ON}	I_{NO} = 2mA, V_{COM} = ±3.5V, V+ = +4.5V, V- = -4.5V		T_A = +25°C		45	75	Ω
				$T_A = T_{MIN}$ to T_{MAX}			100	
On-Resistance Matching Between Channels (Note 4)	ΔR_{ON}	I_{NO} = 2mA, V_{COM} = ±4.5V, V+ = +4.5V, V- = -4.5V		T_A = +25°C		1	8	Ω
				$T_A = T_{MIN}$ to T_{MAX}			12	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	I_{NO} = 2mA; V_{COM} = -3V, 0V, +3V; V+ = 5V; V- = -5V		T_A = +25°C		4	10	Ω
				$T_A = T_{MIN}$ to T_{MAX}			13	
NO-Off Leakage Current (Note 6)	$I_{NO(OFF)}$	V_{NO} = ±4.5V, V_{COM} = ∓4.5V, V+ = 5.5V, V- = -5.5V		T_A = +25°C	-1	0.01	1	nA
				$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM-Off Leakage Current (Note 6)	$I_{COM(OFF)}$	V_{COM} = ±4.5V, V_{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4530	T_A = +25°C	-2	0.01	2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
		V_{COM} = ±4.5V, V_{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4531/ MAX4532	T_A = +25°C	-1	0.01	1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	
COM-On Leakage Current (Note 6)	$I_{COM(ON)}$	V_{COM} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX4530	T_A = +25°C	-2	0.01	2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1	0.01	1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Logic High Threshold	V_{ADD_H}, V_{EN_H}, $V_{\overline{LE}}$		$T_A = T_{MIN}$ to T_{MAX}		1.5	2.4	V
Logic Low Threshold	V_{ADD_L}, V_{EN_L}, $V_{\overline{LE}}$		$T_A = T_{MIN}$ to T_{MAX}	0.8	1.5		V
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, $I_{\overline{LE}}$	$V_{ADD\_H} = 2.4V$, $V_{ADD\_L} = 0.8V$		-0.1	0.01	0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, $I_{\overline{LE}}$	$V_{ADD\_H} = 2.4V$, $V_{ADD\_L} = 0.8V$		-0.1		0.1	µA
SUPPLY							
Power-Supply Range	V+, V-			±2.0		±6	V
Positive Supply Current	I+	$V_{EN\_} = V_{ADD\_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	T_A = +25°C	-1	0.001	1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
Negative Supply Current	I-	$V_{EN\_} = V_{ADD\_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	T_A = +25°C	-1	0.001	1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
I_{GND} Supply Current	I_{GND}	$V_{EN\_} = V_{ADD\_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	T_A = +25°C	-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 1	T_A = +25°C		60	150	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3	T_A = +25°C	4	10		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 2	T_A = +25°C		10	150	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 2	T_A = +25°C		40	100	ns
			$T_A = T_{MIN}$ to T_{MAX}			150	
Setup Time, Channel Select to Latch Enable	t_S	Figure 4	T_A = +25°C	50			ns
			$T_A = T_{MIN}$ to T_{MAX}	60			
Hold Time, Latch Enable to Channel Select	t_H	Figure 6	T_A = +25°C	0			ns
			$T_A = T_{MIN}$ to T_{MAX}	0			
Pulse Width, Latch Enable	t_{MPW}	Figure 5	T_A = +25°C	60			ns
			$T_A = T_{MIN}$ to T_{MAX}	70			
Charge Injection (Note 3)	Q	C_L = 1nF, V_{NO} = 0V, Figure 6	T_A = +25°C		1.5	5	pC
Off Isolation (Note 7)	V_{ISO}	V_{EN2} = 0V, R_L = 1kΩ, f = 1MHz	T_A = +25°C		-65		dB
Crosstalk Between Channels	V_{CT}	$V_{\overline{EN1}}$ = 0V, V_{EN2} = 2.4V, f = 1MHz, $V_{GEN} = 1V_{p-p}$, R_L = 1kΩ	T_A = +25°C		-92		dB

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 2)	UNITS
Distortion, THD				T_A = +25°C		0.025		
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		3		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, $V_{EN} = V_{COM}$ = 0V		T_A = +25°C		3		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, $V_{EN2} = V_{COM}$ = 0V	MAX4530	T_A = +25°C		15		pF
			MAX4531			9		
			MAX4532			6		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, $V_{EN1} = V_{COM}$ = 0V, V_{EN2} = 2.4V	MAX4530	T_A = +25°C		26		pF
			MAX4531			20		
			MAX4532			17		

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 2)	UNITS
SWITCH								
Analog Signal Range	V_{COM}, V_{NO}	(Note 3)			0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		80	150	Ω
				$T_A = T_{MIN}$ to T_{MAX}			200	
On-Resistance Matching Between Channels (Notes 3, 4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		2	15	Ω
				$T_A = T_{MIN}$ to T_{MAX}			20	
On-Resistance Flatness	R_{FLAT}	I_{NO} = 1mA; V_{COM} = 3V, 2V, 1V; V+ = 5V		T_A = +25°C		10		Ω
NO-Off Leakage Current (Note 8)	$I_{NO(OFF)}$	V_{NO} = 4.5V; V_{COM} = 4.5V, 1V; V+ = 5.5V		T_A = +25°C	-1		1	nA
				$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM-Off Leakage Current (Note 8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, 1V; V_{NO} = 1V, 4.5V; V+ = 5.5V	MAX4530	T_A = +25°C	-2		2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1		1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	
COM-On Leakage Current (Note 8)	$I_{COM(ON)}$		MAX4530	T_A = +25°C	-2		2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1		1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{ADD_H} = V_{EN_H} = $V_{\overline{LE}}$ = 2.4V, V_{ADD_L} = V_{EN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Logic-High Threshold	V_{ADD_H}, V_{EN_H}, $V_{\overline{LE}}$		T_A = T_{MIN} to T_{MAX}		1.5	2.4	V
Logic-Low Threshold	V_{ADD_L}, V_{EN_L}, $V_{\overline{LE}}$		T_A = T_{MIN} to T_{MAX}	0.8	1.5		V
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, $I_{\overline{LE}}$	V_H = 2.4V, V_L = 0.8V		-0.1		0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, $I_{\overline{LE}}$	V_H = 2.4V, V_L = 0.8V		-0.1		0.1	µA
SUPPLY							
Power-Supply Range				2.0		12	V
Positive Supply Current	I+	$V_{EN\_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
Negative Supply Current	I-	$V_{EN\_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
I_{GND} Supply Current	I_{GND}	$V_{EN\_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 1, V_{NO} = 3V	T_A = +25°C		90	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3 (Note 3)	T_A = +25°C	10	20		ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	Figure 2	T_A = +25°C		100	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	Figure 3	T_A = +25°C		40	100	ns
			T_A = T_{MIN} to T_{MAX}			125	
Set-Up Time, Channel Select to Latch Enable	t_S	Figure 7	T_A = +25°C	50			ns
			T_A = T_{MIN} to T_{MAX}	60			
Hold Time, Latch Enable to Channel Select	t_H	Figure 7	T_A = +25°C	0			ns
			T_A = T_{MIN} to T_{MAX}	0			
Pulse Width, Latch Enable	t_{MPW}	Figure 7	T_A = +25°C	60			ns
			T_A = T_{MIN} to T_{MAX}	70			
Charge Injection (Note 3)	Q	Figure 7, C_L = 1nF, V_{NO} = 0V	T_A = +25°C		1.5	5	pC

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to 3.6V, V- = 0V, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.5V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V, V+ = 2.7V	T_A = +25°C		220	500	Ω
			$T_A = T_{MIN}$ to T_{MAX}			600	
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V, V_{NO1} = 1.5V, V_{NO8} = 0V	T_A = +25°C		150	350	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		150	350	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		60	150	ns
Set-Up Time, Channel Select to Latch Enable)	t_S	Note 3	T_A = +25°C	100			ns
Hold Time, Latch Enable to Channel Select	t_H	Note 3	T_A = +25°C	0			ns
Pulse Width, Latch Enable	t_{MPW}	Note 3	T_A = +25°C	120			ns

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON}(max) - R_{ON}(min)$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

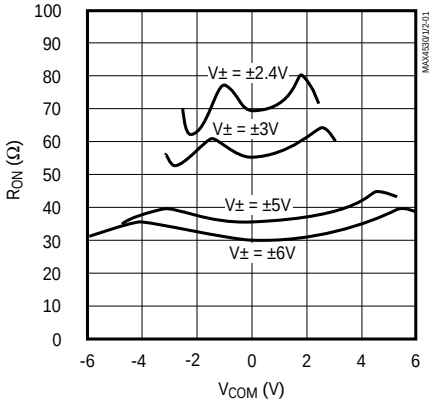
Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM} / V_{NO}, V_{COM} = output, V_{NO} = input to off switch.

Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

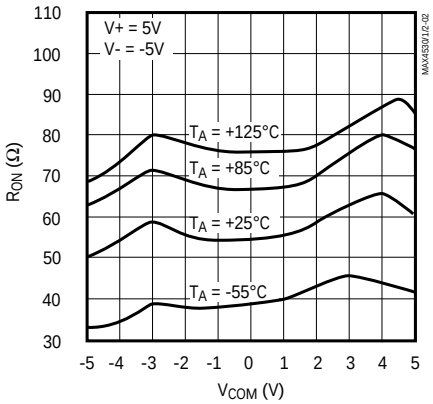
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

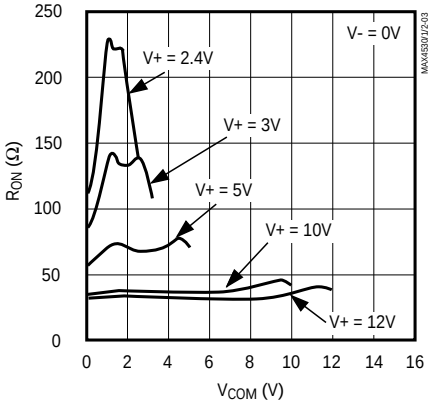
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



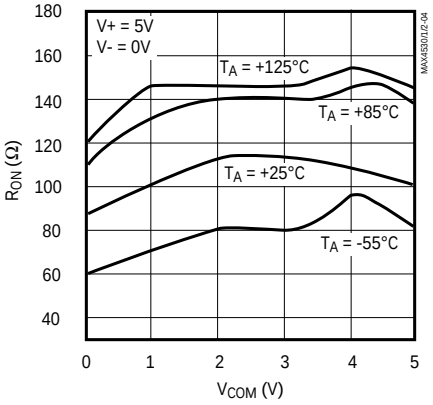
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



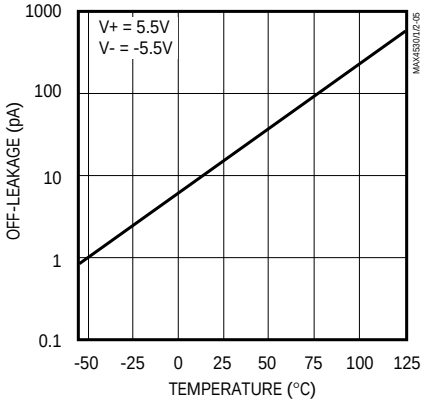
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



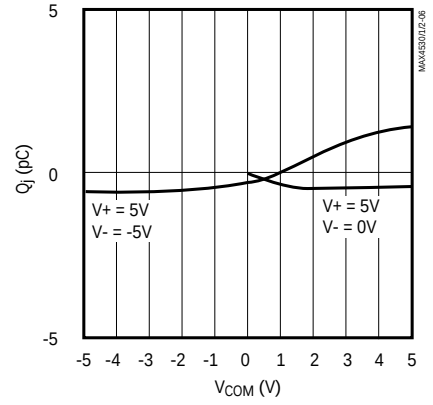
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



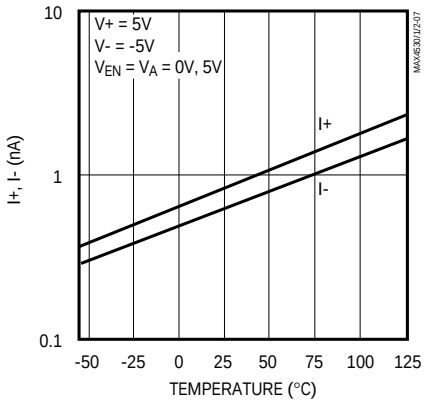
OFF-LEAKAGE vs. TEMPERATURE



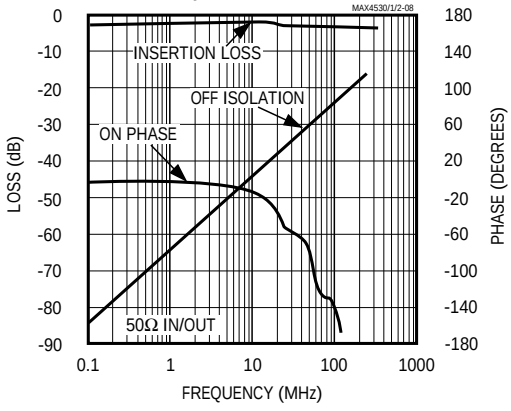
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



FREQUENCY RESPONSE



Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Pin Description

PIN			NAME	FUNCTION
MAX4530	MAX4531	MAX4532		
17, 1, 19, 2, 18, 6, 16, 5	—	—	NO0–NO7	Analog Switch Inputs 0–7
—	1, 2, 6, 5	—	NO0B–NO3B	Analog Switch “B” Inputs 0–3
—	—	1	NOB	Analog Switch “B” Normally Open Input
—	—	2	NCB	Analog Switch “B” Normally Closed Input
3, 14	3, 14	3, 14	N.C.	Not Internally Connected
4	—	—	COM	Analog Switch Common
—	4	19	COMB	Analog Switch “B” Common
—	—	4	NOA	Analog Switch “A” Normally Open Input
—	17	5	COMA	Analog Switch “A” Common
—	—	6	NCA	Analog Switch “A” Normally Closed Input
7	7	7	EN1	Enable Logic Input #1 (see *Truth Table*).
8	8	8	EN2	Enable Logic Input #2 (see *Truth Table*).
9	9	9	V-	Negative Analog Supply Voltage Input. Connect to GND for single supply operation.
10	10	10	GND	Negative Digital Supply Voltage Input. Connect to digital ground. (Analog signals have no ground
11	11	11	LE	Address Latch Logic Input (see *Truth Table*).
12	12	12	ADDA	Address “A” Logic Input (see *Truth Table*).
13	13	13	ADDB	Address “B” Logic Input (see *Truth Table*).
15	—	15	ADDC	Address “C” Logic Input (see *Truth Table*).
—	16, 19, 18, 15	—	NO0A–NO3A	Analog Switch “A” Inputs 0–3
—	—	16	NCC	Analog Switch “C” Normally Closed Input
—	—	17	NOC	Analog Switch “C” Normally Open Input
—	—	18	COMC	Analog Switch “C” Common
20	20	20	V+	Positive Analog and Digital Supply-Voltage Input

NO_, NC_ and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in both directions.

Applications Information

Power-Supply Considerations

Overview

The MAX4530/MAX4531/MAX4532 construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all of the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. For this reason, both sides of a given switch can show leakage currents of either the same or opposite polarity.

The analog-signal paths and GND are not connected.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the analog signals' gates. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ = +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V—above the TTL guaranteed, high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4530/MAX4531/MAX4532 operate with bipolar supplies between ±2.0V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating.

Single Supply

The MAX4530/MAX4531/MAX4532 operate from a single supply between +2V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually work with a single supply at, near, or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

High-Frequency Performance

In 50Ωsystems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -65dB in 50Ωsystems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams

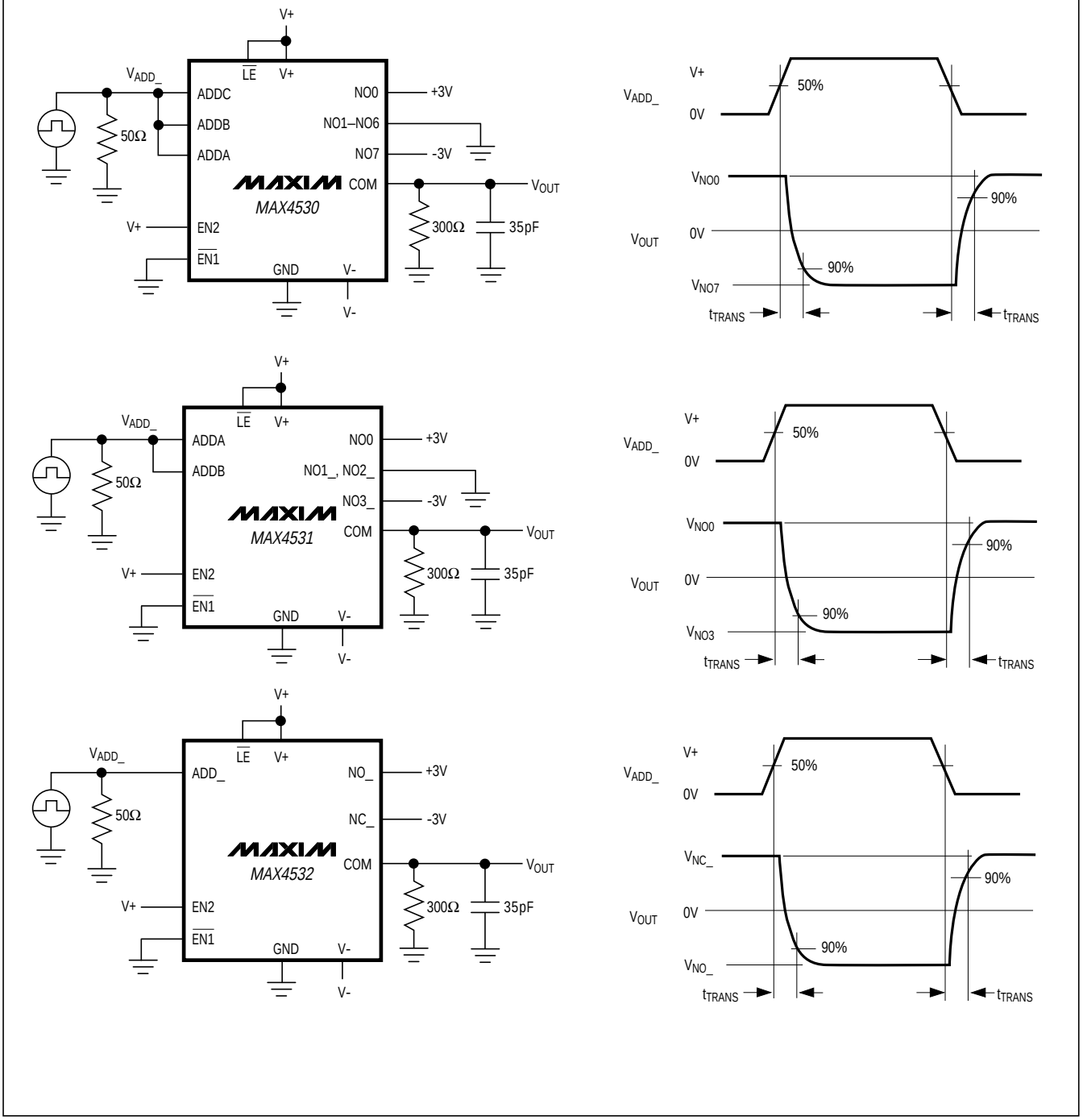


Figure 1. Address Transition Time

Test Circuits/Timing Diagrams (continued)

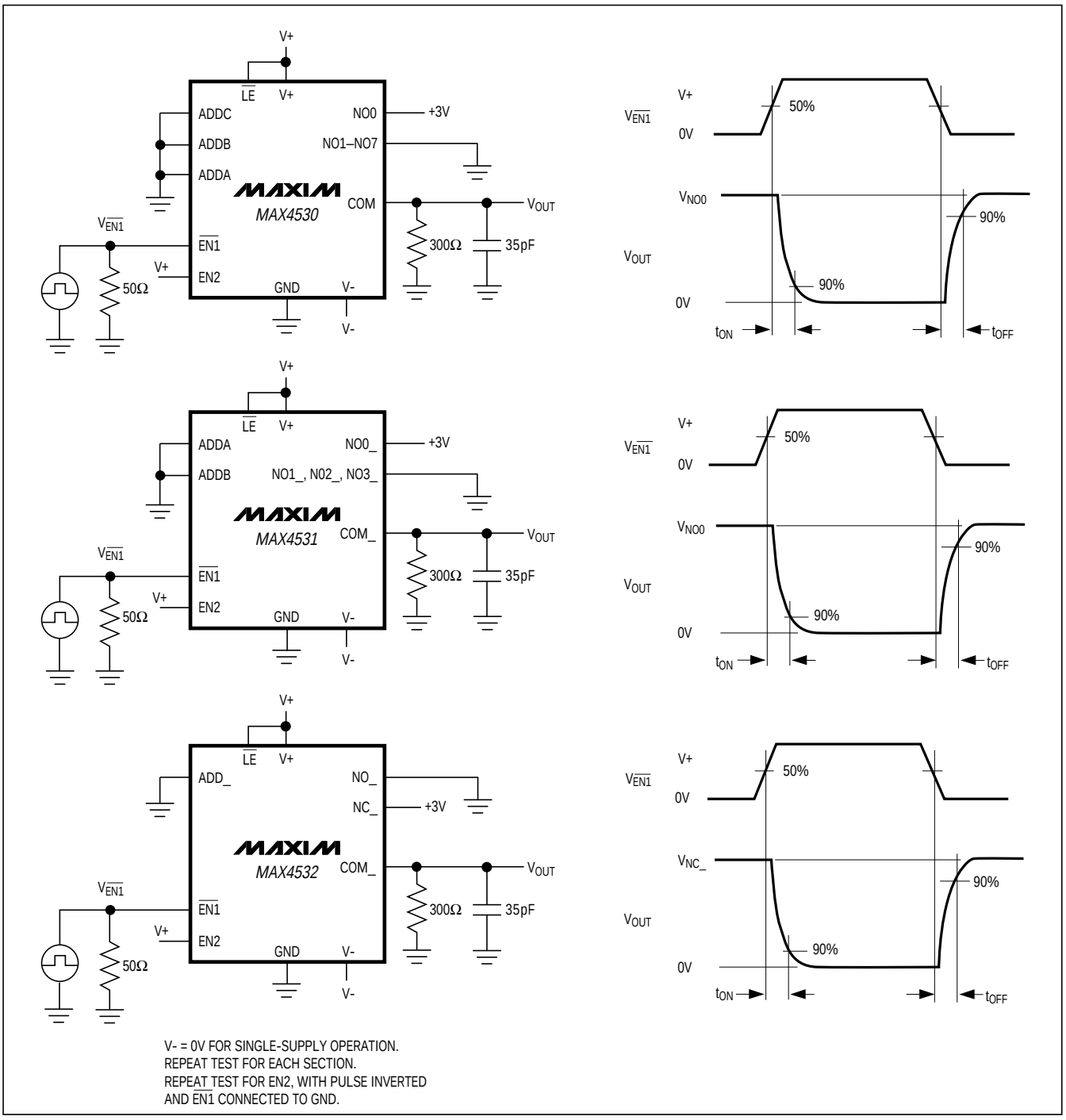


Figure 2. Enable Switching Time

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams (continued)

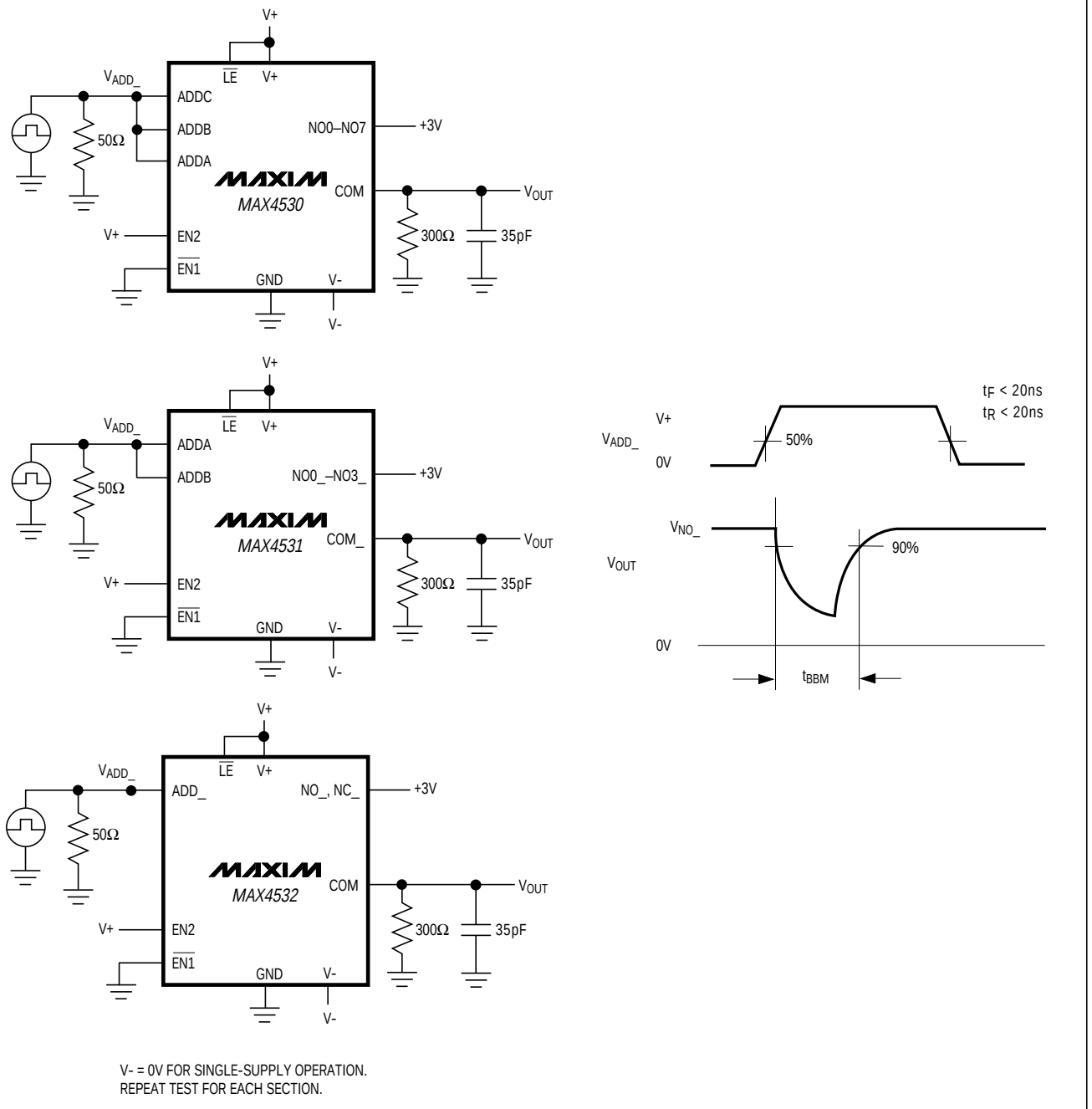


Figure 3. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

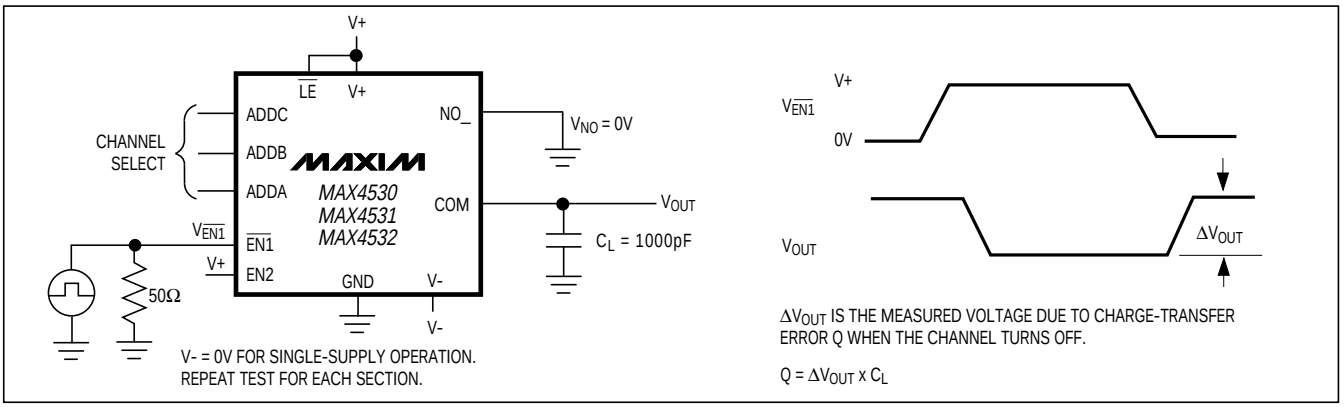


Figure 4. Charge Injection

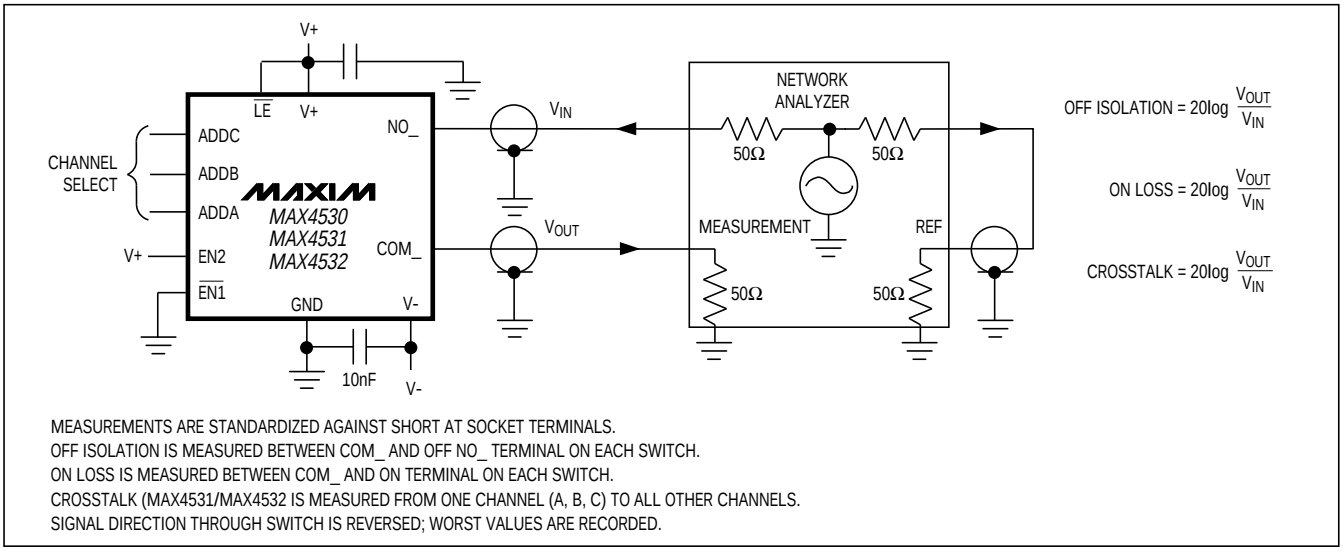


Figure 5. Off Isolation, On Loss, and Crosstalk

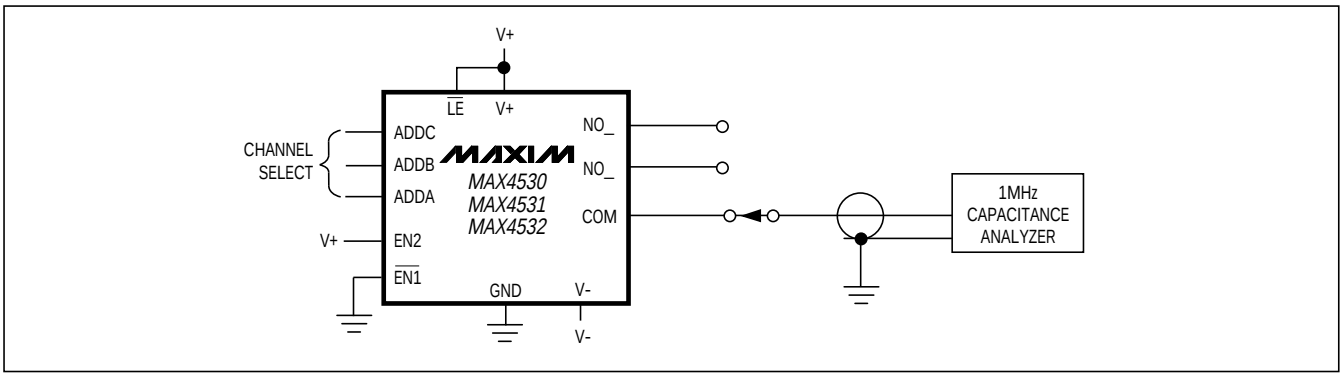
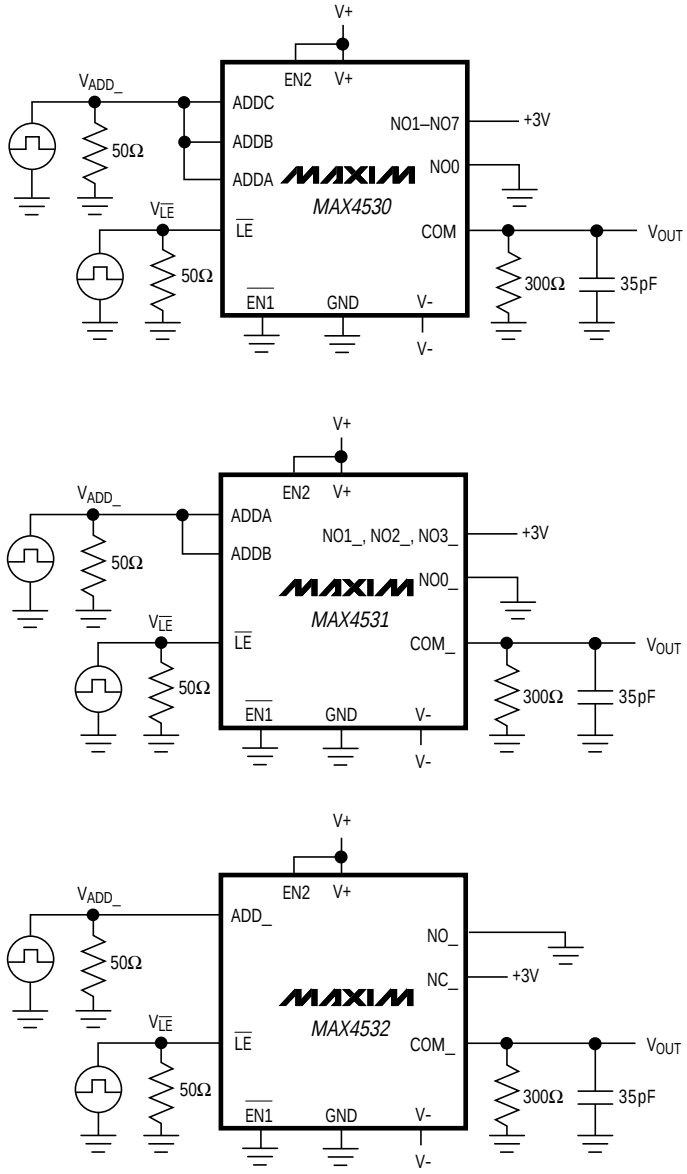
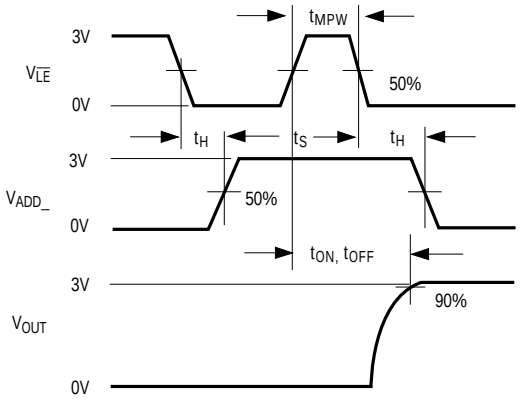


Figure 6. NO/COM Capacitance

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams (continued)





V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 7. Setup and Hold Times, Minimum $\overline{LE}$ Width

Truth Table/Switch Programming

$\overline{LE}$	EN2	$\overline{EN1}$	ADDRESS BITS			ON SWITCHES		
			ADDC*	ADDB	ADDA	MAX4530	MAX4531	MAX4532
0	1	0	X	X	X	Last address	Last address	Last address
X	0	X	X	X	X	All switches open	All switches open	All switches open
X	X	1	X	X	X	All switches open	All switches open	All switches open
1	1	0	0	0	0	COM–NO0	COMA–NO0A, COMB–NO0B	COMA–NCA, COMB–NCB, COMC–NCC
1	1	0	0	0	1	COM–NO1	COMA–NO1A, COMB–NO1B	COMA–NOA, COMB–NCB, COMC–NCC
1	1	0	0	1	0	COM–NO2	COMA–NO2A, COMB–NO2B	COMA–NCA, COMB–NOB, COMC–NCC
1	1	0	0	1	1	COM–NO3	COMA–NO3A, COMB–NO3B	COMA–NOA, COMB–NOB, COMC–NCC
1	1	0	1	0	0	COM–NO4	COMA–NO0A, COMB–NO0B	COMA–NCA, COMB–NCB, COMC–NOC
1	1	0	1	0	1	COM–NO5	COMA–NO1A, COMB–NO1B	COMA–NOA, COMB–NCB, COMC–NOC
1	1	0	1	1	0	COM–NO6	COMA–NO2A, COMB–NO2B	COMA–NCA, COMB–NOB, COMC–NOC
1	1	0	1	1	1	COM–NO7	COMA–NO3A, COMB–NO3B	COMA–NOA, COMB–NOB, COMC–NOC

X = Don't Care **ADDC not present on MAX4531.*

Note: NO_ and COM_ pins are identical and interchangeable. Either may be considered an input or an output; signals pass equally well in either direction. $\overline{LE}$ is independent of $\overline{EN1}$ and EN2.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Ordering Information (continued)

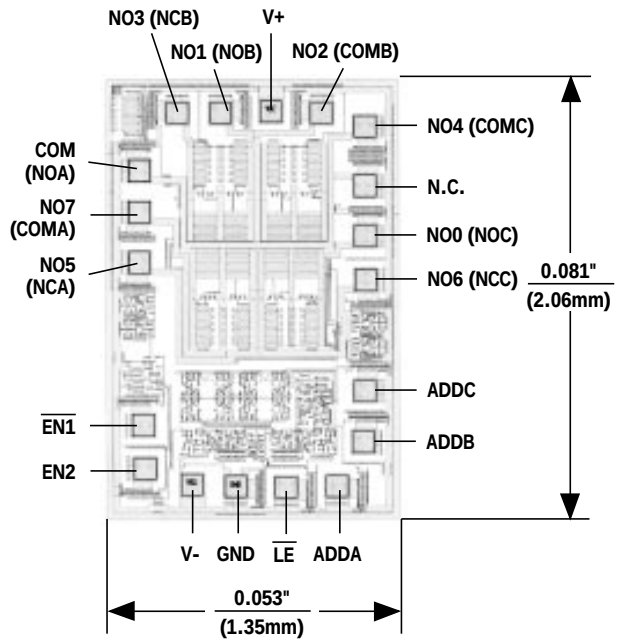
PART	TEMP. RANGE	PIN-PACKAGE
MAX4530EPP	-40°C to +85°C	20 Plastic DIP
MAX4530EWP	-40°C to +85°C	20 SO
MAX4530EAP	-40°C to +85°C	20 SSOP
MAX4531CPP	0°C to +70°C	20 Plastic DIP
MAX4531CWP	0°C to +70°C	20 SO
MAX4531CAP	0°C to +70°C	20 SSOP
MAX4531C/D	0°C to +70°C	Dice*
MAX4531EPP	-40°C to +85°C	20 Plastic DIP
MAX4531EWP	-40°C to +85°C	20 SO
MAX4531EAP	-40°C to +85°C	20 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX4532CPP	0°C to +70°C	20 Plastic DIP
MAX4532CWP	0°C to +70°C	20 SO
MAX4532CAP	0°C to +70°C	20 SSOP
MAX4532C/D	0°C to +70°C	Dice*
MAX4532EPP	-40°C to +85°C	20 Plastic DIP
MAX4532EWP	-40°C to +85°C	20 SO
MAX4532EAP	-40°C to +85°C	20 SSOP

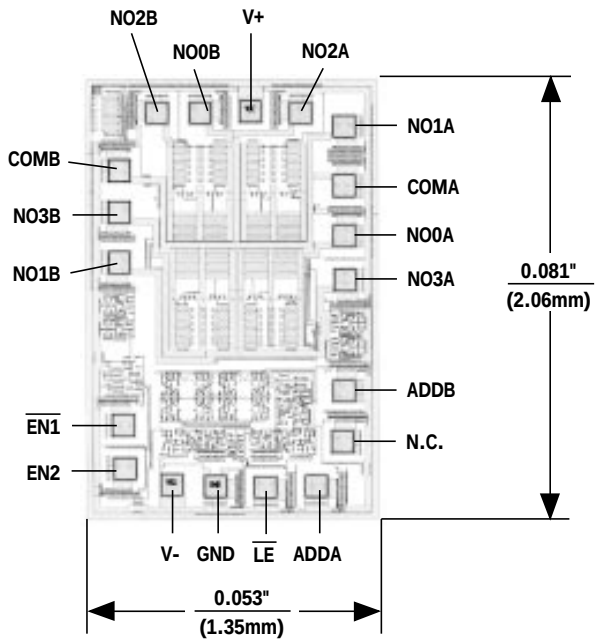
**Contact factory for availability.*

Chip Topographies

MAX4530/MAX4532



MAX4531



( ) ARE FOR MAX4532

TRANSISTOR COUNT: 255

SUBSTRATE CONNECTED TO V+