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19-4780; Rev 1; 6/99

MAXIM

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

General Description

The MAX4539/MAX4540 low-voltage, CMOS 8-channel (MAX4539) and dual 4-channel (MAX4540) multiplexers are ideal for precision ADC calibration and system self-monitoring applications. These calibration multiplexers (cal-muxes) have precision resistor-dividers to generate accurate voltage ratios from an input reference voltage. The reference ratios include 15/4096 and 4081/4096 of the external reference voltage, accurate to 15 bits, and 1/2V+ and 5/8(V+ - V-), accurate to 8 bits. The external reference voltage as well as ground can also be switched to the output. The MAX4539/MAX4540 have enable inputs and address latching. All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using a ±5V or a single +5V supply. Protection diodes at all inputs provide an ESD rating >2kV.

The MAX4539/MAX4540 operate from a single +2.7V to +12V supply, or from dual supplies of ±2.7V to ±6V. On-resistance (100Ω max) is matched between switches to 6Ω max. Each switch can handle Rail-to-Rail® analog signals. The off leakage current is 0.1nA at T_A = +25°C and 2nA at T_A = +85°C.

The MAX4539/MAX4540 are available in small 20-pin DIP, SO, and SSOP packages.

Applications

Battery-Operated Equipment	Avionics
Data-Acquisition Systems	Audio-Signal Routing
Test Equipment	Networking

Ordering Information

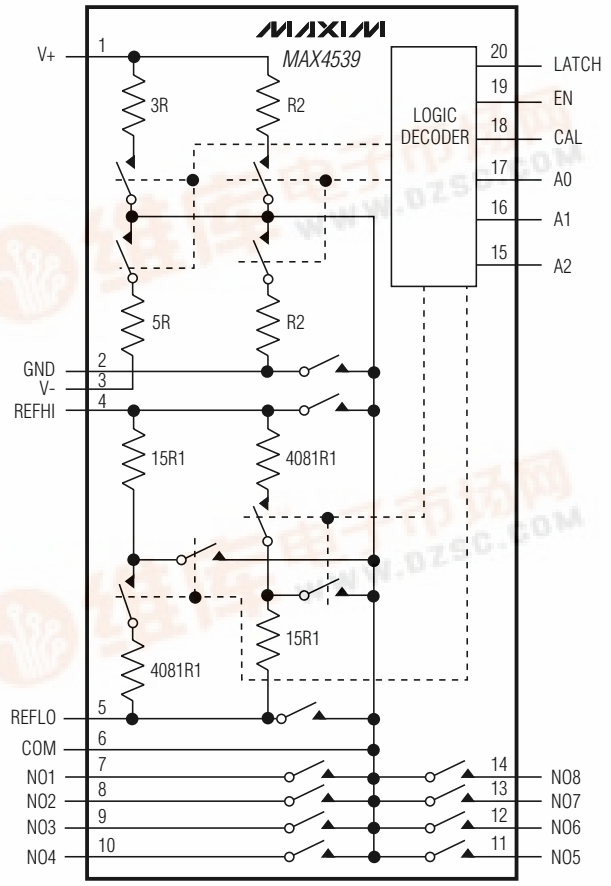
PART	TEMP. RANGE	PIN-PACKAGE
MAX4539CAP	0°C to +70°C	20 SSOP
MAX4539CWP	0°C to +70°C	20 Wide SO
MAX4539CPP	0°C to +70°C	20 Plastic DIP
MAX4539EAP	-40°C to +85°C	20 SSOP
MAX4539EWP	-40°C to +85°C	20 Wide SO
MAX4539EPP	-40°C to +85°C	20 Plastic DIP
MAX4540CAP	0°C to +70°C	20 SSOP
MAX4540CWP	0°C to +70°C	20 Wide SO
MAX4540CPP	0°C to +70°C	20 Plastic DIP
MAX4540EAP	-40°C to +85°C	20 SSOP
MAX4540EWP	-40°C to +85°C	20 Wide SO
MAX4540EPP	-40°C to +85°C	20 Plastic DIP

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

- **On-Chip Gain and Offset Divider Networks Provide 15-Bit Accurate Output Ratios**
- **On-Chip V+ to GND and V+ to V- Divider Networks Provide 8-Bit Accurate Output Ratios**
- **R_{ON}: 100Ω max**
- **R_{ON} Matching Between Channels: 6Ω max**
- **Charge Injection: 5pC max**
- **Low 0.1nA Off Leakage Current**
- **Small 20-Pin SSOP/SO/DIP Packages**

Pin Configurations/ Functional Diagrams



MAX4540 appears at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +13V
V- to GND .....-13V to +0.3V
V+ to V- .....-0.3V to +13V
CAL, LATCH, A_, EN, NO_, COM_,
REFHI, REFLO (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current (any terminal).....±20mA
Peak Current, NO_ or COM_
(pulsed at 1ms, 10% duty cycle max).....±40mA

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8mW/°C above +70°C) 640mW
Wide SO (derate 8mW/°C above +70°C).....800mW
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
MAX4539C_P/MAX4540C_P.....0°C to +70°C
MAX4539E_P/MAX4540E_P .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300° C

Note 1: Signals on NO_, COM_, EN, LATCH, CAL, A_ exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SWITCH								
Analog-Signal Range	$V_{COM_}$, $V_{NO_}$	(Note 3)			V-		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$ = ±3.0V, V+ = 4.5V, V- = -4.5V		T_A = +25°C		45	75	Ω
				T_A = T_{MIN} to T_{MAX}			100	
On-Resistance Matching Between Channels (Note 4)	ΔR_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$ = ±3.0V, V+ = 4.5V, V- = -4.5V		T_A = +25°C		1	4	Ω
				T_A = T_{MIN} to T_{MAX}			6	
On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM_}$ = 1mA; $V_{NO_}$ = -3V, 0, +3V; V+ = 4.5V; V- = -4.5V		T_A = +25°C		7	10	Ω
				T_A = T_{MIN} to T_{MAX}			13	
NO-Off Leakage Current (Note 6)	$I_{NO(OFF)}$	$V_{COM_}$ = ±4.5V, $V_{NO_}$ = ∓4.5V, V+ = 5.5V, V- = -5.5V		T_A = +25°C	-0.1	0.01	0.1	nA
				T_A = T_{MIN} to T_{MAX}	-2		2	
COM-Off Leakage Current (Note 6)	$I_{COM_(OFF)}$	$V_{COM_}$ = ±4.5V, $V_{NO_}$ = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4539	T_A = +25°C	-0.2	0.01	0.2	nA
				T_A = T_{MIN} to T_{MAX}	-10		10	
			MAX4540	T_A = +25°C	-0.1	0.01	0.1	
				T_A = T_{MIN} to T_{MAX}	-5		5	
COM-On Leakage Current (Note 6)	$I_{COM_(ON)}$	$V_{COM_}$ = ±4.5V, $V_{NO_}$ = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX4539	T_A = +25°C	-0.2	0.01	0.2	nA
				T_A = T_{MIN} to T_{MAX}	-10		10	
			MAX4540	T_A = +25°C	-0.1	0.01	0.1	
				T_A = T_{MIN} to T_{MAX}	-5		5	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{IH}			2.4	1.7		V
Input Low Voltage	V_{IL}				1.4	0.8	V
Input Current with Input Voltage High	I_{IH}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = V+		-0.1	0.01	0.1	µA
Input Current with Input Voltage Low	I_{IL}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0		-0.1	0.01	0.1	µA
SUPPLY							
Power-Supply Range				±2.7		±6	V
Positive Supply Current	I+	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0 or V+, V+ = 5.5V, V- = -5.5V (Note 7)	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0 or V+, V+ = 5.5V, V- = -5.5V (Note 7)	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
GND Supply Current	I_{GND}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0 or V+, V+ = 5.5V, V- = -5.5V (Note 7)	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC CHARACTERISTICS							
Transition Time	t_{TRANS}	Figure 1	T_A = +25°C		100	150	ns
			T_A = T_{MIN} to T_{MAX}			200	
Break-Before-Make Interval (Note 3)	t_{OPEN}	Figure 2	T_A = +25°C	4	10		ns
			T_A = T_{MIN} to T_{MAX}	1			
Enable Turn-On Time	t_{ON}	Figure 3	T_A = +25°C		75	115	ns
			T_A = T_{MIN} to T_{MAX}			175	
Enable Turn-Off Time	t_{OFF}	Figure 3	T_A = +25°C		50	100	ns
			T_A = T_{MIN} to T_{MAX}			120	
Charge Injection (Note 3)	V_{CTE}	C_L = 1nF, $V_{NO_}$ = 0, Figure 4	T_A = +25°C		1	5	pC
Off-Isolation (Note 8)	V_{ISO}	V_{EN} = 0, f = 1MHz, Figure 5	T_A = +25°C		-75		dB
Crosstalk Between Channels (Note 9)	V_{CT}	V_{EN} = 2.4V, f = 1MHz, V_{GEN} = 1Vp-p, Figure 5	T_A = +25°C		-75		dB
Logic Input Capacitance	C_{IN}	f = 1MHz	T_A = +25°C		15		pF
NO-Off Capacitance	C_{OFF}	f = 1MHz, V_{EN} = $V_{COM_}$ = 0, Figure 6	T_A = +25°C		3		pF
COM-Off Capacitance	$C_{COM_(OFF)}$	f = 1MHz, V_{EN} = $V_{COM_}$ = 0, Figure 6	T_A = +25°C		15		pF
COM-On Capacitance	$C_{COM_(ON)}$	f = 1MHz, V_{EN} = 2.4V, $V_{COM_}$ = 0, Figure 6	T_A = +25°C		26		pF

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LATCH TIMING (Note 3)							
Setup Time	t_S	Figure 7	T_A = +25°C		45	70	ns
			T_A = T_{MIN} to T_{MAX}			80	
Hold Time	t_H	Figure 7	T_A = +25°C	-10	0		ns
			T_A = T_{MIN} to T_{MAX}	-10			
Pulse Width, Latch Enable	t_{MPW}	Figure 7	T_A = +25°C	30	15		ns
			T_A = T_{MIN} to T_{MAX}	40			
Enable Setup Time	t_{ES}	Figure 8	T_A = +25°C		15	30	ns
			T_A = T_{MIN} to T_{MAX}			40	
INTERNAL DIVIDERS							
Offset Divider Output		V_{REF} = 4.096V, REFHI = 4.096V, REFLO = GND	T_A = +25°C	14.9/ 4096	15/ 4096	15.1/ 4096	LSB
			T_A = T_{MIN} to T_{MAX}	14.9/ 4096	15/ 4096	15.1/ 4096	
Gain Divider Output		V_{REF} = 4.096V, REFHI = 4.096V, REFLO = GND	T_A = +25°C	4080.9/ 4096	4081/ 4096	4081.1/ 4096	LSB
			T_A = T_{MIN} to T_{MAX}	4080.9/ 4096	4081/ 4096	4081.1/ 4096	
(V+ / 2) Divider Output		Referenced to GND	T_A = +25°C	2032/ 4096	2048/ 4096	2064/ 4096	LSB
			T_A = T_{MIN} to T_{MAX}	2032/ 4096	2048/ 4096	2064/ 4096	
(V+ - V-) Divider Output		Referenced to V-	T_A = +25°C	2544/ 4096	2560/ 4096	2576/ 4096	LSB
			T_A = T_{MIN} to T_{MAX}	2544/ 4096	2560/ 4096	2576/ 4096	
Output Resistance Offset Divider		(Note 3)	T_A = +25°C		400	800	Ω
Output Resistance Gain Divider		(Note 3)	T_A = +25°C		400	800	Ω
Output Resistance (V+ / 2) Divider		(Note 3)	T_A = +25°C		6	9	kΩ
Output Resistance (V+ - V-) Divider		(Note 3)	T_A = +25°C		6	9	kΩ
Output Resistance (REFHI, REFLO, GND)		(Note 3)	T_A = +25°C		400	800	Ω
Additional Positive Supply Current		(V+ / 2) divider active, V_{IH} = V+, V_{IL} = 0 (Note 3)	T_A = +25°C		V+ / 24k	V+ / 13k	mA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Additional Positive Supply Current (Note 3)		(V+ - V-) divider active, V_{IH} = V+, V_{IL} = 0	T_A = +25°C		(V+ - V-)/ 24k	(V+ - V-)/ 13k	mA
Additional Negative Supply Current		(V+ - V-) divider active, V_{IH} = V+, V_{IL} = 0 (Note 3)	T_A = +25°C		(V+ - V-)/ 24k	(V+ - V-)/ 13k	mA
REFHI, REFLO Input Range (Note 3)				V- - 0.3		V+ + 0.3	V
Input Resistance (REFHI, REFLO) (Note 3)		Offset divider active, gain divider active	T_A = +25°C	25	40		kΩ

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SWITCH								
Analog-Signal Range	$V_{NO_}$, $V_{COM_}$	(Note 3)			0		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$ = 3.0V, V+ = 4.5V		T_A = +25°C		80	150	Ω
				T_A = T_{MIN} to T_{MAX}			200	
On-Resistance Matching Between Channels (Notes 3, 4)	ΔR_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$ = 3.0V, V+ = 4.5V		T_A = +25°C		2	8	Ω
				T_A = T_{MIN} to T_{MAX}			12	
On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM_}$ = 1mA; $V_{NO_}$ = 3V, 2V, 1V; V+ = 4.5V		T_A = +25°C		8		Ω
NO-Off Leakage Current (Notes 6, 10)	$I_{NO(OFF)}$	$V_{COM_}$ = 1V, 4.5V; $V_{NO_}$ = 4.5V, 1V; V+ = 5.5V		T_A = +25°C	-0.1		0.1	nA
				T_A = T_{MIN} to T_{MAX}	-2		2	
COM-Off Leakage Current (Notes 6, 10)	$I_{COM_(OFF)}$	$V_{COM_}$ = 4.5V, 1V; $V_{NO_}$ = 1V, 4.5V; V+ = 5.5V	MAX4539	T_A = +25°C	-0.2		0.2	nA
				T_A = T_{MIN} to T_{MAX}	-10		10	
			MAX4540	T_A = +25°C	-0.1		0.1	
				T_A = T_{MIN} to T_{MAX}	-5		5	
COM-On Leakage Current (Notes 6, 10)	$I_{COM_(ON)}$	$V_{COM_}$ = 4.5V, $V_{NO_}$ = 4.5V, V+ = 5.5V	MAX4539	T_A = +25°C	-0.2		0.2	nA
				T_A = T_{MIN} to T_{MAX}	-10		10	
			MAX4540	T_A = +25°C	-0.1		0.1	
				T_A = T_{MIN} to T_{MAX}	-5		5	

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS (Note 3)							
Input High Voltage	V_{IH}			2.4	1.6		V
Input Low Voltage	V_{IL}				1.4	0.8	V
Input Current with Input Voltage High	I_{IH}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = V+		-0.1		0.1	µA
Input Current with Input Voltage Low	I_{IL}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0		-0.1		0.1	µA
SUPPLY							
Power-Supply Range				2.7		12	V
Positive Supply Current (Note 3)	I+	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0 or V+, V+ = 5.5V	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
GND Supply Current (Note 3)	I_{GND}	V_{EN} = $V_{A_}$ = V_{LATCH} = V_{CAL} = 0 or V+, V+ = 5.5V	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC CHARACTERISTICS (Note 3)							
Transition Time	t_{TRANS}	Figure 1	T_A = +25°C		150	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_{OPEN}	Figure 2	T_A = +25°C	4	10		ns
			T_A = T_{MIN} to T_{MAX}	1			
Enable Turn-On Time	t_{ON}	Figure 3	T_A = +25°C		115	150	ns
			T_A = T_{MIN} to T_{MAX}			200	
Enable Turn-Off Time	t_{OFF}	Figure 3	T_A = +25°C		60	100	ns
			T_A = T_{MIN} to T_{MAX}			130	
Charge Injection	V_{CTE}	C_L = 1nF, $V_{NO_}$ = 0, Figure 4	T_A = +25°C		1	5	pC
LATCH TIMING (Note 3)							
Setup Time	t_S	Figure 7	T_A = +25°C			70	ns
			T_A = T_{MIN} to T_{MAX}			80	
Hold Time	t_H	Figure 7	T_A = +25°C	-10	0		ns
			T_A = T_{MIN} to T_{MAX}	-10			
Pulse Width, Latch Enable	t_{MPW}	Figure 7	T_A = +25°C	30	15		ns
			T_A = T_{MIN} to T_{MAX}	40			
Enable Setup Time	t_{ES}	Figure 8	T_A = +25°C		15	30	ns
			T_A = T_{MIN} to T_{MAX}			40	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0, V_{IH} = 2.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH							
Analog-Signal Range	$V_{COM_}$	(Note 3)		0		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 0.2mA, $V_{NO_}$ = 1.5V, V+ = 2.7V	T_A = +25°C		220	500	Ω
			T_A = T_{MIN} to T_{MAX}			600	
LOGIC INPUTS (Note 3)							
Input High Voltage	V_{IH}			2.4	1.1		V
Input Low Voltage	V_{IL}				1.1	0.5	V
DYNAMIC (Note 3)							
Transition Time	t_{TRANS}	V_{NO1} = 1.5V, V_{NO8} = 0, Figure 1	T_A = +25°C		260	400	ns
Enable Turn-On Time	t_{ON}	V_{NO1} = 1.5V, Figure 3	T_A = +25°C		220	350	ns
Enable Turn-Off Time	t_{OFF}	V_{NO} = 1.5V, Figure 3	T_A = +25°C		100	150	ns
LATCH TIMING (Note 3)							
Setup Time	t_S	Figure 7	T_A = +25°C			100	ns
Hold Time	t_H	Figure 7	T_A = +25°C	-10	0		ns
Pulse Width, Latch Enable	t_{MPW}	Figure 7	T_A = +25°C	40			ns
Enable Setup Time	t_{ES}	Figure 8	T_A = +25°C			50	ns

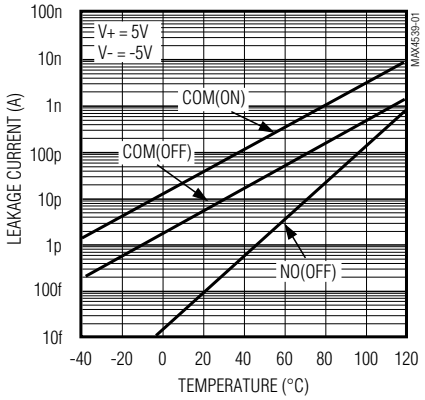
Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 7: If the logic inputs can float during power-on, connect a 1MΩ pull-up from LATCH to V+; see *Applications Information* section.
Note 8: Off Isolation = $20\log_{10} (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.
Note 9: Between any two switches.
Note 10: Leakage testing with a single supply is guaranteed by testing with dual supplies.

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

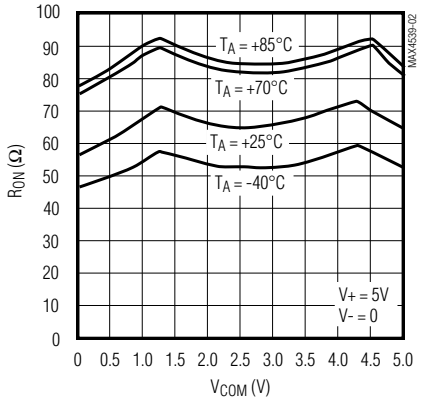
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

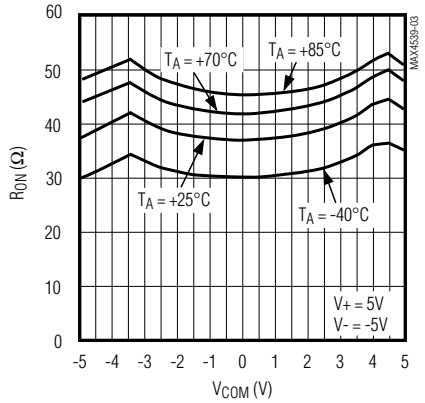
LEAKAGE CURRENT vs. TEMPERATURE



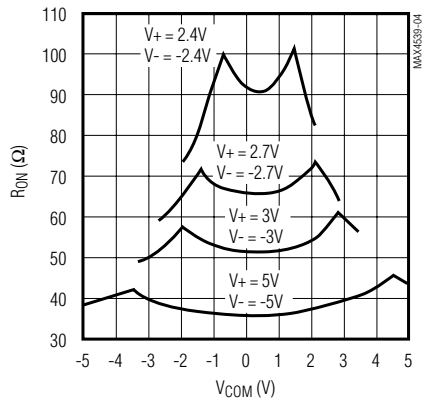
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



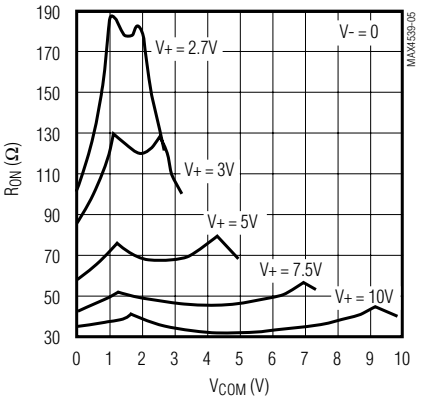
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



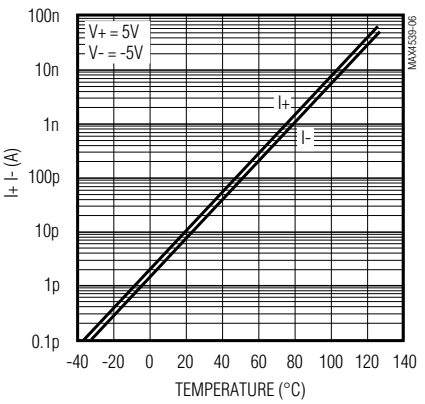
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



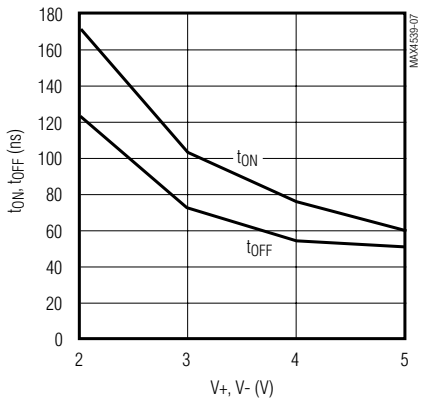
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



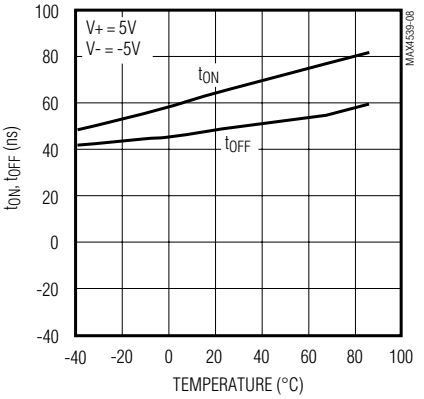
SUPPLY CURRENT vs. TEMPERATURE



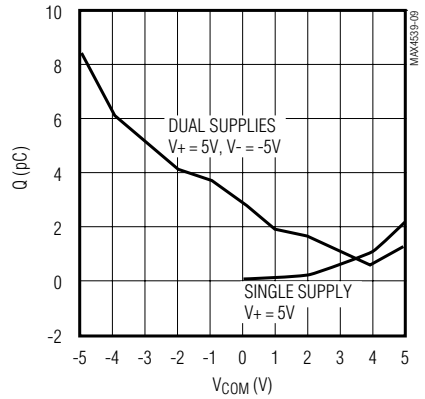
ON/OFF TIME vs. SUPPLY VOLTAGE



ON/OFF TIME vs. TEMPERATURE



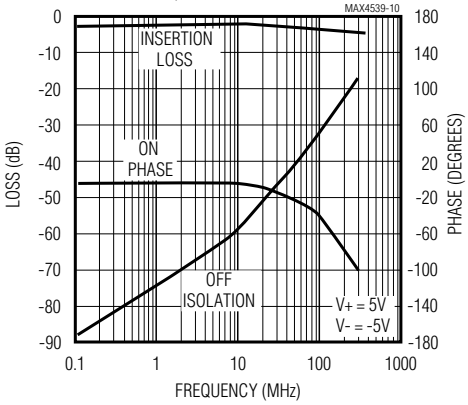
CHARGE INJECTION vs. V_{COM}



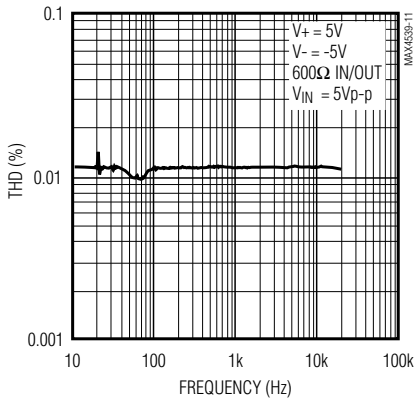
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

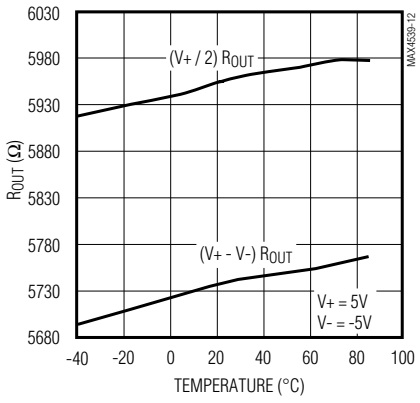
FREQUENCY RESPONSE



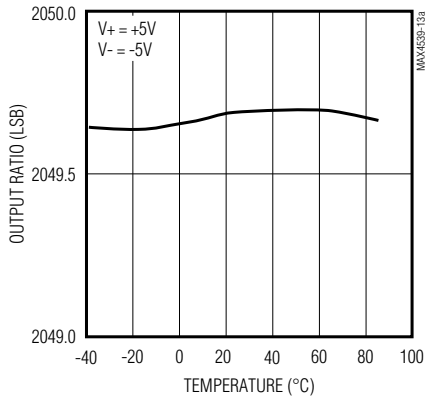
TOTAL HARMONIC DISTORTION vs. FREQUENCY



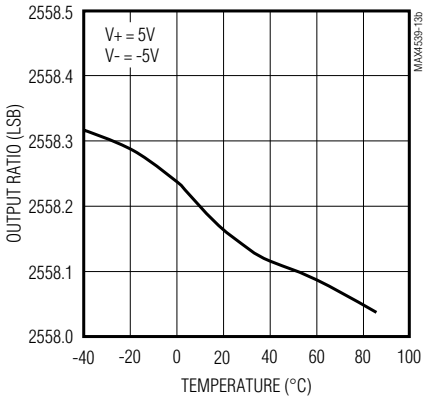
ROUT vs. TEMPERATURE (V+ / 2 DIVIDER AND V+ - V- DIVIDER)



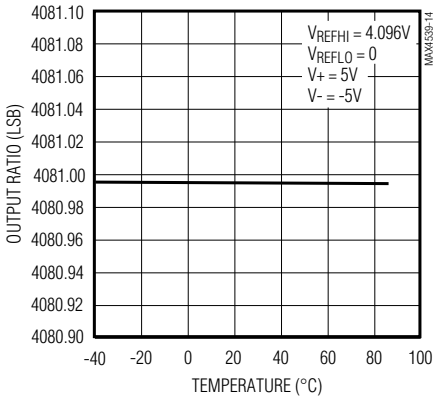
(V+ / 2) DIVIDER OUTPUT vs. TEMPERATURE



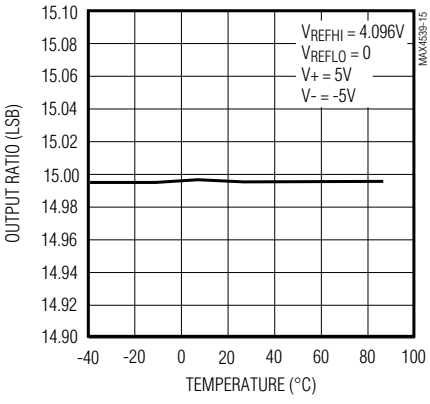
(V+ - V-) DIVIDER OUTPUT vs. TEMPERATURE



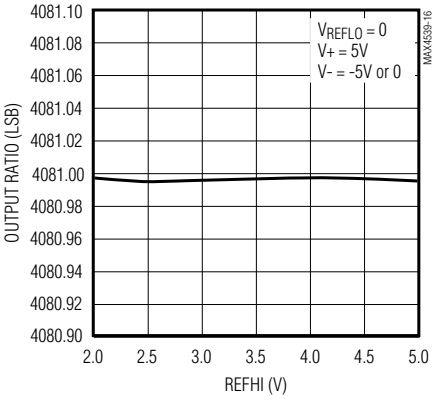
GAIN DIVIDER OUTPUT vs. TEMPERATURE



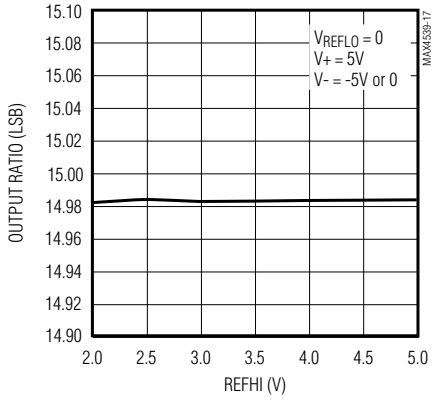
OFFSET DIVIDER OUTPUT vs. TEMPERATURE



GAIN DIVIDER OUTPUT vs. REFHI



OFFSET DIVIDER OUTPUT vs. REFHI

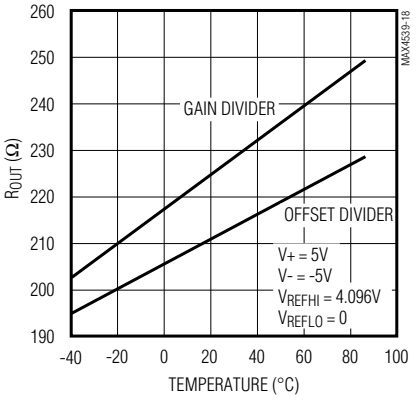


Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

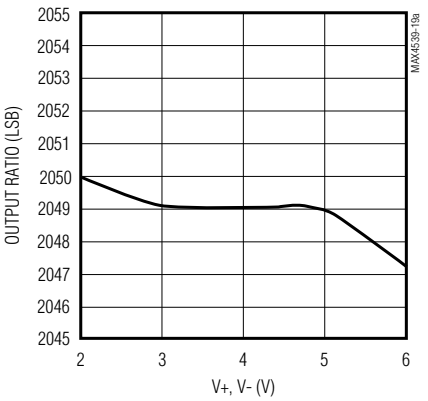
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

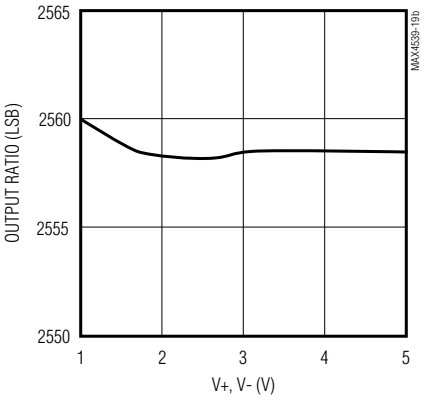
R_{OUT} vs. TEMPERATURE (OFFSET DIVIDER AND GAIN DIVIDER)



(V+ / 2) DIVIDER OUTPUT vs. SUPPLY VOLTAGE



(V+ - V-) DIVIDER OUTPUT vs. SUPPLY VOLTAGE



Pin Descriptions

MAX4539 (Single 8-to-1 Cal-Mux)

PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage
2	GND	Ground
3	V-	Negative Supply Voltage
4	REFHI	Reference High Voltage Input
5	REFLO	Reference Low Voltage Input
6	COM	Multiplexer Output
7	NO1	Channel Input 1
8	NO2	Channel Input 2
9	NO3	Channel Input 3
10	NO4	Channel Input 4
11	NO5	Channel Input 5
12	NO6	Channel Input 6
13	NO7	Channel Input 7
14	NO8	Channel Input 8
15	A2	Address Bit 2
16	A1	Address Bit 1
17	A0	Address Bit 0
18	CAL	Calibration Control Input
19	EN	Multiplexer Enable
20	LATCH	Address Latch Control Input

MAX4540 (Dual 4-to-1 Cal-Mux)

PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage
2	GND	Ground
3	V-	Negative Supply Voltage
4	REFHI	Reference High Voltage Input
5	REFLO	Reference Low Voltage Input
6	COMA	Multiplexer Output A
7	NO1A	Channel Input 1A
8	NO2A	Channel Input 2A
9	NO3A	Channel Input 3A
10	NO4A	Channel Input 4A
11	NO1B	Channel Input 1B
12	NO2B	Channel Input 2B
13	NO3B	Channel Input 3B
14	NO4B	Channel Input 4B
15	COMB	Multiplexer Output B
16	A1	Address Bit 1
17	A0	Address Bit 0
18	CAL	Calibration Control Input
19	EN	Multiplexer Enable
20	LATCH	Address Latch Control Input

Truth Tables

MAX4539 (Single 8-to-1 Cal-Mux)

CAL	A2	A1	A0	EN	LATCH	COM
X	X	X	X	0	X	All switches and dividers open. COM is high-Z. Latch contents set to all 1's.
X	X	X	X	1	1	State is latched when LATCH is high.
0	0	0	0	1	0	NO1
0	0	0	1	1	0	NO2
0	0	1	0	1	0	NO3
0	0	1	1	1	0	NO4
0	1	0	0	1	0	NO5
0	1	0	1	1	0	NO6
0	1	1	0	1	0	NO7
0	1	1	1	1	0	NO8
1	0	0	0	1	0	(V+ / 2) Divider Mode, V_{COM} = 2048/4096 V+
1	0	0	1	1	0	REFHI
1	0	1	0	1	0	REFLO
1	0	1	1	1	0	(V+ - V-) Divider Mode , V_{COM} = 2560/4096 (V+ - V-)
1	1	0	0	1	0	GND
1	1	0	1	1	0	Gain Divider Mode, V_{COM} = 4081/4096 (V_{REFHI} - V_{REFLO})
1	1	1	0	1	0	Offset Divider Mode, V_{COM} = 15/4096 (V_{REFHI} - V_{REFLO})
1	1	1	1	1	0	All switches and dividers open. COM is high-Z.

X = Don't care

MAX4540 (Dual 4-to-1 Cal-Mux)

CAL	A1	A0	EN	LATCH	COMA	COMB
X	X	X	0	X	All switches and dividers open. COMA is high-Z.	All switches and dividers open. COMB is high-Z.
X	X	X	1	1	State is latched	State is latched
0	0	0	1	0	NO1A	NO1B
0	0	1	1	0	NO2A	NO2B
0	1	0	1	0	NO3A	NO3B
0	1	1	1	0	NO4A	NO4B
1	0	0	1	0	GND	GND
1	0	1	1	0	Gain Divider Mode	REFLO
1	1	0	1	0	Offset Divider Mode	REFLO
1	1	1	1	0	All switches and dividers open. COMA is high-Z.	All switches and dividers open. COMB is high-Z.

X = Don't care

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

Detailed Description

The MAX4539/MAX4540 are multiplexers with additional calibration features. Internal resistor-dividers generate accurate voltage ratios from an external voltage reference, allowing zero- and full-scale calibration of ADC systems as well as facilitation of system self-monitoring. To access the resistor-dividers, assert the CAL pin. When CAL and ENABLE are asserted, the three address pins select one of the various resistor-divider or external reference outputs. The MAX4539/MAX4540 also contain a LATCH input that allows the state of the CAL and address signals to be captured.

Calibration Functions

The Gain Divider, Offset Divider, REFHI and REFLO modes allow calibration of offset and gain errors in ADC systems. The Gain Divider mode outputs a voltage ratio that is 4081/4096 of V_{REFHI} - V_{REFLO}, accurate to 0.1/4096, or better than 15 bits. The Offset Divider mode outputs a voltage ratio that is 15/4096 of V_{REFHI} - V_{REFLO}, also accurate to 0.1/4096. The REFHI mode allows the voltage on the REFHI pin to be switched to the output. The REFLO mode allows the voltage on the REFLO pin to be switched to the output.

Self-Monitoring Functions

The self-monitoring functions are intended to allow an ADC to measure its own supply voltage. The MAX4539 has an internal divide-by-two resistor string between V+ and GND that is accurate to 8 bits (16/4096). It also has a 5/8 resistor string between V+ and V- that is also accurate to 8 bits. This divider string allows measurement of the negative supply with a unipolar ADC. GND can also be switched to the output, eliminating the need for an additional multiplexer channel.

Applications Information

The MAX4539/MAX4540's construction is typical of most CMOS analog switches. There are three supply pins: V+, V-, and GND. The positive and negative power supplies provide drive to the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse-biased ESD protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes will conduct. During normal operation, these reverse-biased ESD diodes leak, forming the only current drawn from V-.

Virtually all the analog-leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse-biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakage varies as the signal varies. The difference in the two-diode leakage from the signal path to the V+ and V- pins constitutes the analog-signal path leakage current. All analog-leakage current flows to the supply terminals, not to the other switch terminal, which explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators and set the input-logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. All pins have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, which reduces their on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level thresholds are CMOS- and TTL- compatible when V+ is +5V. As V+ is raised, the threshold increases slightly; when V+ reaches +12V, the level threshold is about 3.2V. Although that is above the TTL output high-level minimum of 2.4V, it is still compatible with CMOS outputs.

Bipolar-Supply Operation

The MAX4539/MAX4540 operate with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13V.

Note: Do not connect the MAX4539/MAX4540 V+ pin to +3V AND connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs can exceed the absolute maximum ratings, which will cause damage to the part and/or external circuits.

Caution: The absolute maximum V+ to V- differential voltage is 13V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4539/MAX4540. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13V.

Single-Supply Operation

The MAX4539/MAX4540 operate from a single supply between +2.7V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. However, these parts are optimized for ±5V operation, and most AC and DC characteristics are degraded significantly when departing from ±5V. As the overall supply voltage (V+ to V-) is lowered, switching speed, on-resistance, off isolation, and distortion will degrade. (see the *Typical Operating Characteristics* section).

Single-supply operation also limits signal levels and interferes with ground referenced signals. When V- = 0, AC signals are limited to -0.3V. Voltages below -0.3V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

Power Up

During power up, on-chip latches will strobe whatever addresses are present if EN goes high before LATCH reaches a logic high. When this condition occurs, one of the internal dividers connected between the supplies may inadvertently turn on, causing higher supply current (~200µA supply current) when the enable input is toggled. Avoid this condition by ensuring that EN pin stays low until the remaining logic inputs are valid. To accomplish this, connect a resistor from EN to ground or apply a low voltage to EN before the other logic inputs go high.

Power Off

When power to the MAX4539/MAX4540 is off (i.e., V+ = V- = 0), the Absolute Maximum Ratings still apply. This means that neither logic-level inputs on NO_ nor signals on COM_ can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, and the parts can be damaged if excessive current flows.

Chip Information

TRANSISTOR COUNT: 561

Test Circuits/Timing Diagrams

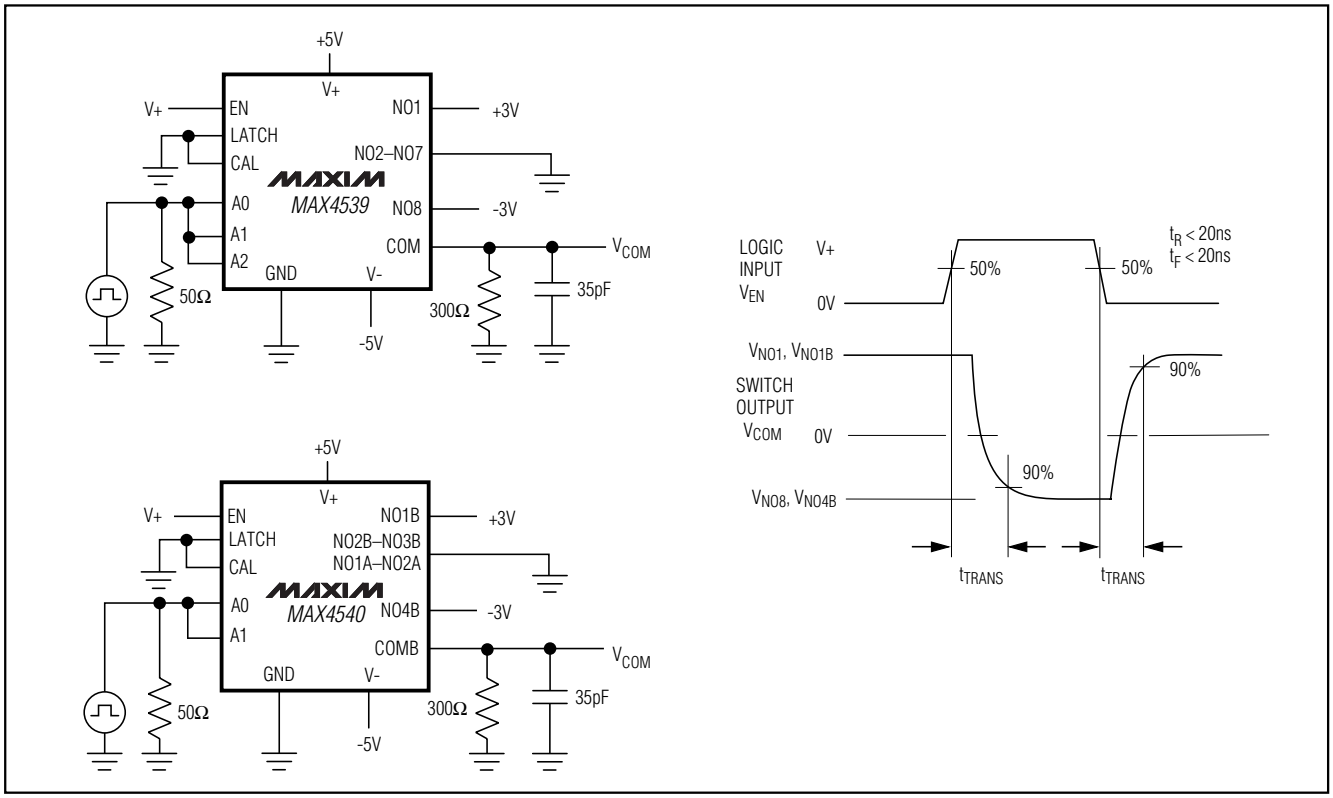


Figure 1. Transition Time

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

Test Circuits/Timing Diagrams (continued)

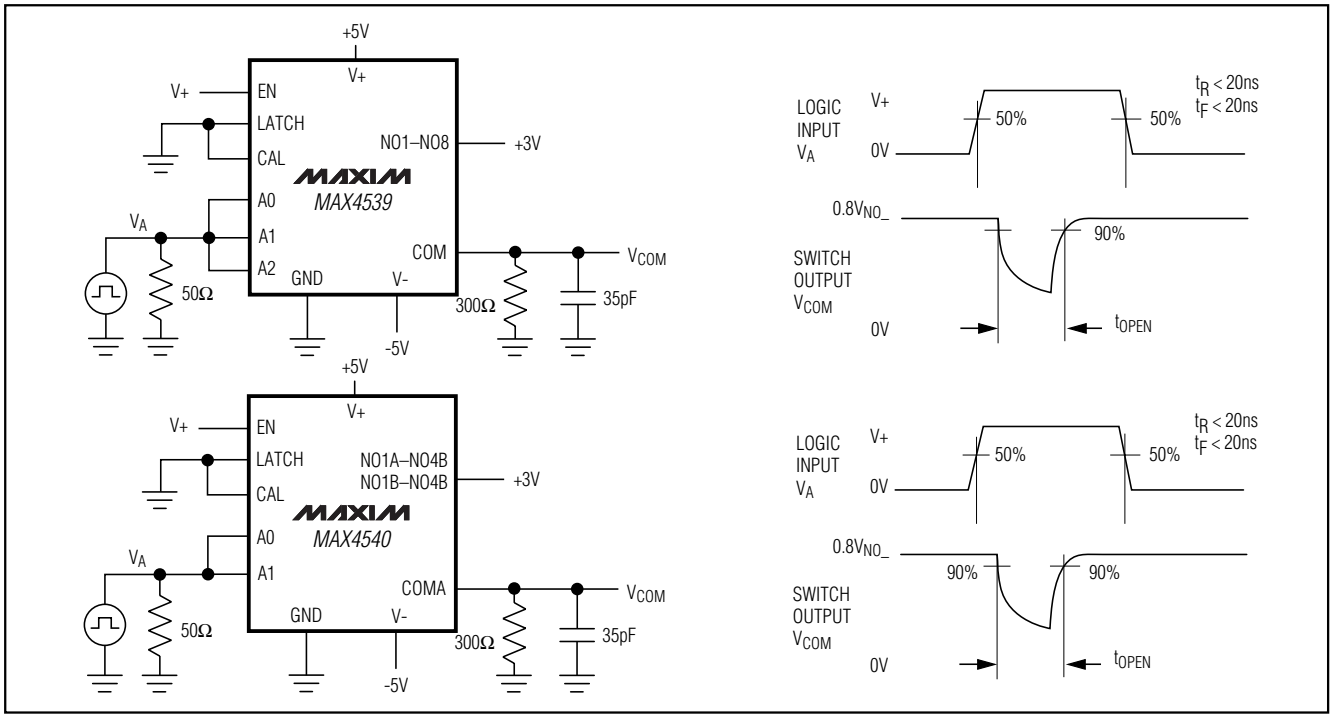


Figure 2. Break-Before-Make Interval

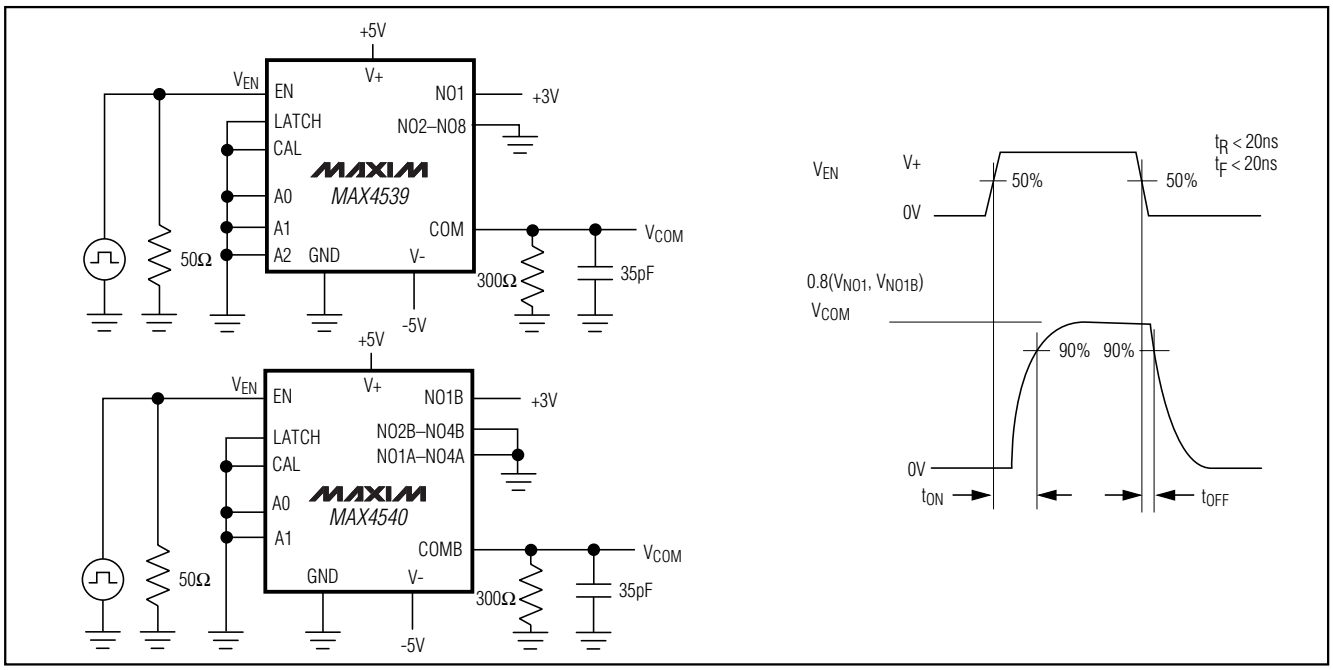


Figure 3. Enable Switching Time

Test Circuits/Timing Diagrams (continued)

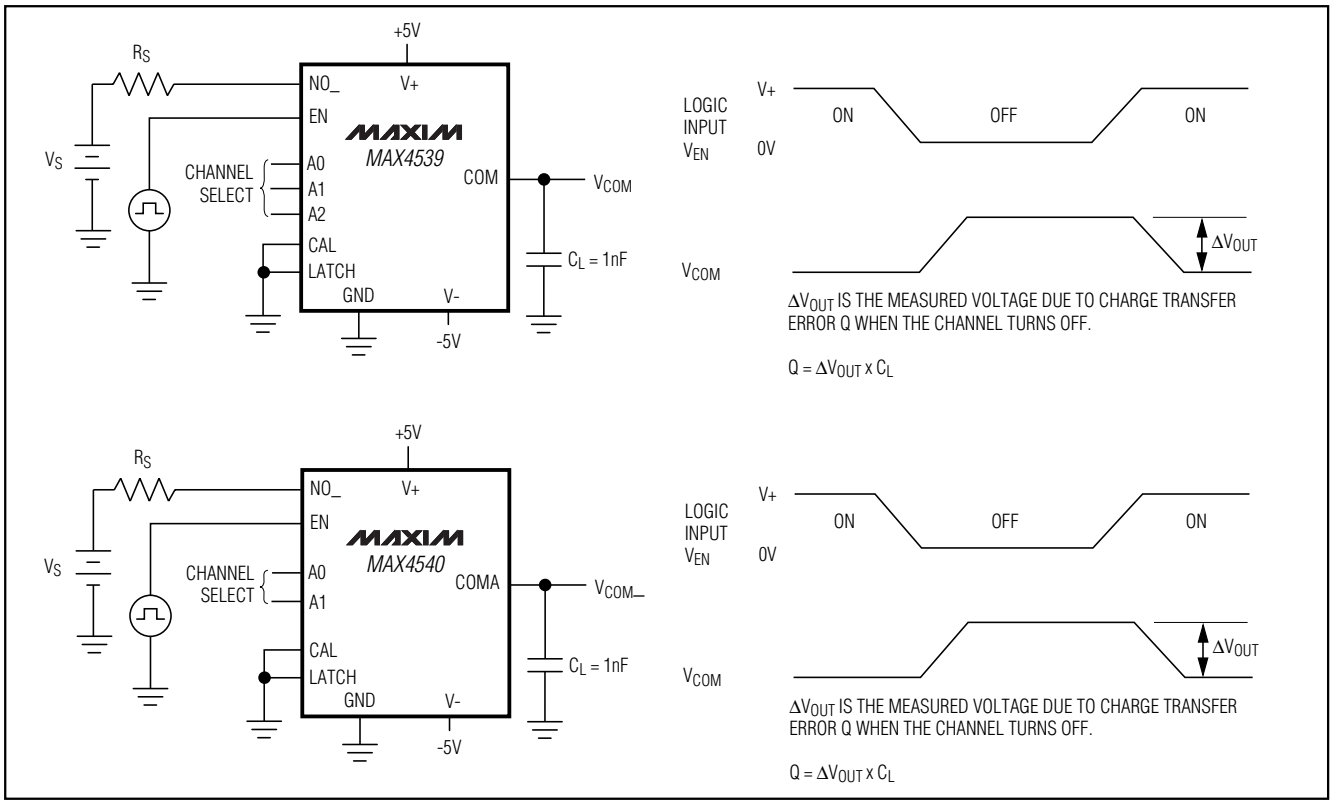


Figure 4. Charge Injection

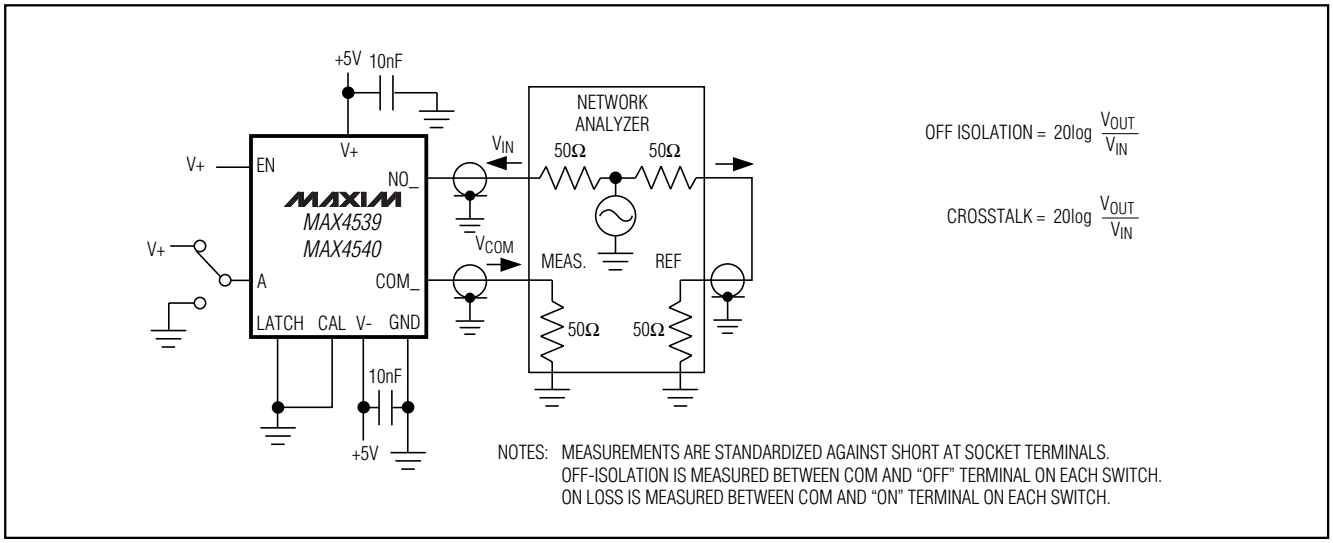


Figure 5. Off-Isolation/Crosstalk

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

Test Circuits/Timing Diagrams (continued)

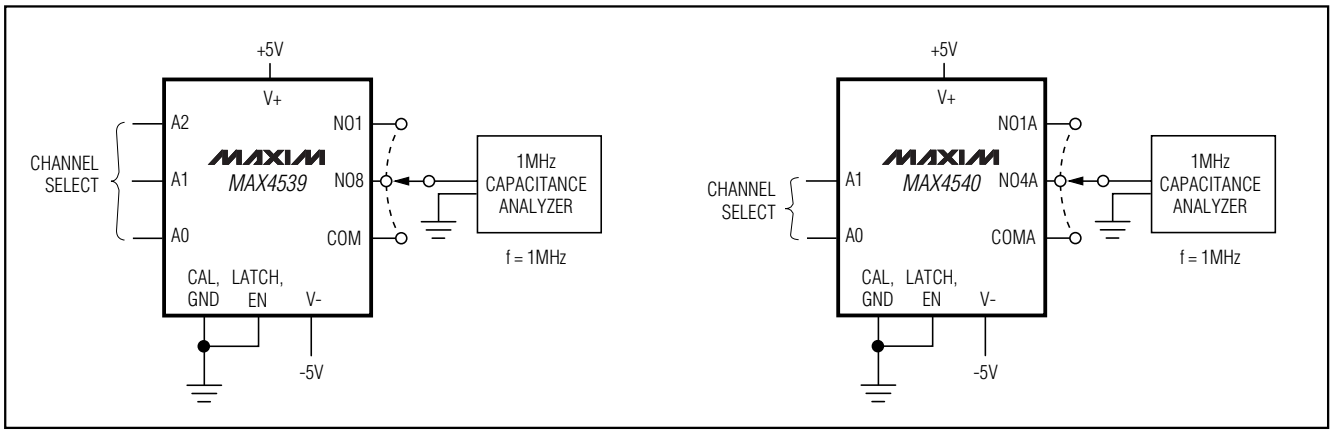


Figure 6. NO_/COM_ Capacitance

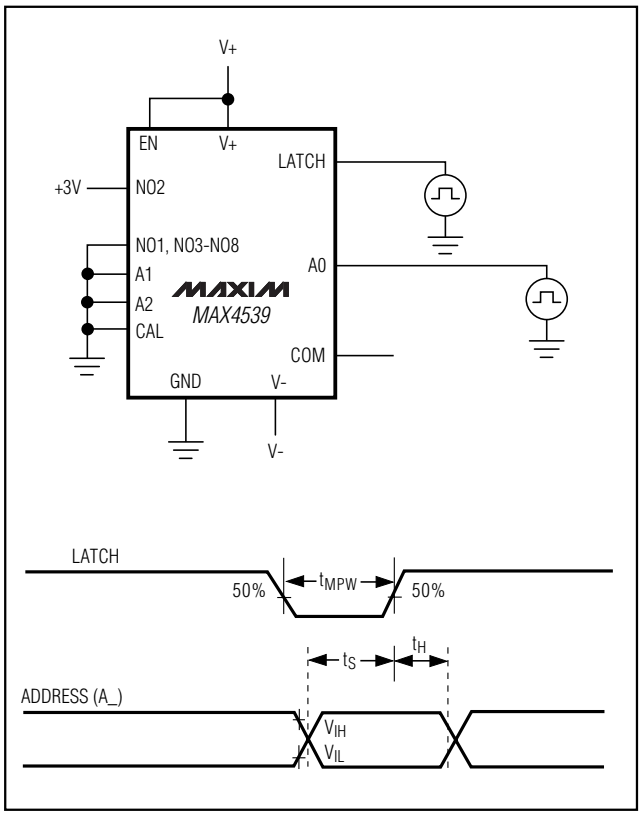


Figure 7. Setup Time, Hold Time, Latch Pulse Width

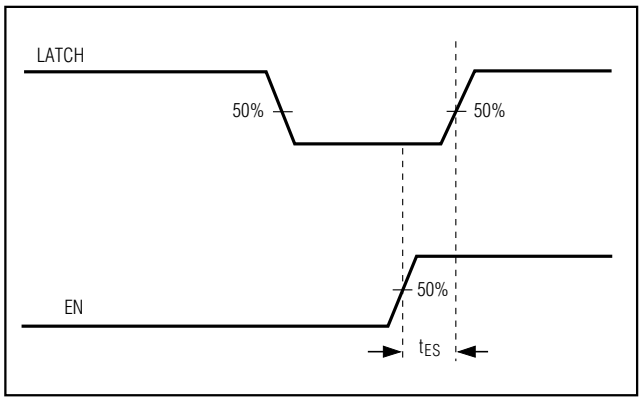
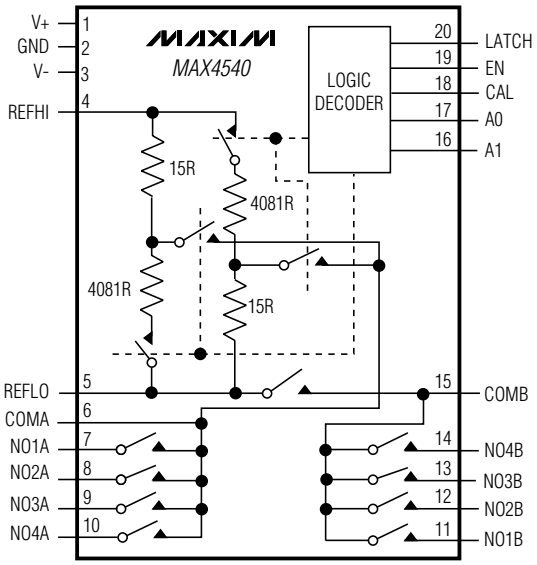


Figure 8. Enable Setup Time

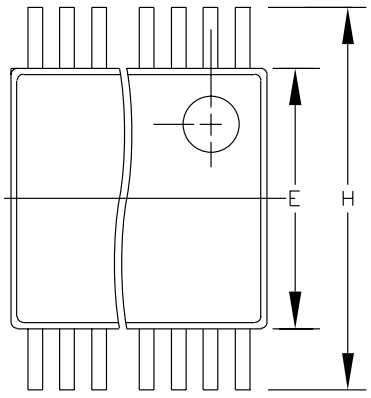
Pin Configurations/Functional Diagrams (continued)



Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

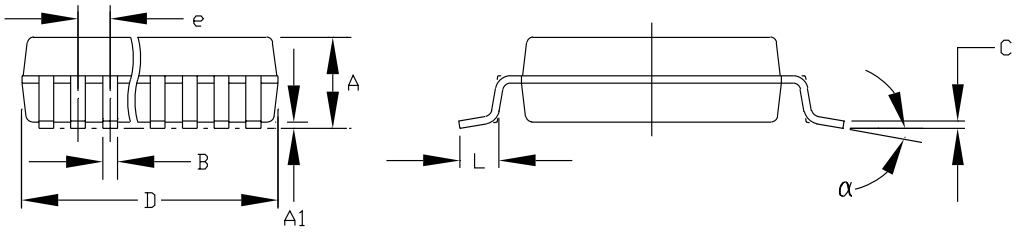
Package Information

SSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

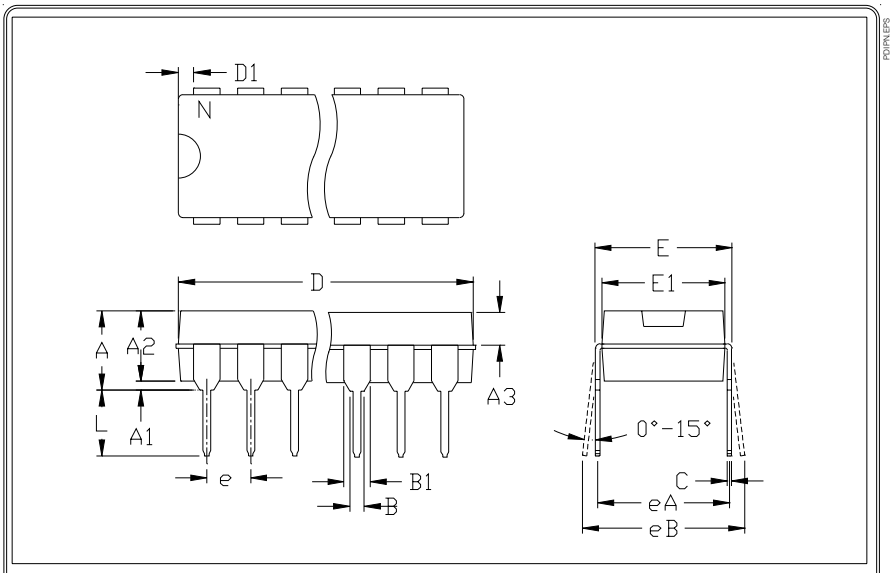


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3X.65mm
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV A | 1/1

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300" (TITLE)

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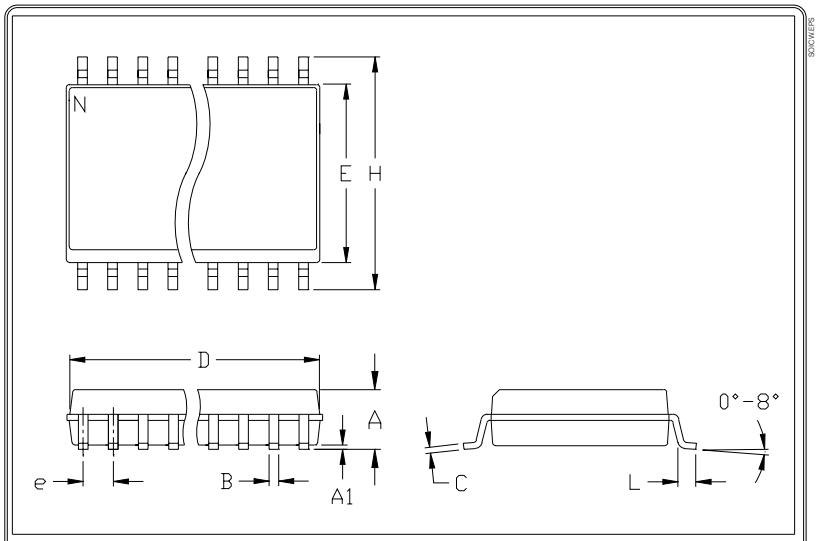
21-0043 A (DOCUMENT CONTROL NUMBER REV)

Low-Voltage, Single 8-to-1 and Dual 4-to-1 Cal-Multiplexers

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .300"

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DOCUMENT CONTROL NUMBER: 21-0042 A REV

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