CS5127

Dual Output Nonsynchronous Buck Controller with Sync Function and Second Channel Enable

Description

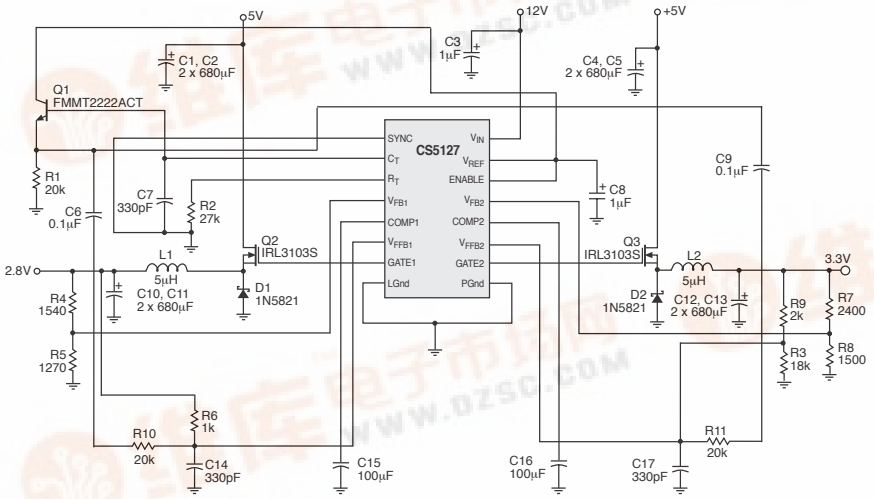
The CS5127 is a fixed frequency dual output nonsynchronous buck controller. It contains circuitry for regulating two separate outputs. Each output channel contains a high gain error amplifier, a comparator and latch, and a totem-pole output driver capable of providing DC current of 100mA and peak current in excess of 0.5A. A common oscillator controls switching for both channels, and a sync lead is provided to allow parallel supply operation or shifting of the switching noise spectrum. An on-chip 5V reference is capable of providing as much as 10mA of current for external circuitry. The CS5127 also contains two undervoltage lockout circuits. The first lockout releases when V_{IN} reaches 8.4V, while the second lockout ensures that V_{REF} is higher than 3.6V. The outputs are held in a low state until both lockouts have released. The controller is configured to utilize the V^{2TM} control method to achieve the fastest possible transient response and best overall regulation. This dual controller is a cost-effective solution for providing V_{CORE} and V_{IO} power solutions in computing applications using a single controller. The CS5127 will operate over an input voltage range of 9.4V to 20V and is available in a 16 lead wide body surface mount package.

Features

- Nonsynchronous Buck Design
- V^{2TM} Control Topology
- 100ns Transient Loop Response
- Programmable Oscillator Frequency
- 30ns Typical Gate Rise and 10ns Fall Times (No Load)
- Frequency Synchronization Input
- ENABLE Input Controls Channel 2 Gate Driver
- 5V/10mA Reference Output

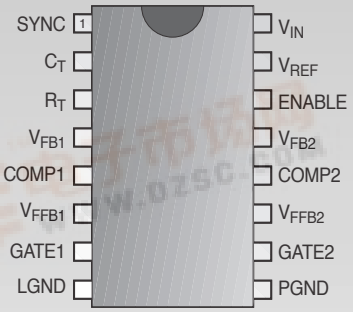
Applications Diagram

12V, 5V to 2.8V @ 7A and 3.3V @ 7A for 233MHz Pentium® Processor with MMX™ Technology



Package Option

16 Lead SOIC Wide



V^2 is a trademark of Switch Power, Inc.

Pentium is a registered trademark and MMX is a trademark of Intel Corporation

Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

Operating Junction Temperature, T_J ..... 150°C
Storage Temperature Range, T_S ..... -65 to 150°C
ESD (Human Body Model) 2kV
Lead Temperature Soldering: Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Lead Symbol	Lead Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
SYNC	Oscillator Synchronization Input	5.5V	-0.3V	5 mA	5 mA
CT	Oscillator Integrating Capacitor	5.5V	-0.3V	1mA	1mA
RT	Oscillator Charge Current Resistor	5.5V	-0.3V	1mA	1mA
V_{FB1}, V_{FB2}	Voltage Feedback Inputs	5.5V	-0.3V	N/A	N/A
COMP1, COMP2	Error Amplifier Outputs	7.5V	-0.3V	2mA	50mA
V_{FFB1}, V_{FFB2}	PWM Ramp Inputs	5.5V	-0.3V	1mA	1mA
GATE1, GATE2	FET Gate Drive Outputs	20V	-0.3V DC, -2.0V for t < 50ns	200mA DC, 1A peak (t < 100µs)	200mA DC, 1A peak (t < 100µs)
LGnd	Reference Ground and IC Substrate	0V	0V	25 mA	N/A
PGnd	Power Ground	0V	0V	1A Peak, 200mA DC	N/A
ENABLE	Channel 2 Enable	5.5V	-0.3V	1mA	N/A
V_{REF}	Reference Voltage Output	5.5V	-0.3V	150mA (short circuit)	5mA
V_{IN}	Power Supply Input	20V	-0.3V	N/A	200mA DC, 1A peak (t < 100µs)

Electrical Characteristics: 0°C < T_A < 70°C; 0°C < T_J < 125°C; 9.4V < V_{IN} < 20V; C_T = 330 pF; R_T = 27kΩ; unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Reference Section					
V_{REF} Output Voltage	Room Temperature, I_{VREF} = 1mA, V_{IN} = 12V	4.9	5.0	5.1	V
Line Regulation			1	20	mV
Load Regulation	1 mA < I_{VREF} < 10 mA		15	26	mV
V_{REF} Variation over Line, Load and Temperature		4.85		5.15	V
Output Short Circuit Current		30	100	150	mA
■ Oscillator Section					
Oscillator Frequency Variation over Line and Temperature		175	210	245	kHz
Maximum Duty Cycle		80	90	98	%
Sync Threshold		0.8	1.6	2.4	V
Sync Bias Current	V_{SYNC} = 2.4V V_{SYNC} = 5.0V		170 430	250 750	µA
Sync Propagation Delay			230		ns

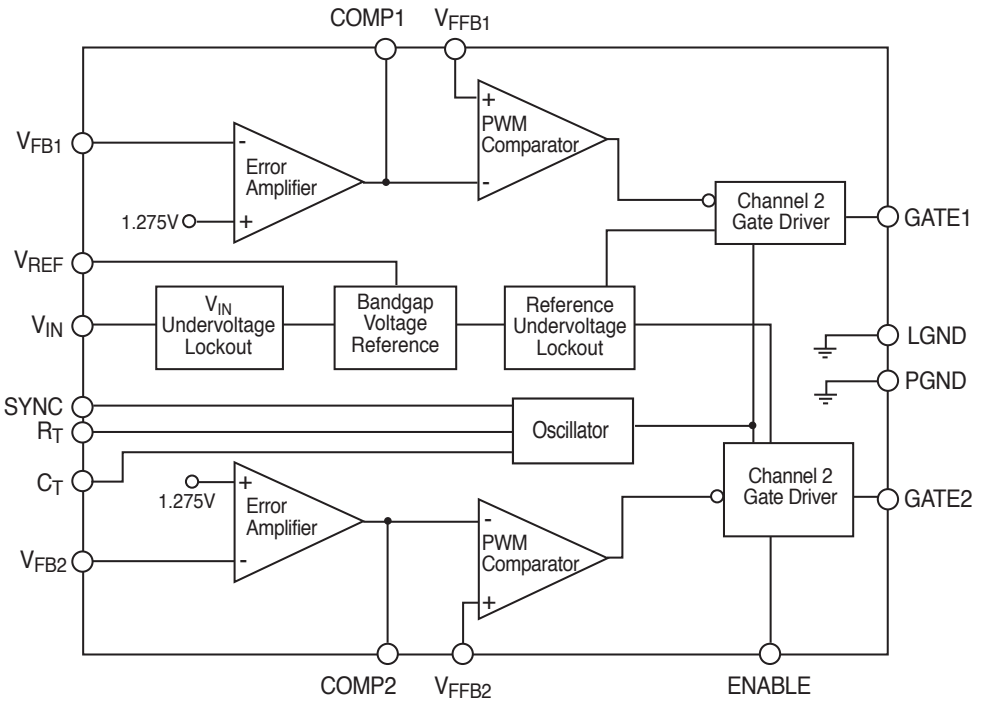
Electrical Characteristics: 0°C < T_A < 70°C; 0°C < T_J < 125°C; 9.4V < V_{IN} < 20V; C_T = 330 pF; R_T = 27kΩ; unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Error Amplifiers					
V_{FB} Reference Voltage	$V_{COMP} = V_{VFB}$	1.245	1.275	1.300	V
Input Bias Current	V_{FB} = 1.275V		0.1	1.0	µA
Open Loop Gain			85		dB
Unity Gain Bandwidth			1.0		MHz
PSRR	f = 120Hz		80		dB
COMP Source Current	V_{COMP} = 3V, V_{VFB} = 1.1V	0.9	1.3	2.0	mA
COMP Sink Current	V_{COMP} = 1.2V, V_{VFB} = 1.45V	10	16	24	mA
COMP Output Low Voltage	V_{VFB} = 1.45V, I_{COMP} = 0.3 mA	0.50	0.85	1.00	V
■ PWM Comparators					
V_{FFB} Bias Current	V_{FFB} = 0		2.0	20	µA
Propagation Delay	V_{FFB} rising to V_{GATE} falling		100	250	ns
Common Mode Maximum Input Voltage		2.9	3.3		V
■ ENABLE Lead					
ENABLE High Threshold	channel 2 enabled	1.5	2.5	3.5	V
ENABLE Bias Current	V_{ENABLE} = 0	100	250	400	µA
■ Gate Driver Outputs					
Output Low Saturation Voltage	I_{GATE} = 20 mA		0.1	0.4	V
	I_{GATE} = 100 mA		0.25	2.50	V
Output High Saturation Voltage	I_{GATE} = 20 mA		1.5	2.0	V
	I_{GATE} = 100 mA		1.6	3.0	V
Output Voltage under Lockout	V_{IN} = 6V, I_{GATE} = 1 mA		0.1	0.2	V
Output Rise Time	no load		30		ns
Output Fall Time	no load		10		ns
■ Undervoltage Lockout					
Turn On Threshold		7.4	8.4	9.4	V
Turn Off Threshold		6.8	7.8	8.8	V
■ Supply Current					
Start Up Current	V_{IN} = 6V		0.4	0.8	mA
Operating Current	V_{CT} = 0V, no load		17.5	25	mA

Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
16 Lead SO Wide		
1	SYNC	A pulse train on this lead will synchronize the oscillator. Sync threshold level is 2.4V. Synchronization frequency should be at least 10% higher than the regular operating frequency. The sync feature is level sensitive.
2	C_T	The oscillator integrating capacitor is connected to this lead.
3	R_T	The oscillator charge current setting resistor is connected to this lead.
4	V_{FB1}	The inverting input of the channel 1 error amplifier is brought out to this lead. The lead is connected to a resistor divider which provides a measure of the output voltage. The input is compared to a 1.275V reference, and channel 1 error amp output is used as the V^{2TM} PWM control voltage.
5	COMP1	Channel 1 error amp output and PWM comparator input.
6	V_{FFB1}	This lead connects to the non-inverting input of the channel 1 PWM comparator.
7	GATE1	This lead is the gate driver for the channel 1 FET. It is capable of providing nearly 1A of peak current.
8	LGND	This lead provides a "quiet" ground for low power circuitry in the IC. This lead should be shorted to the PGND lead as close as possible to the IC for best operating results.
9	PGND	This lead is the power ground. It provides the return path for the FET gate discharge. It should be shorted to the LGND lead as close as possible to the IC for best operating results.
10	GATE2	This lead is the gate driver for the channel 2 FET. See GATE1 lead description for more details.
11	V_{FFB2}	This lead connects to the non-inverting input of the channel 2 PWM comparator.
12	COMP2	Channel 2 error amp output and PWM comparator input.
13	V_{FB2}	Inverting input for the channel 2 error amp. See V_{FBI} for more details.
14	ENABLE	The regulator controlled by channel 2 may be turned on and off selectively by the user. Pulling the ENABLE lead above 3.5V will turn channel 2 on. Setting the ENABLE lead voltage below 1.5V guarantees that channel 2 is off.
15	V_{REF}	This lead is the output of a ± 3% reference. This reference drives most of the on-chip circuitry, but will provide a minimum of 10 mA to external circuitry if needed. The reference is inherently stable and does not require a compensation capacitor, but use of a decoupling capacitor will reduce noise in the IC.
16	V_{IN}	This lead is the power supply input to the IC. The maximum input voltage that can be withstood without damage to the IC is 20V.

Block Diagram



Theory of Operation

The CS5127 is a dual power supply controller that utilizes the V^{2TM} control method. Two nonsynchronous V^{2TM} buck regulators can be built using a single controller IC. This IC is a perfect choice for efficiently and economically providing core power and I/O power for the latest high-performance CPUs. Both switching regulators employ a fixed frequency architecture driven from a common oscillator circuit.

V^{2TM} Control Method

The V^{2TM} method of control uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current in the inductor and is offset by the DC output voltage. V^{2TM} inherently compensates for variation in both line and load conditions since the ramp signal is generated from the output voltage. This differs from traditional methods such as voltage mode control, where an artificial ramp signal must be generated, and current mode control, where a ramp is generated from inductor current.

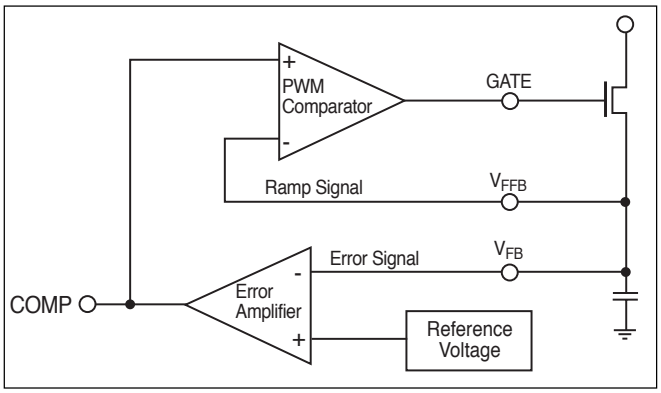


Figure 1: V^{2TM} control diagram.

The V^{2TM} control method is illustrated in Figure 1. Both the ramp signal and the error signal are generated by the output voltage. Since the ramp voltage is defined as the output voltage, the ramp signal is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the output switch from 0% to about 90% duty cycle.

Changes in line voltage will change the current ramp in the inductor, affecting the ramp signal and causing the V^{2TM} control loop to adjust the duty cycle. Since a change in inductor current changes the ramp signal, the V^{2TM} method has the characteristics and advantages of current mode control for line transient response.

Changes in load current will affect the output voltage and thus will also change the ramp signal. A load step will immediately change the state of the comparator output that controls the output switch. In this case, load transient response time is limited by the comparator response time and the transition speed of the switch. Notice that the reaction time of the V^{2TM} loop to a load transient is not dependent on the crossover frequency of the error signal loop. Traditional voltage mode and current mode methods are dependent on the compensation of the error signal loop.

The V^{2TM} error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The "slow" error signal loop provides DC accuracy. Low frequency roll-off of the error amplifier bandwidth will significantly improve noise immunity. This also improves remote sensing of the output voltage, since switching noise picked up in long feedback traces can be effectively filtered.

V^{2TM} line and load regulation are dramatically improved because there are two separate control loops. A voltage

Theory of Operation: continued

mode controller relies on a change in the error signal to indicate a change in the line and/or load conditions. The error signal change causes the error loop to respond with a correction that is dependent on the gain of the error amplifier. A current mode controller has a constant error signal during line transients, since the slope of the ramp signal will change in this case. However, regulation of load transients still requires a change in the error signal. V^{2TM} control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both.

Voltage Mode Control

The CS5127 can be operated in voltage mode if necessary. For example, if very small values of output ripple voltage are required, V^{2TM} control may not operate correctly. Details on how to choose the components for voltage mode operation are provided in the section on V_{FFB} component selection.

Constant Frequency

As output line and load conditions change, the V^{2TM} control loop modifies the switch duty cycle to regulate the output voltage. The CS5127 uses a fixed frequency architecture. Both output channels are controlled from a common oscillator. The CS5127 can typically provide a maximum duty cycle of about 90%.

Sync Function

It is sometimes desirable to shift the switching noise spectrum to different frequencies. A pulse train applied to the SYNC lead will terminate charging of the C_T lead capacitor and pull the C_T lead voltage to ground for the duration of the positive pulse level. This reduces the period of oscillation and increases the switching frequency. Synchronization must always be done at a frequency higher than the typical oscillator frequency. Using a lower frequency will lead to erratic operation and poor regulation. The SYNC pulse train frequency should be at least 10 % higher than the unsynchronized oscillator frequency. Synchronizing the oscillator will also decrease the maximum duty cycle. If the nominal oscillator frequency is 200kHz, increasing the oscillator frequency by 10% (to 220kHz) will decrease the maximum duty cycle from a typical of 90% to about 89%. Increasing the frequency by 25% (to 250kHz) will change the maximum duty cycle to about 87%. A 50% increase (to 300kHz) gives a maximum duty cycle of about 85%. The width of the SYNC pulse should be slightly shorter than the duration of the falling edge of the C_T lead waveform (see Figure 2a) so the SYNC pulse doesn't interfere with the oscillator function.

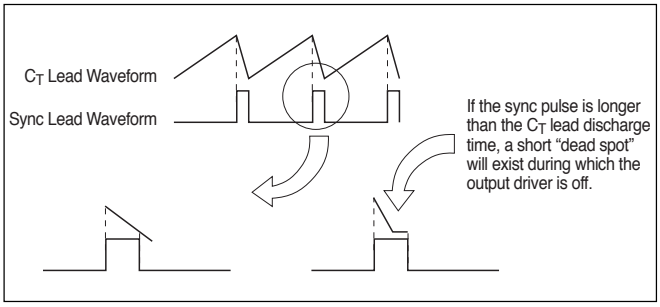


Figure 2a: Sync pulse duration vs. C_T lead discharge time.

The best way to determine if the pulse width is sufficiently short is to examine the C_T lead waveform with an oscilloscope. If "dead spots" are observed in the C_T lead waveform, decreasing the SYNC pulse width should be considered.

Alternatively, the SYNC signal may be AC coupled through a small capacitor. In this case, care must be taken to ensure that current pulled out of the IC during the high-to-low transition of the SYNC signal is limited to less than 5mA.

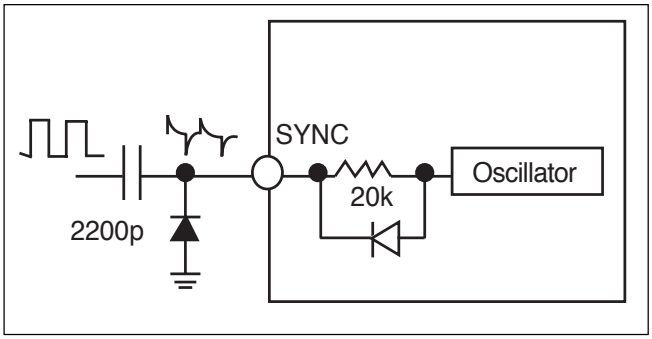


Figure 2b: Capacitive coupling of the SYNC signal. The external diode is used to clamp the IC substrate diode if I_{SYNC} is greater than 5mA during the negative portion of the input waveform.

Overcurrent Protection

The CS5127 has no on-board current limit circuitry. An example current limit circuit is provided in the Additional Application Circuits section of this data sheet.

Selection of Feedback Lead Divider Resistor Values

The feedback (V_{FB}) leads are connected to external resistor dividers to set the output voltage. The on-chip error amplifier is referenced to 1.275V, and the resistor divider values are determined by selecting the desired output voltage and the value of the divider resistor connected between the V_{FB} lead and ground.

Resistor R1 is chosen first based on a design trade-off of system efficiency vs. output voltage accuracy. Low values of divider resistance consume more current which decreases system efficiency. However, the V_{FB} lead has a 1μA maximum bias current which can introduce errors in the output voltage if large resistance values are used. The approximate value of current sinking through the resistor divider is given by

$$I_{V(FB)} = \frac{1.275V}{R1}$$

The output voltage error that can be expected due to the bias current is given by

$$\text{Error Percentage} = \frac{(1E - 6) \times R1}{1.275} \times 100\%$$

where R1 is given in ohms. For example, setting R1 = 5K yields an output voltage error of 0.39% while setting the feedback divider current at 255μA. Larger currents will result in reduced error.

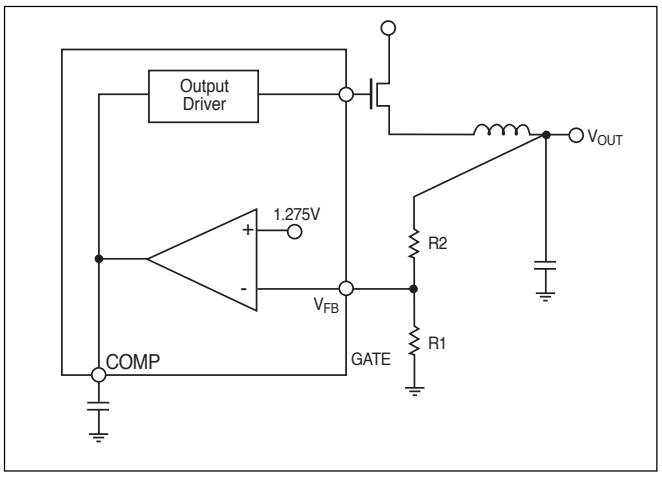


Figure 3: Feedback resistor divider.

R2 can be sized according to the following formula once the desired output voltage and the value of R1 have been determined:

$$R2 = R1\left(\frac{V_{OUT}}{1.275} - 1\right)$$

Selecting the Inductor

There are many factors to consider when choosing the inductor. Maximum load current, core losses, winding losses, output voltage ripple, short circuit current, saturation, component height, EMI/EMC and cost are all variables the designer must consider. Inductance values between 1μH and 50μH are suitable for use with the CS5127. Low values within this range minimize the component size and improve transient response, but larger values reduce ripple current. Choosing the inductor value requires the designer to make some choices early in the design. Output current, output voltage and the input voltage range should be known in order to make a good choice.

The input voltage range is bracketed by the maximum and minimum expected values of V_{IN}. Most computer applications use a fairly well-regulated supply with a typical output voltage tolerance on the order of ±5%. The values of $V_{IN(MAX)}$ and $V_{IN(MIN)}$ are used to calculate peak current and minimum inductance value, respectively. However, if the supply is well-regulated, these calculations may both be made using the typical input voltage value with very little error.

Current in the inductor while operating in the continuous current mode (CCM) is defined as the load current plus the inductor ripple current:

$$I_L = I_{OUT} + I_{RIPPLE}$$

The ripple current waveform is triangular, and the current is a function of the voltage across the inductor, the switch on-time and the inductor value. Switch on-time is the duty cycle divided by the operating frequency, and duty cycle can be defined as the ratio of V_{OUT} to V_{IN}, such that

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{f \times L \times V_{IN}}$$

The peak current can be described as the load current plus half of the ripple current. Peak current must be less than the maximum rated switch current. This limits the maximum load current that can be provided. It is also important that the inductor can deliver the peak current without saturating.

$$I_{OUT(MAX)} = I_{SWITCH(MAX)} - \frac{(V_{IN(MAX)} - V_{OUT})V_{OUT}}{2f \times L \times V_{IN(MAX)}}$$

Since the peak inductor current must be less than or equal to the peak switch current, the minimum value of inductance can be calculated:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{f \times V_{IN(MIN)} \times I_{SWITCH(MAX)}}$$

Load Current Transient Response

The theoretical limit on load current transient response is a function of the inductor value, the load transient and the voltage across the inductor. In conventionally-controlled regulators, the actual limit is the time required by the control loop. Conventional current-mode and voltage-mode control loops adjust the switch duty cycle over many oscillator periods, often requiring tens or even hundreds of

Applications Information: continued

microseconds to return to a steady-state. V^{2TM} control uses the ripple voltage from the output capacitor and a "fast" control loop to respond to load transients, with the result that the transient response of the CS5127 is very close to the theoretical limit. Response times are defined below.

$$t_{RESPONSE(INCREASING)} = \frac{L(\Delta I_{OUT})}{(V_{IN} - V_{OUT}) \times 0.85}$$

$$t_{RESPONSE(DECREASING)} = \frac{L(\Delta I_{OUT})}{V_{OUT}}$$

Note that the response time to a load decrease is limited only by the inductor value.

Other Inductor Selection Concerns

Inductor current rating is an important consideration. If the regulated output is subject to short circuit or overcurrent conditions, the inductor must be sized to handle the fault without damage. Sizing the inductor to handle fault conditions within the maximum DC current rating helps to ensure the coil doesn't overheat. Not only does this prevent damage to the inductor, but it reduces unwanted heat generated by the system and makes thermal management easier.

Selecting an open core inductor will minimize cost, but EMI/EMC performance may be degraded. This is a tough choice, since there are no guidelines to ensure these components will not prove troublesome.

Core materials influence the saturation current and saturation characteristics of the inductor. For example, a slightly undersized inductor with a powdered iron core may provide satisfactory operation because powdered iron cores have a "soft" saturation curve compared to other core materials.

Small physical size, low core losses and high temperature operation will also increase cost. Finally, consider whether an alternate supplier is an important consideration. All of these factors can increase the cost of the inductor.

Operating in Discontinuous Current Mode

For light load designs, the CS5127 will operate in discontinuous current mode (DCM). In this regime, external components can be smaller, since high power dissipation is not an issue. In discontinuous mode, maximum output current is defined as:

$$I_{OUT(MAX)} = \frac{(I_{PK})^2 f \times L(V_{IN})}{2V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}$$

where I_{PK} is the maximum current allowed in the switch FET.

Selecting the Output Capacitor

Output capacitors are chosen primarily on the value of equivalent series resistance, because this is what determines how much output ripple voltage will be present. Most polarized capacitors appear resistive at the typical oscillator frequencies of the CS5127. As a rule of thumb, physically larger capacitors have lower ESR. The capacitor's value in μF is not of great importance, and values from a few tens of μF to several hundreds of μF will work well. Tantalum capacitors serve very well as output capacitors, despite their bad reputation for spectacular failure due to excessive inrush current. This is not usually an issue for output capacitors, because the failure is not associated with discharge surges. Ripple current in the output capacitor is usually small enough that the ripple current rating is not an issue. The ripple current waveform is triangular, and the formula to calculate the ripple current value is:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{f \times L \times V_{IN}}$$

and output ripple voltage due to inductor ripple current is given by:

$$V_{RIPPLE(ESR)} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT} \times ESR}{f \times L \times V_{IN}}$$

A load step will produce an instantaneous change in output voltage defined by the magnitude of the load step, capacitor ESR and ESL.

$$\Delta V_O = (\Delta I_O \times ESD) + \frac{\Delta I}{\Delta T}\ ESL$$

A good practice is to first choose the output capacitor to accommodate voltage transient requirements and then to choose the inductor value to provide an adequate ripple voltage.

Increasing a capacitor's value typically reduces its ESR, but there is a limit to how much improvement can be had. In most applications, placing several smaller capacitors in parallel will result in acceptable ESR while maintaining a small PC board footprint. A warning is necessary at this point. The V^{2TM} topology relies on the presence of some amount of output ripple voltage being present to provide the input signal for the "fast" control loop, and it is important that some ripple voltage be present at the lightest load condition in normal operation to avoid subharmonic oscillation. Externally generated slope compensation can be added to ensure proper operation.

Selecting the V_{FFB} Lead Components

The V_{FFB} lead is tied to the PWM comparator's non-inverting input, and provides the connection for the externally-generated artificial ramp signal that is required whenever duty cycle is greater than 50%.

Applications Information: continued

The DC voltage for the V_{FFB} pin is usually provided from the output voltage through an RC filter if V_{OUT} is less than 3V. If V_{OUT} is greater than 2.9V, a resistor divider from V_{OUT} is recommended for proper circuit bias due to the common mode input range limitations of the PWM comparator. In most cases, the FB pin resistor divider can be used for this purpose with very little error, but a separate divider is recommended if high accuracy is required. The filter network is typically composed of a 1K resistor (R_{FFB}) and a 330 pF capacitor (C_{FFB}). This filter gives a 330 ns time constant which is sufficient to remove switching noise from the DC voltage. Note that in cases where a resistor divider provides the ramp signal, the resistor between V_{OUT} and the V_{FFB} pin serves as R_{FFB}. An artificial ramp signal is generated using an NPN transistor (Q1), a small coupling capacitor (CC) and a second resistor (RR). The NPN transistor collector is connected either to the external 5V supply or to the IC's 5V on-chip reference. The transistor's base is connected to the CT pin, and the ramp on the CT pin is used to provide the artificial ramp. The transistor's emitter is connected to the coupling capacitor. The capacitor value should provide a low impedance at the switching frequency. A 0.1 μF capacitor represents 6.4 ohms at 250 kHz. A resistor is placed in series between this capacitor and the V_{FFB} pin to set the amplitude of the ramp signal.

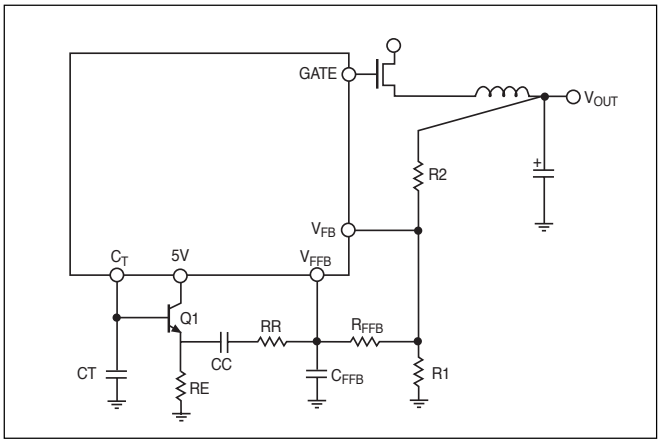


Figure 4: Artificial ramp components CC, C_{FFB}, RR and R_{FFB} must be provided for each channel if duty cycle for that channel exceeds 50%. Q1 and RE are common to both channels. DC voltage is shown supplied to V_{FFB} through the V_{FB} resistor divider.

The amount of artificial ramp is dependent on oscillator frequency, output voltage, output capacitor equivalent series resistance (ESR), and inductor value. It also assumes very small voltage fluctuations on the COMP pin. If the added ramp is too small, it will not be sufficient to prevent subharmonic oscillation. If the ramp is too large, V^{2TM} control will be defeated, and loop regulation will enter voltage mode control. DC regulation will be adequate, but transient response will be degraded. However, this may be desirable in cases where very low values of output ripple voltage are desired.

The artificial ramp amplitude can be calculated as follows:

$$V_{RAMP} = \frac{(R_{ESR})\ (V_{OUT})}{2000\ (L_{OUT})}$$

if DC voltage is provided from the output, or

$$V_{RAMP} = \frac{(R_{ESR})\ (V_{OUT})(R1)}{2000\ (L_{OUT})\ (R1 + R2)}$$

if DC voltage is provided from a resistor divider as in figure 5.

where R_{ESR} is the equivalent series resistance in ohms of the total output capacitance, V_{OUT} is the output voltage in volts and L_{OUT} is the inductor value in Henries. The result is V_{RAMP} given in millivolts per oscillator period. This value is the optimum amplitude for the artificial ramp. Note that COMP pin voltage changes and output ripple voltage must be added to the ramp amplitude for proper operation.

Once the total ramp signal has been determined, the value of the ramp resistor (RR) can be determined. The ramp resistor and filter resistor R_{FFB} create a resistor divider between the output voltage and the artificial ramp voltage. We can assume the output does not change, and that the maximum input voltage to the divider is equal to the DC output voltage plus the CT pin voltage swing of 2.1V. The ramp amplitude on the filter capacitor is then the divider output voltage:

$$V_{RAMP} = \frac{(2.1V)\ (R_{FFB})}{(RR + R_{FFB})}$$

Rearranging, we have

$$RR = R_{FFB}\left(\frac{2.1V}{V_{RAMP}} - 1\right)$$

Selecting the Catch Diode

The schottky "catch" diode must be capable of handling the peak inductor current and must withstand a reverse voltage at least equal to the value of V_{IN}. Since the catch diode only conducts during switch off-time, the average current through the catch diode is defined as:

$$I_{CATCH} = I_{OUT}\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

Minimizing the diode on-voltage will improve efficiency.

Selecting Oscillator Components R_T and C_T

The on-chip oscillator frequency is set by two external components. R_T sets the oscillator charge current. It is connected to a voltage reference approximately equal to 2.5V. The current generated in this fashion charges the C_T capacitor between threshold levels of 1.5V and 3.6V. C_T capacitor discharge is done by a saturating NPN, and the

Applications Information: continued

discharge time is typically less than 10% of the charge time. External components C_T and R_T allow the switching frequency to be set by the user in the range between 10kHz and 500kHz. C_T can be chosen first based on size and cost constraints. For proper operation over temperature, the value of R_T should be chosen within the range from 20kΩ to 40kΩ. Any type of one-eighth watt resistor will be adequate. Larger values of R_T will decrease the maximum duty cycle slightly. This occurs because the sink current on the C_T lead has an exponential relationship to the charge current. Higher charge currents will discharge the C_T lead capacitor more quickly than lower currents, and a shorter discharge time will result in a higher maximum duty cycle.

Once the oscillator frequency and a value of C_T have been selected, the necessary value of R_T can be calculated as follows:

$$R_T = \frac{1.88}{(f_{OSC})(C_T)}$$

where f_{OSC} is the oscillator frequency in hertz, C_T is given in farads, and the value of R_T is given in ohms. ESR effects are negligible since the charge and discharge currents are fairly small, and any type of capacitor is adequate for C_T.

Selecting the Compensation Capacitor

As previously noted, the error amplifier does not contribute greatly to transient response, but it does influence noise immunity. The fast feedback loop input is compared against the COMP pin voltage. The DC bias to the V_{FFB} pin may be provided directly from the output voltage, or through a resistor divider if output voltage is greater than 2.9V. The desired percentage value of DC accuracy translates directly to the V_{FFB} pin, and the minimum COMP pin capacitor value can be calculated:

$$C_{COMP} = \frac{(16mA)(T_{OSC})}{(V_{FFB}\text{DC Bias Voltage})(\text{tolerance})}$$

If f_{OSC} = 200kHz, V_{FFB} DC bias voltage is 2.8V and tolerance is 0.1%, C_{COMP} = 28.6μF. This is the minimum value of COMP pin capacitance that should be used. It is a good practice to guard band the tolerance used in the calculation. Larger values of capacitance will improve noise immunity, and a 100μF capacitor will work well in most applications.

The type of capacitor is not critical, since the amplifier output sink current of 16mA into a fairly large value or wide range of ESR will typically result in a very small DC output voltage error. The COMP pin capacitor also determines the length of the soft start interval.

Selecting the Input Bypass Capacitor

The input bypass capacitors minimize the ripple current in the input supply, help to minimize EMI, and provide a charge reservoir to improve transient response. The capacitor ripple current rating places the biggest constraint on component selection. The input bypass capacitor network should conduct all the ripple current. RMS ripple current can be as large as half the load current, and can be calculated as:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}^2}}$$

Peak current requirement, load transients, ambient operating temperature and product reliability requirements all play a role in choosing this component. Capacitor ESR and the maximum load current step will determine the maximum transient variation of the supply voltage during normal operation. The drop in the supply voltage due to load transient response is given as:

$$\Delta V = I_{RIPPLE(RMS)} \times ESR$$

The type of capacitor is also an important consideration. Aluminum electrolytic capacitors are inexpensive, but they typically have low ripple current ratings. Choosing larger values of capacitance will increase the ripple current rating, but physical size will increase as well. Size constraints may eliminate aluminum electrolytics fro consideration. Aluminum electrolytics typically have shorter operating life because the electrolyte evaporates during operation. Tantalum electrolytic capacitors have been associated with failure from inrush current, and manufacturers of these components recommended derating the capacitor voltage by a ratio 2:1 in surge applications. Some manufacturers have product lines specifically tested to withstand high inrush current. AVX TPS capacitors are one such product. Ceramic capacitors perform well, but they are also large and fairly expensive.

Startup

At startup, output switching does not occur until two undervoltage lockouts release. The first lockout monitors the V_{IN} lead voltage. No internal IC activity occurs until V_{IN} lead voltage exceeds the V_{IN} turn-on threshold. This threshold is typically 8.4V. Once this condition is met, the on-chip reference turns on. As the reference voltage begins to rise, a second undervoltage lockout disables switching until V_{REF} lead voltage is about 3.5V. The GATE leads are held in a low state until both lockouts are released.

As switching begins, the V_{FB} lead voltage is lower than the output voltage. This causes the error amplifier to source current to the COMP lead capacitor. The COMP lead voltage will begin to rise. As the COMP lead voltage begins to rise, it sets the threshold level at which the rising V_{FFB} lead voltage will trip the PWM comparator and terminate switch conduction. This process results in a soft start interval. The DC bias voltage on V_{FFB} will determine the final COMP voltage after startup, and the soft start time can be approximately calculated as:

$$T_{SOFT\ START} = \frac{V_{FFB} \times C_{COMP}}{I_{COMP(SOURCE)}}$$

Applications Information: continued

where $T_{SOFT\ START}$ is given in seconds if C_{COMP} is given in farads, $I_{COMP(SOURCE)}$ in amperes, and V_{FFB} in volts. Note that a design trade off will be made in choosing the value of the COMP lead capacitor. Larger values of capacitance will result in better regulation and improved noise immunity, but the soft start interval will be longer and capacitor price may increase.

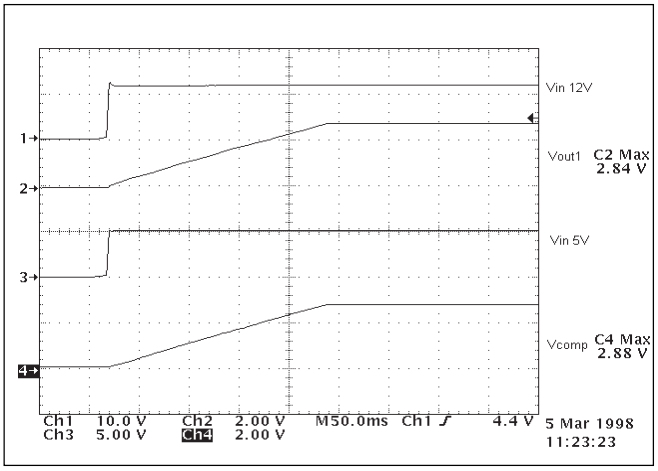


Figure 5: Measured performance of the CS5127 at start up.
C_{COMP} =100µF, $I_{COMP(SOURCE)}$=1.3mA, V_{FFB} = 2.8V, $T_{SOFTSTART}$ = 0.22s.

Normal Operation

During normal operation, the gate driver switching duty cycle will remain approximately constant as the V²™ control loop maintains the regulated output voltage under steady state conditions. Changes in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Voltage Mode Control

Voltage Mode Operation

There are two methods by which a user can operate the CS5127 in voltage mode. The first method is simple, but the transient response is typically very poor. This method uses the same components as V²™ operation, but by increasing the amplitude of the artificial ramp signal, V²™ control is defeated and the controller operates in voltage mode. Calculate RR using the formula above and divide the value obtained by 10. This should provide an adequately large artificial ramp signal and cause operation under voltage mode control. There may be some dependence on board layout, and further optimization of the value for RR may be done empirically if required.

Voltage mode control may be refined by removing the COMP pin capacitor and adding a two pole, one zero compensation network. Consider the system block diagram shown in figure 6.

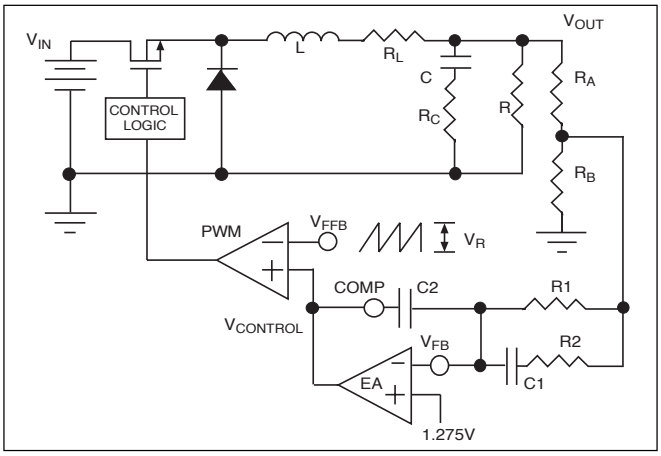


Figure 6: Voltage mode control equivalent circuit with two pole, one zero compensation network.

V_{IN} is the switch supply voltage, R represents the load, RL is the combined resistance of the FET RDS (on) and the inductor DC resistance, L is the inductor value, C is the output capacitance, RC is the output capacitor ESR, RA and RB are the feedback resistors and VR is the peak to peak amplitude of the artificial ramp signal at the V_{FFB} pin. C1, C2, R1 and R2 are the components of the compensation network. Based on the application circuit from page 1, values for the 2.8V output equivalent circuit are:

V_{IN} = 5V
R = 0.4Ω
RL = 0.02Ω
C = 1320µF
RC = 0.025Ω
RA = 1540Ω
RB = 1270Ω
L = 5µH

A resistor change is necessary to increase the artificial ramp magnitude to V_{FFB1}. Changing R10 from 20k to 2k will give a peak to peak amplitude of about 2V. Thus, V_R = 2V.

The transfer function from $V_{CONTROL}$ to V_{OUT} is

$$\frac{V_{OUT}}{V_{CONTROL}} = \frac{R \times V_{IN} \times (sCR_C + 1)}{s^2LC\,(R + R_C) + s[L + R_LC(R + R_C) + RCR_C] + R + R_C} \times \frac{1}{V_R}$$

Using the component values provided, this reduces to

Applications Information: continued

$$\frac{1 + s(3.3E\text{-}5)}{s^2(2.772E\text{-}9) + s(2.902E\text{-}5) + 0.42}$$

The zero frequency due to the output capacitor ESR is given as

$$\frac{1}{(2\pi CR_C)} = 4.8 \text{ kHz.}$$

The double pole frequency of the power output stage is

$$\frac{1}{(2\pi)} = \frac{R + R_1}{LC(R + R_C)} = 1.95 \text{ kHz.}$$

The ESR zero approximately cancels one of the poles, and the total phase shift is limited to 90. Bode plots are provided below.

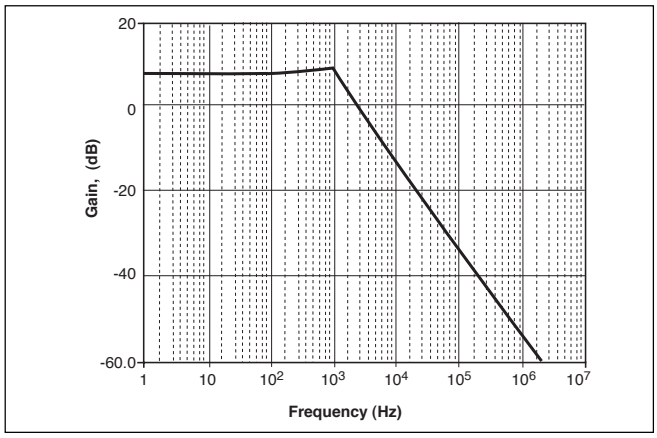


Figure 7: Bode plot of gain response for $V_{OUT}/V_{CONTROL}$.

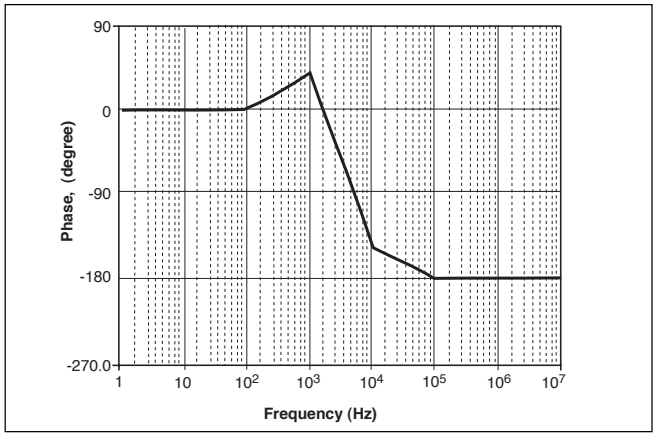


Figure 8: Bode plot of phase response for $V_{OUT}/V_{CONTROL}$.

This uncompensated system is stable, but the low gain will result in poor DC accuracy, and the low cutoff frequency will result in poor transient response. Note that we have not yet included the gain factor from the feedback resistor divider. This factor will further reduce the overall system gain.

By adding the two pole, one zero compensation network shown in figure 6, we can maximize the DC gain and push out the crossover frequency. The transfer function for the compensation network is

$$\frac{V_{CONTROL}}{V_{FB}} = \frac{s\ C1(R1 + R2) + 1}{-s\ C2\ R1(s\ C1\ R2 + 1)}$$

This can be rewritten in terms of pole and zero frequencies and a gain constant A.

$$\frac{V_{CONTROL}}{V_{FB}} = \frac{s/(2\pi f_Z + 1)}{-A\ s\ ((s/2f_P) + 1)}$$

where $$f_Z = \frac{1}{(2\pi\ C1\ (R1 + R2))}$$

$$f_P = \frac{1}{2\pi\ C1R2} \text{ and } A = R1\ C2$$

Note that, due to the first s term in the denominator, a pole is located at f = 0. This will provide the maximum DC gain.

The optimum performance can be obtained by choosing f_Z equal to the output double pole frequency and setting f_P to approximately half of the switching frequency. Gain factors can be chosen somewhat arbitrarily.

Values between
1E-6ΩF and 20E-6ΩF are practical. We then have a set of equations that can be solved for component values:

$$C1\ R1 = \frac{1}{2\pi}\left[\frac{1}{f_Z} - \frac{1}{f_P}\right],\ C1\ R2 = \frac{1}{2\pi f_P},\ C2 = \frac{A}{R1}$$

Since there are only three equations, we must arbitrarily choose one of the components. One option is to set the value of R1 fairly large. This provides a high impedance path between the V_{FB} pin and the COMP pin.

For our design, we have f_Z = the double pole frequency = 1.95 kHz and $f_P = f_{OSC}/2$ = 100kHz. Let's arbitrarily choose R1 = 4.7K. Then we solve the first equation for C1 and obtain C1 = 17nF. Use a standard value of 22 nF.

We next solve for R2. With C1 =22 nF, R2= 72Ω. Use a standard value of 75Ω.

We can choose a gain factor from somewhere in the middle of our range and solve for C2. If A = 10E-6ΩF, we have

C2 = 2.1 nF. Use a standard value of 2.2 nF.

Applications Information: continued

Now that we have the compensation components chosen, we can put together a transfer function for the entire control loop. The transfer function is the product of the VOUT to $V_{CONTROL}$ transfer function, the gain of the feedback resistor divider and the negative inverse of the compensation loop transfer function. That is,

$$T_{LOOP} = - (T_{VC\text{-}VO} \times T_{DIVIDER} \times T_{COMPENSATION})$$

or

$$T_{LOOP} = \left[\frac{R \times V_{IN} \times (sCR_C + 1)}{s^2LC\,(R + R_C) + s[L + R_LC(R + R_C) + RCR_C] + R + R_C}\right] \times \left[\frac{1}{V_R}\right] \times \left[\frac{RB}{RA + RB}\right] \times \left[\frac{sC1\,(R1 + R2) + 1}{sC2\,R1\,(sC1\,R2 + 1)}\right]$$

Bode plots for this transfer function are shown below.

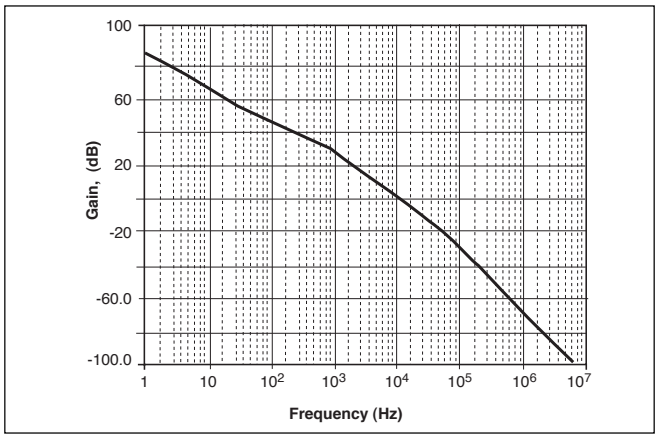


Figure 9: Bode plot of gain response for compensated voltage mode system.

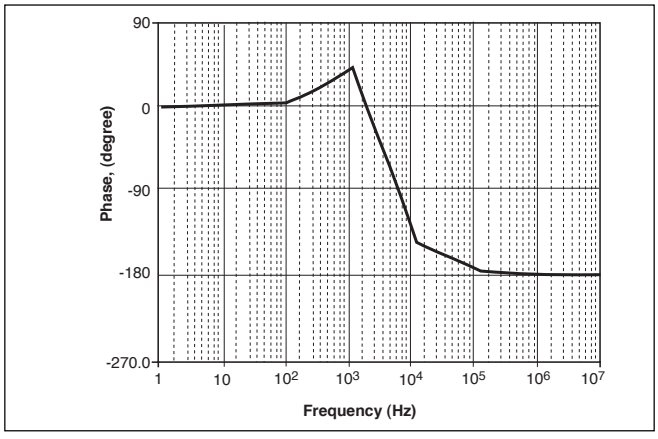


Figure 10: Bode plot of phase response for compensated voltage mode system.

Entering the loop transfer function in a mathematics program or a spreadsheet and evaluating the performance from resulting Bode plots may help to further optimize the compensation network component values.

Compensation may be further optimized by using a two pole–two zero compensation network as shown below.

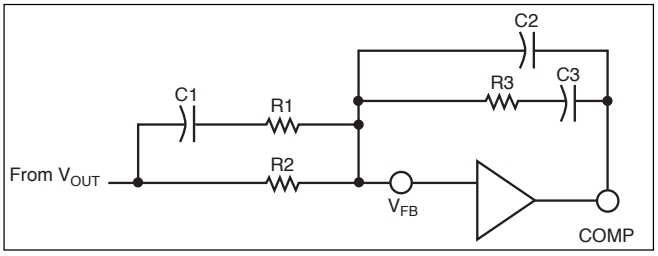


Figure 11: Two pole–two zero compensation network.

The two zeros are placed close to the resonant frequency of the LC output circuit. That is,

$$\frac{1}{2\pi\sqrt{LC}} \approx \frac{1}{2\pi\,C1\,R2} \approx \frac{1}{2\pi\,R3\,C3}$$

The two poles are placed near half the switching frequency, or

$$\frac{f_{SW}}{2} \approx \frac{1}{2\pi\,C1\,R1} \approx \frac{1}{2\pi\,R3\,C2}$$

Channel 2 ENABLE Feature

The ENABLE lead controls operation of channel 2. Channel 2 operates normally if the ENABLE lead voltage is greater than 3.5V. Setting the ENABLE lead voltage below 1.5V will guarantee that channel 2 is disabled. In this case, the GATE2 lead will be held low and no switching will occur. This feature can be used to selectively power up or power down circuitry that may not always need to be on. For example, in a laptop computer, channel 1 could power the microprocessor while channel 2 controlled the disk drive. Channel 2 could be turned off if the drive was not in use.

Thermal Management for Semiconductor Components

Semiconductor components will deteriorate in high temperature environments. It is necessary to limit the junction temperature of control ICs, power MOSFETs and diodes in order to maintain high levels of reliability. Most semiconductor devices have a maximum junction temperature of 125°C, and manufacturers recommend operating their products at lower temperatures if at all possible.

Power dissipation in a semiconductor device results in the generation of heat in the pin junctions at the surface of the

Applications Information: continued

IC. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the thermal properties of the package molding compound. The magnitude of this thermal gradient is denoted in manufacturer's data sheets as Θ_{JA} , or junction-to-air thermal resistance. The on-chip junction temperature can be calculated if Θ_{JA} , the air temperature at the IC's surface and the on-chip power dissipation are known:

$$T_J = T_A + (\Theta_{JA} \times P)$$

T_J and T_A are given in degrees centigrade, P is IC power dissipation in watts and Θ_{JA} is thermal resistance in degrees centigrade per watt. Junction temperature should be calculated for all semiconductor devices to ensure they are operated below the manufacturer's maximum junction temperature specification. If any component's temperature exceeds the manufacturer's maximum specification, some form of heatsink will be required.

Heatsinking will improve the thermal performance of any IC. Adding a heatsink will reduce the magnitude of Θ_{JA} by providing a larger surface area for heat transfer to the surrounding air. Typical heat sinking techniques include the use of commercial heatsinks for devices in TO-220 packages, or printed circuit board techniques such as thermal bias and large copper foil areas for surface mount packages.

When choosing a heatsink, it is important to break Θ_{JA} into several different components.

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$$

where all components of Θ_{JA} are given in °C/W.

Θ_{JC} is the thermal impedance from the junction to the surface of the package case. This parameter is also included in manufacturer's data sheets. Its value is dependent on the mold compound and lead frames used in assembly of the semiconductor device in question.

Θ_{CS} is the thermal impedance from the surface of the case to the heatsink. This component of the thermal impedance can be modified by using thermal pads or thermal grease between the case and the heat sink. These materials replace the air gap normally found between heatsink and case with a higher thermal conductivity path. Values of Θ_{CS} are found in catalogs published by manufacturers of heatsinks and thermal compounds.

Finally, Θ_{SA} is the thermal impedance from the heatsink to ambient temperature. Θ_{SA} is the important parameter when choosing a heatsink. Smaller values of Θ_{SA} allow higher power dissipation without exceeding the maximum junction temperature of the semiconductor device. Values of Θ_{SA} are typically provided in catalogs published by heatsink manufacturers.

The basic equation for selecting a heatsink is

$$P_D = \frac{T_J - T_A}{\Theta_{JC} + \Theta_{CS} + \Theta_{SA}}$$

where P_D is on-chip power dissipation in watts, T_J is junction temperature in °C, T_A is ambient temperature in°C, and thermal impedance Θ_{JC} , Θ_{CS} , and Θ_{SA} are in°C/W. All these quantities can be calculated or obtained from data sheets. The choice of a heatsink is based on the value of Θ_{SA} required such that the calculated power dissipation does not cause junction temperature to exceed the manufacturer's maximum specification.

EMI Management

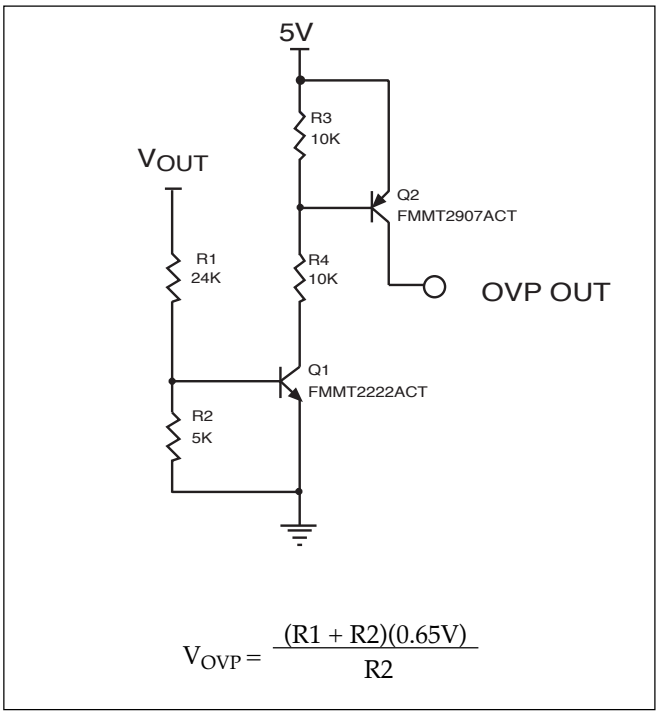
Switching regulators generate noise a consequence of the large values of current being switched on and off in normal operation. Careful attention to layout of the printed circuit board will usually minimize noise problems. Layout guidelines are provided in the next section. However, it may be necessary in some cases to add filter inductors or bypass capacitors to the circuitry to achieve the desired performance.

Layout Considerations

The following guidelines should be observed in the layout of PC boards for the CS5127:

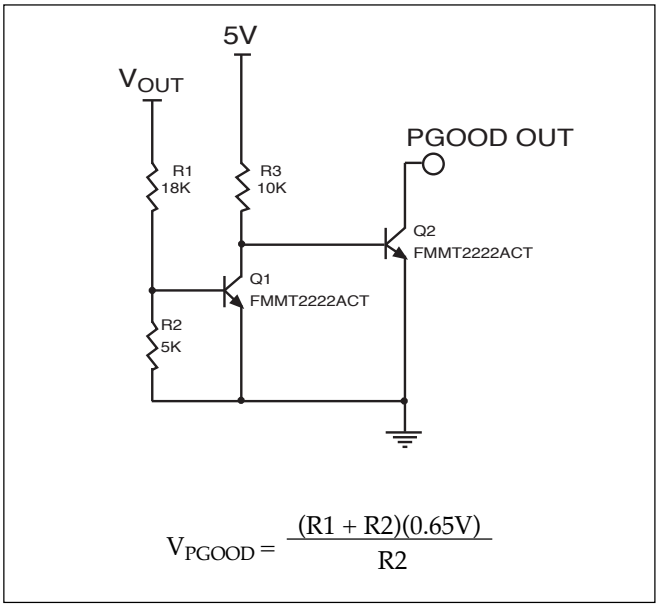
1. Connect the PGND lead to the external ground with a wide metal trace.
2. Connect both LGND and PGND together with a wide trace as close to the IC as possible.
3. Make all ground connections to a common ground plane with as few interruptions as possible. Breaks in the ground plane metal should be made parallel to an imaginary line between the supply connections and the load.
4. Connect the ground side of the COMP lead capacitors back to LGND with separate traces.
5. Place the V_{FFB} lead capacitors as close to the V_{FFB} leads as possible.
6. Place the 5V line bypass capacitors as close to the switch FETs as possible.
7. Place the output capacitor network as close to the load as possible.
8. Route the GATE lead signals to the FET gates with a metal trace at least 0.025 inches wide.
9. Use wide straight metal traces to connect between the 5V line and FETs, between FETs and inductors and between inductors and loads to minimize resistance in the high current paths. Avoid sharp turns, loops and long lengths.

Additional Application Circuits



$$V_{OVP} = \frac{(R1 + R2)(0.65V)}{R2}$$

Figure 12: Example external over voltage protection circuit. If V_{OUT} exceeds V_{OVP}, OVP out goes high. Resistor values shown above provide a +10% tolerance for a 3.3V output.



$$V_{PGOOD} = \frac{(R1 + R2)(0.65V)}{R2}$$

Figure 13: Example external Power GOOD circuit. $P_{GOOD(OUT)}$ is low until V_{OUT} exceeds V_{PGOOD}. V_{PGOOD} is typically chosen to be 10% below nominal V_{OUT}. Resistor values above provide a -10% tolerance on V_{OUT} =3.3V.

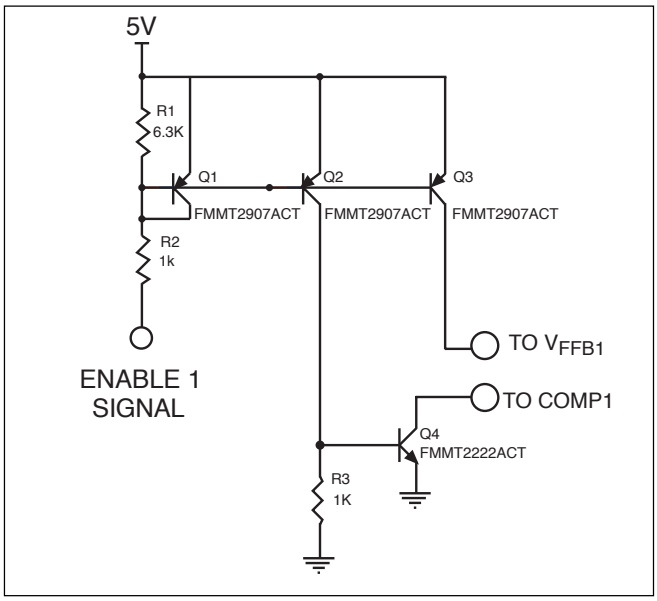


Figure 14: An external circuit can be built to provide an enable function for channel 1. The circuit shown above connects to the V_{FB1} and COMP1 pins as indicated. If the ENABLE1 signal is left floating or is pulled high, channel 1 is enabled. If the ENABLE1 pin is pulled below 1V, Q1 will conduct, and mirror Q3 pulls V_{FFB1} up at the same time as Q2 and Q4 pull COMP1 low. This will force GATE1 to go low and turn off the switch FET. The circuit above will provide about 1mA of additional drive to the V_{FFB1} pin components. This additional current must be sufficient to pull V_{FFB1} up to about 1V in order to guarantee GATE1 is held low.

Additional Application Circuits continued

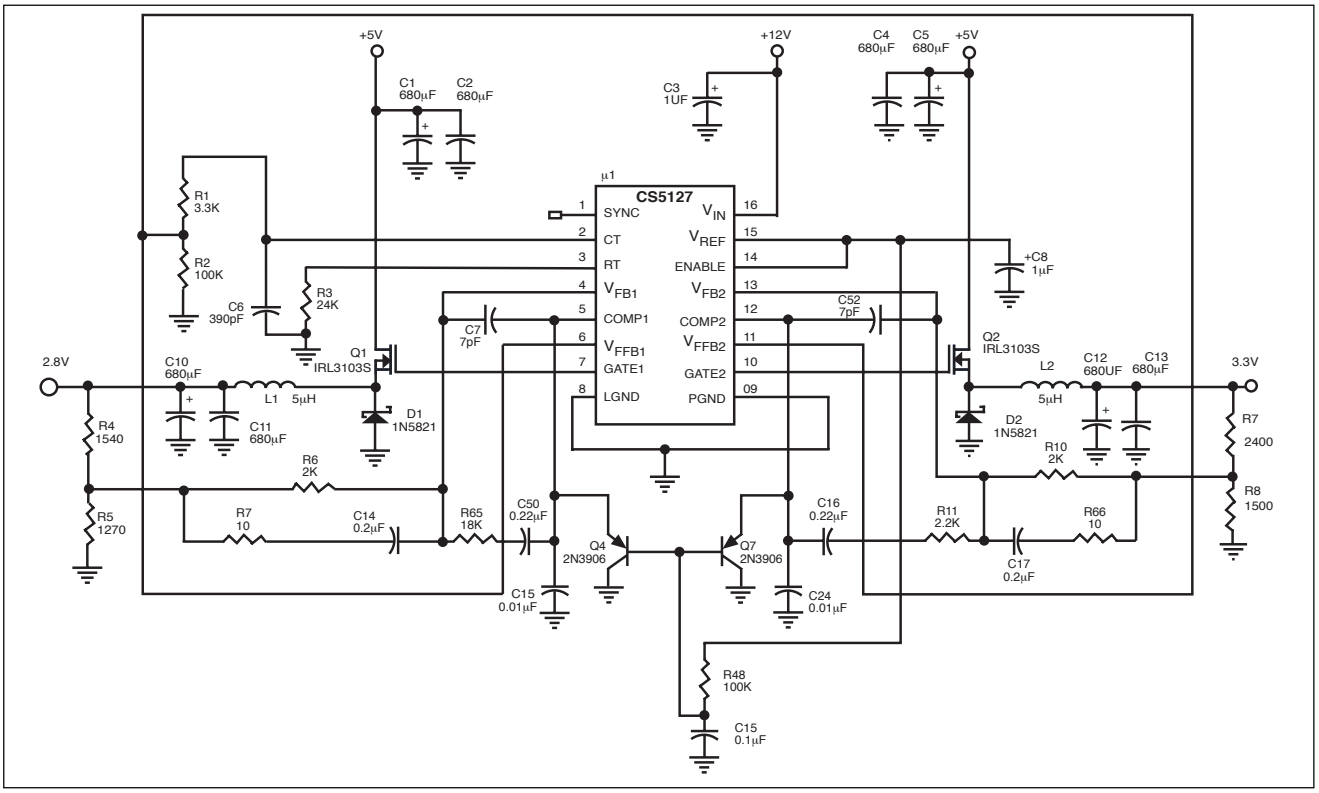


Figure 15: CS5127 12V, 5V input to 2.8V @ 7A and 3.3V @ 7A Voltage Mode Control Application Circuit with External Soft Start.

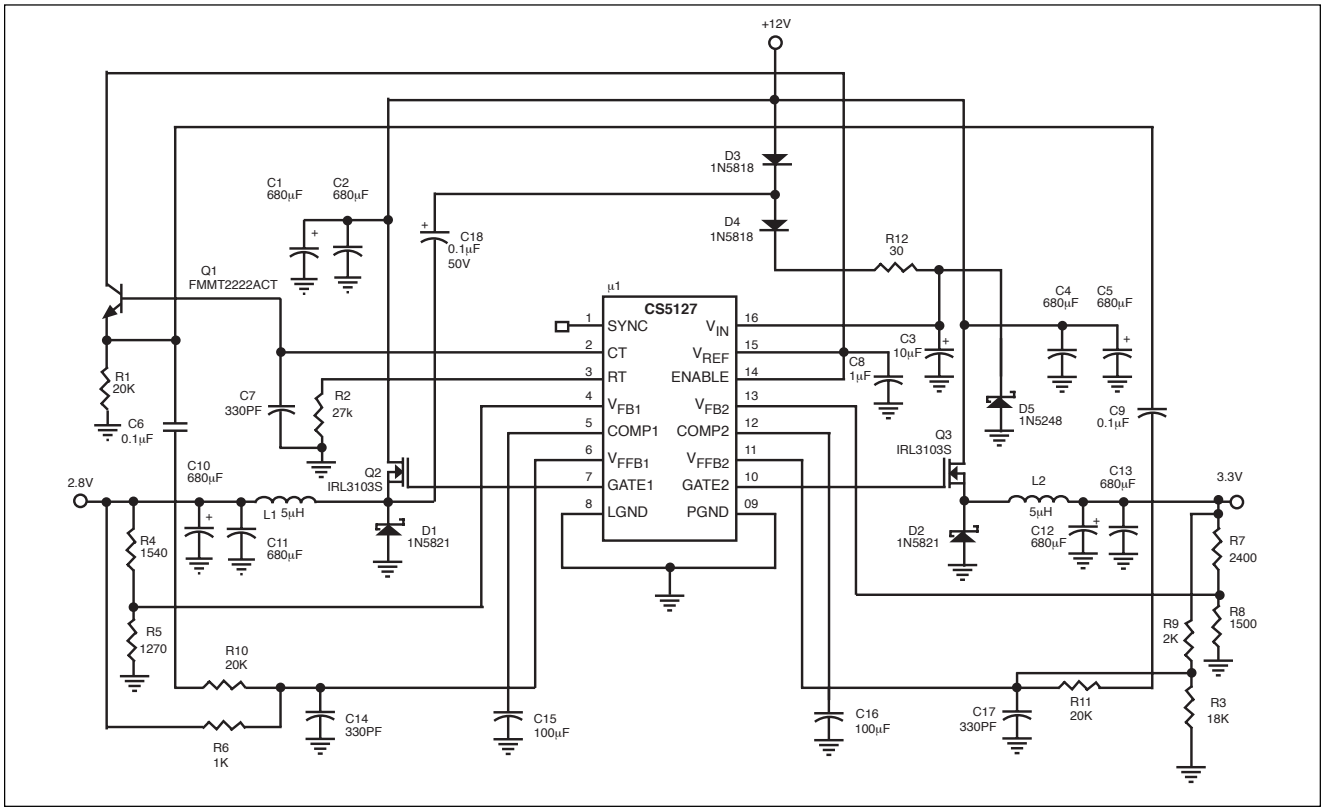


Figure 16: CS5127 12V only to 2.8V @ 7A and 3.3V @ 7A Application Circuit.

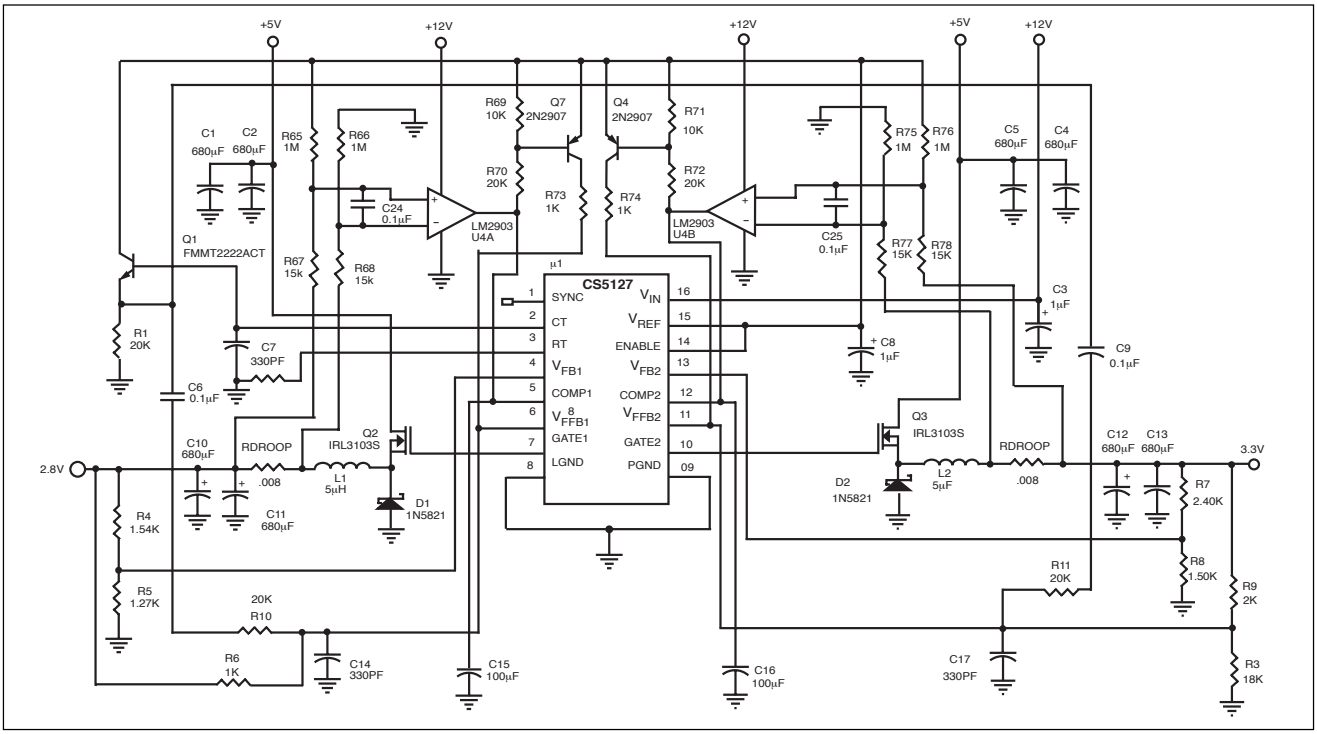


Figure 17: 200kHz, V²™, 5V/12V input, 2.8V@ 7A and 3.3V @ 7A outputs with current limit.

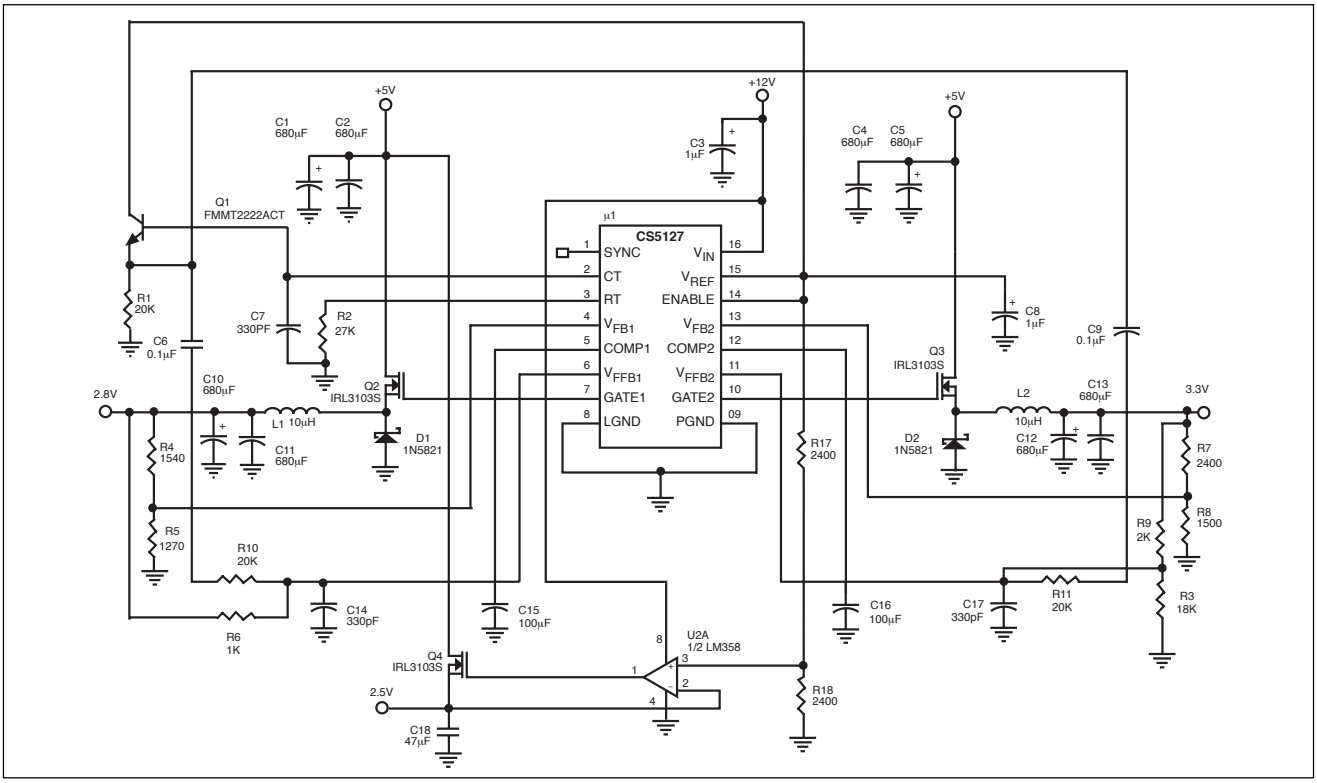


Figure 18: CS5127 12V, 5V input to 2.8V @7A and 3.3V @ 7A Switching Regulator with External 1A, 2.5V Linear Output for Vclock.

Typical Performance Characteristics

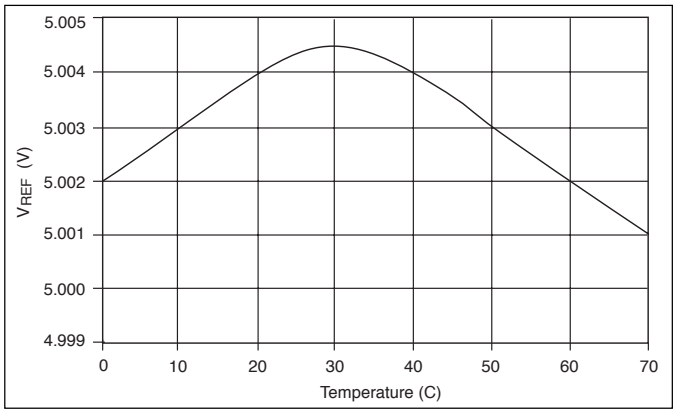


Figure 19: V_{REF} vs Temperature, 1mA Load.

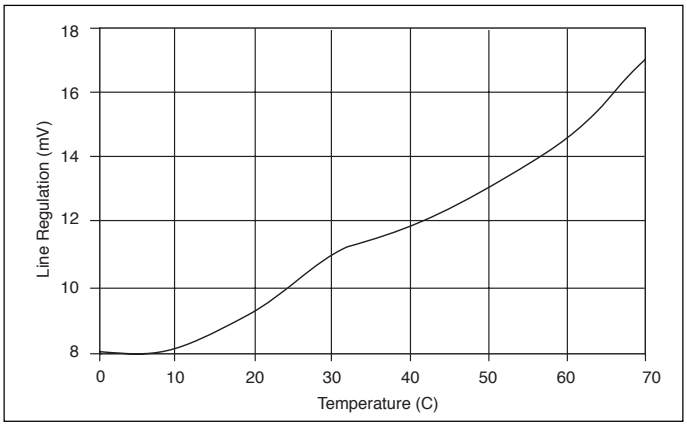


Figure 22: Line Regulation vs Temperature 9V to 20V.

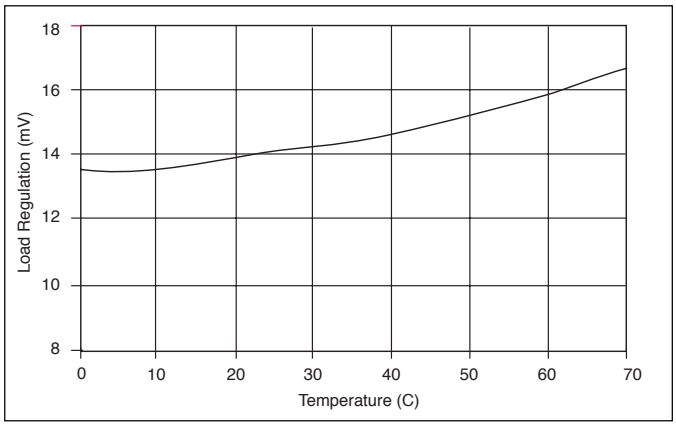


Figure 20: Load Regulation vs Temperature 1mA to 10mA.

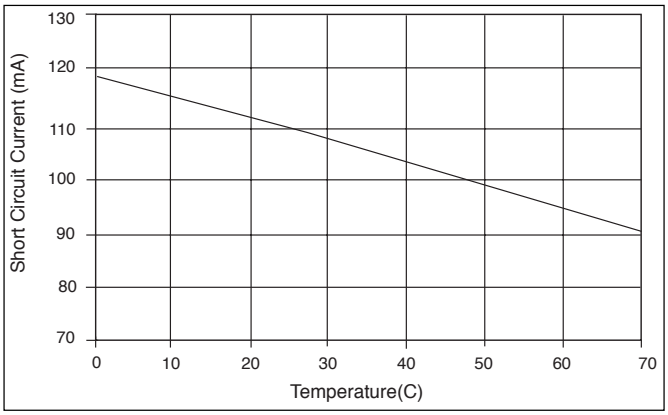


Figure 23: V_{REF} Short Circuit Current vs Temperature.

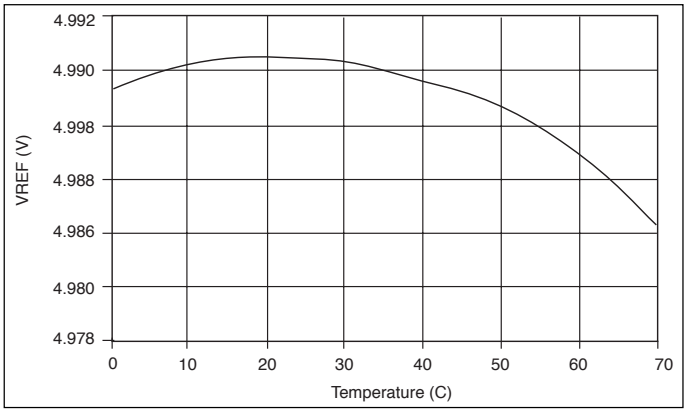


Figure 21: V_{REF} vs Temperature, 10mA Load.

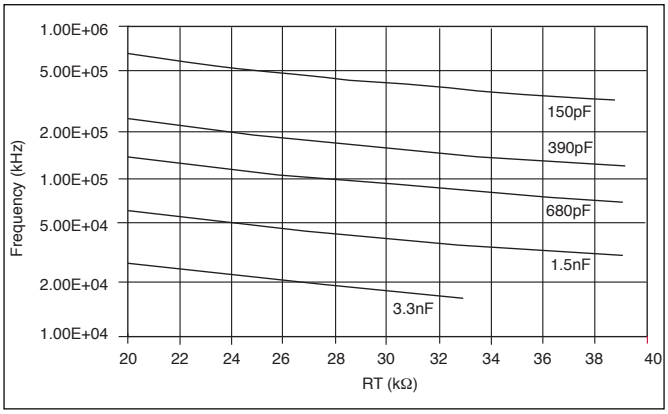


Figure 24: Oscillator Frequency vs R_T,C_T (V_{IN} = 12V, T = 25C)

Typical Performance Characteristics: continued

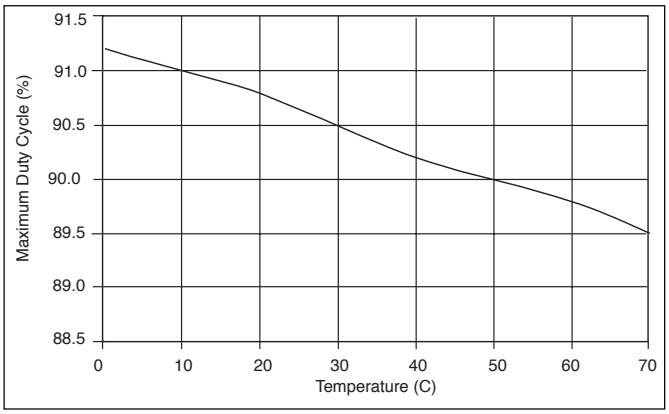


Figure 25: Oscillator Maximum Duty Cycle vs Temperature.

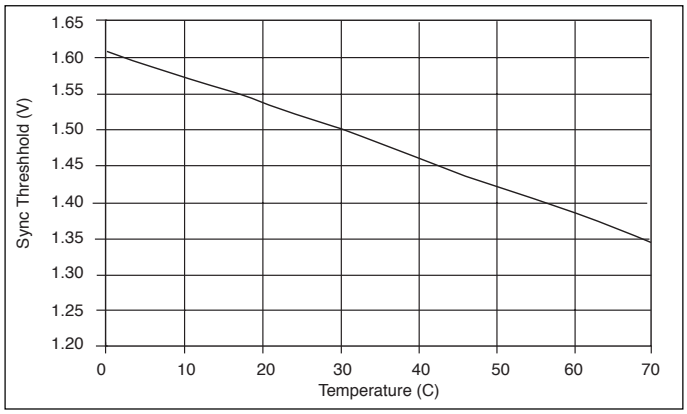


Figure 28: SYNC Threshold vs Temperature.

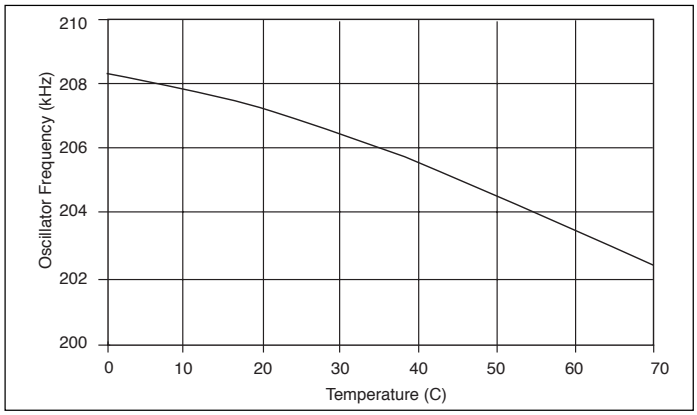


Figure 26: Oscillator Frequency vs Temperature. C_T = 330pF, R_T =27k

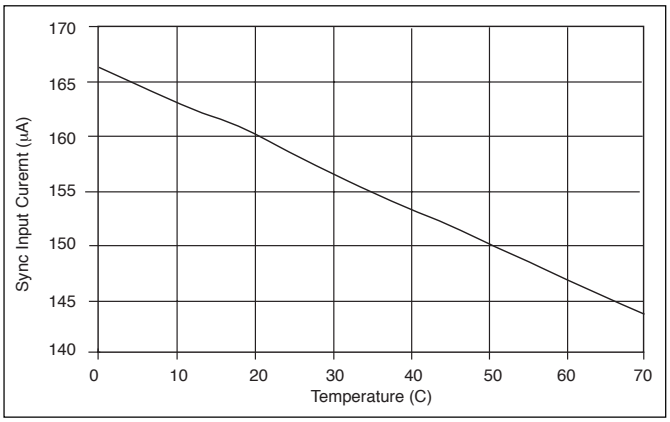


Figure 29: SYNC Input Current vs Temperature (V_{SYNC} = 2.4V).

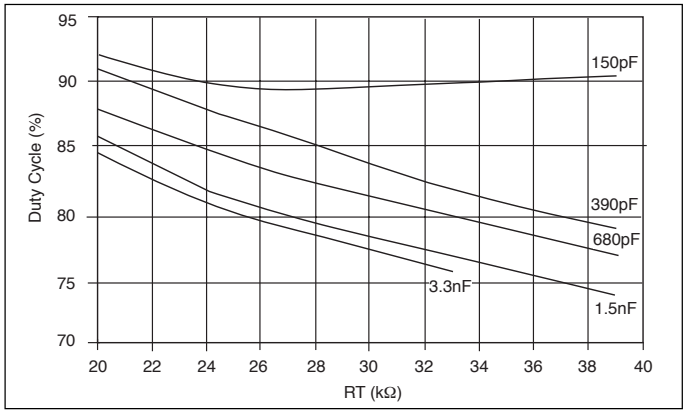


Figure 27: Oscillator Duty Cycle vs C_T, R_T (V_{IN} = 12V, T = 25C).

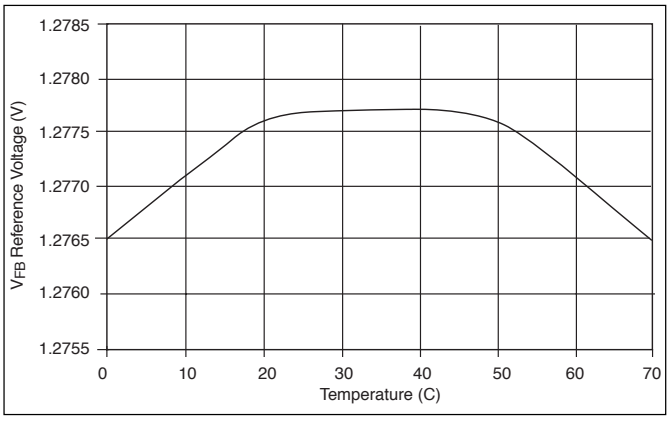


Figure 30: V_{FB} Reference Voltage vs Temperature.

Typical Performance Characteristics: continued

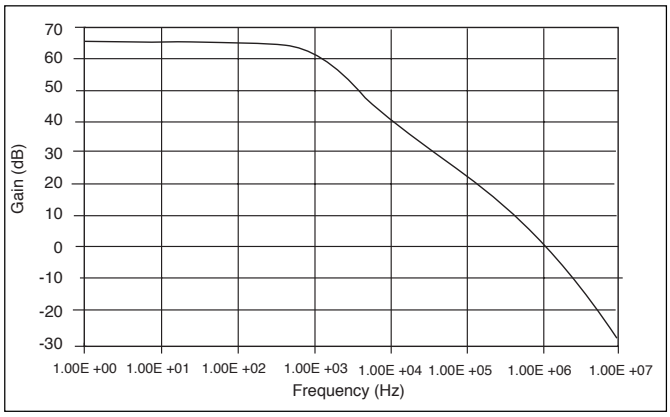


Figure 31: Error Amplifier Gain vs Frequency.

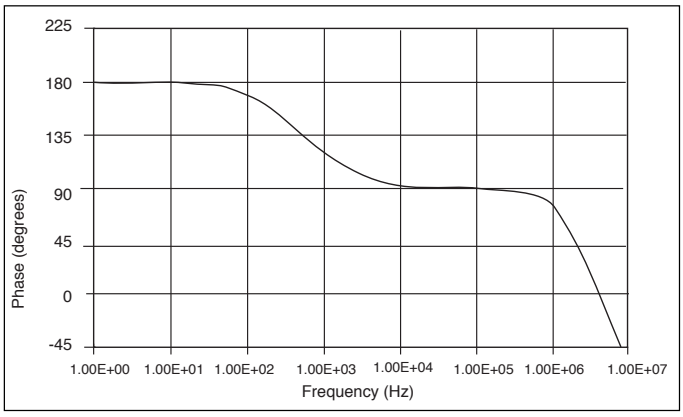


Figure 34: Error Amplifier Phase vs Frequency.

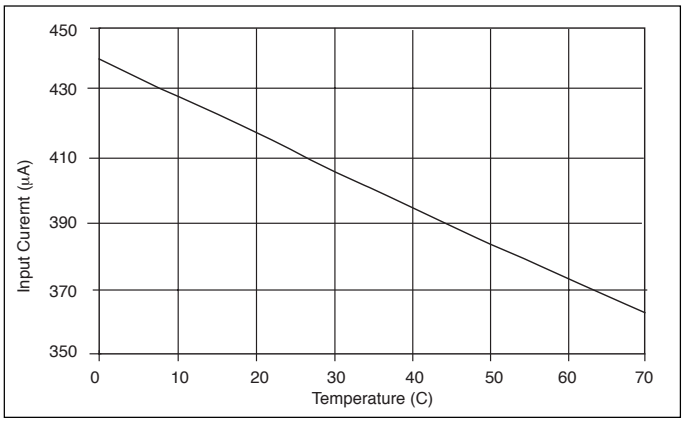


Figure 32: SYNC Input Current vs Temperature (V_{SYNC} = 5V).

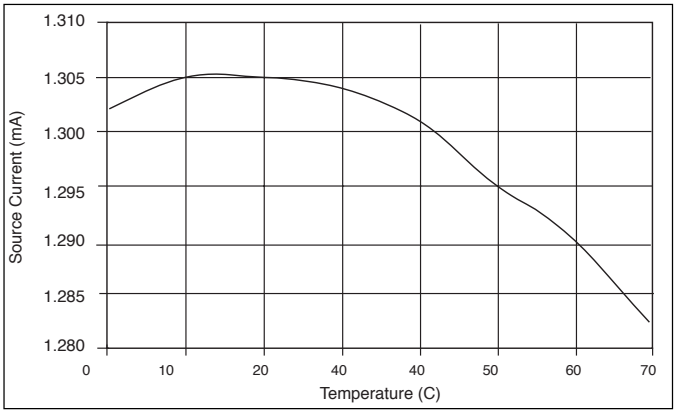


Figure 35: Error Amplifier Source Current vs Temperature.

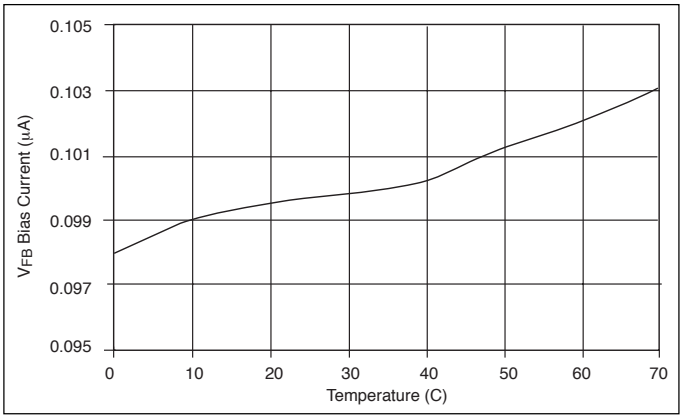


Figure 33: V_{FB} Bias Current vs Temperature.

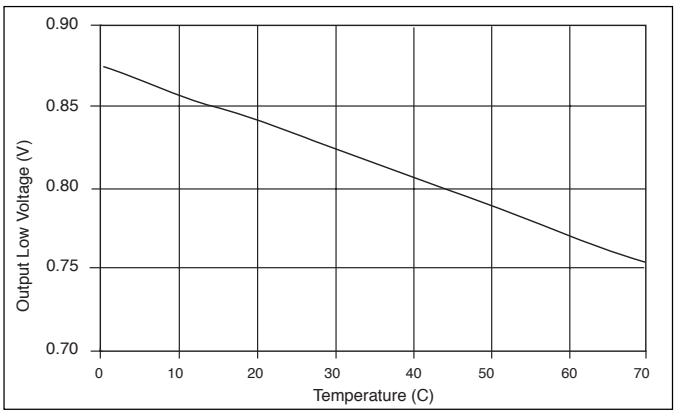


Figure 36: Error Amplifier Output Low Voltage (500μA) vs Temperature.

Typical Performance Characteristics: continued

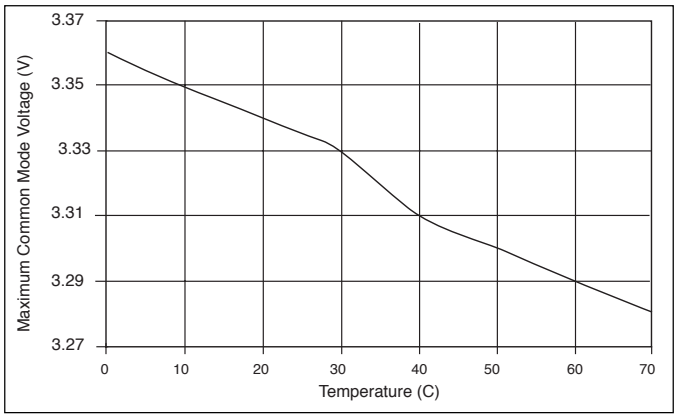


Figure 37: PWM Comparator Maximum Common Mode Input Voltage vs Temperature.

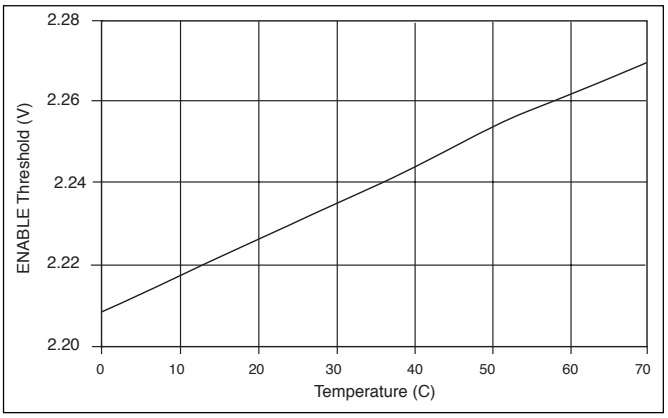


Figure 40: ENABLE Threshold vs Temperature.

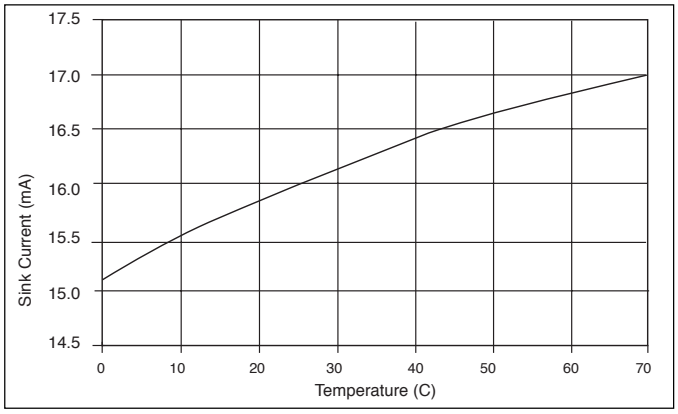


Figure 38: Error Amplifier Sink Current vs Temperature.

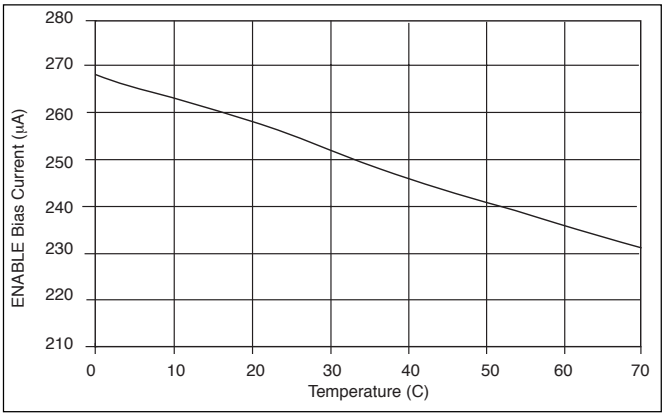


Figure 41: ENABLE Bias Current vs Temperature.

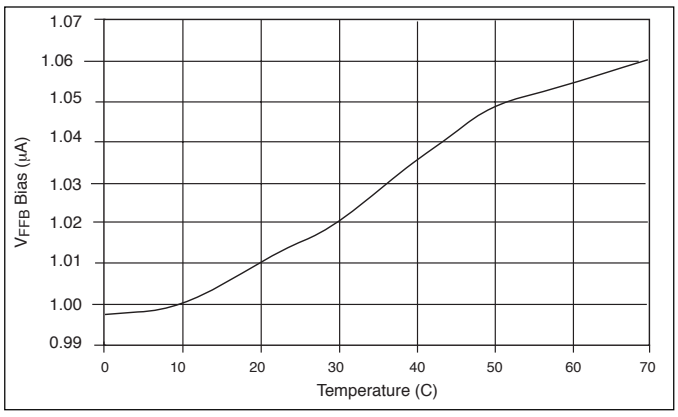


Figure 39: V_{FFB} Bias Current vs Temperature.

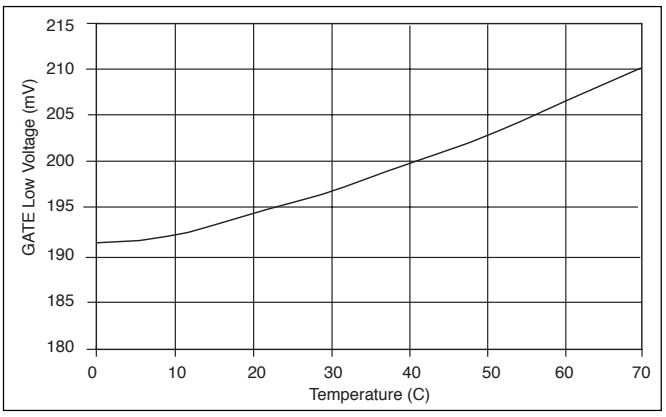


Figure 42: GATE Low Voltage (100mA) vs Temperature.

Typical Performance Characteristics: continued

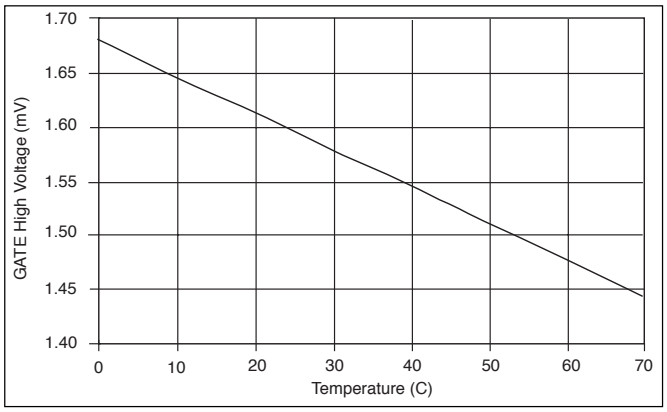


Figure 43: GATE High Voltage (100mA) vs Temperature.

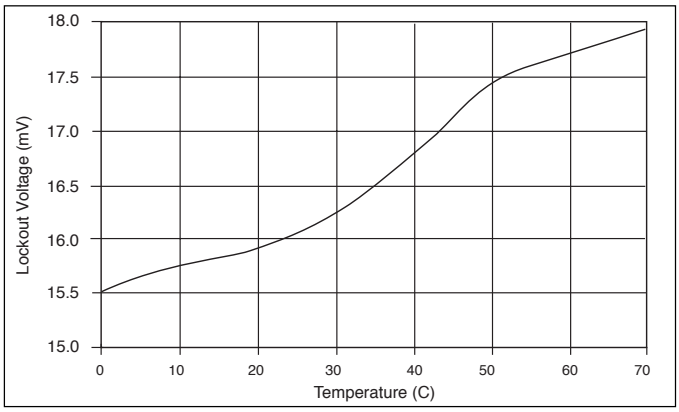


Figure 46: GATE Low Voltage (Lockout) vs Temperature.

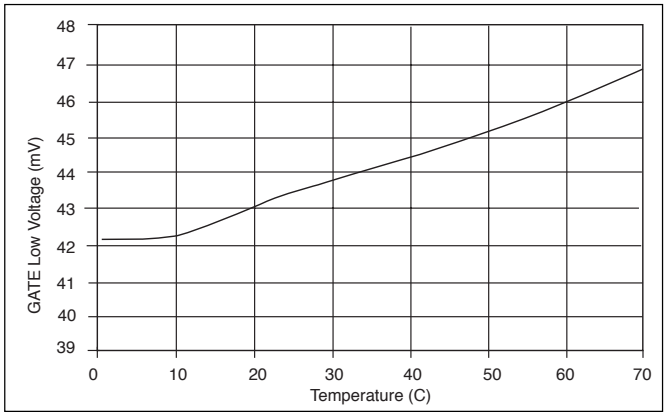


Figure 44: GATE low voltage (20mA) vs Temperature.

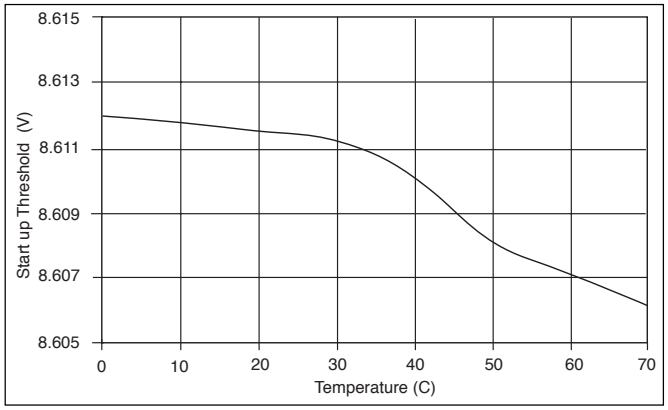


Figure 47: V_{IN} Start-up Threshold vs Temperature.

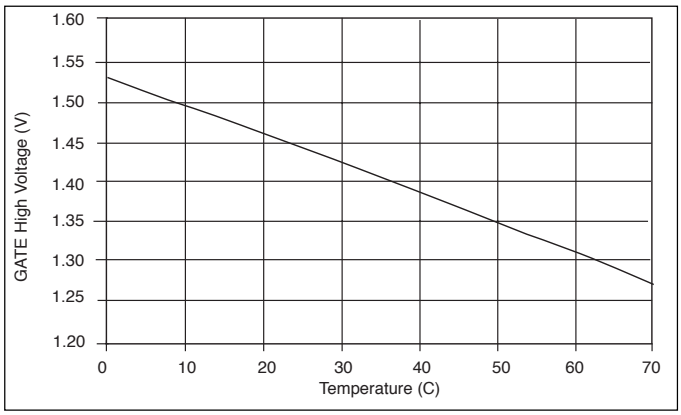


Figure 45: GATE High Voltage (20mA) vs Temperature.

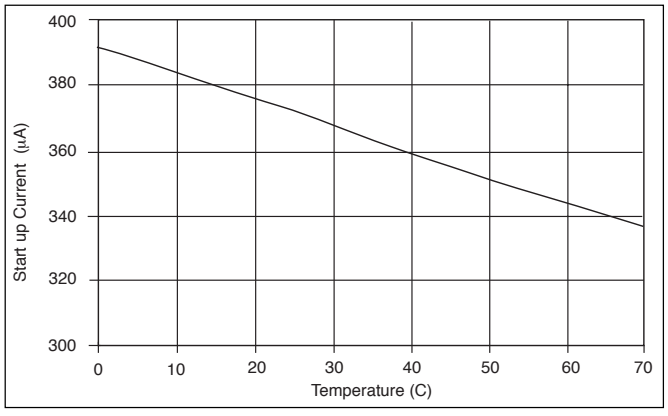


Figure 48: Start-up Current vs Temperature.

Typical Performance Characteristics: continued

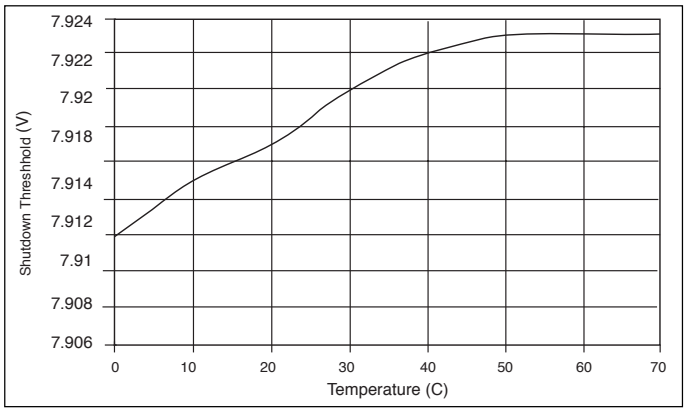


Figure 49: V_{IN} Shutdown Threshold vs Temperature.

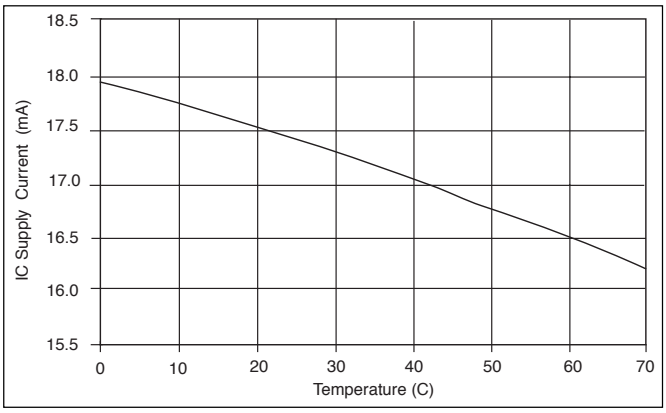


Figure 50: IC Supply Current vs Temperature. No Load on GATE pins. R_T = 27k, C_T = 330pF

Package Specification

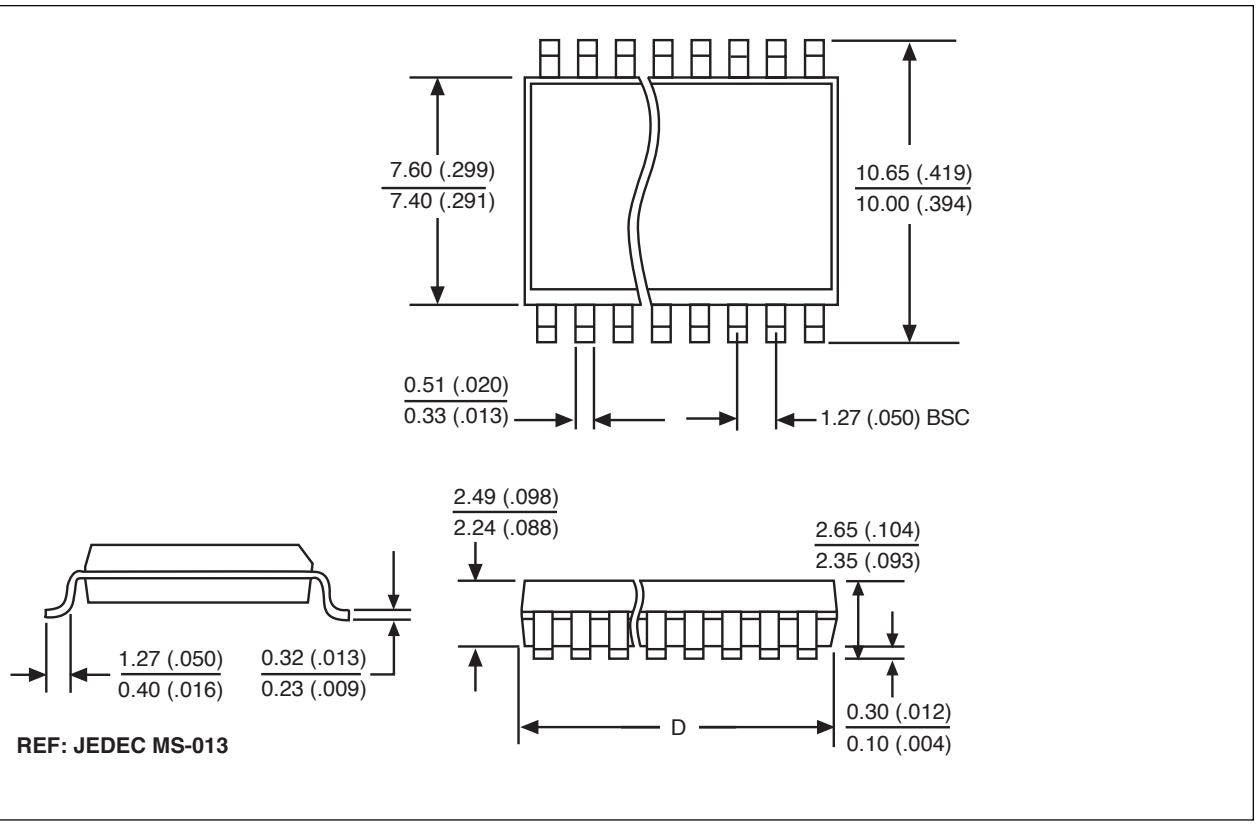
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead SOIC Wide	10.50	10.10	.413	.398

PACKAGE THERMAL DATA

Thermal Data		16 Lead SOIC Wide	
$R_{\Theta JC}$	typ	23	°C/W
$R_{\Theta JA}$	typ	105	°C/W

Surface Mount Wide Body (DW); 300mil wide



Ordering Information

Part Number	Description
CS5127GDW16	16 Lead SOIC Wide
CS5127GDWR16	16 Lead SOIC Wide *(tape & reel)*

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.