**CRYSTAL**

**A Cirrus Logic Company**

**CS61305A**

# T1/E1 Line Interface

## Features

● Provides Analog Transmission Line Interface for T1 and E1 Applications

● Provides Line Driver, Jitter Attenuator and Clock Recovery Functions

● Transmit Side Jitter Attenuation Starting at 3 Hz, with > 300 UI of Jitter Tolerance

● B8ZS/HDB3/AMI Encoders/Decoders

● Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

● 50 mA Transmitter Short-Circuit Current Limiting

## General Description

The CS61305A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61305A is a pin-compatible replacement for the LXT305A in most applications.

The CS61305A provides a transmitter jitter attenuator making it ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The transmitter features internal pulse shaping and a low impedance output stage allowing the use of external resistors for transmitter impedance matching. The receiver uses a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

## Applications

● Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.

● Interfacing customer premises equipment to a CSU.

**ORDERING INFORMATION**
CS61305A-IP1    28 Pin Plastic DIP
CS61305A-IL1    28 Pin Plastic PLCC
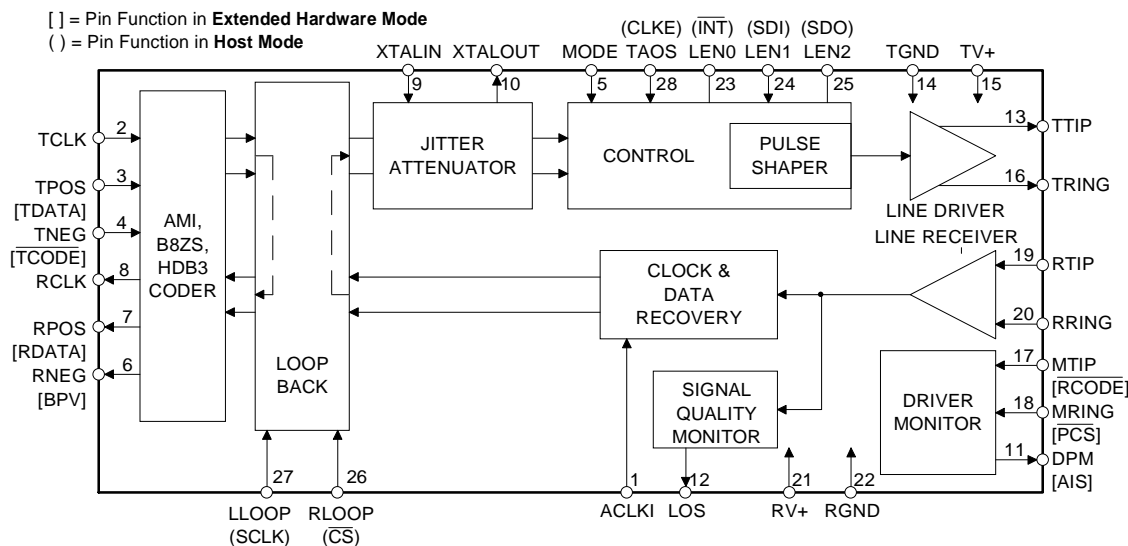


*Preliminary Product Information* | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

MAY '96
DS157PP3
**1**

# ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Supply (referenced to RGND=TGND=0V) | RV+ | - | 6.0 | V |
| | TV+ | - | (RV+) + 0.3 | V |
| Input Voltage, Any Pin (Note 1) | $V_{in}$ | RGND-0.3 | (RV+) + 0.3 | V |
| Input Current, Any Pin (Note 2) | $I_{in}$ | -10 | 10 | mA |
| Ambient Operating Temperature | $T_A$ | -40 | 85 | °C |
| Storage Temperature | $T_{stg}$ | -65 | 150 | °C |

WARNING: Operations at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

# RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| DC Supply (Note 3) | RV+, TV+ | 4.75 | 5.0 | 5.25 | V |
| Ambient Operating Temperature | $T_A$ | -40 | 25 | 85 | °C |
| Power Consumption (Notes 4,5) | $P_C$ | - | - | 350 | mW |

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.

# DIGITAL CHARACTERISTICS  (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage (Notes 6, 7)<br>PINS 1-4, 17, 18, 23-28 | $V_{IH}$ | 2.0 | - | - | V |
| Low-Level Input Voltage (Notes 6, 7)<br>PINS 1-4, 17, 18, 23-28 | $V_{IL}$ | - | - | 0.8 | V |
| High-Level Output Voltage (Notes 6, 7, 8)<br>$I_{OUT}$ = -400 μA PINS 6-8, 11, 12, 25 | $V_{OH}$ | 2.4 | - | - | V |
| Low-Level Output Voltage (Notes 6, 7, 8)<br>$I_{OUT}$ = 1.6 mA PINS 6-8, 11, 12, 23, 25 | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current (Except Pin 5) | | - | - | ±10 | μA |
| Low-Level Input Voltage, PIN 5 | $V_{IL}$ | - | - | 0.2 | V |
| High-Level Input Voltage, PIN 5 | $V_{IH}$ | (RV+) - 0.2 | - | - | V |
| Mid-Level Input Voltage, PIN 5 (Note 9) | $V_{IM}$ | 2.3 | - | 2.7 | V |

Notes: 6. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate digital output.
7. This specification guarantees TTL compatibility ($V_{OH}$ = 2.4V @ $I_{OUT}$ = -40μA).
8. Output drivers will drive CMOS logic levels into a CMOS load.
9. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

## ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| *Transmitter* | | | | | |
| AMI Output Pulse Amplitudes | (Note 10) | | | | |
|     E1, 75 Ω | (Note 11) | 2.14 | 2.37 | 2.6 | V |
|     E1, 120 Ω | (Note 12) | 2.7 | 3.0 | 3.3 | V |
|     T1, FCC Part 68 | (Note 13) | 2.7 | 3.0 | 3.3 | V |
|     T1, DSX-1 | (Note 14) | 2.4 | 3.0 | 3.6 | V |
| E1 Zero (space) level (LEN2/1/0 = 000) | | | | | |
|     1:1 transformer and 75Ω load | | -0.237 | - | 0.237 | V |
|     1:1.26 transformer and 120Ω load | | -0.3 | - | 0.3 | V |
| Load Presented To Transmitter Output | (Note 10) | - | 75 | - | Ω |
| Jitter Added by the Transmitter | (Note 15) | | | | |
|     10Hz - 8kHz | | - | - | 0.01 | UI |
|     8kHz - 40kHz | | - | - | 0.025 | UI |
|     10Hz - 40kHz | | - | - | 0.025 | UI |
|     Broad Band | | - | - | 0.05 | UI |
| Power in 2kHz band about 772kHz | (Notes 10, 16) | 12.6 | 15 | 17.9 | dBm |
| Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz) | (Notes 10, 16) | -29 | -38 | - | dB |
| Positive to Negative Pulse Imbalance | (Notes 10, 16) | | | | |
|     T1, DSX-1 | | - | 0.2 | 0.5 | dB |
|     E1 amplitude at center of pulse | | -5 | - | 5 | % |
|     E1 pulse width at 50% of nominal amplitude | | -5 | - | 5 | % |
| E1 Transmitter Return Loss | (Notes 10, 16, 17) | | | | |
|     51 kHz to 102 kHz | | 20 | 28 | - | dB |
|     102 kHz to 2.048 MHz | | 20 | 28 | - | dB |
|     2.048 MHz to 3.072 MHz | | 20 | 24 | - | dB |
| E1 Transmitter Short Circuit Current | (Notes 10, 18) | - | - | 50 | mA RMS |

Notes: 10. Using a 0.47 μF capacitor in series with the primary of a transformer recommended in the Applications Section.
11. Pulse amplitude measured at the output of a 1:1 transformer across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
12. Pulse amplitude measured at the output of a 1:1.26 transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0 or at the output of a 1:1 transformer across a 120 Ω load for LEN2/1/0 = 001.
13. Pulse amplitude measured at the output of a 1:1.15 transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
14. Pulse amplitude measured at the DSX-1 Cross-Connect across a 100 Ω load for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1 using a 1:1.5 transformer.
15. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
16. Not production tested. Parameters guaranteed by design and characterization.
17. Return loss = $20 \log_{10} ABS((z_1 + z_0)/(z_1 - z_0))$ where $z_1$ = impedance of the transmitter, and $z_0$ = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:2 transformer with two 9.4 Ω series resistors terminated by a 75Ω load, or for LEN2/1/0 = 0/0/1 with a 1:2 transformer and two 15 Ω series resistors terminated by a 120Ω load.
18. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0 or 0/0/1with a 1:2 transformer and the series resistors specified in Table A1.

## ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| *Transmitter Jitter Attenuator* | | | | | |
| Jitter Attenuation Curve Corner Frequency | (Notes 16, 19) | - | 3 | - | Hz |
| Attenuation at 10kHz Jitter Frequency | (Notes 16, 19) | - | 50 | - | dB |
| Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection) | (Notes 16, 19) | 138 | - | - | UI |
| *Receiver* | | | | | |
| RTIP/RRING Input Impedance | | - | 50k | - | $\Omega$ |
| Sensitivity Below DSX (0dB = 2.4V) | | -13.6 | - | - | dB |
| | | 500 | - | - | mV |
| Data Decision Threshold | | | | | |
| T1, DSX-1 | (Note 20) | 53 | 65 | 77 | % of peak |
| T1, (FCC Part 68) and E1 | (Note 21) | 45 | 50 | 55 | % of peak |
| Allowable Consecutive Zeros before LOS | | 160 | 175 | 190 | bits |
| Receiver Input Jitter Tolerance | (Note 22) | | | | |
| 10kHz - 100kHz | | 0.4 | - | - | UI |
| 2kHz | | 6.0 | - | - | UI |
| 10Hz and below | | 300 | - | - | UI |
| Loss of Signal Threshold | | - | 0.30 | - | V |

Notes: 19. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 10. Output jitter can increase significantly when more than 12 UI's are input to the attenuator. See discussion in the text section.
20. For input amplitude of 1.2 $V_{pk}$ to 4.14 $V_{pk}$.
21. For input amplitude of 1.05 $V_{pk}$ to 3.3 $V_{pk}$.
22. Jitter tolerance increases at lower frequencies. See Figure 12.

## E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Crystal Frequency | (Note 23) | $f_c$ | - | 8.192000 | - | MHz |
| ACLKI Duty Cycle | | $t_{pwh3}/t_{pw3}$ | 40 | - | 60 | % |
| ACLKI Frequency | (Note 24) | $f_{aclki}$ | - | 2.048 | - | MHz |
| RCLK Cycle Width | (Note 25) | $t_{pw1}$ | 310 | 488 | 620 | ns |
| | | $t_{pwh1}$ | 90 | 140 | 190 | ns |
| | | $t_{pwl1}$ | 120 | 348 | 500 | ns |
| Rise Time, All Digital Outputs | (Note 26) | $t_r$ | - | - | 85 | ns |
| Fall Time, All Digital Outputs | (Note 26) | $t_f$ | - | - | 85 | ns |
| TCLK Frequency | | $f_{tclk}$ | - | 2.048 | - | MHz |
| TCLK Pulse Width | (Notes 27, 28) | $t_{pwh2}$ | 80 | - | - | ns |
| | (Notes 29, 30) | | 150 | - | 340 | ns |
| TPOS/TNEG (TDATA) to TCLK Falling Setup Time | | $t_{su2}$ | 25 | - | - | ns |
| TCLK Falling to TPOS/TNEG (TDATA) Hold Time | | $t_{h2}$ | 25 | - | - | ns |
| RPOS/RNEG Valid Before RCLK Falling | (Note 27) | $t_{su1}$ | 100 | 194 | - | ns |
| RDATA Valid Before RCLK Falling | (Note 29) | $t_{su1}$ | 100 | 194 | - | ns |
| RPOS/RNEG Valid Before RCLK Rising | (Note 28) | $t_{su1}$ | 100 | 194 | - | ns |
| RPOS/RNEG Valid After RCLK Falling | (Note 27) | $t_{h1}$ | 100 | 194 | - | ns |
| RDATA Valid After RCLK Falling | (Note 29) | $t_{h1}$ | 100 | 194 | - | ns |
| RPOS/RNEG Valid After RCLK Rising | (Note 28) | $t_{h1}$ | 100 | 194 | - | ns |

## T1 SWITCHING CHARACTERISTICS  (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;
GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Crystal Frequency | (Note 23) | $f_c$ | - | 6.176000 | - | MHz |
| ACLKI Duty Cycle | | $t_{pwh3}/t_{pw3}$ | 40 | - | 60 | % |
| ACLKI Frequency | (Note 24) | $f_{aclki}$ | - | 1.544 | - | MHz |
| RCLK Cycle Width | (Note 25) | $t_{pw1}$ | 320 | 648 | 980 | ns |
| | | $t_{pwh1}$ | 130 | 190 | 240 | ns |
| | | $t_{pwl1}$ | 100 | 458 | 850 | ns |
| Rise Time, All Digital Outputs | (Note 26) | $t_r$ | - | - | 85 | ns |
| Fall Time, All Digital Outputs | (Note 26) | $t_f$ | - | - | 85 | ns |
| TCLK Frequency | | $f_{tclk}$ | - | 1.544 | - | MHz |
| TCLK Pulse Width | (Notes 16, 27, 28) | $t_{pwh2}$ | 80 | - | - | ns |
| | (Notes 29, 30) | | 150 | - | 500 | ns |
| TPOS/TNEG (TDATA) to TCLK Falling Setup Time | | $t_{su2}$ | 25 | - | - | ns |
| TCLK Falling to TPOS/TNEG (TDATA) Hold Time | | $t_{h2}$ | 25 | - | - | ns |
| RPOS/RNEG Valid Before RCLK Falling | (Note 27) | $t_{su1}$ | 150 | 274 | - | ns |
| RDATA Valid Before RCLK Falling | (Note 29) | $t_{su1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid Before RCLK Rising | (Note 28) | $t_{su1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid After RCLK Falling | (Note 27) | $t_{h1}$ | 150 | 274 | - | ns |
| RDATA Valid After RCLK Falling | (Note 29) | $t_{h1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid After RCLK Rising | (Note 28) | $t_{h1}$ | 150 | 274 | - | ns |

Notes: 23. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
24. ACLKI provided by an external source or TCLK but not RCLK.
25. RCLK duty cycle will vary with extent by which pulses are displaced by jitter. Specified under worst case jitter conditions: 0.4 UI AMI data displacement for T1 and 0.2 UI AMI data displacement for E1.
26. At max load of 1.6 mA and 50 pF.
27. Host Mode (CLKE = 1).
28. Hardware Mode, or Host Mode (CLKE = 0).
29. Extended Hardware Mode.
30. The maximum TCLK burst rate is 5 MHz and $t_{pw2}$ (min) = 200ns. The maximum gap size that can be tolerated on TCLK is 138 VI.

## SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| SDI to SCLK Setup Time | $t_{dc}$ | 50 | - | - | ns |
| SCLK to SDI Hold Time | $t_{cdh}$ | 50 | - | - | ns |
| SCLK Low Time | $t_{cl}$ | 240 | - | - | ns |
| SCLK High Time | $t_{ch}$ | 240 | - | - | ns |
| SCLK Rise and Fall Time | $t_r, t_f$ | - | - | 50 | ns |
| $\overline{CS}$ to SCLK Setup Time | $t_{cc}$ | 50 | - | - | ns |
| SCLK to $\overline{CS}$ Hold Time | $t_{cch}$ | 50 | - | - | ns |
| $\overline{CS}$ Inactive Time | $t_{cwh}$ | 250 | - | - | ns |
| SCLK to SDO Valid                                    (Note 31) | $t_{cdv}$ | - | - | 200 | ns |
| $\overline{CS}$ to SDO High Z | $t_{cdz}$ | - | 100 | - | ns |
| Input Valid To $\overline{PCS}$ Falling Setup Time | $t_{su4}$ | 50 | - | - | ns |
| $\overline{PCS}$ Rising to Input Invalid Hold Time | $t_{h4}$ | 50 | - | - | ns |
| $\overline{PCS}$ Active Low Time | $t_{pcsl}$ | 250 | - | - | ns |

Notes: 31. Output load capacitance = 50pF.
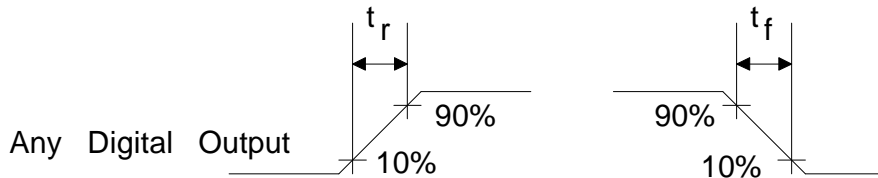


**Figure 1. Signal Rise and Fall Characteristics**
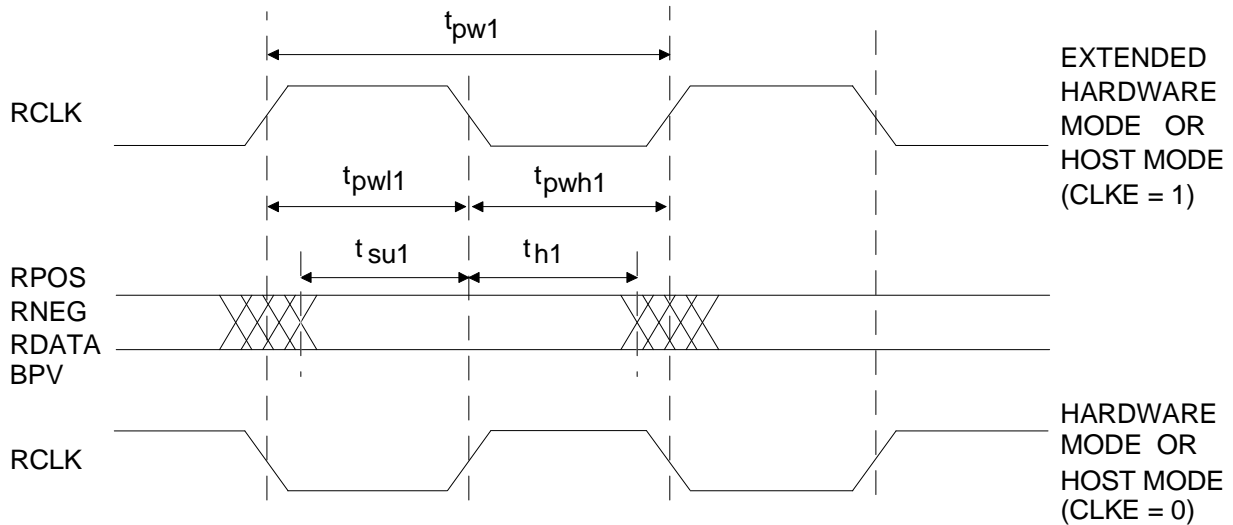


**Figure 2. Recovered Clock and Data Switching Characteristics**
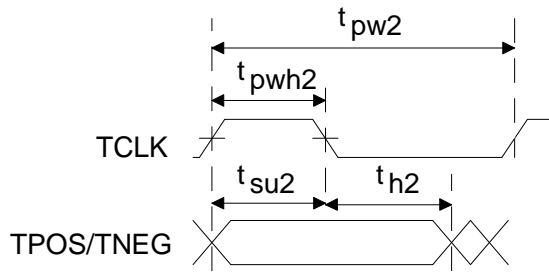
Figure 3a. Transmit Clock and Data Switching
Characteristics
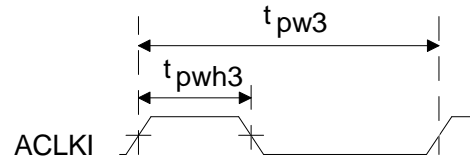


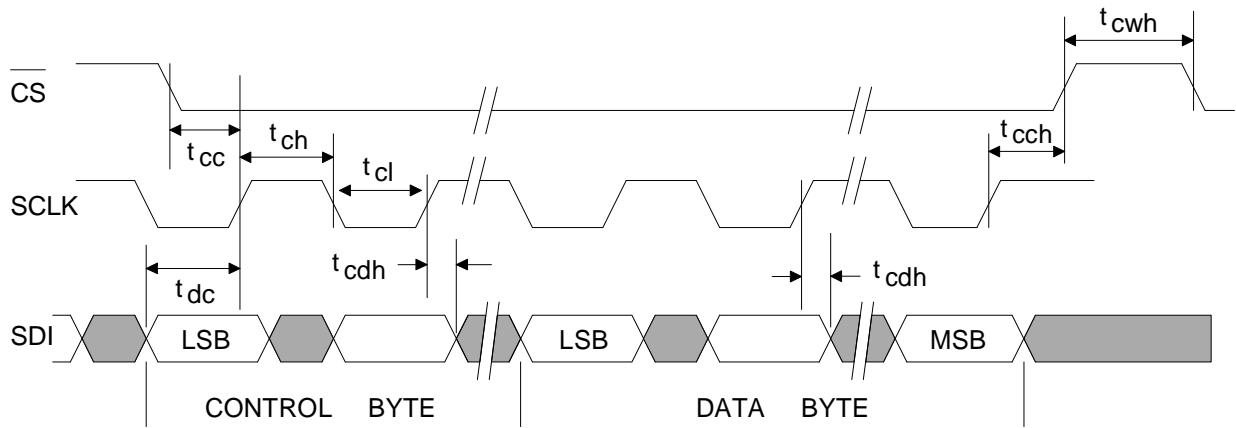Figure 3b. Alternate External Clock Characteristics



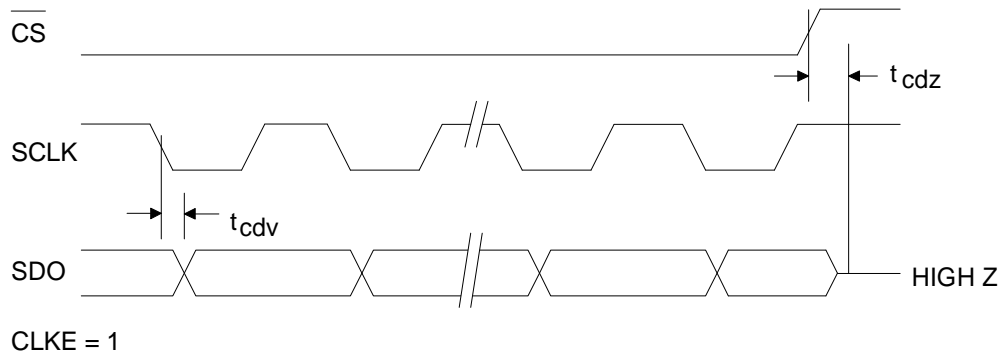Figure 4. Serial Port Write Timing Diagram



CLKE = 1

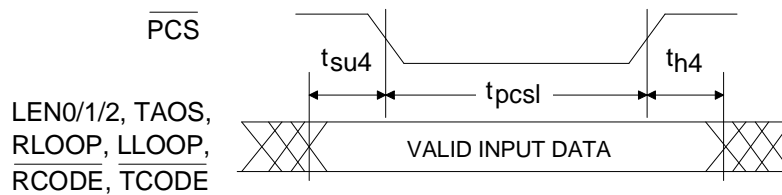Figure 5. Serial Port Read Timing Diagram



Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

## THEORY OF OPERATION

### Key Enhancements of the CS61305A Relative to the LXT305A

- 12.5% lower power consumption,
- 50 mA$_{RMS}$ transmitter short-circuit current limiting for E1 (per OFTEL OTR-001),
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- Improved receiver Loss of Signal handling (LOS set at power-up, reset upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros),
- Transmitter TTIP and TRING outputs are forced low when TCLK is static.

### Introduction to Operating Modes

The CS61305A supports three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2). The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface.

| | Hardware Mode | Extended Hardware Mode | Host Mode |
|---|---|---|---|
| **Control Method** | Control Pins | Control Pins with Parallel Chip Select | Serial Interface |
| **MODE Pin Level** | <0.2 V | Floating or 2.5 V | >(RV+)-0.2 V |
| **Line Coding** | External | Internal-AMI, B8ZS, or HDB3 | External |
| **AIS Detection** | No | Yes | No |
| **Driver Performance Monitor** | Yes | No | Yes |

**Table 1. Differences Between Operating Modes**

| FUNCTION | PIN | MODE | | |
|---|---|---|---|---|
| | | HARDWARE | EXTENDED HARDWARE | HOST |
| TRANSMITTER | 3 | TPOS | TDATA | TPOS |
| | 4 | TNEG | $\overline{\text{TCODE}}$ | TNEG |
| RECEIVER/DPM | 6 | RNEG | BPV | RNEG |
| | 7 | RPOS | RDATA | RPOS |
| | 11 | DPM | AIS | DPM |
| | 17 | MTIP | $\overline{\text{RCODE}}$ | MTIP |
| | 18 | MRING | - | MRING |
| CONTROL | 18 | - | $\overline{\text{PCS}}$ | - |
| | 23 | LEN0 | LEN0 | $\overline{\text{INT}}$ |
| | 24 | LEN1 | LEN1 | SDI |
| | 25 | LEN2 | LEN2 | SDO |
| | 26 | RLOOP | RLOOP | $\overline{\text{CS}}$ |
| | 27 | LLOOP | LLOOP | SCLK |
| | 28 | TAOS | TAOS | CLKE |

**Table 2. Pin Definitions**

## HARDWARE MODE



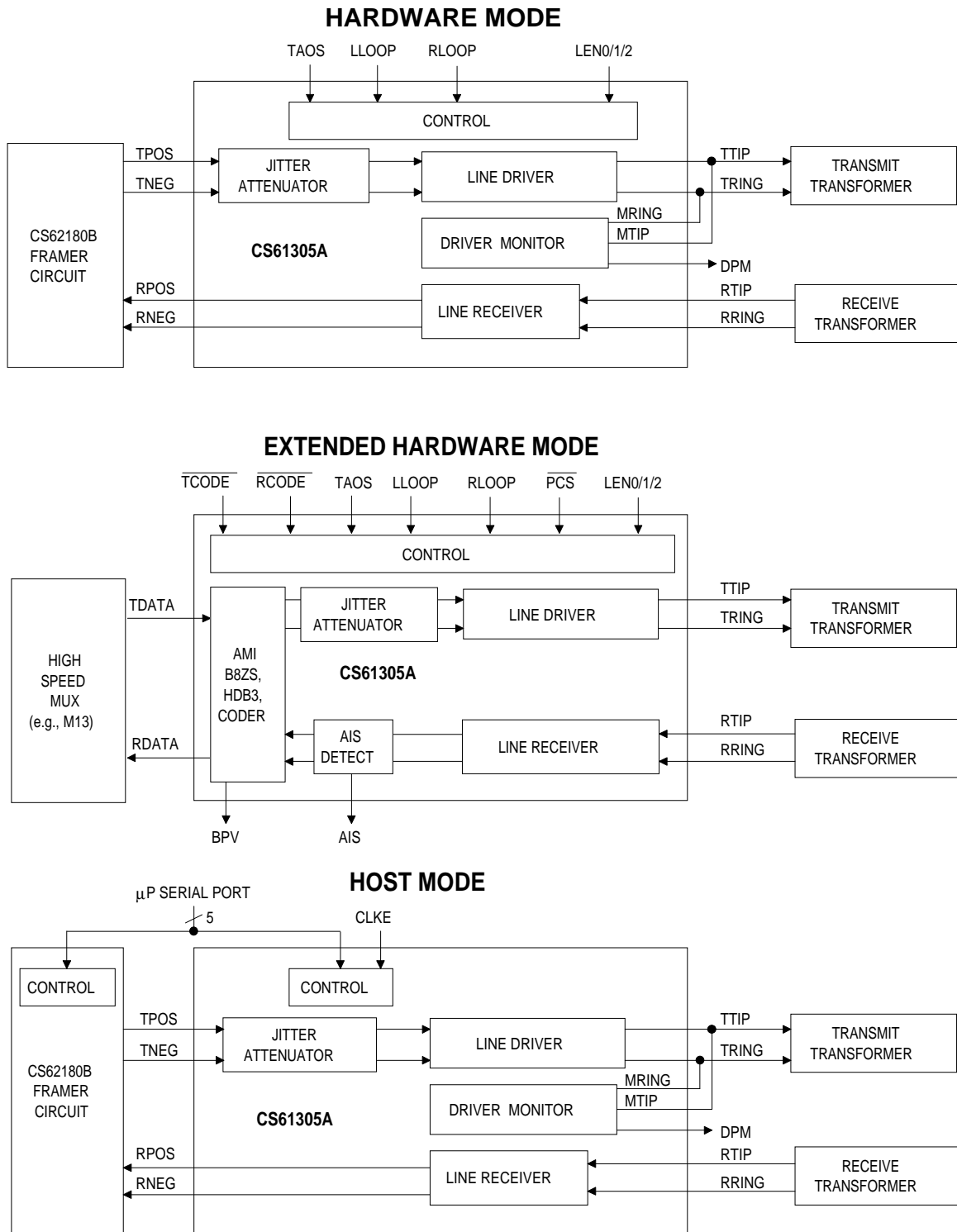## EXTENDED HARDWARE MODE



## HOST MODE



Figure 7. Overview of Operating Modes

*Transmitter*

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3. The output options in Table 3 are specified with a 1:1.15 transmitter transformer turns ratio for T1 and a 1:1 turns ratio for E1 without external series resistors. Other turns ratios may be used if approriate resistors are placed in series with the TTIP and TRING pins. Table A1 in the applications section lists other combinations which can be used to provide transmitter impedance matching.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102-1993 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61305A automatically adjusts the pulse width based upon the "line length" selection made.

The E1 G.703 pulse shape is supported with line length selections LEN2/1/0 = 0/0/0 and 0/0/1. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

| LEN2 | LEN1 | LEN0 | Option Selected | Application |
|------|------|------|-----------------|-------------|
| 0 | 1 | 1 | 0-133 ft | DSX-1 ABAM (AT&T 600B or 600C) |
| 1 | 0 | 0 | 133-266 ft | |
| 1 | 0 | 1 | 266-399 ft | |
| 1 | 1 | 0 | 399-533 ft | |
| 1 | 1 | 1 | 533-655 ft | |
| 0 | 0 | 0 | 75Ω coax | E1 CCITT G.703 |
| 0 | 0 | 1 | 120Ω twisted-pair | |
| 0 | 1 | 0 | FCC PART 68, OPT. A | Network Interface |
| 0 | 1 | 1 | ANSI T1.403 | |

**Table 3. Line Length Selection**

The CS61305A transmitter provides short-circuit current limiting protection and meets OFTEL OTR-001 short-circuit current limiting requirements for E1 applications.

The CS61305A will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.
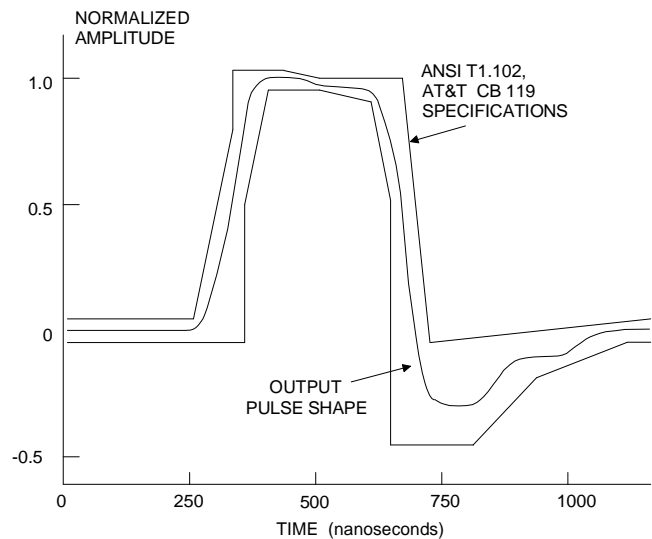


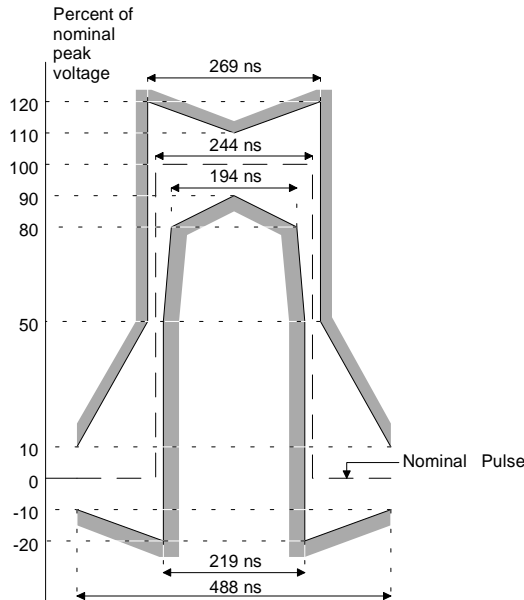**Figure 8. Typical Pulse Shape at DSX-1 Cross Connect**

Figure 9. Mask of the Pulse at the 2048 kbps Interface



**Figure 10. Typical Jitter Attenuation Curve**

### Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of ACLKI. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. A TAOS request will be ignored if remote loopback is in effect. ACLKI jitter will be attenuated. TAOS is not available on the CS61305A when ACLKI is grounded.

### Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the transmit clock signal. It consists of a 192 bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 10.

The jitter attenuator works in the following manner. Data on TPOS and TNEG (or TDATA) are

| | For coaxial cable, 75Ω load and transformer specified in Application Section. | For shielded twisted pair, 120Ω load and transformer specified in Application Section. |
|---|---|---|
| Nominal peak voltage of a mark (pulse) | 2.37 V | 3 V |
| Peak voltage of a space (no pulse) | 0 ±0.237 V | 0 ±0.30 V |
| Nominal pulse width | 244 ns | |
| Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval | 0.95 to 1.05* | |
| Ratio of the widths of positive and negative pulses at the nominal half amplitude | 0.95 to 1.05* | |

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

**Table 4. CCITT G.703 Specifications**

written into the jitter attenuator's FIFO by TCLK. The rate at which data is read out of the FIFO and transmitted is determined by the oscillator. Logic circuits adjust the capacitive loading on the crystal to set its oscillation frequency to the average of the TCLK frequency. Signal jitter is absorbed in the FIFO.

*Jitter Tolerance of Jitter Attenuator*

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should the pointers attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. When a divide by 3 1/2 or 4 1/2 occurs, the data bit will be driven on to the line either an eighth bit period early or an eighth bit period late.

The FIFO of the jitter attenuator in the transmit path is 192 bits deep. This FIFO will typically be near the half full point under normal operating conditions, buffering about 96 bits of data. The number of bits actually buffered depends on the relationship of the nominal TCLK frequency to the center frequency of the crystal oscillator. As these frequencies deviate, a few bits of FIFO depth will be lost.

TCLK can have gaps or bursts. As long as the gap or burst is less than the remaining FIFO depth, normal operation will continue. For example, if the nominal TCLK frequency was less than the oscillator's center frequency by 40 Hz. The FIFO will operate 3-4 bits off center or 92 bits full. A gap in TCLK of 80 cycles would empty the FIFO by 80 bits but would still not envoke the divide by 4 1/2 circuitry, as about 12 bits would remain in the FIFO.

The crystal frequency must be 4 times the nominal signal frequency: 6.176 MHz for 1.544 MHz operation; 8.192 MHz for 2.048 MHz applica-

tions. Internal capacitors load the crystal, controlling the oscillation frequency. The crystal must be designed so that over operating temperature, the oscillator frequency range exceeds the system frequency tolerance. Crystal Semiconductor offers the CXT6176 & CXT8192 crystals, which yield optimum performance with the CS61305A.

*Receiver*

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 11. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI or the jitter attenuator's oscillator, into 13 equal divisions or phases. Continuous calibration assures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The out-
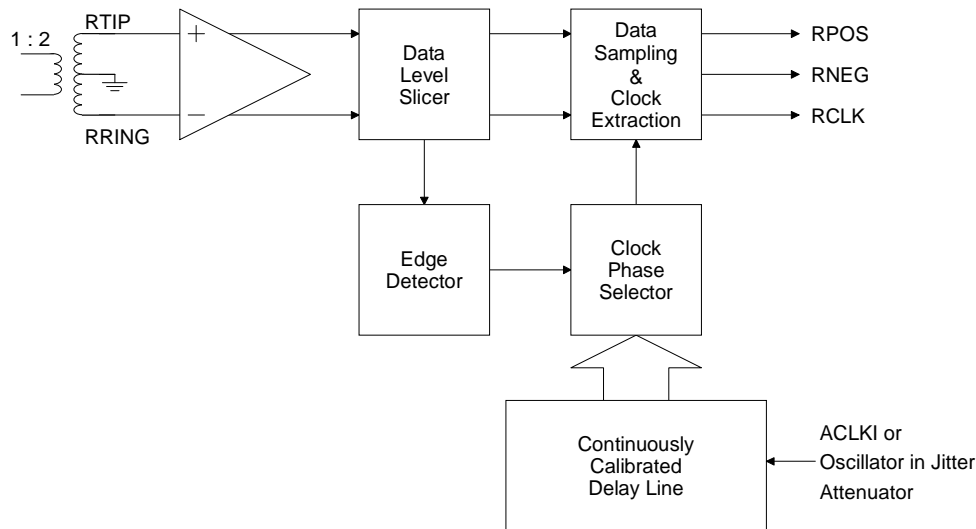
**Figure 11. Receiver Block Diagram**

put from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that shown in Figure 12.

The CS61305A outputs a clock immediately upon power-up and will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Extended Hardware Mode, data at RDATA is stable and may be sampled on the fallings edge of the recovered clock. In the Host Mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

*Jitter and Recovered Clock*

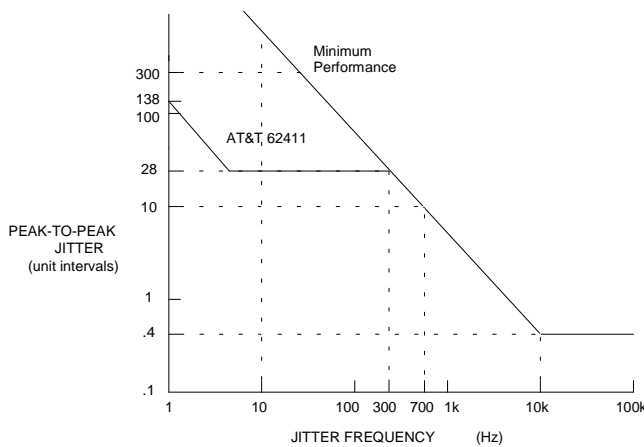The CS61305A is designed for error free clock and data recovery from an AMI encoded data



**Figure 12. Minimum Input Jitter Tolerance of Receiver**

| MODE (pin 5) | CLKE (pin 28) | DATA | CLOCK | Clock Edge for Valid Data |
|---|---|---|---|---|
| LOW (<0.2V) | X | RPOS RNEG | RCLK RCLK | Rising Rising |
| HIGH (>(V+) - 0.2V) | LOW | RPOS RNEG SDO | RCLK RCLK SCLK | Rising Rising Falling |
| HIGH (>(V+) - 0.2V) | HIGH | RPOS RNEG SDO | RCLK RCLK SCLK | Falling Falling Rising |
| MIDDLE (2.5V) | X | RDATA | RCLK | Falling |

X = Don't care

**Table 5. Data Output/Clock Relationship**

stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until a data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UIpp. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation the instantaneous period can be 14/13 * 648 ns = 698 ns or 12/13 * 648 ns = 598 ns when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the E1 rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 μs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. The data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by

less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS61305A is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns. For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns.

### Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt issued on INT. LOS will go low (and flag the INT pin again if serial I/O is used) when a valid signal is detected. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12.

In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. LOS returns to logic zero when 3 ones are received out of 32 bit periods containing no more than 15 consecutive zeros. Also, a power-up or manual reset will set LOS high.

*Local Loopback*

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), and outputs it at RCLK, RPOS and RNEG (or RDATA). Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect. The jitter attenuator is not in the local loop back path.

*Remote Loopback*

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 7). The recovered

| RLOOP Input Signal | TAOS Input Signal | Source of Data for TTIP & TRING | Source of Clock for TTIP & TRING |
|---|---|---|---|
| 0 | 0 | TDATA | TCLK |
| 0 | 1 | all 1s | TCLK |
| 1 | X | RTIP & RRING | RTIP & RRING (RCLK) |

Notes: 1. X = Don't Care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

**Table 7. Interaction of RLOOP with TAOS**

incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{RCODE}$ is low.

*Driver Performance Monitor*

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from both the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance.

| | LEN 2/1/0 | |
|---|---|---|
| | 000 | 010-111 |
| $\overline{\text{TCODE}}$ (Transmit Encoder Selection) LOW | HDB3 Encoder | B8ZS Encoder |
| $\overline{\text{TCODE}}$ (Transmit Encoder Selection) HIGH | AMI Encoder | |
| $\overline{\text{RCODE}}$ (Receiver Decoder Selection) LOW | HDB3 Decoder | B8ZS Decoder |
| $\overline{\text{RCODE}}$ (Receiver Decoder Selection) HIGH | AMI Decoder | |

**Table 8. Encoder/Decoder Selection**

### Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when unframed all-ones condition (blue alarm) is detected using the criteria of less than 3 zeros out of 2048 bit periods.

### Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

### Parallel Chip Select

In the Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

### Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI, or the crystal oscillator. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function eliminates any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

### Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a
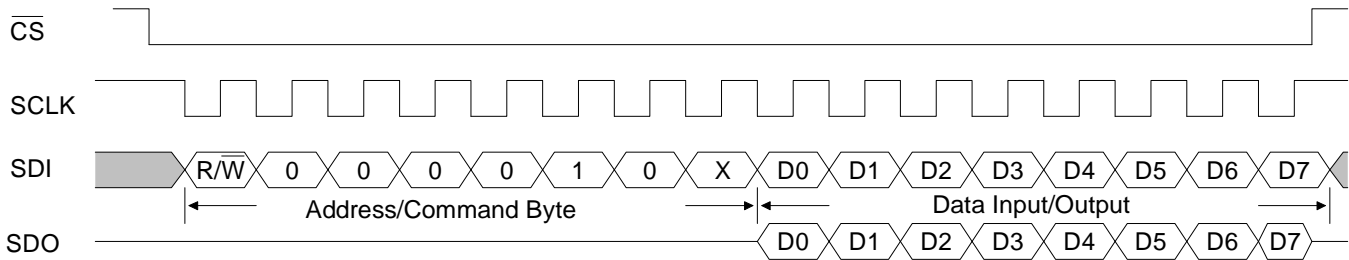
**Figure 13. Input/Output Timing**

host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes to the high impedance state when the serial port is being written (R/$\overline{W}$ = 0), or if $\overline{CS}$ goes high, or at the end of the hold period of data bit D7.

An address/command byte, shown in Table 9, precedes the data byte. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

| Bit | Designation | Description |
|-----|-------------|-------------|
| 0 | R/$\overline{W}$ | Read/Write Select; 0 = write, 1 = read |
| 1 | ADD0 | LSB of address, Must be 0 |
| 2 | ADD1 | Must be 0 |
| 3 | ADD2 | Must be 0 |
| 4 | ADD3 | Must be 0 |
| 5 | ADD4 | Must be 1 |
| 6 | - | Reserved - Must be 0 |
| 7 | X | Don't Care |

Note:   Bit 0 is the first bit input (LSB).

**Table 9. Address/Command Byte**

During a write cycle (R/$\overline{W}$ = 0), data is written to the input data register on the eight clock cycles immediately following the address/command byte. The input data format over SDI is shown in Table 10.

| Bit | Designation | Description |
|-----|-------------|-------------|
| D0 | clr LOS | Clear Loss of Signal |
| D1 | clr DPM | Clear Driver Performance Monitor |
| D2 | LEN0 | Bit 0 - Line Length Select |
| D3 | LEN1 | Bit 1 - Line Length Select |
| D4 | LEN2 | Bit 2 - Line Lenght Select |
| D5 | RLOOP | Remote Loopback |
| D6 | LLOOP | Local Loopback |
| D7 | TAOS | Transmit All Ones Select |

Note:   Bit D0 is the first bit input (LSB).

**Table 10. Input Data Register**

Bits D0 and D1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits D5, D6 and D7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

| Bit | Designation | Description |
|---|---|---|
| D0 | LOS | Loss of Signal |
| D1 | DPM | Driver Performance Monitor |
| D2 | LEN0 | Bit 0 - Line Length Select |
| D3 | LEN1 | Bit 1 - Line Length Select |
| D4 | LEN2 | Bit 2 - Line Lenght Select |

Note: Bit D0 is the first bit output (LSB)

**Table 11. Output Data Register (bits D0-D4)**

During a read cycle (R/$\overline{W}$ = 1), data is read from the output data register on the eight clock cycles immediately following the address/ command byte. The output data format over SDO is shown in Tables 11 and 12.

Bits D2, D3 and D4 can be read to verify line length selection. Bits D5, D6 and D7 must be decoded according to Table 12. Codes 101, 110 and 111 (Bits D5, D6 and D7) indicate intermittent losses of signal and/or driver problems.

The SDO pin goes to a high impedance state when not in use. The SDO and SDI pins may be tied together in applications where the host processor has a bi-directional I/O port.

*Power Supply*

The device operates from a single +5 Volt supply. Separate pins for transmit (TV+, TGND) and receive (RV+, RGND) supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their

| Bits D5 | D6 | D7 | Status |
|---|---|---|---|
| 0 | 0 | 0 | Reset has occurred or no program input. |
| 0 | 0 | 1 | TAOS in effect. |
| 0 | 1 | 0 | LLOOP in effect. |
| 0 | 1 | 1 | TAOS/LLOOP in effect. |
| 1 | 0 | 0 | RLOOP in effect |
| 1 | 0 | 1 | DPM changed state since last "clear DPM" occured. |
| 1 | 1 | 0 | LOS changed state since last "clear LOS" occured. |
| 1 | 1 | 1 | LOS and DPM have changed state since last "clear LOS" and "clear DPM". |

**Table 12. Output Data Register (bits D5-D7)**

respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

# PIN DESCRIPTIONS

| Extended Hardware | Hardware/Host | | | Hardware | Extended Hardware | Host |
|---|---|---|---|---|---|---|
| | ACLKI | 1 | 28 | TAOS | | CLKE |
| | TCLK | 2 | 27 | LLOOP | | SCLK |
| TDATA | TPOS | 3 | 26 | RLOOP | | CS |
| TCODE | TNEG | 4 | 25 | LEN2 | | SDO |
| | MODE | 5 | 24 | LEN1 | | SDI |
| BPV | RNEG | 6 | 23 | LEN0 | | INT |
| RDATA | RPOS | 7 | 22 | RGND | | |
| | RCLK | 8 | 21 | RV+ | | |
| | XTALIN | 9 | 20 | RRING | | |
| | XTALOUT | 10 | 19 | RTIP | | |
| AIS | DPM | 11 | 18 | MRING | PCS | |
| | LOS | 12 | 17 | MTIP | RCODE | |
| | TTIP | 13 | 16 | TRING | | |
| | TGND | 14 | 15 | TV+ | | |

DIP top view

PLCC top view
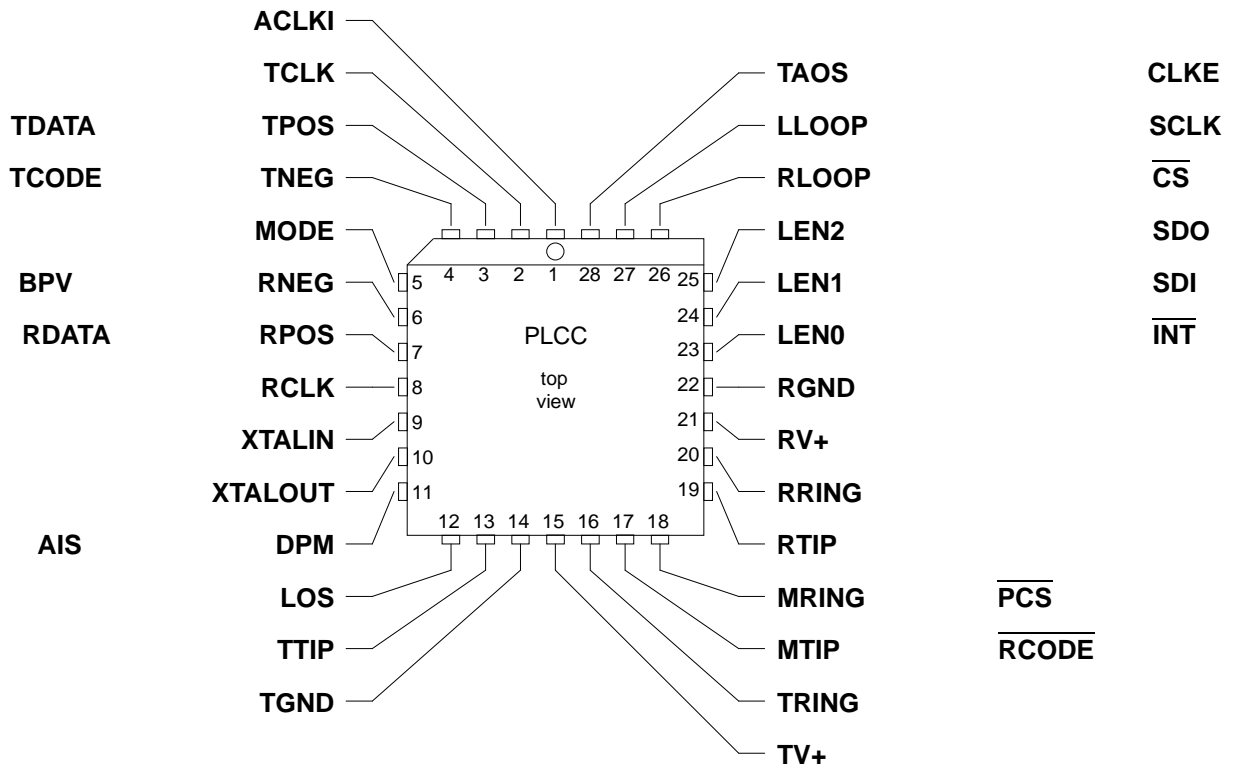
_Power Supplies_

**RGND - Ground, Pin 22.**
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

**RV+ - Power Supply, Pin 21.**
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

**TGND - Ground, Transmit Driver, Pin 14.**
Power supply ground for the transmit driver; typically 0 Volts.

**TV+ - Power Supply, Transmit Driver, Pin 15.**
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

_Oscillator_

**XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.**
A 6.176 MHz (T1 operation) or 8.192 MHz (E1 operation) crystal should be connected across these pins. Overdriving the oscillator with an external clock is not supported.

_Control_

**ACLKI - Alternate External Clock Input, Pin 1.**
A 1.544 MHz or 2.048 MHz clock signal may be input on ACLKI to calibrate the clock recovery circuit and control the transmit clock during TAOS. If a clock is not provided on ACLKI, this input must be grounded, and the oscillator in the jitter attenuator is used to calibrate the clock recovery circuit and TAOS is not available. ACLKI may not be provided by RCLK.

**CLKE - Clock Edge, Pin 28. (Host Mode)**
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

**CS - Chip Select, Pin 26. (Host Mode)**
This pin must transition from high to low to read or write the serial port.

**INT - Receive Alarm Interrupt, Pin 23. (Host Mode)**
Goes low when LOS or DPM change state to flag the host processor. $\overline{INT}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{INT}$ is an open drain output and should be tied to the power supply through a resistor (47k - 100k).

**LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)**

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. These pins also control the receiver slicing level.

**LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)**

Setting LLOOP to a logic 1 routes the transmit clock and data through to the receive clock and data pins. TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored during LLOOP. The jitter attenuator is bypassed.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

**MODE - Mode Select, Pin 5.**

Driving the MODE pin high places the line interface in the Host Mode. In the Host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin places the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 V places the device in Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

**PCS - Parallel Chip Select, Pin 18. (Extended Hardware Mode)**

Setting $\overline{PCS}$ low causes the line interface to accept the $\overline{TCODE}$, $\overline{RCODE}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

**RCODE - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)**

Setting $\overline{RCODE}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{RCODE}$ high enables the AMI receiver decoder (see Table 8).

**RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)**

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

**SCLK - Serial Clock, Pin 27. (Host Mode)**

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{CS}$ pin.

**SDI - Serial Data Input, Pin 24. (Host Mode)**

Input for the input data register. Sampled on the rising edge of SCLK.

**SDO - Serial Data Output, Pin 25. (Host Mode)**

Status and control output from the output data register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written, or if CS is high, or after bit D7 is output.

**TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)**

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLKI.

**TCODE - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)**

Setting TCODE low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting TCODE high enables the AMI transmitter encoder .

*Data*

**RCLK - Recovered Clock, Pin 8.**

The receiver recovered clock is output on this pin.

**RDATA - Receive Data - Pin 7. (Extended Hardware Mode)**

Data recovered from the RTIP and RRING inputs is output in NRZ format at this pin, after being decoded by the line code decoder. RDATA is stable and valid on the falling edge of RCLK.

**RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)**

The receiver recovered NRZ digital data from RTIP and RRING is output on these pins. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse (with respect to ground) received on the RRING pin generates a logic 1 on RNEG. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid (see Table 5).

**RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.**

The AMI receive signal is input on these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 of the *Applications* section. Clock and data are recovered and output on RCLK and RPOS/RNEG or RDATA.

**TCLK - Transmit Clock, Pin 2.**

The 1.544 MHz (T1 operation) or 2.048 MHz (E1 operation) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

**TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)**

Data to be transmitted by the TTIP and TRING outputs is input in NRZ format at this pin, after being encoded by the line code encoder. TDATA is sampled on the falling edge of TCLK.

**TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)**

> The transmit NRZ digital data to TTIP and TRING is input on these pins. A logic 1 on TPOS causes a positive pulse (with respect to ground) to be transmitted on the TTIP pin, and a logic 1 on TNEG causes a negative pulse (with respect to ground) to be transmitted on the TRING pin. TPOS and TNEG are sampled on the falling edge of TCLK.

**TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.**

> The AMI signal is driven to the line through these pins. This output is designed to drive a 75 Ω load. A transformer is required as shown in Figure A1 of the *Applications* section. Clock and data are sourced on TCLK and TPOS/ TNEG or TDATA.

*Status*

**AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)**

> AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than three zeros out of 2048 bit periods.

**BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)**

> BPV strobes high when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

**DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)**

> DPM goes high if no activity is detected on MTIP and MRING.

**LOS - Loss of Signal, Pin 12.**

> LOS goes high when 175 consecutive zeros have been received. LOS returns low when 3 ones are received within 32 bit periods containing no more than 15 consecutive zeros.

**MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)**

> These pins are normally connected to TTIP and TRING and monitor the transmitter output. If the INT pin in the Host mode is used, and the monitor is not used, writing a "1" to the "clear DPM" bit will prevent an interrupt from the driver performance monitor.

**28 pin
Plastic DIP**
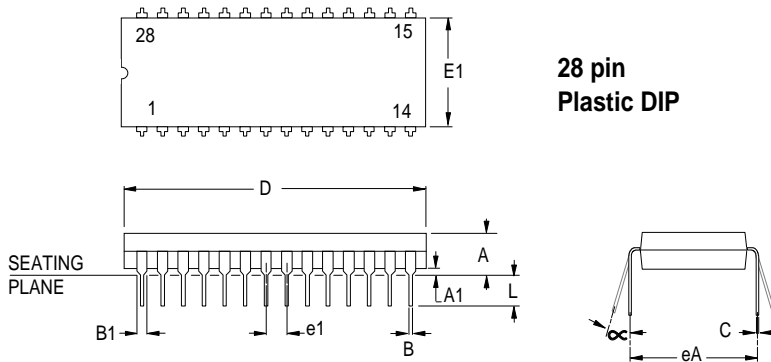
| DIM | MILLIMETERS | | | INCHES | | |
|-----|-----|-----|-----|-----|-----|-----|
|     | MIN | NOM | MAX | MIN | NOM | MAX |
| A   | 3.94 | 4.32 | 5.08 | 0.155 | 0.170 | 0.200 |
| A1  | 0.51 | 0.76 | 1.02 | 0.020 | 0.030 | 0.040 |
| B   | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 |
| B1  | 1.02 | 1.27 | 1.65 | 0.040 | 0.050 | 0.065 |
| C   | 0.20 | 0.25 | 0.38 | 0.008 | 0.010 | 0.015 |
| D   | 36.45 | 36.83 | 37.21 | 1.435 | 1.450 | 1.465 |
| E1  | 13.72 | 13.97 | 14.22 | 0.540 | 0.550 | 0.560 |
| e1  | 2.41 | 2.54 | 2.67 | 0.095 | 0.100 | 0.105 |
| eA  | 15.24 | - | 15.87 | 0.600 | - | 0.625 |
| L   | 3.18 | - | 3.81 | 0.125 | - | 0.150 |
| ∝   | 0° | - | 15° | 0° | - | 15° |

SEATING
PLANE

NOTES:

　　1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN
　　　 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN
　　　 RELATION TO SEATING PLANE AND EACH OTHER.
　　2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
　　3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.

**28-pin PLCC**
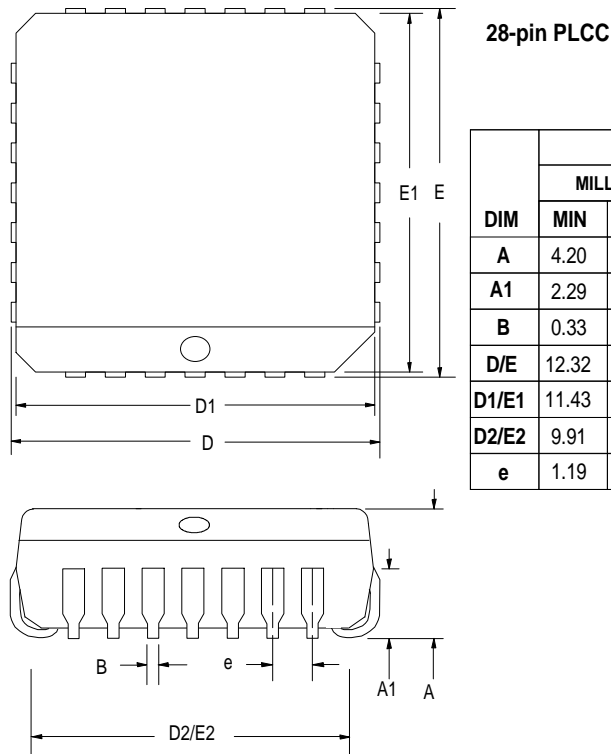
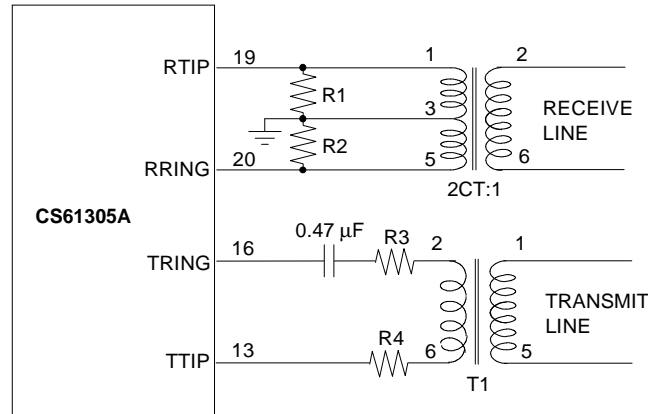| DIM | 28 | | | | | |
|-----|-----|-----|-----|-----|-----|-----|
|     | MILLIMETERS | | | INCHES | | |
|     | MIN | NOM | MAX | MIN | NOM | MAX |
| A   | 4.20 | 4.45 | 4.57 | 0.165 | 0.175 | 0.180 |
| A1  | 2.29 | 2.79 | 3.04 | 0.090 | 0.110 | 0.120 |
| B   | 0.33 | 0.41 | 0.53 | 0.013 | 0.016 | 0.021 |
| D/E | 12.32 | 12.45 | 12.57 | 0.485 | 0.490 | 0.495 |
| D1/E1 | 11.43 | 11.51 | 11.58 | 0.450 | 0.453 | 0.456 |
| D2/E2 | 9.91 | 10.41 | 10.92 | 0.390 | 0.410 | 0.430 |
| e   | 1.19 | 1.27 | 1.35 | 0.047 | 0.050 | 0.053 |

## APPLICATIONS



**Figure A1. Line Interface Circuitry**

| Frequency MHz | Crystal XTL | Cable Ω | R1 and R2 Ω | LEN2/1/0 | T1 turns ratio | R3 and R4 Ω | Typical TX Return Loss (dB) |
|---|---|---|---|---|---|---|---|
| 1.544 (T1) | CXT6176 | 100 | 200 | 0/1/1 - 1/1/1 | 1:1.15 | 0 | 0.5 |
|  |  |  |  |  | 1:2 | 9.4 | 20 |
|  |  |  |  |  | 1:2.3 | 9.4 | 28 |
| 2.048 (E1) | CXT8192 | 120 | 240 | 0/0/0 | 1:1.26 | 0 | 0.5 |
|  |  |  |  | 0/0/0 | 1:2 | 8.7 | 12 |
|  |  |  |  | 0/0/1 | 1:1 | 0 | 0.5 |
|  |  |  |  | 0/0/1 | 1:2 | 15 | 30 |
|  |  | 75 | 150 | 0/0/0 | 1:1 | 0 | 0.5 |
|  |  |  |  | 0/0/0 | 1:2 | 9.4 | 24 |
|  |  |  |  | 0/0/1 | 1:1 | 10 | 5 |
|  |  |  |  | 0/0/1 | 1:2 | 14.3 | 12 |

Note: Refer to Table A3 for specific transformer recommendations.

**Table A1. External Component Values**

*Line Interface*

Figure A1 illustrates the external components for the line interface circuitry and Table A1 shows the specific components for each application. Figures A2-A4 show typical T1 and E1 line interface application circuits. Figure A2 illustrates a T1 interface in the Host Mode. Figure A3 illustrates a 120 Ω E1 interface in the Hardware Mode. Figure A4 illustrates a 75 Ω E1 interface in the Extended Hardware Mode.

The receiver transformer has a grounded center tap on the IC side. Resistors between the RTIP and RRING pins to ground provide the termination for the receive line.
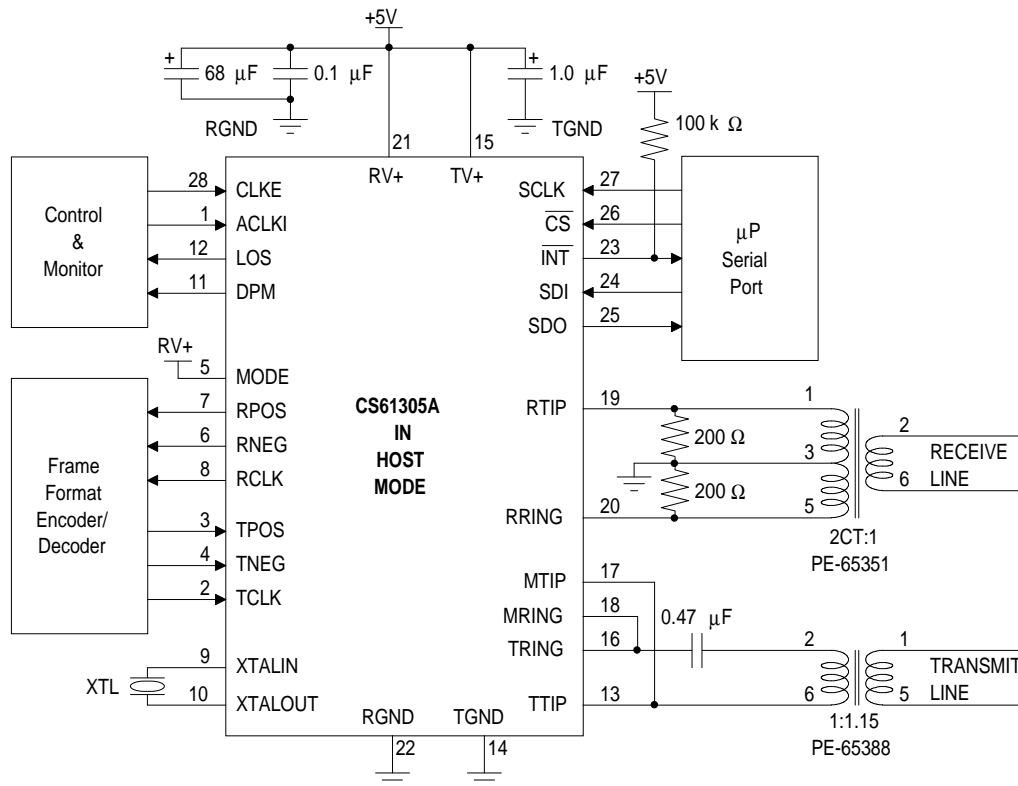
**Figure A2. T1 Host Mode Configuration**

Figures A2-A4 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

*Transformers*

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 are recommended for use with the CS61305A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

*Selecting an Oscillator Crystal*

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

*Line Protection*

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the Application Note "Secondary Line Protection for T1 and E1 Line Cards" for detailed information on the different electrical safety standards and specific application circuit recommendations.
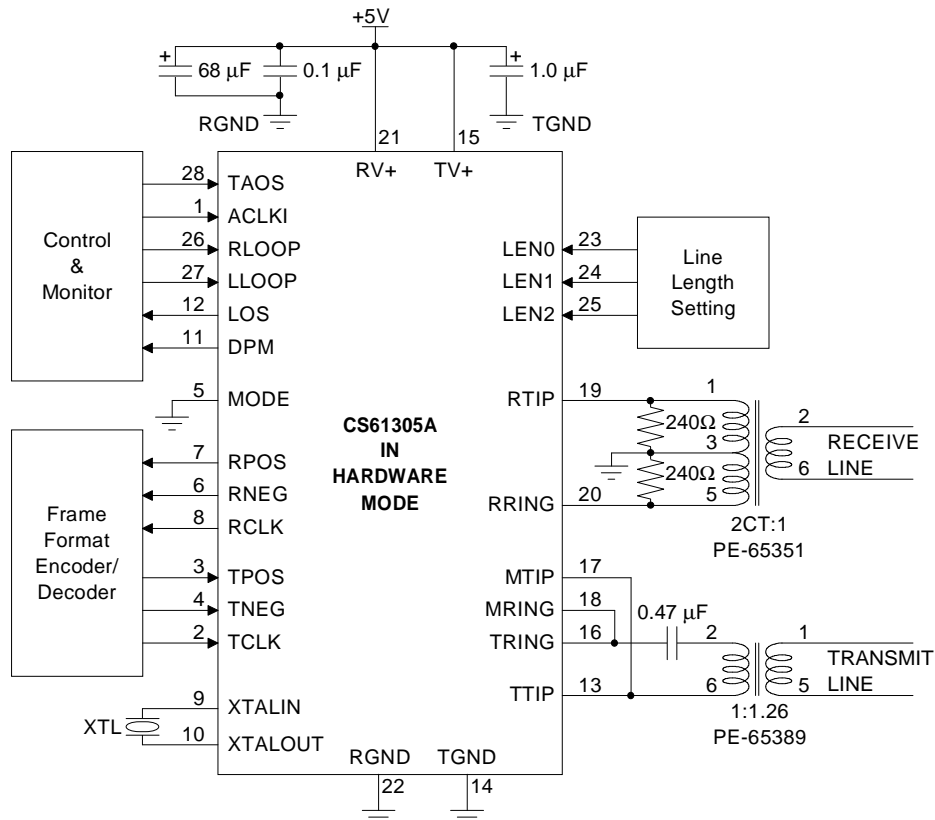
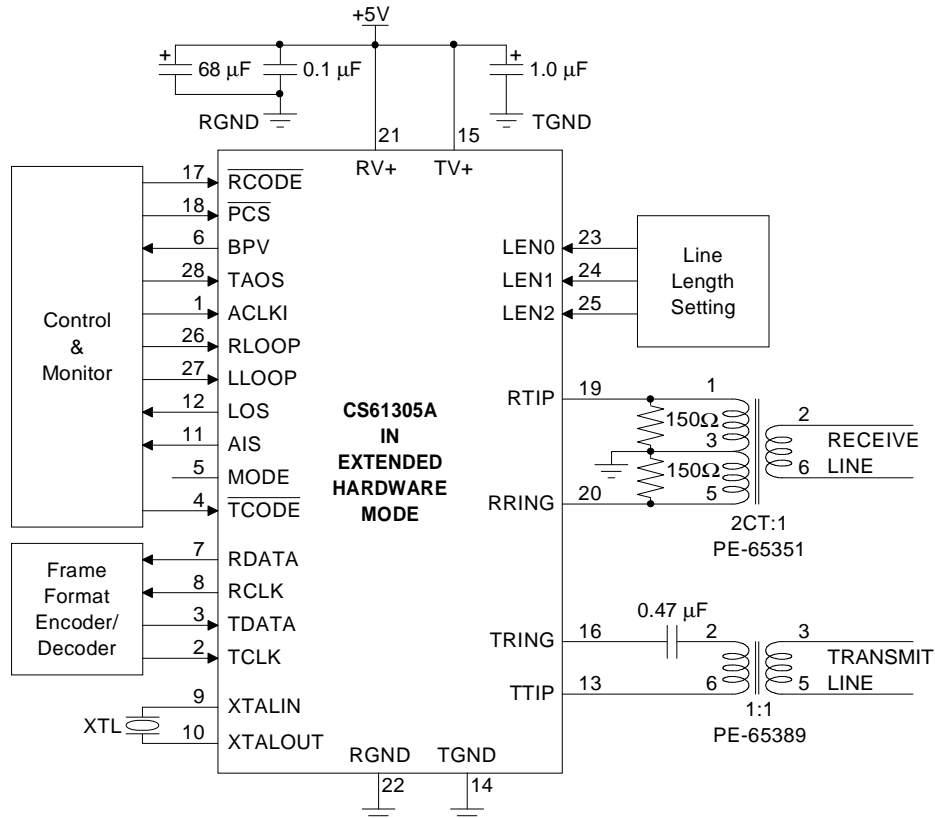**Figure A3. 120 Ω, E1 Hardware Mode Configuration**



**Figure A4. 75 Ω, E1 Extended Hardware Mode Configuration**

| Parameter | Receiver | Transmitter |
|---|---|---|
| Turns Ratio | 1:2 CT ± 5% | 1:1 ± 1.5 % for 75 Ω E1<br>1:1.15 ± 5 % for 100 Ω T1<br>1:1.26 ± 1.5 % for 120 Ω E1 |
| Primary Inductance | 600 µH min. @ 772 kHz | 1.5 mH min. @ 772 kHz |
| Primary Leakage Inductance | 1.3 µH max. @ 772 kHz | 0.3 µH max. @ 772 kHz |
| Secondary Leakage Inductance | 0.4 µH max. @ 772 kHz | 0.4 µH max. @ 772 kHz |
| Interwinding Capacitance | 23 pF max. | 18 pF max. |
| ET-constant | 16 V-µs min. for T1<br>12 V-µs min. for E1 | 16 V-µs min. for T1<br>12 V-µs min. for E1 |

**Table A2. Transformer Specifications**

*Interfacing The CS61305A With the*
*CS62180B T1 Transceiver*

To interface with the CS62180B, connect the devices as shown in Figure A5. In this case, the line interface and CS62180B are in Host mode controlled by a microprocessor serial interface. If the line interface is used in Hardware mode, then the line interface RCLK output must be inverted before being input to the CS62180B. If the CS61305A is used in Extended Hardware Mode, the RCLK output does not have to be inverted before being input to the CS62180B.
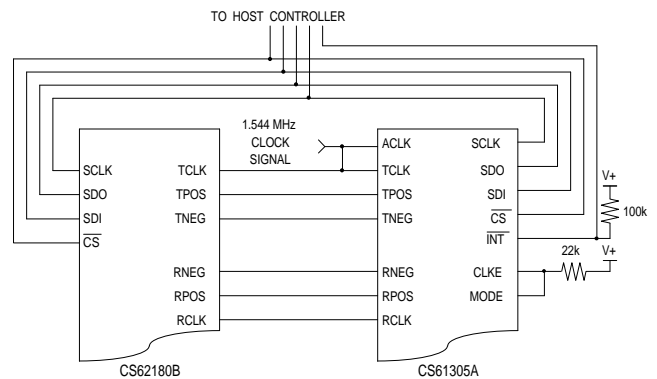


**Figure A5. Interfacing the CS61305A with a CS62180B (Host Mode)**

| Application | Turns Ratio(s) | Manufacturer | Part Number | Package Type |
|---|---|---|---|---|
| RX: T1 & E1 | 1:2CT | Pulse Engineering | PE-65351 | 1.5 kV through-hole, single |
| | | Schott | 67129300 | |
| | | Bel Fuse | 0553-0013-HC | |
| TX: T1 | 1:1.15 | Pulse Engineering | PE-65388 | 1.5 kV through-hole, single |
| | | Schott | 67129310 | |
| | | Bel Fuse | 0553-0013-RC | |
| TX: E1 (75 & 120 Ω) | 1:1.26 1:1 | Pulse Engineering | PE-65389 | 1.5 kV through-hole, single |
| | | Schott | 67129320 | |
| | | Bel Fuse | 0553-0013-SC | |
| RX &TX: T1 | 1:2CT 1:1.15 | Pulse Engineering | PE-65565 | 1.5 kV through-hole, dual |
| | | Bel Fuse | 0553-0013-7J | |
| RX &TX: E1 (75 & 120 Ω) | 1:2CT 1:1.26 1:1 | Pulse Engineering | PE-65566 | 1.5 kV through-hole, dual |
| | | Bel Fuse | 0553-0013-8J | |
| RX &TX: T1 | 1:2CT 1:1.15 | Pulse Engineering | PE-65765 | 1.5 kV surface-mount, dual |
| | | Bel Fuse | S553-0013-06 | |
| RX &TX: E1 (75 & 120 Ω) | 1:2CT 1:1.26 1:1 | Pulse Engineering | PE-65766 | 1.5 kV surface-mount, dual |
| | | Bel Fuse | S553-0013-07 | |
| RX : T1 & E1 | 1:2CT | Pulse Engineering | PE-65835 | 3 kV through-hole, single EN60950, EN41003 approved |
| TX: E1 (75 & 120 Ω) | 1:1.26 1:1 | Pulse Engineering | PE-65839 | 3 kV through-hole, single EN60950, EN41003 approved |

**Table A3. Recommended Transformers**

**• Notes •**

# Line Interface Evaluation Board

## Features

● Socketed Line Interface Device

● All Required Components for Complete Line Interface Evaluation

● Configuration by DIP Switch or Serial Interface

● LED Status Indicators for Alarm Conditions

● Support for Host, Hardware, and Extended Hardware Modes

## General Description

The evaluation board includes a socketed line interface device and all support components necessary for evaluation. The board is powered by an external 5 Volt supply.

The board may be configured for 100 Ω twisted-pair T1, 75 Ω coax E1, or 120 Ω twisted-pair E1 operation. Binding posts are provided for line connections. Several BNC connectors are available to provide system clocks and data I/O. Two LED indicators monitor device alarm conditions. The board supports all line interface operating modes.

**ORDERING INFORMATION:**
CDB61534, CDB61535. CDB61535A, CDB6158, CDB6158A, CDB61574, CDB61574A, CDB61575, CDB61577, CDB61304A, CDB61305A
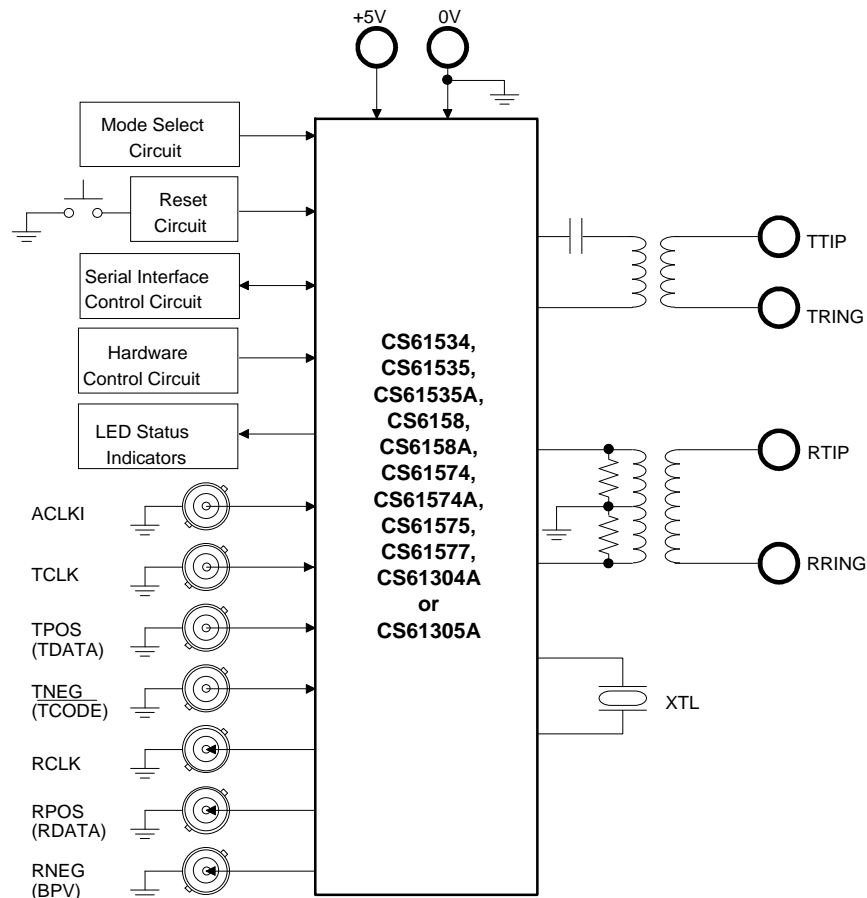
## POWER SUPPLY

As shown on the evaluation board schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labeled +5V and GND. Transient suppressor D10 protects the components on the board from over-voltage damage and reversed supply connections. The recommended power supply decoupling is provided by C1, C2 and C3. Ceramic capacitor C1 and electrolytic capacitor C2 are used to decouple RV+ to RGND. Capacitor C3 decouples TV+ to TGND. The TV+ and RV+ power supply traces are connected at the device socket U1. A ground plane on the component side of the evaluation board insures optimum performance.

## BOARD CONFIGURATION

Pins on line interface device U1 with more than one pin name have different functions depending on the operating mode selected. Pin names not enclosed in parenthesis or square brackets describe the Hardware mode pin function. Pin names enclosed in parenthesis describe the Extended Hardware mode pin function. Pin names enclosed in square brackets describe the Host mode pin function.

Table 1 explains how to configure the evaluation board jumpers depending on the device installed and the desired operating mode. Mode selection is accomplished with slide switch SW1 and jumpers JP2, JP6, and JP7. The CS61535A, CS61574A, CS61575, CS61577, CS61304A, and CS61305A support the Hardware, Extended Hardware, and Host operating modes. The CS61534, CS61535, and CS61574 support the Hardware and Host operating modes. The CS6158 and CS6158A only support the Hardware operating mode.

### Hardware Mode

In the Hardware operating mode, the line interface is configured using DIP switch S2. The digital control inputs to the device selected by S2 include: transmit all ones (TAOS), local loopback (LLOOP), remote loopback (RLOOP), and transmit line length selection (LEN2,LEN1,LEN0). Closing a DIP switch on S2 towards the label sets the device control pin of the same name to logic 1 (+5 Volts). Note that S2 switch positions $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ have no function in Hardware mode. In addition, the host processor interface connector JP1 should not be used in the Hardware mode.

Two LED status indicators are provided in Hardware mode. The LED labeled DPM (AIS) illuminates when the line interface asserts the Driver

| JUMPER | POSITION | FUNCTION SELECTED |
|---|---|---|
| JP1 | - | Connector for external processor in Host operating mode. |
| JP2, JP6, JP7 | A-A | Extended Hardware operating mode. |
| | B-B | Hardware or Host operating modes. |
| JP3 | IN | Hardware or Extended Hardware operating modes. |
| | OUT | Host operating mode. |
| JP4 | C-C | Connects the ACLKI BNC input to pin 1 of device. |
| | D-D | Grounds the ACLKI BNC input through 51Ω resistor R1. |
| JP5 | E-E | Transmit line connection for all applications except those listed for "F-F" on the next line. |
| | F-F | 75Ω coax E1 applications using the Schott 12932/12532 or PE-65389/65566 at transformer T1. |
| JP8 | IN | Shorts resistor R2 for all applications except those listed for "OUT" on the next line. |
| | OUT | Inserts resistor R2 for 75Ω coax E1 applications using the CS61534, 35, 58, 74, or 77. |

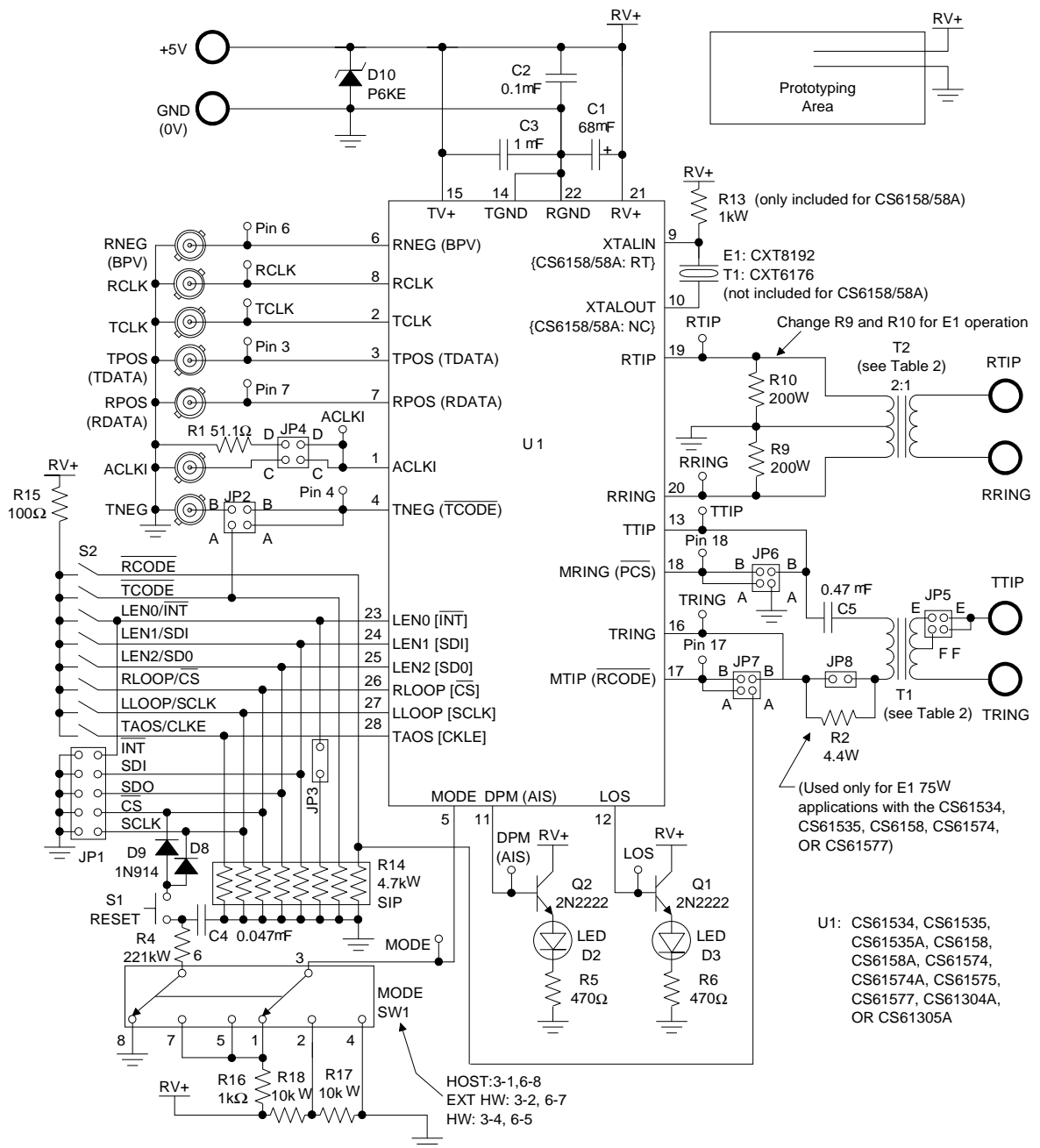**Table 1. Evaluation Board Jumper Settings**

**Figure 1. Evaluation Board Schematic**

Performance Monitor alarm. The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

**Extended Hardware Mode**

In the Extended Hardware operating mode, the line interface is configured using DIP switch S2. The digital control inputs to the device selected by S2 include: transmit all ones (TAOS), local loopback (LLOOP), remote loopback (RLOOP), transmit line length selection (LEN2, LEN1, LEN0), transmit line code ($\overline{\text{TCODE}}$), and receive line code ($\overline{\text{RCODE}}$). Closing a DIP switch (moving it towards the S2 label) sets the device control pin of the same name to logic 1 (+5 Volts). Note that the $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ options are active low and are enabled when the switch is moved away from the S2 label. The parallel chip select input $\overline{\text{PCS}}$ is tied to ground in Extended Hardware mode to enable the device to be reconfigured when S2 is changed. In addition, the host processor interface connector JP1 should not be used in Extended Hardware mode.

Two LED status indicators are provided in Extended Hardware mode. The LED labeled DPM (AIS) illuminates when the line interface detects the receive blue alarm (AIS). The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

**Host Mode**

In the Host operating mode, the line interface is configured using a host processor connected to the serial interface port JP1. The S2 switch position labeled CLKE selects the active edge of SCLK and RCLK. Closing the CLKE switch selects RPOS and RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK as required by the CS2180B T1 framer.

All other DIP switch positions on S2 should be open (logic 0) to prevent shorting of the serial in-

terface signals. Resistor R15 is a current limiting resistor that prevents the serial interface signals from being shorted directly to the +5 Volt supply if any S2 switch, other than CLKE, is closed. Jumper JP3 should be out so the $\overline{\text{INT}}$ pin may be externally pulled-up at the host processor interrupt pin.

Two LED status indicators are provided in Host mode. The LED labeled DPM (AIS) illuminates when the line interface asserts the Driver Performance Monitor alarm. The LED labeled LOS illuminates when the line interface receiver has detected a loss of signal.

**Manual Reset**

A manual reset circuit is provided that can be used in Hardware and Extended Hardware modes. The reset circuit consists of S1, R4, R16, C4, D8, and D9. Pressing switch S1 forces both LLOOP and RLOOP to a logic 1 and causes a reset. A reset is only necessary for the CS61534 device to calibrate the center frequency of the receiver clock recovery circuit. All other line interface units use a continuously calibrated clock recovery circuit that eliminates the reset requirement.

**TRANSMIT CIRCUIT**

The transmit clock and data signals are supplied on BNC inputs labeled TCLK, TPOS(TDATA), and TNEG. In the Hardware and Host operating modes, data is supplied on the TPOS(TDATA) and TNEG connectors in dual NRZ format. In the Extended Hardware operating mode, data is supplied in NRZ format on the TPOS(TDATA) connector and TNEG is not used.

The transmitter output is transformer coupled to the line through a transformer denoted as T1 in Figure 1. The signal is available at the TTIP and TRING binding posts. Capacitor C5 is the recommended 0.47 µF DC blocking capacitor.

The evaluation board supports 100Ω twisted-pair T1, 75Ω coax E1, and 120Ω twisted-pair E1 operation. The CDB61534, CDB61535, CDB6158, CDB61574, and CDB61577 are supplied from the factory with a 1:2 transmit transformer that may be used for all T1 and E1 applications. The CDB61535A, CDB6158A, CDB61574A, CDB61575, CDB61304A, and CDB61305A are supplied with a 1:1.15 transmit transformer installed for T1 applications. An additional 1:1:1.26 transformer for E1 applications is provided with the board. This transformer requires JP5 to be jumpered across F-F for 75Ω coax E1 applications.

The CDB61534, CDB61535, CDB6158, CDB61574, and CDB61577 require the JP8 jumper to be out for 75Ω coax E1 applications. This inserts resistor R2 to reduce the transmit pulse amplitude and meet the 2.37 V nominal pulse amplitude requirement in CCITT G.703. In addition, R2 increases the equivalent load impedance across TTIP and TRING.

## RECEIVE CIRCUIT

The receive line interface signal is input at the RTIP and RRING binding posts. The receive signal is transformer coupled to the line interface device through a center-tapped 1:2 transformer. The transformer produces ground referenced pulses of equal amplitude and opposite polarity on RTIP and RRING.

The receive line interface is terminated by resistors R9 and R10. The evaluation boards are supplied from the factory with 200Ω resistors for terminating 100Ω T1 twisted-pair lines. Resistors R9 and R10 should be replaced with 240Ω resistors for terminating 120Ω E1 twisted-pair lines or 150Ω resistors for terminating 75Ω E1 coaxial lines. Two 243Ω resistors and two 150Ω resistors are included with the evaluation board for this purpose.

The recovered clock and data signals are available on BNC outputs labeled RCLK, RPOS(RDATA), and RNEG(BPV). In the Hardware and Host operating modes, data is output on the RPOS(RDATA) and RNEG(BPV) connectors in dual NRZ format. In the Extended Hardware operating mode, data is output in NRZ format on the RPOS(RDATA) connector and bipolar violations are reported on the RNEG(BPV) connector.

## QUARTZ CRYSTAL

A quartz crystal must be installed in socket Y1 for all devices except the CS6158 and CS6158A. A Crystal Semiconductor CXT6176 crystal is recommended for T1 operation and a CXT8192 is recommended for E1 operation. The evaluation board has a CXT6176 installed at the factory and a CXT8192 is also provided with the board.

The CDB6158 and CDB6158A have resistor R13 installed instead of a crystal. This connects the RT pin of the device to the +5 Volt supply.

## ALTERNATE CLOCK INPUT

The ACLKI BNC input provides the alternate clock reference for the line interface device (ACLK for the CS61534) when JP4 is jumpered across C-C. This clock is required for the CS61534, CS61535, CS6158, and CS6158A operation but is optional for all other line interface devices. If ACLKI is provided, it may be desirable to connect both C-C and D-D positions on JP4 to terminate the external clock source providing ACLKI with the 51Ω resistor R1. If ACLKI is optional and not used, connector JP4 should be jumpered across D-D to ground pin 1 of the device through resistor R1.

## TRANSFORMER SELECTION

To permit the evaluation of other transformers, Table 2 lists the transformer and line interface device combinations that can be used in T1 and E1

applications. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the device. The transformer is installed in the evaluation board with pin 1 positioned to match the letter illustrated on the drawing in Table 2. For example, the Pulse Engineering PE-65388 transformer may be used with the transmitter of the CS61575 device for 100Ω T1 applications only (as indicated by note 3) when installed in transformer socket T1 with pin 1 at position D (upper right).

## PROTOTYPING AREA

A prototyping area with power supply and ground connections is provided on the evaluation board. This area can be used to develop and test a variety of additional circuits like a data pattern generator, CS2180B framer, system synchronizer PLL, or specialized interface logic.

## EVALUATION HINTS

1. Properly terminate TTIP/TRING when evaluating the transmit output signal. For more information concerning pulse shape evaluation, refer to the Crystal application note entitled "Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems."

2. Change the receiver terminating resistors R9 and R10 when evaluating E1 applications. Resistors R9 and R10 should be replaced with 240Ω resistors for terminating 120Ω E1 twisted-pair lines or 150Ω resistors for terminating 75Ω E1 coaxial lines. Two 243Ω resistors and two 150Ω resistors are included with the evaluation board for this purpose.

3. Closing a DIP switch on S2 towards the label sets the device control pin of the same name to logic 1 (+5 Volts).

4. To avoid damage to the external host controller connected to JP1, all S2 switch positions (except CLKE) should be open. In the Host operating mode, the CLKE switch selects the active edge of SCLK and RCLK.

| TRANSFORMER (Turns Ratio)[1,2] | LINE INTERFACE UNIT | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | '34 | | '35 | | '35A | | '58 | | '58A | | '74,'77 | | '74A | | '75 | | '304A, '305A | |
| | RX | TX | RX | TX | RX | TX | RX | TX | RX | TX | RX | TX | RX | TX | RX | TX | RX | TX |
| PE-65351 (1:2CT) | A | D | A | D | A | | A | D | A | | A | D | A | | A | | A | |
| Schott 12930 (1:2CT) | B | C | B | C | B | | B | C | B | | B | C | B | | B | | B | |
| PE-65388 (1:1.15) | | | | | | $D^3$ | | | | $D^3$ | | | | $D^3$ | | $D^3$ | | $D^{3,5}$ |
| Schott 12931 (1:1.15) | | | | | | $C^3$ | | | | $C^3$ | | | | $C^3$ | | $C^3$ | | $C^{3,5}$ |
| PE-65389 (1:1:1.26) | | | | | | $D^4$ | | | | $D^4$ | | | | $D^4$ | | $D^4$ | | $D^{4,5}$ |
| Schott 12932 (1:1:1.26) | | | | | | $C^4$ | | | | $C^4$ | | | | $C^4$ | | $C^4$ | | $C^{4,5}$ |
| PE-64951 (dual 1:2CT) | E | | E | | | | E | | | | E | | | | | | | |
| Schott 11509 (dual 1:2CT) | E | | E | | | | E | | | | E | | | | | | | |
| PE-65565 (dual 1:1.15 & 1:2CT) | | | | | $E^3$ | | | | $E^3$ | | | | $E^3$ | | $E^3$ | | $E^{3,5}$ | |
| Schott 12531 (dual 1:1.15 & 1:2CT) | | | | | $E^3$ | | | | $E^3$ | | | | $E^3$ | | $E^3$ | | $E^{3,5}$ | |
| PE-65566 (dual 1:1:1.26 & 1:2CT) | | | | | $E^4$ | | | | $E^4$ | | | | $E^4$ | | $E^4$ | | $E^{4,5}$ | |
| Schott 12532 (dual 1:1:1.26 & 1:2CT) | | | | | $E^4$ | | | | $E^4$ | | | | $E^4$ | | $E^4$ | | $E^{4,5}$ | |



NOTES:

1. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the device. The transformer is installed in the evaluation board with pin 1 positioned to match the letter illustrated in the drawing to the left.

2. The receive transformer (RX) is soldered at location T2 on the evaluation board and is used for all applications. The transmit transformer (TX) is socketed at location T1 on the evaluation board and may be changed according to the application.

3. For use in 100Ω T1 twisted-pair applications only.

4. For use in 75Ω and 120Ω E1 applications only. Place jumper JP5 in position F-F for 75Ω E1 applications requiring a 1:1 turns ratio.

5. Transmitter return loss improves when using a 1:2 turns ratio transformer with the appropriate transmit resistors.
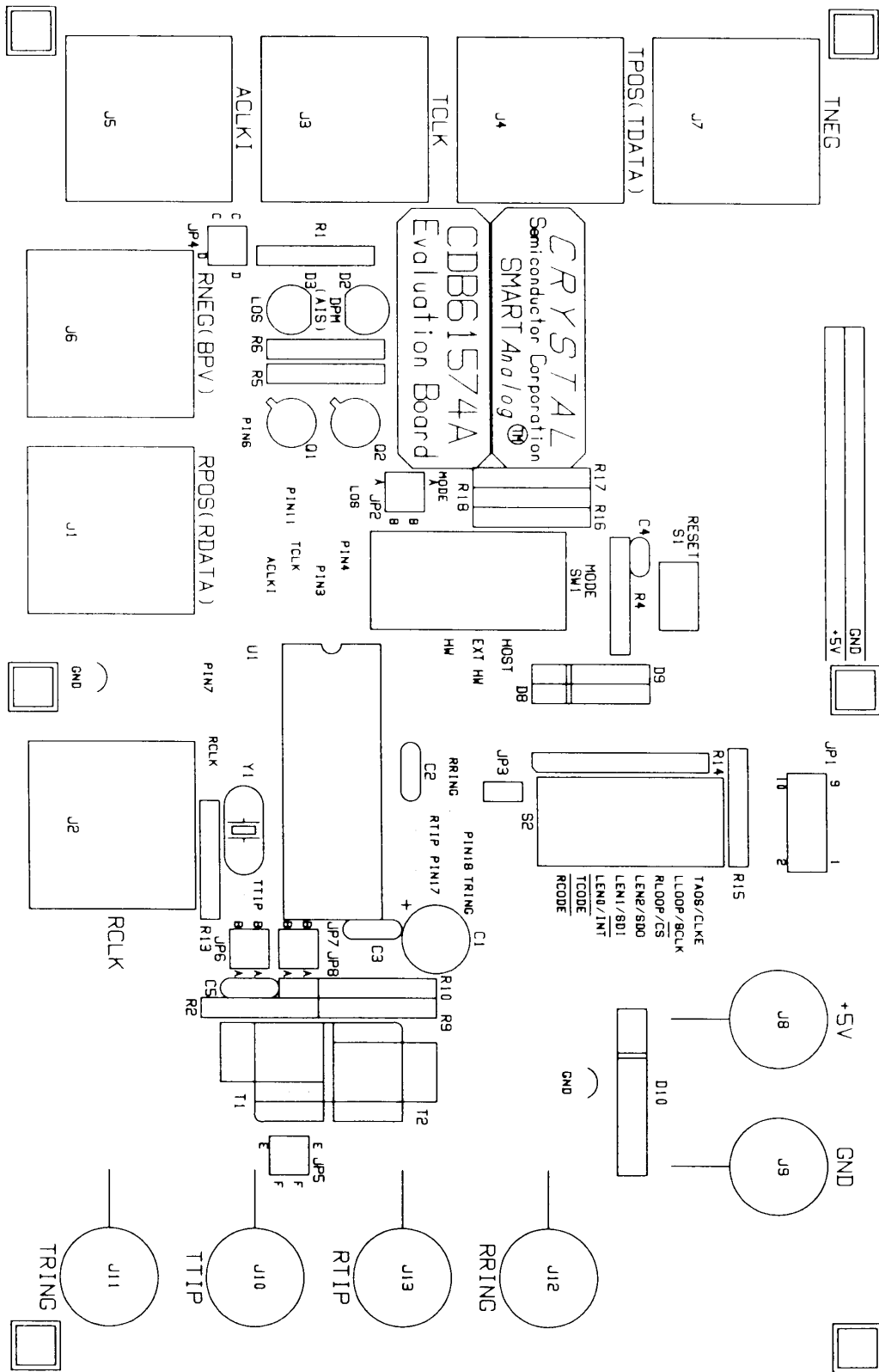
**Table 2. Transformer Applications**
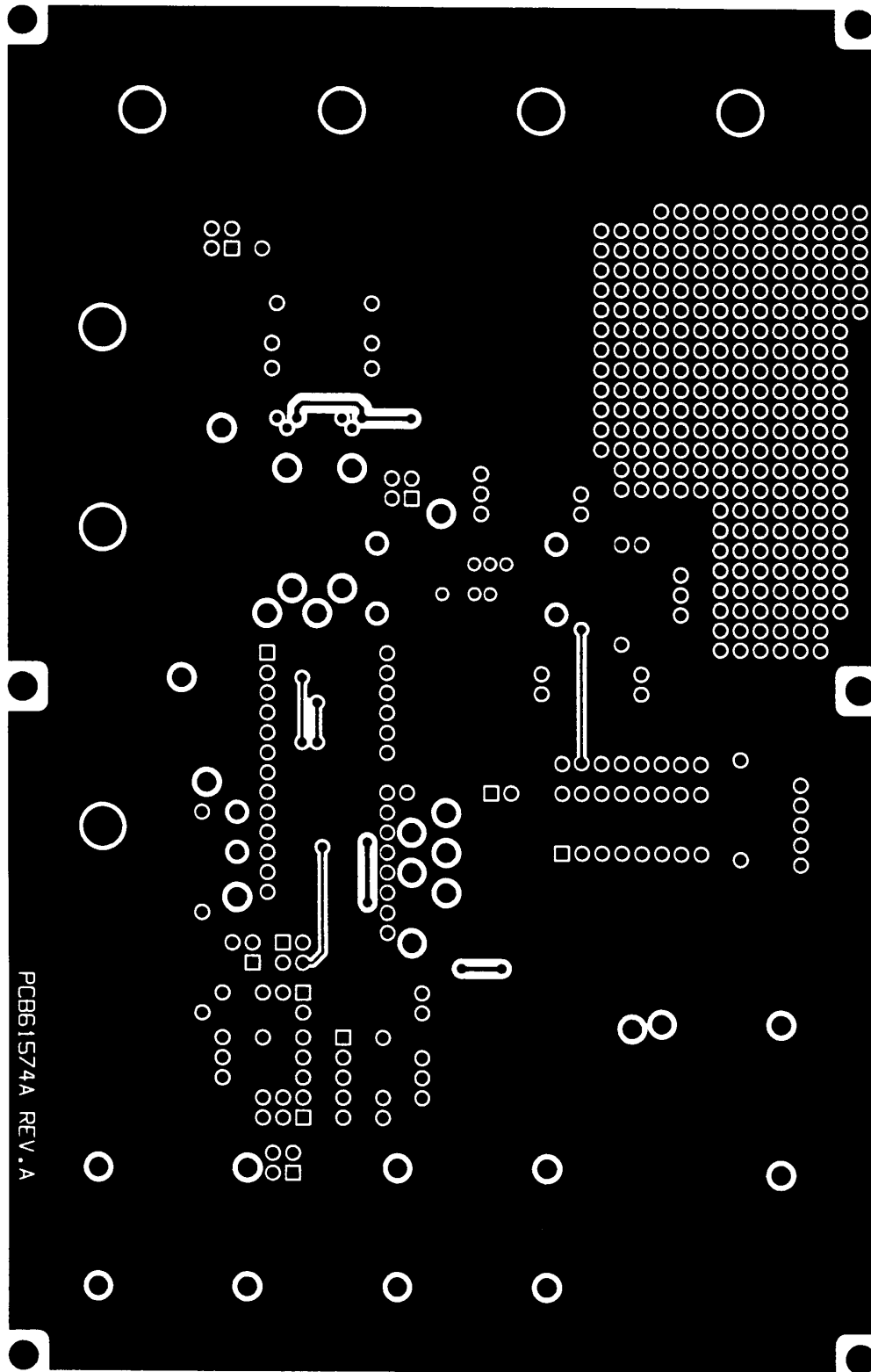
**Figure 2. Silk Screen Layer (NOT TO SCALE)**

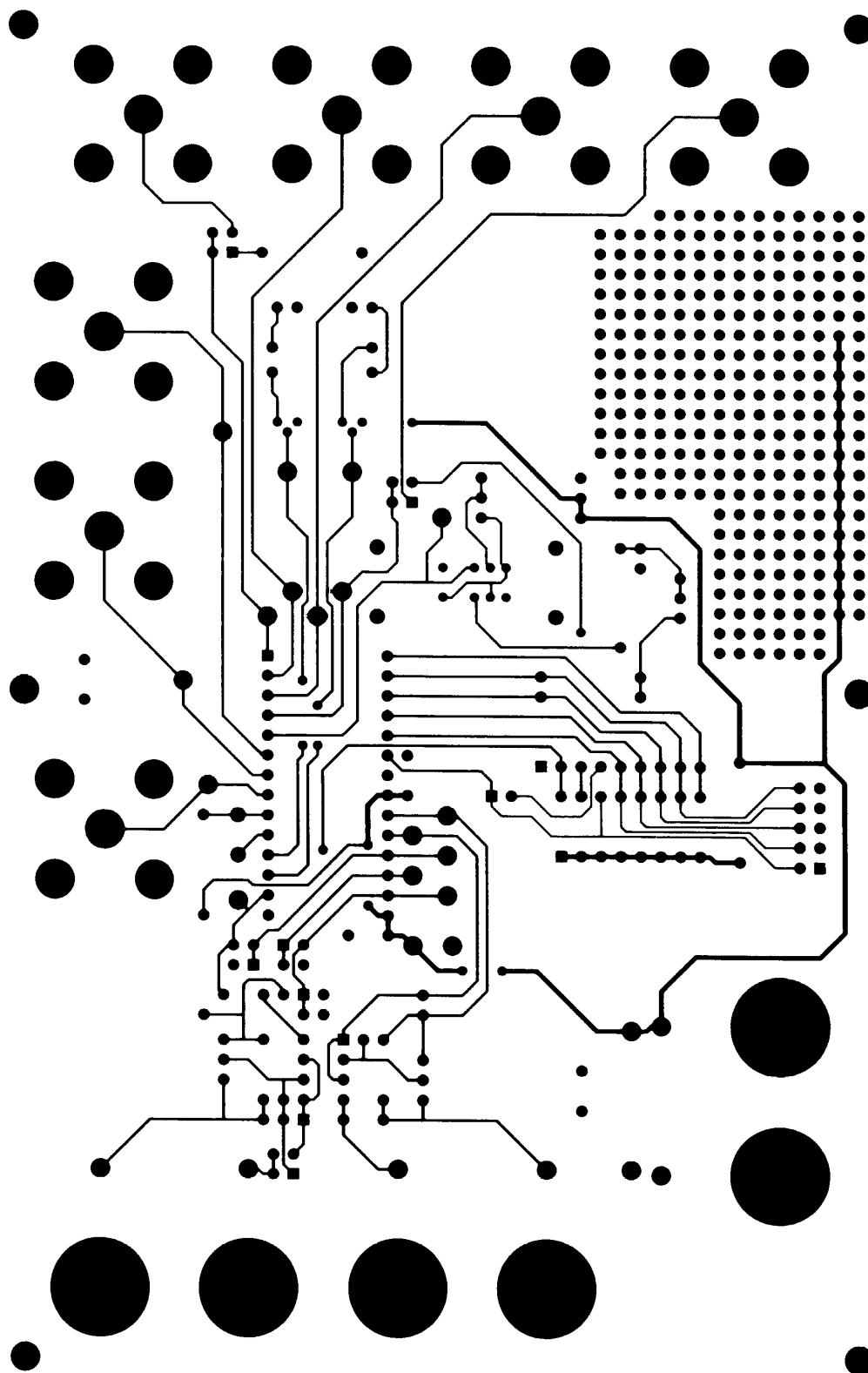**Figure 3.  Top Ground Plane Layer (NOT TO SCALE)**

**Figure 4.  Bottom Trace Layer (NOT TO SCALE)**

**CRYSTAL**

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