



CS7622

CCD Imager Analog Processor

Features

- 13-Bit A/D Conversion Using DRX™ Technology
- Backlight Compensation
- Supports Full Scale Analog Input Voltage Ranges from 300 mV to 1 V in 100 mV Increments
- High Resolution Output Mode
- Low Resolution (Preview) Output Mode for LCD Driver
- Integrated Correlated Double Sampler
- Digital Black Level Clamp
- Digital Outputs Selectable for 13, 12, or 10 Bits
- Low Power Consumption
- Power Down Mode
- High Speed Serial Interface
- Supports a Large Variety of Clock Input Frequencies
- Low power mode option

Description

The CS7622 is a low-power analog front-end processor for interline or frame transfer CCD imagers. Main applications include digital still image cameras and video cameras.

The architecture includes a correlated double sampler, black level clamp and a 13-bit A/D conversion module using patented DRX technology.

Chip parameters can be programmed using a high speed 4-wire asynchronous digital interface.

The chip outputs digitized CCD data in either 13-bit, 12-bit or 10-bit format. 10-bit outputs are generated from the 13-bit A/D output by a programmable companding curve.

ORDERING INFORMATION

CS7622-IQ -40 to +85 °C 32-pin TQFP 7x7x1.4mm

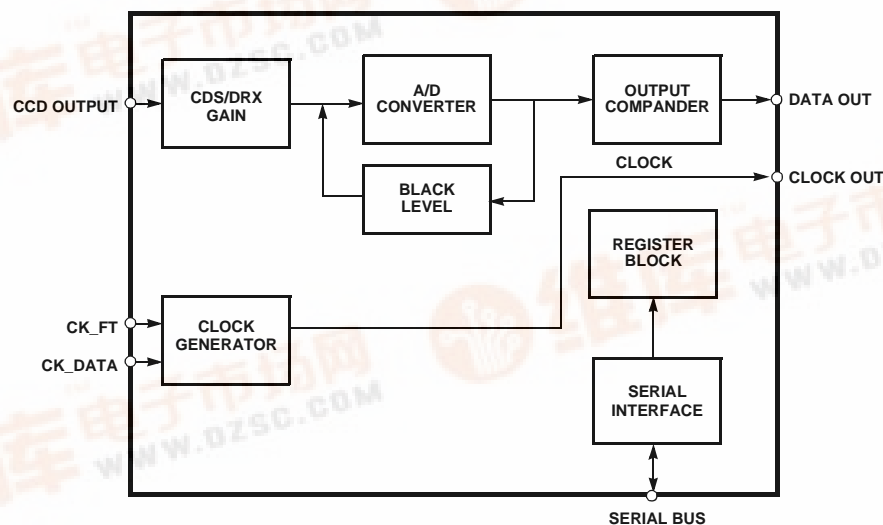


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1.0 CHARACTERISTICS/SPECIFICATIONS

DIGITAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{DD} = 3.3\text{ V}$)

Parameter	Symbol	Min	Typ	Max	Units
Logic Inputs					
High-Level Input Voltage	V_{IH}	$V_{DD}-0.8$	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
Input Leakage Current	I_{IN}	-	-	10	mA
Logic Outputs					
High-Level Output Source Current @ $I_{OH} = 4\text{ mA}$	V_{OH}	$V_{DD}-0.4$	-	-	mV
Low-Level Output Sink Current @ $I_{OL} = 4\text{ mA}$	V_{OL}	-	-	0.4	mV
3-State Leakage Current	I_{OZ}	-	-	10	μA

POWER CONSUMPTION ($T_A = 25^\circ\text{C}$; $V_{DDA} = V_{DDD} = 3.3\text{ V}$; Output Load = 30 pF; Input Clock = 15MHz)

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation	Peak Mode P_D	-	214	-	mW
	Preview Mode P_{DLR}	-	162	-	mW
	Stand By Down P_{DPD}	-	0.0825	-	mW
Analog Power Supply Current	Peak Mode I_{AN}	-	53	-	mA
	Preview Mode I_{ALR}	-	37	-	mA
	Stand By Down I_{APD}	-	0.025	-	mA
Digital Power Supply Current	Peak/Preview Mode I_{DN}	-	12	-	mA
	Preview Mode I_{DPD}	-	0	-	mA

RECOMMENDED OPERATING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V_{DDA}	3.0	3.3	3.6	V
	V_{DDD}	2.5		3.6	V
GNDA to GNDD Voltage Differential				10	mV
Analog Full Scale Input Voltage Range	A_{IN}	300 mV	-	1 V	V_{p-p}
Input Clock Rate		-	20 MHz	-	MHz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DDA}, V_{DDD}	-0.3	6.0	V
Digital Input Voltage		GNDD-0.3	$V_{DDD}+0.3$	V
Analog Input Voltage	A_{IN}	GNDA-0.3	$V_{DDA}+0.3$	V
Input Current (except supply pins)			10	mA
Ambient Temperature Range		-0	+70	$^\circ\text{C}$
Lead Solder Temperature (10sec duration)			+260	$^\circ\text{C}$
Storage Temperature Range		-65	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

ADC (ANALOG-TO-DIGITAL CONVERTER)

Parameter	Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage Range		300 mV		1 V	V _{0-p}
Full Scale Input Voltage Range Resolution			100		mV
ADC resolution		-	10	-	bits
Total Differential Non-Linearity		-	±1	-	LSB
Total Integral Non-Linearity		-	±1	-	LSB

CDS/VGA PARAMETERS

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range		300 mV		1 V	V _{0-p}
Total Gain Range	A _{VGA}	-	18	-	dB
Input Referred Noise (rms) Maximum Gain Setting	V _{nVGA}	-	-	0.2	mV

SERIAL INTERFACE TIMING SPECIFICATIONS

Description	Symbol	Minimum	Maximum	Unit
Enable Setup	t1	10	-	ns
SDAT Setup	t2	10	-	ns
SDAT Hold	t3	10	-	ns
Serial Clock Period (Note 1)	t4	143	-	ns
Write Data Invalid	t5	0	10	ns
Read Data Valid	t6	0	10	ns
Clock to Disable	t7	143	-	ns
SEN Rise to SEN Fall	t8	200	-	ns

Notes: 1. the minimum serial clock period must be longer than two pixel clock periods.

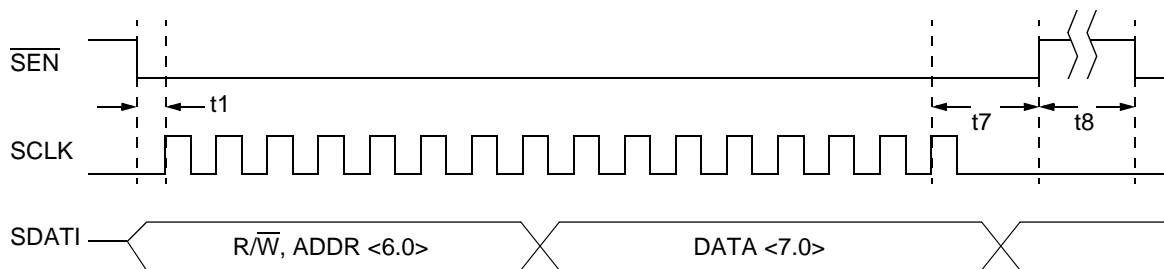


Figure 1. \overline{SEN} Timing

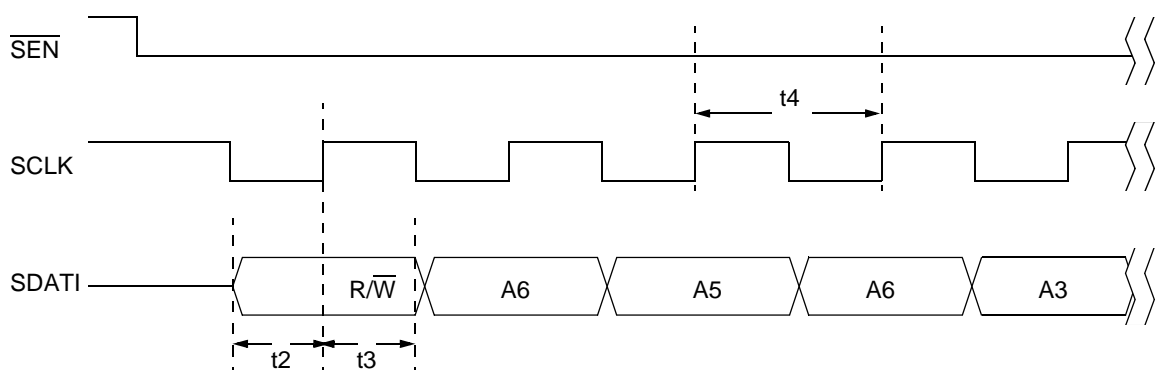


Figure 2. Serial Write Timing

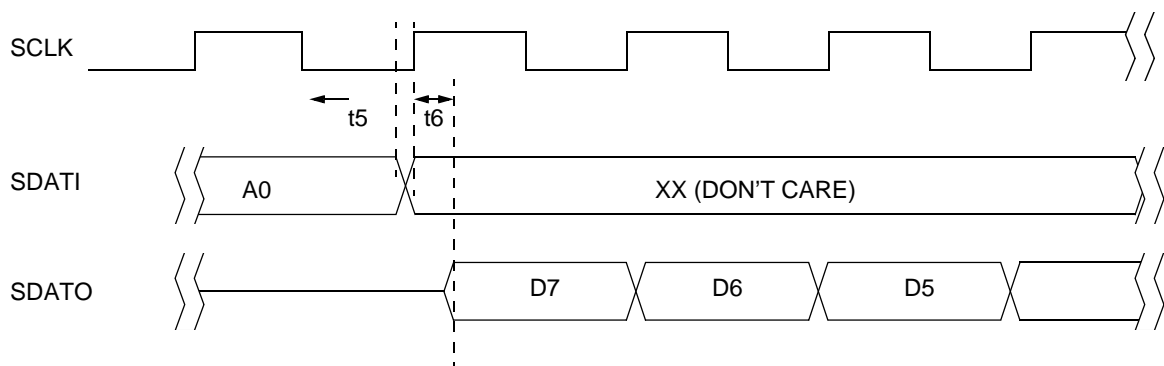


Figure 3. Read Data Timing

2.0 GENERAL DESCRIPTION

The CS7622 forms the heart of a four chip digital CCD Camera. The four chips include the CCD imager, the CS7622 CCD digitizer, a vertical drive interface chip and a backend DSP chip to further process the digital data (see Figure 4.)

The patented DRX technology allows the CS7622 to output data with 13-bit dynamic range, and at the same time reducing the power consumption to a 10-bit equivalent A/D converter.

The digitized output is either available in 13-bits, 12-bits or 10-bits. The 10-bit output is created by companding the 13-bit A/D output to 10-bits. The companding curve consists of 4 linear segments, where each slope and each start point is user programmable.

A block diagram of the CS7622 chip is shown in Figure 5.

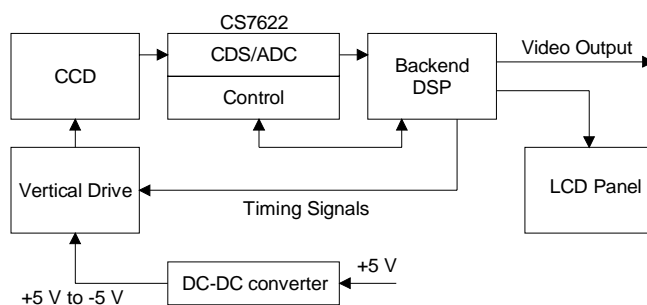


Figure 4. Digital Camera Block Diagram

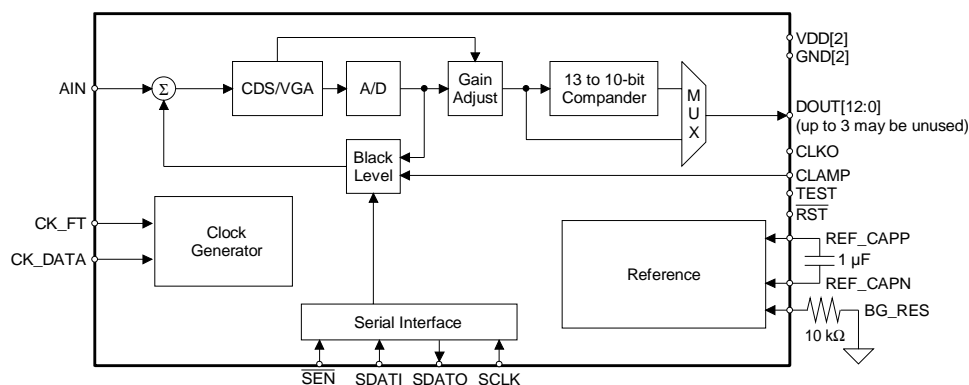


Figure 5. CS7622 Block Diagram

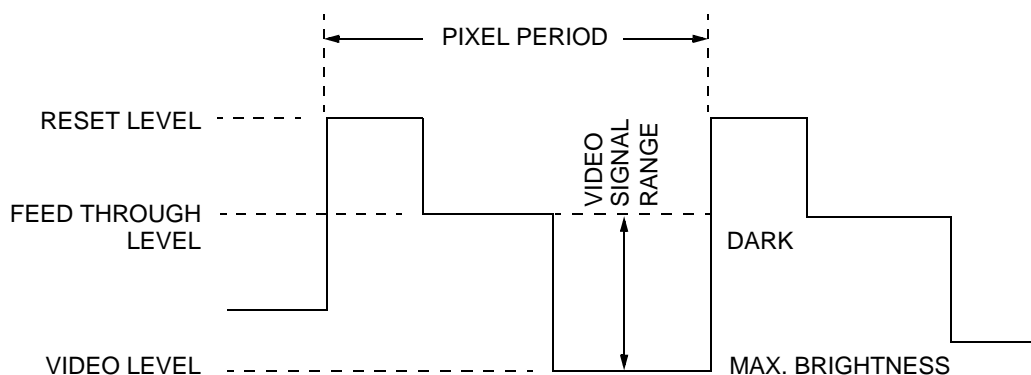


Figure 6. Idealized CCD output waveform

3.0 OPERATION

3.1 CDS/VGA (correlated double sampling/variable gain amplification)

An idealized waveform of the CCD output is shown in Figure 6.

The CCD output contains reset noise, thermal noise, and 1/f noise generated in the CCD output circuit. This degrades the S/N ratio and must be cancelled. Since the noise during the active video portion of the CCD signal is assumed to be correlated with the noise during the feed through portion of the signal, this noise can be cancelled by subtracting the feed through level from the video level. This operation is called correlated double sampling. The active video signal is the difference between the feed through and video levels. The active video signal varies according to light conditions. In order to insure that the full dynamic range of the ADC is utilized even under low light conditions, the CCD output is amplified using a VGA. The gain control is provided by a 2 bit control word generated by an ADC after stage 1, which has a gain of 1. Based on the input voltage, a gain of 1x, 2x, 4x, or 8x is subsequently applied to the signal. The amount of gain is later adjusted in the digital section. After the VGA, the signal gets digitized by a 10 bit ADC. The 2 bit ADC output is used in

combination with the 10 bit ADC output to produce a 13 bit output.

Adding more gain before the ADC does not offer performance improvement because the noise of the CCD (after gain is applied to it) begins to dominate over the quantization noise. Any additional gain should be done in digital since the performance is the same as when the ADC output has the additional gain applied.

In order to add more flexibility, the full scale input range is programmable through register 05h. This setting will determine what input level maps to the highest ADC output code. Thus depending on the saturation level of the particular CCD used in the system, an appropriate full scale input level can be chosen in the CS7622. The choices of full scale input level are 300 mV to 1 V in 100 mV increments. In the remainder of this document, all the figures and discussions assume a full scale level of 1 V is used.

The transfer function of the VGA portion of the circuit is shown in Figure 7 with full scale level = 1 V. It is assumed that the CDS has already been performed. If desired, the gain switching functionality can be disabled and forced to a fixed gain of 8x, 4x, 2x, or 1x. This way any dynamic range enhancement is lost and the digital output is only 10 bits. If

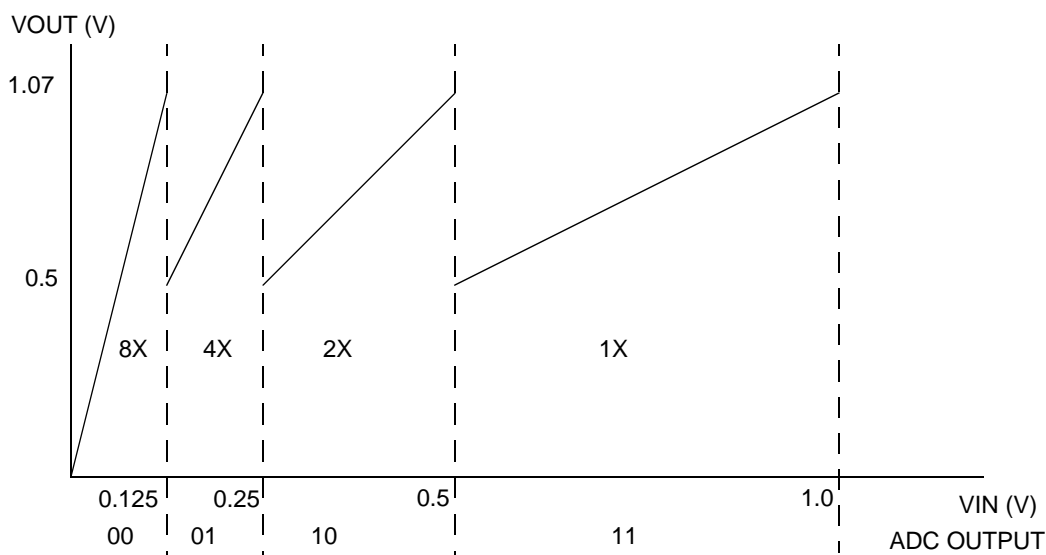


Figure 7. Transfer function of VGA circuit (assuming full scale level of 1.0 V)

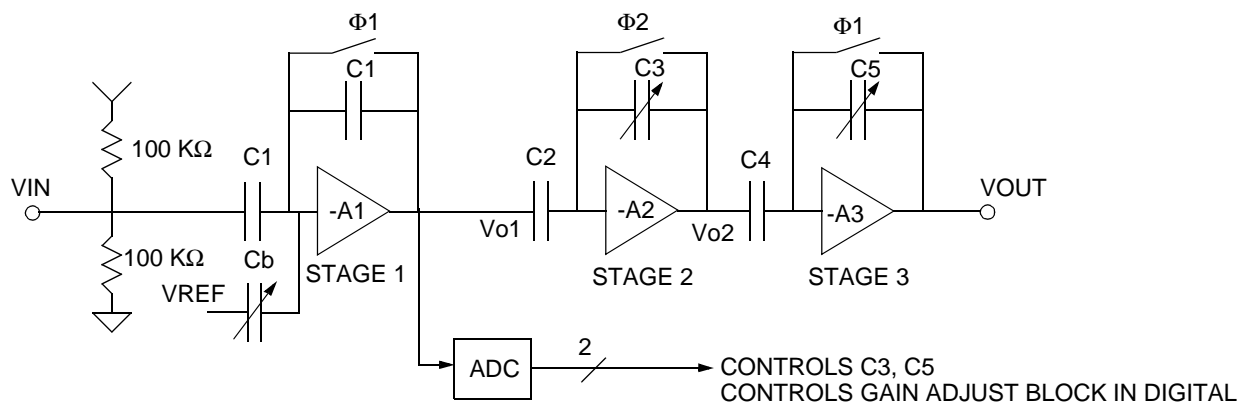


Figure 8. Block diagram of CDS/VGA circuit

a fixed gain of 1x is selected, DOUT[12:3] is used as the output, a fixed gain of 2x will use DOUT[11:2], etc. In order to use this mode, the fixed gain register (14h) should be set and the calibration offset registers (OEh - 10h) should be set to 0.

The CDS/VGA circuit is composed of three stages. The first stage has a fixed gain of 1, and the second and third stages have variable gain with a combined gain range of 1 to 8 (0-18 dB). Figure 8 shows a block diagram of the CDS/VGA circuit. The total gain is $A = (C2/C3)(C4/C5)$ which is adjusted by varying C3 and C5. The capacitor Cb on the front

of stage 1 is for black level adjustment and will be discussed in detail later.

This circuit utilizes a two phase non-overlapping clock to perform the desired CDS function. The two phase clock also allows the video signal to be passed to the output while retaining a positive polarity signal. Figure 9 shows a timing diagram of the two phase clock along with the CCD signal and output signals of stages one, two and three.

There is an internal mid-scale DC bias level circuit at the input pin. This allows AC coupling into the CS7622 with a capacitor and having the input auto-

matically biased to mid-supply without worrying about external circuitry to perform this task.

3.2 Black Level Adjustment

In order to maintain a constant reference level for black pixels, a feedback loop is implemented that sets the black level value at the output of the ADC to 64 in the 13 bit digital code. This loop is active during the optically black pixels which are output at the beginning and end of a frame as well as during a portion of the horizontal blanking period. The presence of black pixels in the CCD output is indicated by the CLAMP pulse, which is supplied externally through the CLAMP pin. The black level can also be written to through the serial port.

In order to acquire a starting value for the black level, the loop will run over the several lines of black pixels at the beginning of the frame. The block diagram of the loop is shown in Figure 10. The update rate is once per line during active pixel lines as long as the Clamp pulse is $\leq n+10$ cycles. Where n is the number of pixels accumulated before the black loop is updated and is programmable through register 0Dh bits 5:0. If the Clamp pulse is longer

than $n+10$ cycles the black loop is updated every $n+10$ cycles. For example, during optical back lines the loop is updated several times at a rate of once every $n+10$ cycles.

The open-loop transfer function of the black level adjustment loop is

$$H(z) = \frac{K \times n}{z-1} \quad K = \frac{1}{256} \text{blk_gain}$$

blk_gain = 1, 2, 4, or 8

where blk_gain is programmable through a register and n = # of black pixels during clamp time, which is also programmable. The value of $K \times n$ will determine the open-loop gain of the system. The settling time for the loop can be calculated using the following formula:

For offset range=1 (reg 06h, bit 0)

$$\tau = \left(-\frac{1}{\ln(1-nK)} \right) \left(\frac{1}{f_u} \right)$$

For offset range =0

$$\tau = \left(-\frac{1}{\ln\left(1-\frac{nK}{2}\right)} \right) \left(\frac{1}{f_u} \right)$$

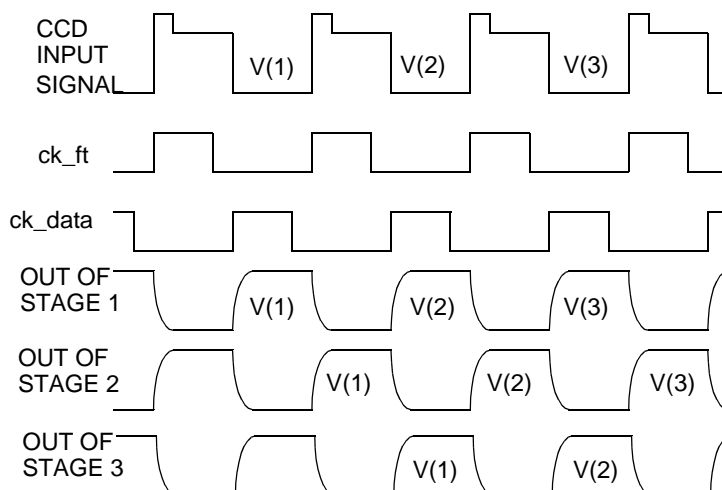


Figure 9. Idealized timing diagram of VGA/CDS circuit

During fixed gain mode the time constant is a little different.

For a fixed gain of 1:

$$\tau = \left(-\frac{1}{\ln\left(1 - \frac{nK}{8}\right)} \right) \left(\frac{1}{f_u} \right)$$

For a fixed gain of 2:

$$\tau = \left(-\frac{1}{\ln\left(1 - \frac{nK}{4}\right)} \right) \left(\frac{1}{f_u} \right)$$

For a fixed gain of 4:

$$\tau = \left(-\frac{1}{\ln\left(1 - \frac{nK}{2}\right)} \right) \left(\frac{1}{f_u} \right)$$

For a fixed gain of 8:

$$\tau = \left(-\frac{1}{\ln(1 - nK)} \right) \left(\frac{1}{f_u} \right)$$

In order to achieve no ringing in the settling use, $\frac{n}{K} \leq 1$ for offset range = 1, and $\frac{n}{2K} \leq 1$ for offset range = 0.

The 9 MSBs of the black level accumulator can be read or written through a register. If written, the LSBs are set to zero. The black level is set to “8” in a 10-bit digital output representation. In a 13-bit representation, it is set to “64.” The power-up default value in the accumulator is at mid level.

Also note that the black level adjust loop can be disabled. In addition, the black level can be programmed through the serial port.

3.3 Gain Adjust Block

In order to increase the dynamic range of the ADC, a variable gain, whose value is determined by the signal level, is applied to each pixel. This allows for 13 bits of dynamic range and 10 bits of resolution after accounting for the significance of the ADC output bits. The gain applied in the analog is illustrated in the transfer curve in Figure 7. Once the signal is digitized, the gain adjust block uses the gain information for a given pixel word and shifts its bits accordingly. For example, using a full scale level of 1.0 V, if $V_{in} = 0.3$ V, the VGA would choose a gain of 2X so the ADC input is 0.6 V. The 10-bit output of the ADC (with no black level) is $(0.6/1.0) \times 1024 = 614$, or “1001100110.” in binary. The gain adjust block will take this value plus the bits representing the 2x gain and divide the output by two (shift right by 1). The output of the gain adjust block is then “0100110011.000.” Note that the decimal point is virtual, having no existence in silicon. It is representing the fact that we keep 3 extra bits of lower significance in the output. In the same manner, if $V_{in} = 0.75$ V, a gain of 1X would be chosen and the output of the gain adjust block

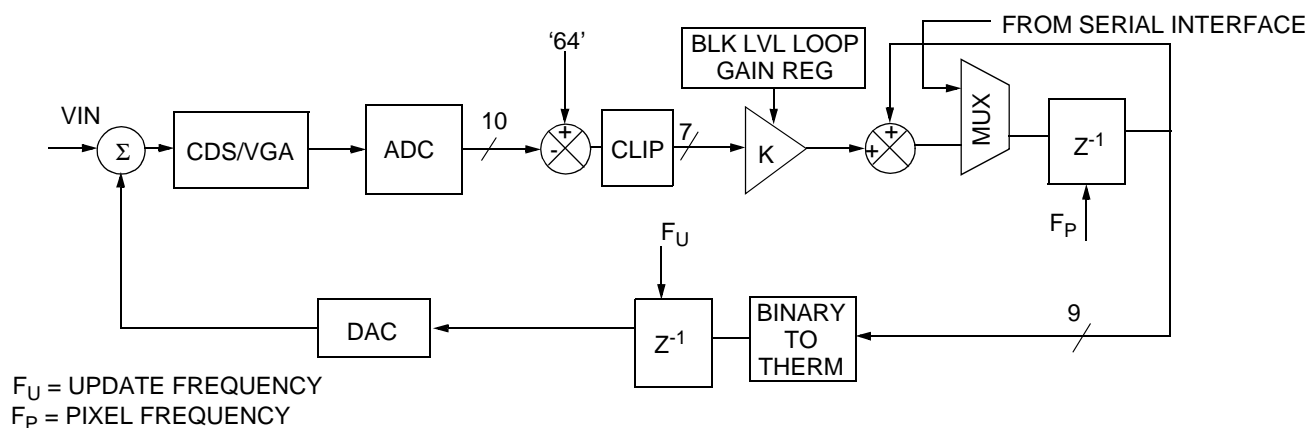


Figure 10. Black level adjustment loop

would be “1100000000000.” The transfer function of the Vin/gain adjust out is shown in Figure 11.

A block diagram of the gain adjust block is shown in Figure 12.

Since the analog gain changes do not match the digital shifts exactly, there is a potential to have non-monotonic digital output. In order to remove this problem, calibration is performed. During calibration, offset values are found that will be used to counteract the errors caused by the analog gain mismatch. Using these offset values, the final output is a monotonic continuous 13-bit value.

3.4 13-to-10 Bit Compander

While a 13 bit output may be useful in some applications, others may require the standard 10 bit output. To accommodate this and yet still retain the advantages of the increased dynamic range, a 13-to-10 (or 13-to-12) bit compander is included. By using the picture content as a guide, the user can select which curve will lead to the best overall dynamic range in the picture. The Companding module takes 13-bit data as input, and outputs either 10-bit companded data, 12-bit MSB-clipped data or it lets the original 13-bit data pass through.

By programming the compander in the way that is shown in Figure 13, it is possible to compensate for

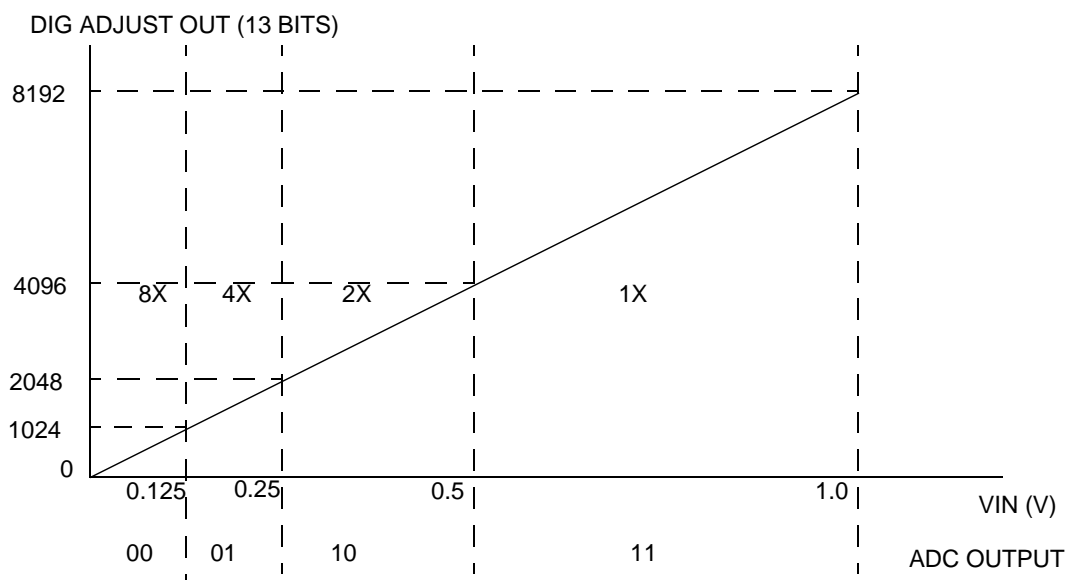


Figure 11. Transfer function of Vin to Gain Adjust output Block (assuming full scale level of 1.0 V)

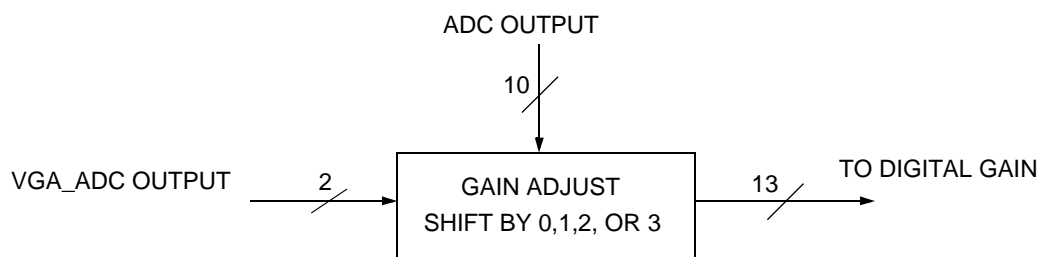


Figure 12. Gain Adjust output Block

backlighting conditions. Details in dark areas stay visible, even in very complex lighting conditions.

These three modes can be selected through 2 register bits in operational control.

Bits_out register bits	Output mode
0x	10 bits companded
10	13 bits
11	12 bits (clipped)

Table 1.

In the 12-bit clipped mode, any input above 4095 gets clipped to 4095. In the 10-bit companded mode, the input gets companded through a four segment, three knees, fully programmable curve.

To program the curve, the placement of the three knees in the companding curve must be determined. The next step is to determine the slope of the four segments created by the three knees (slope for each segment is defined as delta y / delta x). Finally, offsets must be calculated to keep the companding curve continuous.

A fourth knee exists in the curve, which represents the black level value. There are two options for the 10-bit black value. In case one, a linear mapping is employed such that “blacker-than-black” pixel information is kept, with black (code 64 in the 13 bit data) being defined as code 8 in the 10 bit domain. The second option clips all pixel values less than black (code 64 in the 13 bit data) to a programma-

ble offset value, offset1. This may be set to 0 if desired. This option will lose the “blacker-than-black” pixel information, but allow for slightly more dynamic range. Note: If using the linear mode (option 1), offset1 must be set to 8.

Registers x1 through x3 should be programmed with the x coordinates of each one of the three knees.

Registers slope1 through slope4 should be programmed with 256 multiplied by the calculated slopes.

Finally, the offsets can be programmed following the formulas below:

$$y1 = \text{slope1}/256 \times (x1-64) + \text{offset1}$$

$$y2 = \text{slope2}/256 \times (x2-x1) + y1$$

$$y3 = \text{slope3}/256 \times (x3-x2) + y2$$

$$\text{offset2} = y1 - (x1 \times \text{slope2} / 256)$$

$$\text{offset3} = y2 - (x2 \times \text{slope3} / 256)$$

$$\text{offset4} = y3 - (x3 \times \text{slope4} / 256)$$

(use integer division and discard the remainder)

When using the 10 bit companded output, be aware of the non-linearity of the output data. If linear output is needed to perform Auto White Balance (AWB) or Automatic Gain Control (AGC), a linear curve can be implemented to gather statistics. This can be achieved by writing 8191 to x1 (set register

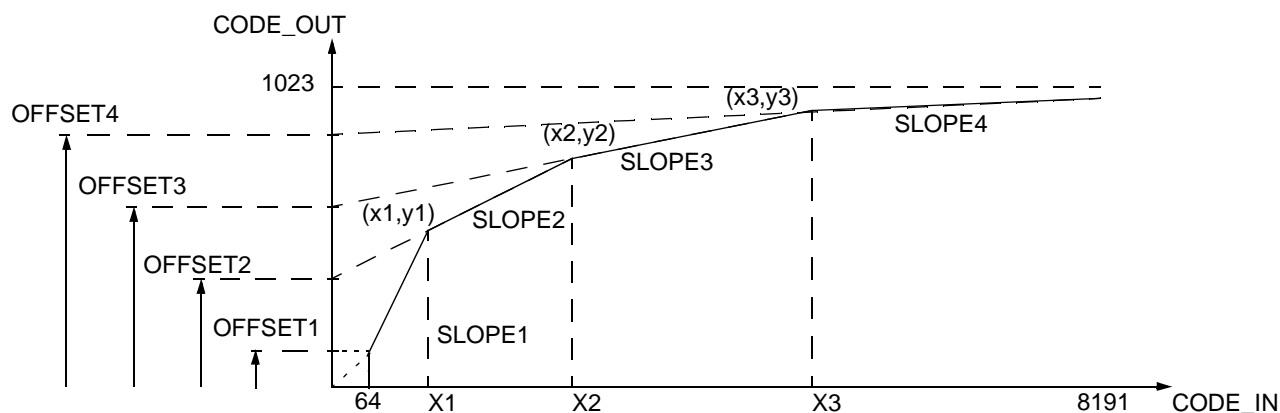


Figure 13. 13-to-10 bit compander

1Fh to 1fh and set register 20h to ffh) and setting slope1 to 32 (set register 15h to 00010xxxh and set register 16h to 20h). Once the statistics have been gathered, all four registers should be returned to their previous values before taking the actual picture.

The output of the compander is available at the pins DOUT<9:0> and it makes transitions either at the falling or rising edges of the pixel rate clock CLKO, controlled by a register bit. The Falling edge option is shown in Figure 14.

3.5 Stand By and Preview Mode

In order to enter power down mode a value of 07h must be written to register 01h. This will power down all the analog sections. Stopping the input clocks will power down the digital. To power up again, the input clocks must be turned on first then a value of 00h needs to be written to register 01h. The user must wait at least 500μs for the internal analog references to settle to their appropriate values before normal operation is resumed. It is

strongly recommend that the chip should be kept in Stand By mode when not in use in order to save power. When in preview mode, a user may wish to cut down the resolution of the ADC output to 6 bits in order to reduce the power consumption of the CS7622. In this mode, the current is reduced by 20 mA. With the DRX (Dynamic Range eXtension) circuitry, 3 bits of dynamic range are added to the 6-bit ADC output producing a 9-bit output. The pins DOUT[12:4] are used to output the digitized data in preview or Stand By mode.

3.6 Serial Interface

The serial interface is designed to allow high speed input to control the chip's registers. The specifications on this interface are as follows:

Asserting the enable pin, \overline{SEN} , enables the serial interface to perform data transfers. Data present on the SDATI pin is latched into the CS7622 on each rising edge of the serial clock, SCLK. Data output on SDATO from the CS7622 is clocked out on the rising edge of SCLK.

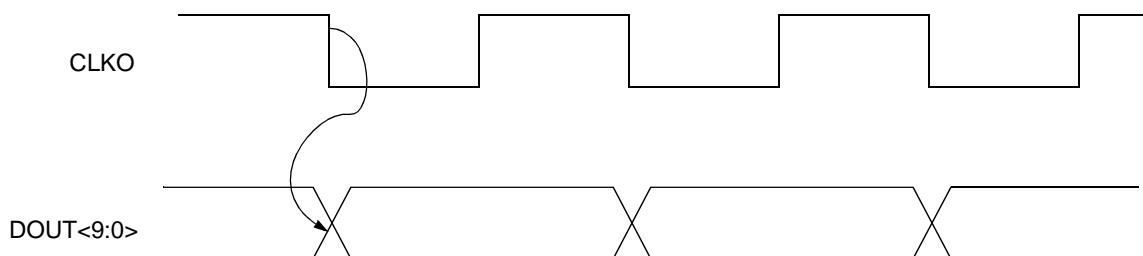


Figure 14. CS7622 output data and clocks

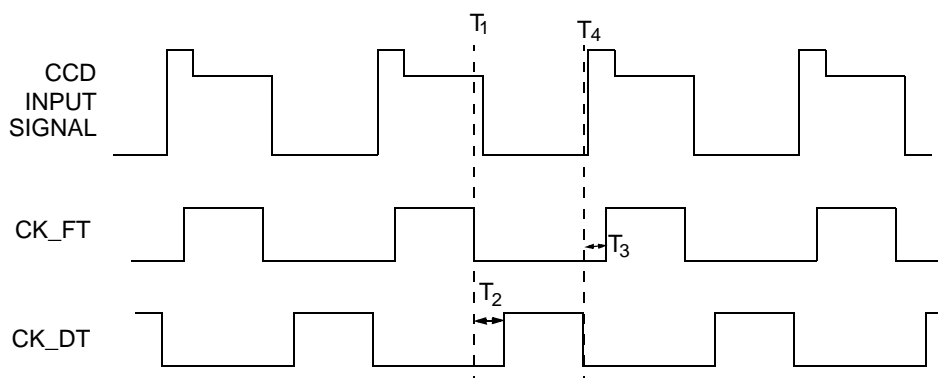


Figure 15. Input Timing

The CS7622 receives only the first 16 rising edges of the SCLK while $\overline{\text{SEN}}$ is low and then ignores any remaining SCLK and SDATI information. If $\overline{\text{SEN}}$ goes high before 16 SCLK pulses have been received, the CS7622 aborts the serial transfer.

The first bit is the $\text{R}/\overline{\text{W}}$ bit. $\text{R}/\overline{\text{W}} = 1$ identifies the transfer as a read. If (0), the transfer is a write. The next seven bits define the address. For write transfers, the second byte of the 16-bit packet contains the data byte. For read transfers, the CS7622 outputs the read data on SDATO after accepting the address. Address and data are transferred MSB first. When not reading out data, the SDATO pin is not driven by the chip (Hi-Z state).

The timing diagrams and specifications are shown in “Serial Interface Timing Specifications” on page 5 and Figures 1, 2, and 3 on page 5.

3.7 Input Timing for Sampling Clocks

The input clocks CK_FT and CK_DT are used to set up the sampling times and also to generate the internal digital clock. These clocks need to be running when processing pixels from the CCD, writing to the chip registers, or performing calibration (See

Register Description of Operation Control 2 reg 05h bit 0 for the details of performing a calibration). The timing of these clocks is important to ensure optimum settling times and sampling the correct value. CK_FT and CK_DT need to be non-overlapping pulses made as wide as possible to give long settling times. The falling edge of CK_FT should be close to the end of feedthrough while the falling edge of CK_DT should be close to the end of the data section of the CCD signal. See figure 15. Typical timing is given in table 2.

Timing Parameter	Typical Operating Values
T_1, T_4	2 ns
T_2, T_3	5 ns

Table 2.

Longer non-overlapping values for T1 and T4 will increase the recovery time, thus requiring a slower clock rate.

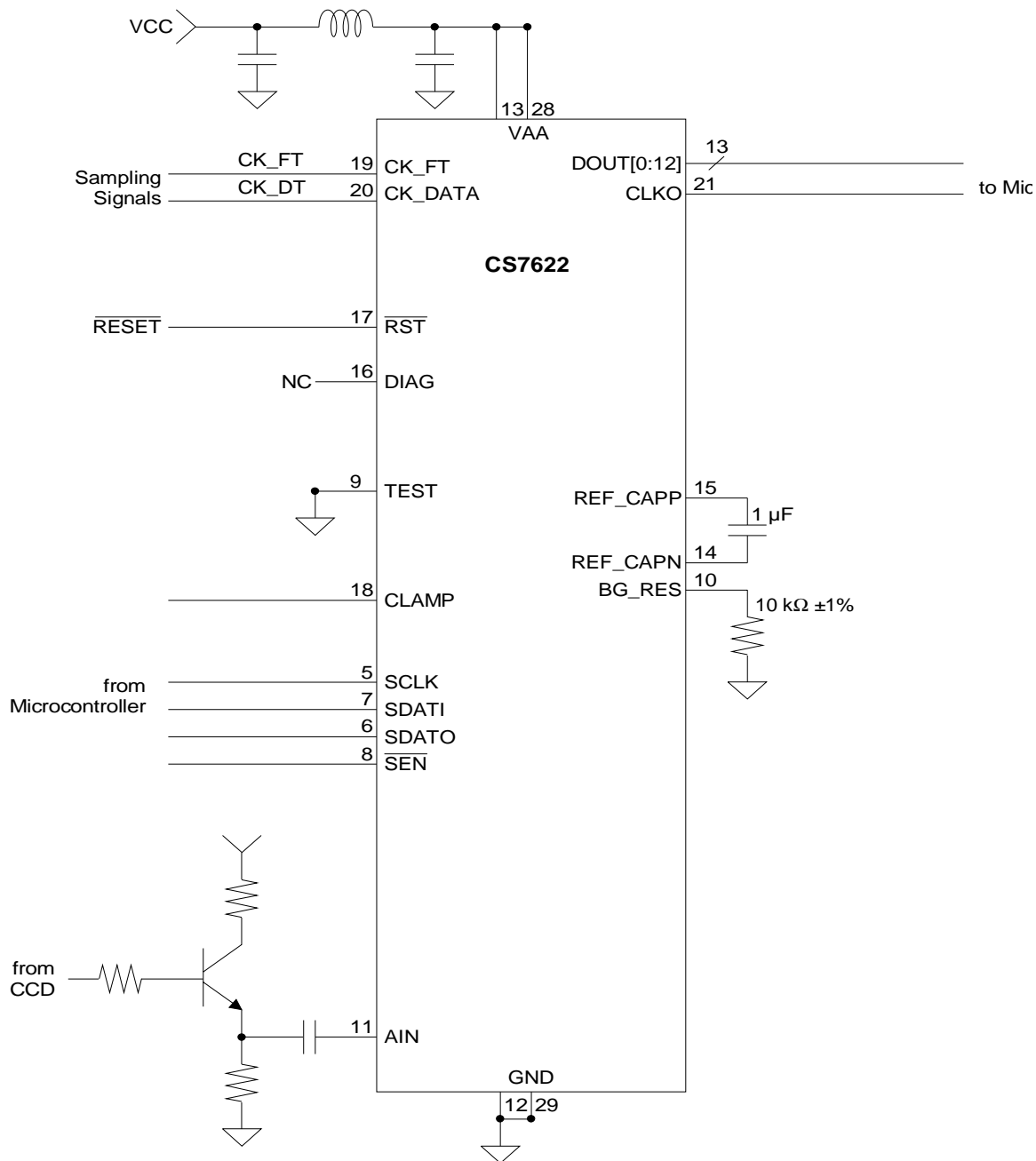


Figure 16. Typical Connection Diagram

4.0 REGISTER DESCRIPTIONS

Register (hex)	Register Function	Access	Default value (hex)
00h	Software Reset	W	00h
01h	Power Down Control 1	R/W	00h
02h - 03h	Reserved	R/W	00h
04h	Operation Control 1	R/W	0Ah
05h	Operation Control 2	R/W	04h
06h-0Ah	Reserved		
0Bh	Black Level Control - Accumulator (LSB)	R/W	00h
0Ch	Black Level Control - Accumulator (MSB)	R/W	01h
0Dh	Black Level Control - Loop Gain, Clamp Length	R/W	2Ah
0Eh	Gain Calibration - Offset 1	R/W	00h
0Fh	Gain Calibration - Offset 2	R/W	00h
10h	Gain Calibration - Offset 3	R/W	00h
11h - 13h	Reserved		
14h	Gain Calibration - Fixed Gains	R/W	00h
15h	Compander - Black slope, Slopes (MSBs)	R/W	10h
16h	Compander - Slope1 (LSBs)	R/W	B2h
17h	Compander - Slope2 (LSBs)	R/W	60h
18h	Compander - Slope3 (LSBs)	R/W	20h
19h	Compander - Slope4 (LSBs)	R/W	07h
1Ah	Compander - Offset1	R/W	08h
1Bh	Compander - Offsets (MSBs)	R/W	0Bh
1Ch	Compander - Offset2 (LSBs)	R/W	BFh
1Dh	Compander - Offset3 (LSBs)	R/W	05h
1Eh	Compander - Offset4 (LSBs)	R/W	20h
1Fh	Compander - X1 (MSBs)	R/W	03h
20h	Compander - X1 (LSBs)	R/W	20h
21h	Compander - X2 (MSBs)	R/W	05h
22h	Compander - X2 (LSBs)	R/W	18h
23h	Compander - X3 (MSBs)	R/W	0Bh
24h	Compander - X3 (LSBs)	R/W	58h
25h	Device ID	R	CCh
26h	Rev Code	R	00h

Table 3. Register Description

Reset

Default = 00h; Read/Write (address 00h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED							sft_rst
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:1	-	reserved
0	sft_rst	Software Reset: When this bit is written with a '1', all of the digital circuitry and the registers will reset to their default values. It automatically clears after 4 pixel clock periods. The clocks remain running during the reset period.

Power down Control 1

Default = 00h; Read/Write (address 01h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED					pd_vga	pd_adc	pd_ref
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:3	-	reserved
2	pd_vga	DRX Front End Power Down: When written with a '1', the DRX front end circuitry powers down.
1	pd_adc	ADC Power Down: When written with a '1', the Analog-to-Digital converter circuitry powers down.
0	pd_ref	Voltage Reference Power Down: When written with a '1', the Analog-to-Digital converter circuitry powers down.

Operation Control 1

Default = 0Ah; Read/Write (address 04h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED		dout_edge	low_res	bits_out1	bits_out0	blk_dis	off_range
Default	0	0	0	0	1	0	1	0

Bit	Mnemonic	Function
7:6	-	reserved
5	dout_edge	This register is used to set when dout changes values. Relative to CLKO 0 - dout output changes on the falling edge of CLKO 1 - dout output changes on the rising edge of CLKO
4	low_res	Preview Mode: This mode can be used to cut the current consumption of the chip by 20 mA. The output of the ADC will have 6 bits of resolution in this mode, and the output of the chip will have 9 bits after using the DRX circuitry. It is intended to be used when driving an LCD display or any other time when a lower resolution picture is acceptable.
3:2	bits_out1-0	Number of Data Bits Out: The range of the output data can be determined by these bits. The data internal to the chip has a 13-bit range. The output can be this full range, half this range (12 bits), or an eighth of this range (10 bits). If 12-bit data is selected, the top half of the 13-bit range is saturated to the maximum 12-bit code. If 10-bit data is selected, the compander curve which is user programmable is employed to map the 13-bit data to the 10-bit output. 0 - 10 bits output; 1 - 10 bits output 2 - 13 bits output; 3 - 12 bits output
1	blk_dis	Black Level Loop Disabled: If the user chooses to adjust the black level himself through register access, he may disable the internal black level loop. This loop usually updates the black level to what it calculates to be the correct level. If disabled, the offset used will be determined from the value written in the black level accumulator register. 0 - internal black level loop is enabled 1 - black level loop is disabled
0	off_range	Offset Range: The black level loop is used to cancel any offsets from the CCD and chip circuitry. If the offsets are small, the user has the option to decrease the offset cancellation range for the added advantage of increasing the resolution of the offset cancellation. 0 - smaller offset cancellation range used (~50 mV) 1 - larger offset cancellation range used (~100 mV)

Operation Control 2

Default = 04h; Read/Write (address 05h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED				fs_lvl2	fs_lvl1	fs_lvl0	gain_cal
Default	0	0	0	0	0	1	0	0

Bit	Mnemonic	Function
7:4	-	reserved
3:1	fs_lvl2-0	Full Scale Level: This is used to set the full scale input range of the CS7622. Since CCDs have various saturation levels, it is advantageous to set the full scale input range of the CS7622 to match the saturation level of the CCD used. The table below shows the full scale level choices. (See Table 4)
0	gain_cal	Gain Calibration: A calibration of the gain stages is required to insure a monotonic digital output. If the user wishes to initiate a calibration, he may do so by setting this bit to '1', which will invoke a gain calibration sequence immediately. This bit automatically clears itself after a calibration has been initiated. During the calibration sequence the output will not contain valid data. The input clocks must be running throughout the whole calibration sequence which lasts for ~760 clocks.

fs_lvl	Full Scale Voltage
000	0.3 V
001	0.4 V
010	0.5 V
011	0.6 V
100	0.7 V
101	0.8 V
110	0.9 V
111	1.0 V

Table 4.

Black Level Control (8 LSBs)

Default = 00h; Read/Write (address 0Bh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	accumulator 7	accumulator 6	accumulator 5	accumulator 4	accumulator 3	accumulator 2	accumulator 1	accumulator 0
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:0	accumulator7-0	Black Level Accumulator: See the description of register 0Ch.

Black Level Control (MSB)

Default = 01h; Read/Write (address 0Ch)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED							accumulator8
Default	0	0	0	0	0	0	0	1

Bit	Mnemonic	Function
7:1	-	Reserved
0	accumulator8	Black Level Accumulator: is a 9 bit number representing an amount of offset added to the input of the CDS circuit. The black level loop alters the black level accumulator value to make the output of the ADC settle to code 64 during black pixels. If desired the black loop may be disabled and written to manually to add any desired amount of offset. There is a total of ~100 mV of offset range if the offset range register setting is set to "1" or ~50 mV when this register setting is set to "0". This offset range is used to correct for CCD offsets plus internal offsets generated in the analog path of this chip. The offset range before subtracting the internal offsets is as shown in the table below with the worst case internal offsets being ± 17 mV. (See Table 5)

Offset Range (Reg 06h bit 0)	Max Offset Blk Acc=511	Min Offset Blk Acc=0	Accumulator LSB Size
1	~30 mV	~-72 mV	~0.2 mV
0	~11 mV	~-40 mV	~0.1 mV

Table 5.

Black Level Control - General

The black loop is a feedback system that causes the ADC output to settle to 64 during the register defined black pixels. This has the purpose of removing any CCD and system offsets and defining 64 as the known black level. The loop has an exponential settling response and the time constant of this loop is effected by the black loop gain and the number of black pixels to accumulate before updating the black accumulator. See Figure 10 for a block diagram of the black level loop.

Black Level Control - Loop Gain, Clamp Length

Default = 2Ah; Read/Write (address 0Dh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	blk_gain1	blk_gain0	blk_clp_15	blk_clp_14	blk_clp_13	blk_clp_12	blk_clp_11	blk_clp_10
Default	0	0	1	0	1	0	1	0

Bit	Mnemonic	Function
7:6	blk_gain1-0	Black Loop Gain Factor: can be set to 1x,2x,4x,or 8x and is simply a multiplying constant to effect the weight of each black pixel before it is accumulated. 00 - defines a gain of 1x 01 - defines a gain of 2x 10 - defines a gain of 4x 11 - defines a gain of 8x
5:0	blk_clp_15-10	Black Loop Clamp Length: The black clamp length effects the loop time constant and also acts to average out noise in the black level. The larger this value the more pixels that are summed before the loop is updated which causes greater averaging and a smaller settling time constant. The table below shows the black loop time constant for various settings of Offset Range (register 04h, bit 0) and Fixed Gain Settings (register 14h, bits 5-3). (See Table 5)

Fixed Gain (Register 16h)	Offset Range = 1	Offset Range = 0
not fixed	$-1/(\ln(1-nK))(1/f_u)$	$-1/(\ln(1-nK/2))(1/f_u)$
x1	$-1/(\ln(1-nK/8))(1/f_u)$	$-1/(\ln(1-nK/16))(1/f_u)$
x2	$-1/(\ln(1-nK/4))(1/f_u)$	$-1/(\ln(1-nK/8))(1/f_u)$
x4	$-1/(\ln(1-nK/2))(1/f_u)$	$-1/(\ln(1-nK/4))(1/f_u)$
x8	$-1/(\ln(1-nK))(1/f_u)$	$-1/(\ln(1-nK/2))(1/f_u)$

Table 6.

Where:

$K = 1/256 \cdot \text{blk_gain}$

$n = \text{Black loop clamp length} = \text{blk_clp_l}[5:0]$

$f_u = \text{update rate}$

Gain Calibration Offset 1

Default = 00h; Read only (address 0Eh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	gain_offset 17	gain_offset 16	gain_offset 15	gain_offset 14	gain_offset 13	gain_offset 12	gain_offset 11	gain_offset 10
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:0	gain_offset17-10	offset added to 4x gain segment, values are in 2's complement. See details in register 10h.

Gain Calibration Offset 2

Default = 00h; Read only (address 0Fh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	gain_offset 27	gain_offset 26	gain_offset 25	gain_offset 24	gain_offset 23	gain_offset 22	gain_offset 21	gain_offset 20
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:0	gain_offset27-20	offset added to 2x gain segment, values are in 2's complement. See details in register 10h.

Gain Calibration Offset 3

Default = 00h; Read only (address 10h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	gain_offset 37	gain_offset 36	gain_offset 35	gain_offset 34	gain_offset 33	gain_offset 32	gain_offset 31	gain_offset 30
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:0	gain_offset37-30	<p>Offset added to 1x gain segment. Values are in 2's complement. These registers are used to report some of the calibration settings. After calibration is performed the gain offset registers are automatically updated with values needed for the DRX circuitry to operate correctly. These registers should not be written to since this will remove the proper settings found during calibration. The gain offset values are used to add an offset to the output of the ADC when using different analog gain settings (See equations below). The purpose of this is to produce a continuous transition between the different gain settings so that the final 13 bit output is monotonic and has no undesired artifacts. (See Figure 17)</p> $\text{dout}[12:0] = \begin{cases} \text{ADC_out} & \text{if in the 8x gain segment} \\ \text{ADC_out} * 2 + \text{Offset1} & \text{if in the 4x gain segment} \\ \text{ADC_out} * 4 + \text{Offset2} * 2 & \text{if in the 2x gain segment} \\ \text{ADC_out} * 8 + \text{Offset3} * 4 & \text{if in the 1x gain segment} \end{cases}$

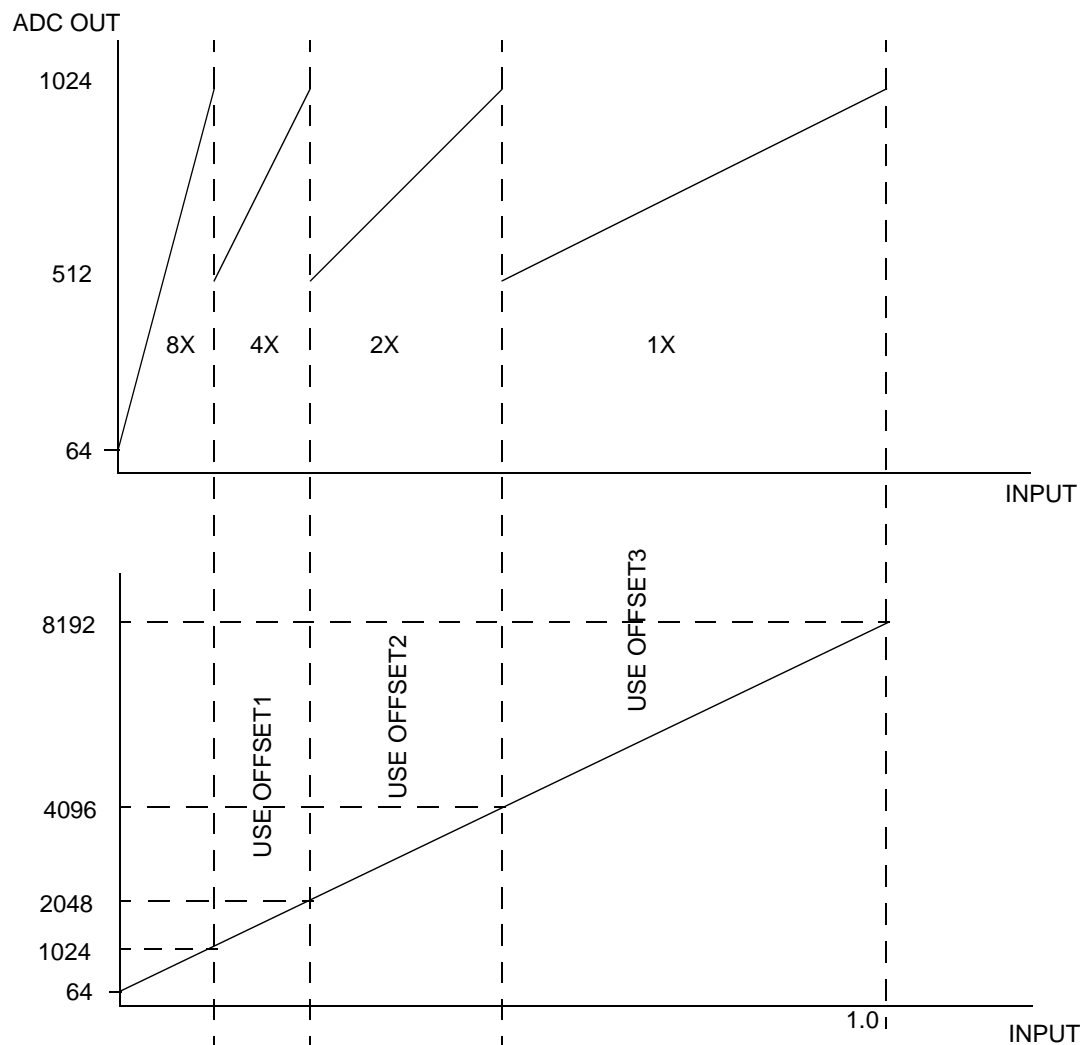


Figure 17. Transfer Function of Analog Input to Digital Output (assuming full scale level of 1.0 V)

Fixed Gain

Default = 00h; Read/Write (address 14h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED		fixed_gain2	fixed_gain1	fixed_gain0	RESERVED		
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:6, 2:0	-	Reserved
5:3	fixed_gain2-0	Fixed Gain: This is used to turn off the DRX functionality and apply a fixed gain to the input before reaching the ADC. A setting of 000 is used for normal operation this will yield the largest dynamic range by switching the front end gain relative to the amplitude of the input signal. The settings 001, 010, 011, and 100 are for fixed gains of 1x, 2x, 4x, and 8x respectively. Figure 18 shows the transfer function of the output of the ADC for a given input with the various fixed gain settings.

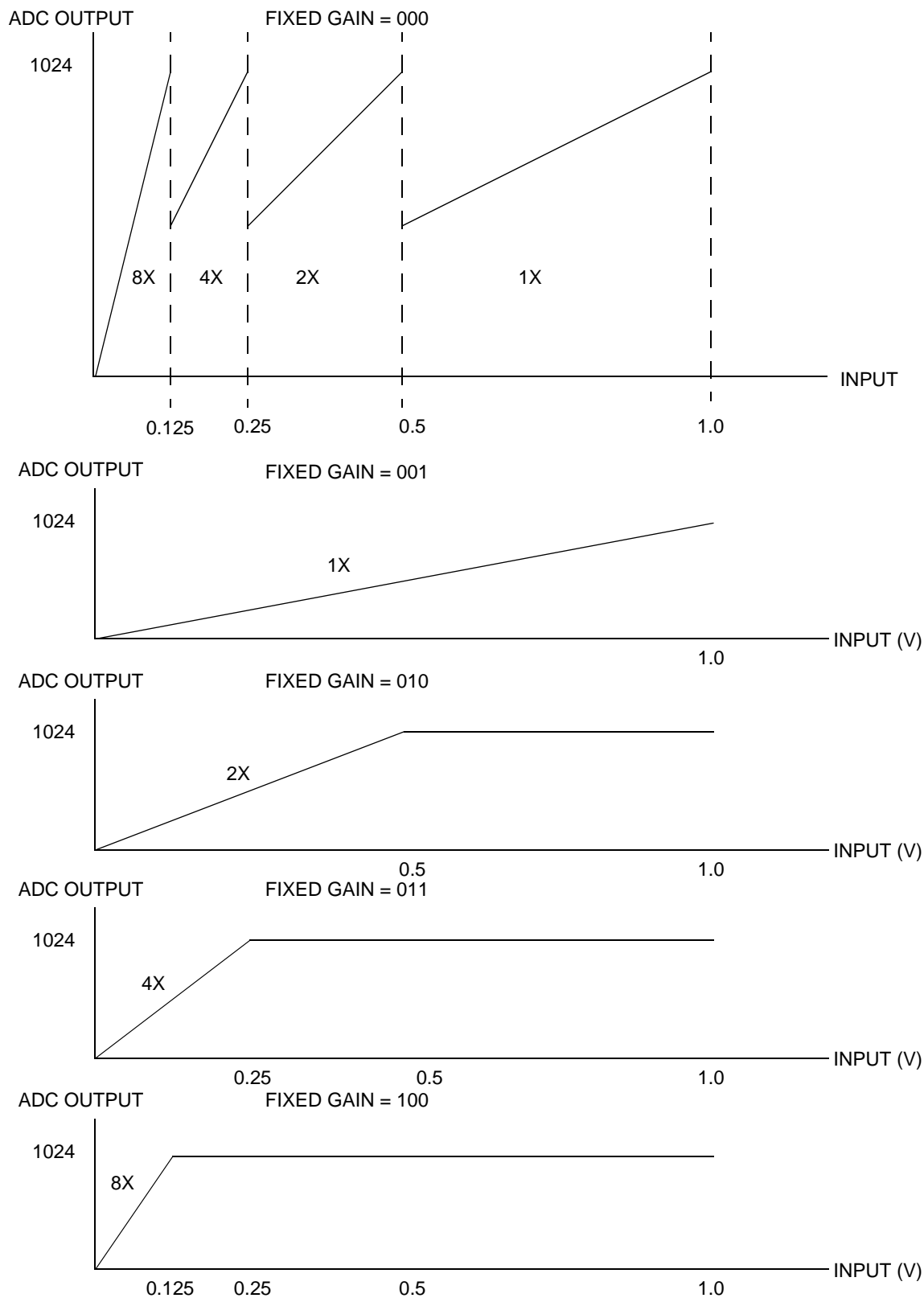


Figure 18. Transfer Function of ADC with Fixed Gain Settings (assuming full scale level of 1.0 V)

Compander - Black slope, Slopes (MSBs)

Default = 10h; Read/Write (address 15h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED			comp_linear	slope18	slope28	slope38	slope48
Default	0	0	0	1	0	0	0	0

Bit	Mnemonic	Function
7:5	-	Reserved
4	comp_linear	Compander Black Level Slope: 0 - The values of “0” to “64” in a 13 bit representation are set to “offset1” in a 10 bit representation. Offset1 can be set in register 33h. 1 - In this case the black level is mapped linearly from 13 bit values to 10 bit values. “64” is mapped into “8”. All the other values between “0” and “64” are divided by 8 in order to get the 10 bit representation. (See Figure 13)
3	slope18	Compander Slope 1: MSB of slope of first segment of companding curve. (See Figure 13)
2	slope28	Compander Slope 2: MSB of slope of second segment of companding curve. (See Figure 13)
1	slope38	Compander Slope 3: MSB of slope of third segment of companding curve. (See Figure 13)
0	slope48	Compander Slope 4: MSB of slope of fourth segment of companding curve. (See Figure 13)

Compander Slope 1 (LSBs)

Default = B2h; Read/Write (address 16h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	slope17	slope16	slope15	slope14	slope13	slope12	slope11	slope10
Default	1	0	1	1	0	0	1	0

Bit	Mnemonic	Function
7:0	slope17-10	Compander - Slope1: Slope of first segment (slope1[8:0]) of companding curve. Max value is 1.996. The LSB step size is 0.0039. (See Figure 13)

Compander Slope 2 (LSBs)

Default = 60h; Read/Write (address 17h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	slope27	slope26	slope25	slope24	slope23	slope22	slope21	slope20
Default	0	1	1	0	0	0	0	0

Bit	Mnemonic	Function
7:0	slope27-20	Compander - Slope2: Slope of second segment (slope2[8:0]) of companding curve. Max value is 1.996. The LSB step size is 0.0039. (See Figure 13)

Comander Slope 3 (LSBs)

Default = 20h; Read/Write (address 18h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	slope37	slope36	slope35	slope34	slope33	slope32	slope31	slope30
Default	0	0	2	0	0	0	0	0

Bit	Mnemonic	Function
7:0	slope37-30	Comander - Slope3: Slope of third segment (slope3[8:0]) of companding curve. Max value is 1.996. The LSB step size is 0.0039. (See Figure 13)

Comander Slope 4 (LSBs)

Default = 07h; Read/Write (address 19h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	slope47	slope46	slope45	slope44	slope43	slope42	slope41	slope40
Default	0	0	0	0	0	1	1	1

Bit	Mnemonic	Function
7:0	slope47-40	Comander - Slope4: Slope of fourth segment (slope4[8:0]) of companding curve. Max value is 1.996. The LSB step size is 0.0039. (See Figure 13)

Comander Offset 1

Default = 08h; Read/Write (address 1Ah)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	offset17	offset16	offset15	offset14	offset13	offset12	offset11	offset10
Default	0	0	0	0	1	0	0	0

Bit	Mnemonic	Function
7:0	offset17-10	Comander - Offset1: Black level value of companding curve if not in linear mapping mode (comp_linear = 0). (See Figure 13)

Comander Offset 2 (MSBs)

Default = 0Bh; Read/Write (address 1Bh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED		offset29	offset28	offset39	offset38	offset49	offset48
Default	0	0	0	0	1	0	1	1

Bit	Mnemonic	Function
7:6	-	Reserved
5:4	offset29-28	MSBs of offset of second segment of companding curve. (See Figure 13)
3:2	offset39-38	MSBs of offset of third segment of companding curve. (See Figure 13)
1:0	offset49-48	MSBs of offset of fourth segment of companding curve. (See Figure 13)

Comander Offset 2 (LSBs)

Default = BFh; Read/Write (address 1Ch)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	offset27	offset26	offset25	offset24	offset23	offset22	offset21	offset20
Default	1	0	1	1	1	1	1	1

Bit	Mnemonic	Function
7:0	offset27-20	Offset of second segment (offset2[9:0]) of companding curve. (See Figure 13)

Comander Offset 3 (LSBs)

Default = 05h; Read/Write (address 1Dh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	offset37	offset36	offset35	offset34	offset33	offset32	offset31	offset30
Default	0	0	0	0	0	1	0	1

Bit	Mnemonic	Function
7:0	offset37-30	Offset of third segment (offset3[9:0]) of companding curve. (See Figure 13)

Comander Offset 4 (LSBs)

Default = 20h; Read/Write (address 1Eh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	offset47	offset46	offset45	offset44	offset43	offset42	offset41	offset40
Default	0	0	1	0	0	0	0	0

Bit	Mnemonic	Function
7:0	offset47-40	Offset of fourth segment (offset4[9:0]) of companding curve. (See Figure 13)

Compander X1 (MSBs)

Default = 03h; Read/Write (address 1Fh)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED			x112	x111	x110	x19	x18
Default	0	0	0	0	0	0	1	1

Bit	Mnemonic	Function
7:5	-	Reserved
4:0	x112-x18	End value of first segment of companding curve (MSBs). (See Figure 13)

Compander X1 (LSBs)

Default = 20h; Read/Write (address 20h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	x17	x16	x15	x14	x13	x12	x11	x10
Default	0	0	1	0	0	0	0	0

Bit	Mnemonic	Function
7:0	x17x10	End value of first segment (x1[12:0]) of companding curve (LSBs). (See Figure 13)

Compander X2 (MSBs)

Default = 05h; Read/Write (address 21h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED			x212	x211	x210	x29	x28
Default	0	0	0	0	0	1	0	1

Bit	Mnemonic	Function
7:5	-	Reserved
4:0	x212-x28	End value of second segment of companding curve (MSBs). (See Figure 13)

Compander X2 (LSBs)

Default = 18h; Read/Write (address 22h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	x27	x26	x25	x24	x23	x22	x21	x20
Default	0	0	0	1	1	0	0	0

Bit	Mnemonic	Function
7:0	x27-x20	End value of second segment (x2[12:0]) of companding curve (LSBs). (See Figure 13)

Compander X3 (MSBs)

Default = 0Bh; Read/Write (address 23h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RESERVED			x312	x311	x310	x39	x38
Default	0	0	0	0	1	0	1	1

Bit	Mnemonic	Function
7:5	-	Reserved
4:0	x312-x38	End value of third segment of companding curve (MSBs). (See Figure 13)

Compander X3 (LSBs)

Default = 58h; Read/Write (address 24h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	x37	x36	x35	x34	x33	x32	x31	x30
Default	0	1	0	1	1	0	0	0

Bit	Mnemonic	Function
7:0	x37-x30	End value of third segment (x3[12:0]) of companding curve (LSBs). (See Figure 13)

Device ID

Default = CCh; Read only (address 25h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	device_ID7	device_ID6	device_ID5	device_ID4	device_ID3	device_ID2	device_ID1	device_ID0
Default	1	0	0	0	1	1	0	0

Bit	Mnemonic	Function
7:0	device_ID7-0	This read-only register is the unique ID for the CS7622.

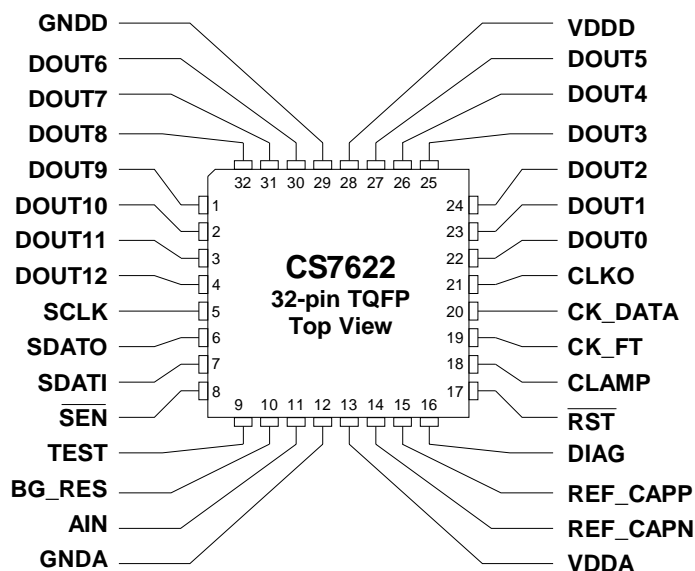
Revision Code

Default = 00h; Read only (address 26h)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	rev_code7	rev_code6	rev_code5	rev_code4	rev_code3	rev_code2	rev_code1	rev_code0
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Function
7:0	rev_code7-0	This read-only register is the revision code for the CS7622.

5.0 PIN DESCRIPTIONS



Supply

VDDA - Supply for analog

Pin 13 3.3 V analog supply.

VDDD - Supply for digital

Pin 28 3.3 V or 2.7 V digital supply.

Ground

GNDA - Ground for analog

Pin 12 GNDA is supplied by VDDA.

GNDD - Ground for digital

Pin 27 Supplied by VDDD.

CMOS Input

CLAMP - Black level clamp signal

Pin 18 Provided by the external timing generator. Supplied by VDDD.

CK_FT - Clock in feed-through

Pin 19 Sampling clock for feed-through level.

CK_DATA - Clock in data

Pin 20 Sampling clock for data level. Supplied by VDDD

REF_CAPN - Reference capacitor- negative terminal

Pin 14 Supplied by VDDA. A 1 μ F ceramic capacitor should be connected between REF_CAPN and REF_CAPP.

REF_CAPP - Reference capacitor- positive terminal

Pin 15 Supplied by VDDA. A 1 μ F ceramic capacitor should be connected between REF_CAPN and REF_CAPP.

RST - Reset pin, negative true

Pin 17 May be connected to external power-on-reset-circuit. Supplied by VDDD.

SCLK - Serial bus clock signal

Pin 5 Supplied by VDDD.

SDATI - Serial bus data input signal

Pin 7 Supplied by VDDD.

SEN - Serial bus enable signal-chip select (active low)

Pin 8 Supplied by VDDD.

TEST - Test enable pin

Pin 9 Supplied by VDDD.

CMOS Analog Input**AIN - Video data input from CCD**

Pin 11 Supplied by VDDA.

BG_RES - Band-gap resistor

Pin 10 Supplied by VDDA. A 10 k Ω resistor should be connected between BG_RES and GNDA.

CMOS 4 mA Output**CLKO - Clock = output**

Pin 21 Signal on this pin can either be the pixel clock output or data_valid signal output. Supplied by VDDD.

DOUT[0:12] - Digitized CCD data output

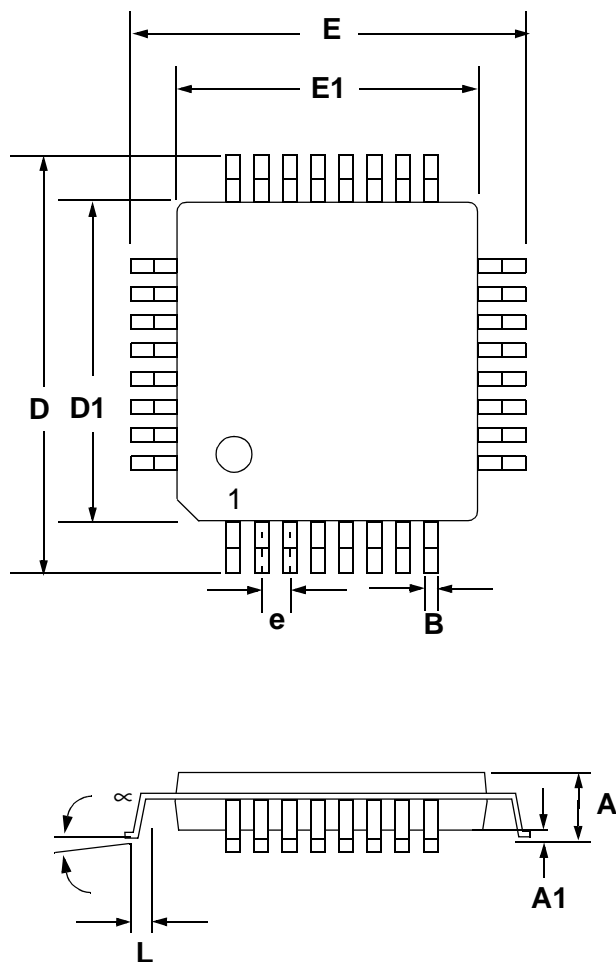
Pins 22-32, and 1-4 DOUT0 is LSB. Supplied by VDDD.

SDATO - Serial bus data output signal

Pin 6 Supplied by VDDD.

6.0 PACKAGE DIMENSIONS

32L TQFP PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.063	---	1.60
A1	0.002	0.006	0.05	0.15
B	0.012	0.018	0.30	0.45
D	0.343	0.366	8.70	9.30
D1	0.272	0.280	6.90	7.10
E	0.343	0.366	8.70	9.30
E1	0.272	0.280	6.90	7.10
e*	0.028	0.035	0.70	0.90
L	0.018	0.030	0.45	0.75
∞	0.000°	7.000°	0.00°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.

JEDEC Designation: MS026

CRYSTAL

• Notes •

SMARTTM
Analog