October 2000
Revision 2.1

National Semiconductor®

Geode™ CS9211 Graphics Companion Flat Panel Display Controller

General Description

The National Semiconductor® Geode™ CS9211 graphics companion is suitable for systems that use any GX-series processor (e.g., GX1, GXLV, GXm) along with the CS5530A I/O companion, also members of the Geode family of products.

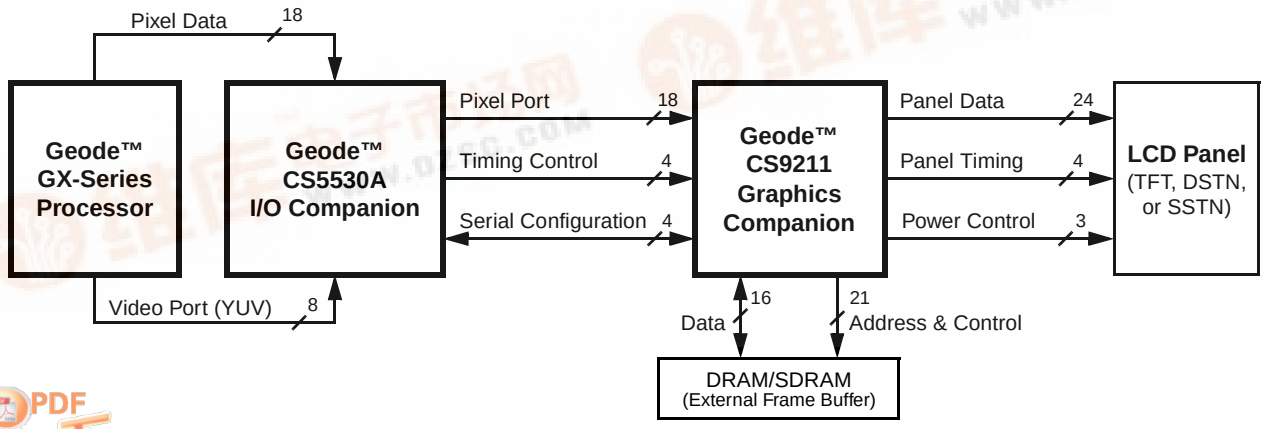
The CS9211 converts the digital pixel stream output of the CS5530A to the digital RGB inputs used by standard single and dual-scan STN LCD display panels. Support is provided for both color and monochrome dual-scan STN (DSTN) flat panels up to 1024x768 resolution, and for color single-scan panels up to 640x480 resolution.

The typical system connection shows how to connect the CS9211 with other system components. Note that the external frame buffer is only required for DSTN panels.

Features

- Supports most SVGA DSTN panels and the VESA FPDI (Flat Panel Display Interface) Revision 1.0 Specification.
- Directly interfaces to panels; no external drivers needed (excluding backlight inverter).
- Supports 18-bit color pixel input data stream in 6:6:6 format, for a maximum display of 262,144 colors.
- Supports up to 65 MHz pixel clock (DOTCLK).
- Supports resolutions up to 1024x768 pixels.
- Fast display refresh rate, up to 120 Hz for DSTN panels, achieved by writing both panel halves simultaneously.
- 16- or 24-bit dual-scan color STN (DSTN) support.
- 8- or 16-bit dual-scan monochrome STN (DSTN) support.
- 8-bit single-scan color STN (SSTN) panel support.
- TFT panel support provided via pass-through mode.
- 9-, 12- or 18-bit TFT support.
- 9+9 or 12+12-bit, 2 pixels per clock TFT panel support.
- Frame rate modulation (FRM) allows up to 32 shades of gray (intensities) for each primary color (R,G,B) with no loss of spatial resolution.
- Proprietary dithering algorithm allows display of additional colors for a maximum of 262,144 colors.
- Programmable control of input and output sync pulse widths, delays, and polarities allows interfaces to many panel types.
- Programmable panel power sequence controls.
- Built-in memory controller supports either SDRAM or EDO memory for the DSTN frame buffer.
- Configuration via a serial programming interface.
- Low-power, 3.3V operation.
- 144-pin LQFP (Low-profile Quad Flat Pack).

Typical System Connection



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1.0 Architecture Overview

The major functional blocks, as shown in Figure 1-1, of the CS9211 graphics companion flat panel display controller:

- Serial Interface
- Dither Engine
- Frame Rate Modulator (FRM)
- Control Registers
- DSTN Timing Generator
- Panel Interface
- Frame Accelerator
- CRC (Cyclical Redundancy Check) Engine
- SDRAM/DRAM Interface Controller

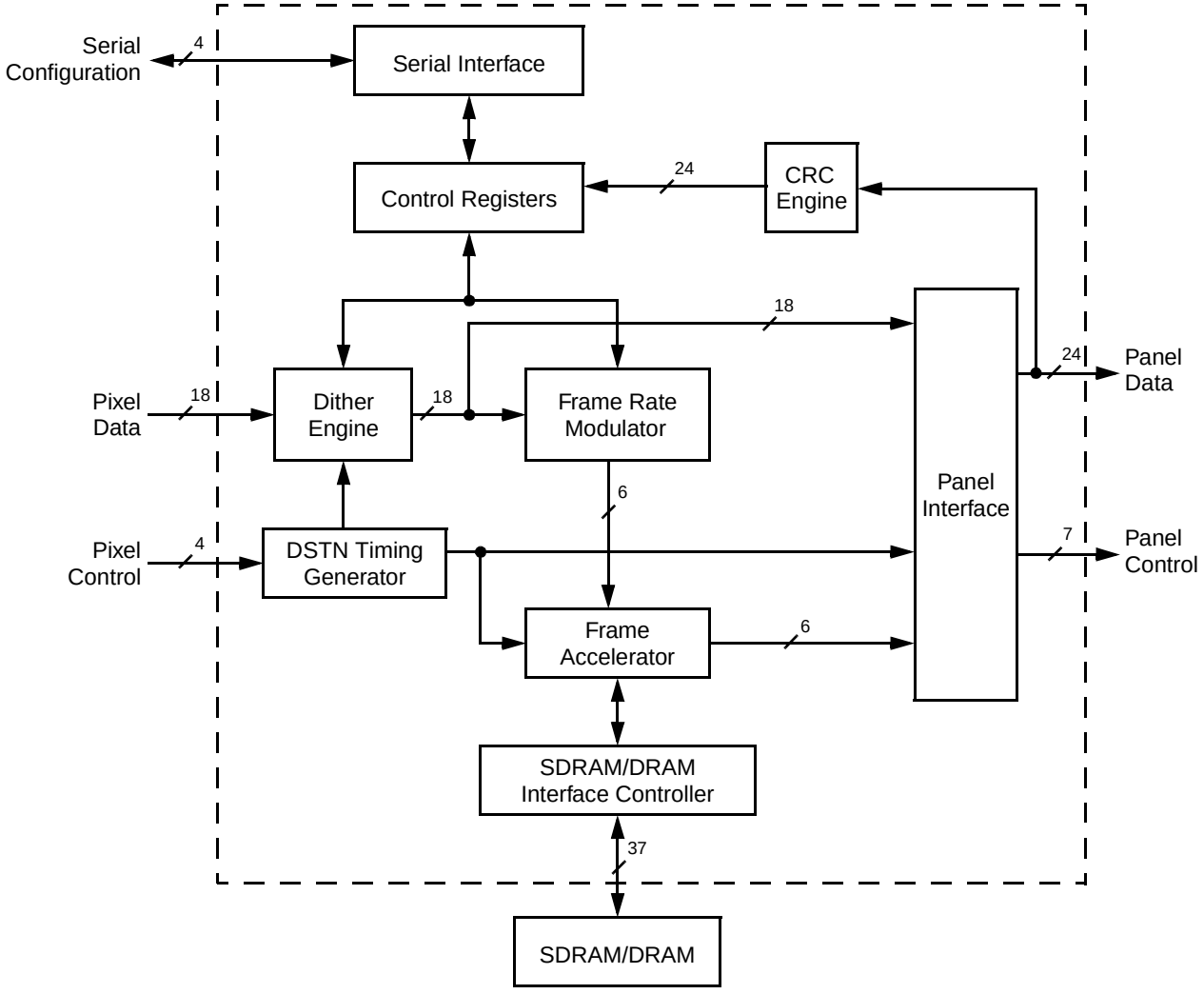


Figure 1-1. Internal Block Diagram

2.0 Signal Definitions

This section defines the signals and external interface of the CS9211. Figure 2-1 shows the pins organized by their functional groupings (internal test and electrical pins are not shown).

2.1 PIN ASSIGNMENTS

The tables in this section use several common abbreviations. Table 2-1 lists the mnemonics and their meanings.

Figure 2-2 shows the pin assignment for the CS9211 with Tables 2-2 and 2-3 listing the pin assignments sorted by pin number and alphabetically by signal name, respectively.

In Section 2.2 "Signal Descriptions" on page 9 a description of each signal within its associated functional group is provided.

Table 2-1. Pin Type Definitions

Mnemonic	Definition
I	Standard input pin
I/O	Bidirectional pin
O	Totem-pole output
OD	Open-drain output structure that allows multiple devices to share the pin in a wired-OR configuration
PU	Pull-up resistor
PD	Pull-down resistor
smt	Schmitt Trigger
t/s	TRI-STATE signal
VDD (PWR)	Power pin
VSS (GND)	Ground pin
#	The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the a high voltage level.

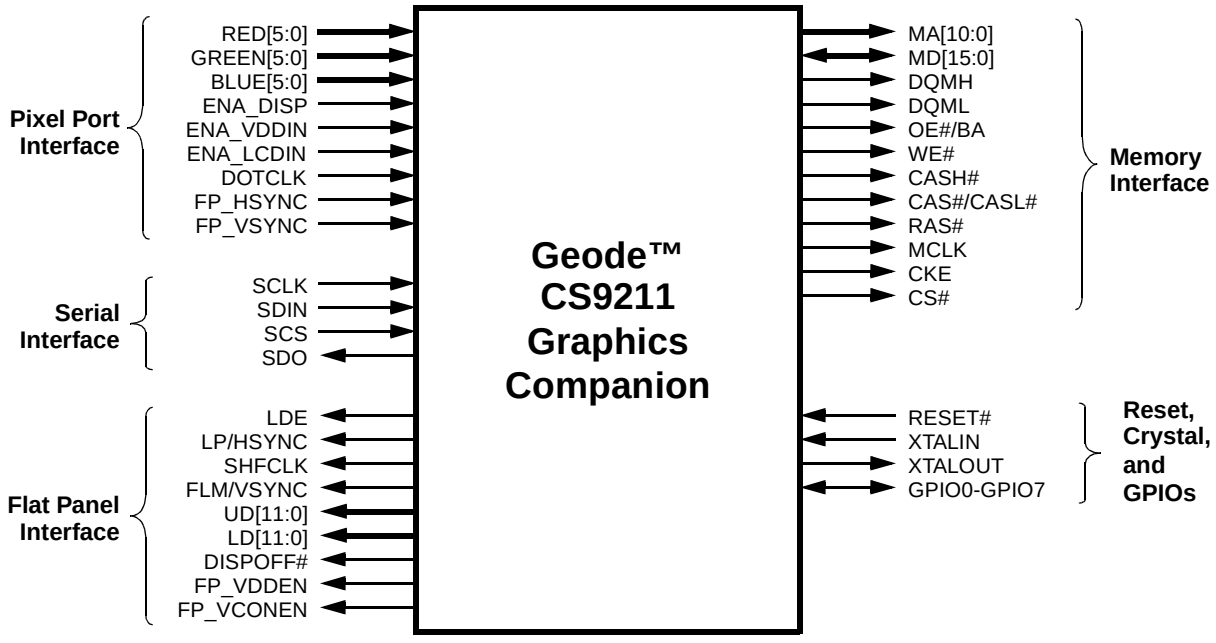


Figure 2-1. Signal Groups

Signal Definitions (Continued)

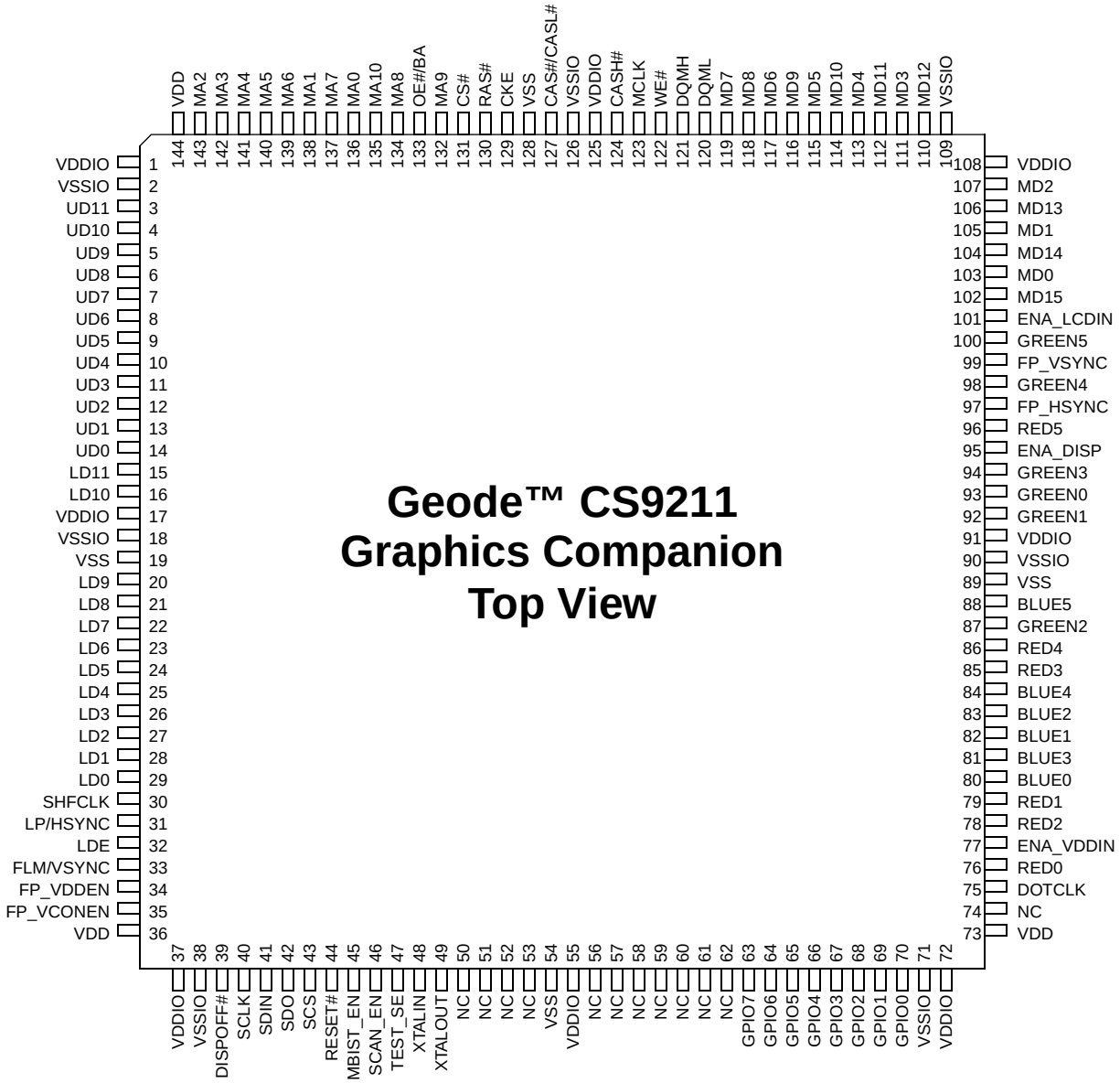


Figure 2-2. 144-Pin LQFP Pin Assignment Diagram Order Number: CS9211-VNG

Signal Definitions (Continued)

Table 2-2. Pin Assignments - Sorted by Pin Number

Pin No.	Signal Name	Type	Drive (mA)
1	VDDIO	PWR	--
2	VSSIO	GND	--
3	UD11	O	8
4	UD10	O	8
5	UD9	O	8
6	UD8	O	8
7	UD7	O	8
8	UD6	O	8
9	UD5	O	8
10	UD4	O	8
11	UD3	O	8
12	UD2	O	8
13	UD1	O	8
14	UD0	O	8
15	LD11	O	8
16	LD10	O	8
17	VDDIO	PWR	--
18	VSSIO	GND	--
19	VSS	GND	--
20	LD9	O	8
21	LD8	O	8
22	LD7	O	8
23	LD6	O	8
24	LD5	O	8
25	LD4	O	8
26	LD3	O	8
27	LD2	O	8
28	LD1	O	8
29	LD0	O	8
30	SHFCLK	O	12
31	LP/HSYNC	O	8
32	LDE	O	8
33	FLM/VSYNC	O	8
34	FP_VDDEN	O	8
35	FP_VCONEN	O	8
36	VDD	PWR	--
37	VDDIO	PWR	--
38	VSSIO	GND	--
39	DISPOFF#	O	8
40	SCLK	I	--
41	SDIN	I	--
42	SDO	O	8
43	SCS	I	--
44	RESET#	I	--
45	MBIST_EN	I	--
46	SCAN_EN	I	--
47	TEST_SE	I	--
48	XTALIN	I	--
49	XTALOUT	O	--
50	NC	--	--
51	NC	--	--
52	NC	--	--
53	NC	--	--
54	VSS	GND	--
55	VDDIO	PWR	--
56	NC	--	--
57	NC	--	--
58	NC	--	--
59	NC	--	--
60	NC	--	--
61	NC	--	--
62	NC	--	--
63	GPIO7	I/O	4
64	GPIO6	I/O	4
65	GPIO5	I/O	4
66	GPIO4	I/O	4
67	GPIO3	I/O	4
68	GPIO2	I/O	4
69	GPIO1	I/O	4
70	GPIO0	I/O	4
71	VSSIO	GND	--
72	VDDIO	PWR	--
73	VDD	PWR	--
74	NC	--	--
75	DOTCLK	I	--
76	RED0	I	--
77	ENA_VDDIN	I	--
78	RED2	I	--
79	RED1	I	--
80	BLUE0	I	--
81	BLUE3	I	--
82	BLUE1	I	--
83	BLUE2	I	--
84	BLUE4	I	--
85	RED3	I	--
86	RED4	I	--
87	GREEN2	I	--
88	BLUE5	I	--
89	VSS	GND	--
90	VSSIO	GND	--
91	VDDIO	PWR	--
92	GREEN1	I	--
93	GREEN0	I	--
94	GREEN3	I	--
95	ENA_DISP	I	--
96	RED5	I	--
97	FP_HSYNC	I	--
98	GREEN4	I	--
99	FP_VSYNC	I	--
100	GREEN5	I	--
101	ENA_LCDIN	I	--
102	MD15	I/O	8
103	MD0	I/O	8
104	MD14	I/O	8
105	MD1	I/O	8
106	MD13	I/O	8
107	MD2	I/O	8
108	VDDIO	PWR	--
109	VSSIO	GND	--
110	MD12	I/O	8
111	MD3	I/O	8
112	MD11	I/O	8
113	MD4	I/O	8
114	MD10	I/O	8
115	MD5	I/O	8
116	MD9	I/O	8
117	MD6	I/O	8
118	MD8	I/O	8
119	MD7	I/O	8
120	DQML	O	8
121	DQMH	O	8
122	WE#	O	8
123	MCLK	O	12
124	CASH#	O	8
125	VDDIO	PWR	--
126	VSSIO	GND	--
127	CAS#/CASL#	O	8
128	VSS	GND	--
129	CKE	O	8
130	RAS#	O	8
131	CS#	O	8
132	MA9	O	8
133	OE#/BA	O	8
134	MA8	O	8
135	MA10	O	8
136	MA0	O	8
137	MA7	O	8
138	MA1	O	8
139	MA6	O	8
140	MA5	O	8
141	MA4	O	8
142	MA3	O	8
143	MA2	O	8
144	VDD	PWR	--

Signal Definitions (Continued)

Table 2-3. Pin Assignments - Sorted Alphabetically by Signal Name

Signal Name	Type	Drive (mA)	Pin No.
BLUE0	I	--	80
BLUE1	I	--	82
BLUE2	I	--	83
BLUE3	I	--	81
BLUE4	I	--	84
BLUE5	I	--	88
CAS#/CASL#	O	8	127
CASH#	O	8	124
CKE	O	8	129
CS#	O	8	131
DISPOFF#	O	8	39
DOTCLK	I	--	75
DQMH	O	8	121
DQML	O	8	120
ENA_DISP	I	--	95
ENA_LCDIN	I	--	101
ENA_VDDIN	I	--	77
FLM/VSYNC	O	8	33
FP_HSYNC	I	--	97
FP_VCONEN	O	8	35
FP_VDDEN	O	8	34
FP_VSYNC	I	--	99
GPIO0	I/O	4	70
GPIO1	I/O	4	69
GPIO2	I/O	4	68
GPIO3	I/O	4	67
GPIO4	I/O	4	66
GPIO5	I/O	4	65
GPIO6	I/O	4	64
GPIO7	I/O	4	63
GREEN0	I	--	93
GREEN1	I	--	92
GREEN2	I	--	87
GREEN3	I	--	94
GREEN4	I	--	98
GREEN5	I	--	100
LD0	O	8	29
LD1	O	8	28
LD2	O	8	27
LD3	O	8	26
LD4	O	8	25
LD5	O	8	24
LD6	O	8	23
LD7	O	8	22
LD8	O	8	21
LD9	O	8	20
LD10	O	8	16
LD11	O	8	15
LDE	O	8	32
LP/HSYNC	O	8	31
MA0	O	8	136
MA1	O	8	138
MA2	O	8	143
MA3	O	8	142
MA4	O	8	141
MA5	O	8	140
MA6	O	8	139
MA7	O	8	137
MA8	O	8	134
MA9	O	8	132
MA10	O	8	135
MBIST_EN	I	--	45
MCLK	O	12	123
MD0	I/O	8	103
MD1	I/O	8	105
MD2	I/O	8	107
MD3	I/O	8	111
MD4	I/O	8	113
MD5	I/O	8	115
MD6	I/O	8	117
MD7	I/O	8	119
MD8	I/O	8	118
MD9	I/O	8	116
MD10	I/O	8	114
MD11	I/O	8	112
MD12	I/O	8	110
MD13	I/O	8	106
MD14	I/O	8	104
MD15	I/O	8	102
NC	--	--	50
NC	--	--	51
NC	--	--	52
NC	--	--	53
NC	--	--	56
NC	--	--	57
NC	--	--	58
NC	--	--	59
NC	--	--	60
NC	--	--	61
NC	--	--	62
NC	--	--	74
OE#/BA	O	8	133
RAS#	O	8	130
RED0	I	--	76
RED1	I	--	79
RED2	I	--	78
RED3	I	--	85
RED4	I	--	86
RED5	I	--	96
RESET#	I	--	44
SCAN_EN	I	--	46
SCLK	I	--	40
SCS	I	--	43
SDIN	I	--	41
SDO	O	8	42
SHFCLK	O	12	30
TEST_SE	I	--	47
UD0	O	8	14
UD1	O	8	13
UD2	O	8	12
UD3	O	8	11
UD4	O	8	10
UD5	O	8	9
UD6	O	8	8
UD7	O	8	7
UD8	O	8	6
UD9	O	8	5
UD10	O	8	4
UD11	O	8	3
VDD	PWR	--	36
VDD	PWR	--	73
VDD	PWR	--	144
VDDIO	PWR	--	1
VDDIO	PWR	--	17
VDDIO	PWR	--	37
VDDIO	PWR	--	55
VDDIO	PWR	--	72
VDDIO	PWR	--	91
VDDIO	PWR	--	108
VDDIO	PWR	--	125
VSS	GND	--	19
VSS	GND	--	54
VSS	GND	--	89
VSS	GND	--	128
VSSIO	GND	--	2
VSSIO	GND	--	18
VSSIO	GND	--	38
VSSIO	GND	--	71
VSSIO	GND	--	90
VSSIO	GND	--	109
VSSIO	GND	--	126
WE#	O	8	122
XTALIN	I	--	48
XTALOUT	O	--	49

2.2 SIGNAL DESCRIPTIONS

2.2.1 Pixel Port Interface Signals

Signal Name	Pin No.	Type (Drive)	Description
RED[5:0]	96, 86, 85, 78, 79, 76	I	**Red Pixel Channel** These six pins are the red component of the pixel port input. The six most significant bits of the pixel port (FP_DATA[17:12] on an 18-bit pixel port) from the CS5530A are connected to these pins. RED5 is the MSB (most significant bit) and RED0 is the LSB (least significant bit).
GREEN[5:0]	100, 98, 94, 87, 92, 93	I	**Green Pixel Channel** These six pins are the green component of the pixel port input. The six middle bits of the pixel port (FP_DATA[11:6] on an 18-bit pixel port) from the CS5530A are connected to these pins. GREEN5 is the MSB and GREEN0 is the LSB.
BLUE[5:0]	88, 84, 81, 83, 82, 80	I	**Blue Pixel Channel** These six pins are the blue component of the pixel port input. The six least significant bits of the pixel port (FP_DATA[5:0] on an 18-bit pixel port) from the CS5530A are connected to these pins. BLUE5 is the MSB and BLUE0 is the LSB.
ENA_DISP	95	I	**Active Display Enable** This input is asserted when the pixel data stream is presenting valid display data to the pixel port.
ENA_VDDIN	77	I	**Input VDD Enable** When this input is asserted high, it indicates that the CS9211 should apply voltage to the LCD panel. FP_VDDEN (pin 34) follows this assertion if external power sequencing is selected; it is ignored if internal power sequencing is selected.
ENA_LCDIN	101	I	**Input LCD Enable** When this input is asserted high, it indicates that the CS9211 should drive the contrast voltage to the LCD panel. FP_VCONEN (pin 35) follows this assertion if external power sequencing is selected; it is ignored if internal power sequencing is selected.
DOTCLK	75	I	**DOT Clock** This signal is the pixel clock from the video controller within the CS550A. It clocks data in from the pixel port on the rising edge. Additionally, this signal is used as the input clock for the entire CS9211 device. This clock must be running at all times after reset for the CS9211 to function correctly.
FP_HSYNC	97	I	**Flat Panel Horizontal Sync Input** When the input data stream is in a horizontal blanking period, this input is asserted. It is a pulse used to synchronize display lines and to indicate when the pixel data stream is not valid due to blanking.
FP_VSYNC	99	I	**Flat Panel Vertical Sync Input** When the input data stream is in a vertical blanking period, this input is asserted. It is a pulse used to synchronize display frames and to indicate when the pixel data stream is not valid due to blanking.

Signal Definitions (Continued)

2.2.2 Serial Interface Signals

Signal Name	Pin No.	Type (Drive)	Description
SCLK	40	I	**Serial Interface Clock** This input signal is the clock for the serial control interface. Data is clocked in and out on the rising edge. The other serial interface signals (SDIN, SCS, and SDO) are synchronous to this signal.
SDIN	41	I	**Serial Data Input** This is the data input line for the serial control interface. Input data is serialized on this pin, including the command stream for register reads and writes.
SDO	42	O (8 mA)	**Serial Data Output** This is the data output line for the serial control interface. Output data is serialized on this pin in response to register read commands.
SCS	43	I	**Serial Chip Select** This active high chip select indicates when valid data is being clocked in or out via the SDIN/SDO pins.

2.2.3 Flat Panel Interface Signals

Signal Name	Pin No.	Type (Drive)	Function Selection	Description
SHFCLK	30	O (12 mA)	---	**Panel Clock (Shift Clock)** This is the shift clock or pixel clock for the flat panel data. This signal is used to clock pixel data into the LCD panel. Depending on the type of panel being interfaced, this signal can also be referred to as CL2 or SHIFT.
UD[11:0] LD[11:0]	3:14 15, 16, 20:29	O (8 mA)	---	**Upper and Lower Scan Data** These outputs are the panel pixel data bus to the LCD panel. The data format is dependent on the panel type selected. Refer to Section 3.2.2 “Mode Selection” on page 19.
LDE	32	O (8 mA)	Offset 404h[25] = 1	**Flat Panel Display Enable (TFT Panels)** LDE is the display enable for active-matrix TFT panels and is used to indicate the active pixel data on UD[11:0] and LD[11:0].
LP	31	O (8 mA)	Offset 404h[26] = 0	**Latch Pulse (SSTN/DSTN Panels)** Latch Pulse is the line pulse or latch pulse for the flat panel data, indicating that a display line is about to start. Depending on the type of panel being interfaced, this signal can also be referred to as CL1 or LINE.
HSYNC			Offset 404h[26] = 1	**Horizontal Sync (TFT Panels)** HSYNC is the horizontal sync for the active-matrix TFT panel. This is a delayed version of the input HSYNC signal with the appropriate pipeline delay relative to the pixel data on UD[11:0] and LD[11:0]. If pin 31 is set as HSYNC at Offset 404h[26], its polarity is programmable through Offset 404h[22]: 0 = Active high; 1 = Active low.

Signal Definitions (Continued)

2.2.3 Flat Panel Interface Signals (Continued)

Signal Name	Pin No.	Type (Drive)	Function Selection	Description
FLM	33	O (8 mA)	Offset 404h[24] = 0	**First Line Marker (SSTN/DSTN Panels)** This is the frame pulse for the flat panel data indicating a display frame is about to start. Depending on the type of panel being interfaced, this signal can also be referred to as FP or FRAME.
VSYNC			Offset 404h[24] = 1	**Vertical Sync (TFT Panels)** VSYNC is the vertical sync for active-matrix TFT panel. This is a delayed version of the input VSYNC signal with the appropriate pipeline delay relative to the pixel data on UD[11:0] and LD[11:0]. If pin 33 is selected as VSYNC at Offset 404h[24], its polarity is programmable through Offset 404h[23]: 0 = Active high; 1 = Active low.
DISPOFF#	39	O (8 mA)	---	**Disables Backlight** When this output is asserted low, it turns the backlight off.
FP_VDDEN	34	O (8 mA)	---	**Controls LCD VDD FET** When this output is asserted high, VDD voltage is applied to the panel. This signal is intended to control a power FET to the LCD panel. The FET may be internal to the panel or not, depending on the panel manufacturer
FP_VCONEN	35	O (8 mA)	---	**Controls LCD Bias Voltage Enable** When this output is asserted high, the contrast voltage is applied to the panel. This signal should be connected directly to the panel.

2.2.4 Memory Interface Signals

Signal Name	Pin No.	Type (Drive)	Description
MA[10:0]	135, 132, 134, 137, 139, 140, 141, 142, 143, 138, 136	O (8 mA)	**Memory Address Bus** These signals are the address bits to the external frame buffer. Ten bits are used for EDO (Extended Data Out) DRAM and eleven bits are used for SDRAM. Row and column addresses are multiplexed on the same pins.
MD[15:0]	102, 104, 106, 110, 112, 114, 116, 118, 119, 117, 115, 113, 111, 107, 105, 103	I/O (8 mA)	**Memory Data Bus** These bidirectional signals are the external frame buffer data bus.

Signal Definitions (Continued)

2.2.4 Memory Interface Signals (Continued)

Signal Name	Pin No.	Type (Drive)	Description
DQMH	121	O (8 mA)	**Data Input/Output Mask** DQMx is an input mask signal to the frame buffer SDRAM for write accesses and an output enable signal for read accesses. • Input data to the SDRAM is masked when DQMx is sampled high during a write cycle. • The output buffers are placed in a High-Z state (two-clock latency) when DQMx is sampled high during a read cycle. DQMH corresponds to DQ8-DQ15 of the SDRAM. DQML corresponds to DQ0-DQ7 of the SDRAM. This signal is not used for EDO DRAM.
DQML	120	O (8 mA)	
OE#/BA	133	O (8 mA)	**Output Enable and Bank Select Address** This pin is the output enable for the DRAM and the bank address selection for SDRAM. BA defines to which bank the active, read, write or precharge command is being applied. This function is not used in the CS9211.
RAS#	130	O (8 mA)	**Row Address Strobe** The row address strobe for DRAM/SDRAM.
CASH#	124	O (8 mA)	**Column Address Strobe** The column address strobe for the upper byte of EDO DRAM. This pin should not be connected if SDRAM is used.
CAS#/CASL#	127	O (8 mA)	**Column Address Strobe** The column address strobe for the lower byte of DRAM. This pin should be connected (to CAS#) if SDRAM is used.
WE#	122	O (8 mA)	**Write Enable** The write enable output for DRAM/SDRAM.
MCLK	123	O (12 mA)	**Memory Clock** This clock output from the CS9211 should be connected to the SDRAM. It is not used for EDO DRAM.
CKE	129	O (8 mA)	**Clock Enable** This output signal should be connected to the SDRAM. When CKE is active (high), the MCLK signal is low. Deactivating the clock provides precharge power-down and self-refresh operations (all banks idle), active power-down (row active CKE in either bank) or clock Suspend operation (burst/access in progress). CKE is synchronous to MCLK, except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including MCLK, are disabled during power-down and self refresh modes, and provide low power. CKE may be tied high. This signal is not used for EDO DRAM.
CS#	131	O (8 mA)	**Chip Select** This output is connected to the chip select of SDRAM. CS# enables (registered low) and disables (registered high) the command decoder of the SDRAM. All commands are masked when CS# is deasserted (high).

Signal Definitions (Continued)

2.2.5 Reset, Crystal, and GPIO Pins

Signal Name	Pin No.	Type (Drive)	Description
RESET#	44	I	**System Reset Input** A system reset should be at least as long as one clock cycle of the slowest of DOTCLK, XTALIN or SCLK. RESET# should be active for at least 1 ms.
XTALIN	48	I	**Crystal Oscillator Connection** This pin is the crystal input for the on-chip reference oscillator or a CMOS clock input from an external reference source. It should be 14.318 MHz.
XTALOUT	49	O	**Crystal Oscillator Connection** This pin is the crystal output for the on-chip reference oscillator. If an external clock is used, leave this pin unconnected.
GPIO0-GPIO7	70:63	I/O (4 mA)	**General Purpose Inputs/Outputs** Each GPIO pin can be configured independently as an input or output. For further programming information refer to Section 3.2.13 “General Purpose I/O Pins” on page 38.

2.2.6 National Semiconductor Internal Test Pins

Signal Name	Pin No.	Type (Drive)	Description
TEST_SE	47	I	**Reserved** This pin must be tied to ground for normal operation. It is a National Semiconductor internal test mode pin only.
MBIST_EN	45	I	**Reserved** This pin must be tied to ground for normal operation. It is a National Semiconductor internal test mode pin only.
SCAN_EN	46	I	**Reserved** This pin must be tied to ground for normal operation. It is a National Semiconductor internal test mode pin only.

2.2.7 Power and Ground Pins

Signal Name	Pin No.	Type (Drive)	Description
VDDIO	1, 17, 37, 55, 72, 91, 108, 125	PWR	**Power Connection (total of 8 pins)** Power for the DRAM and system interface signals. These pins should be supplied with 3.3V.
VSSIO	2, 18, 38, 71, 90, 109, 126	GND	**Ground Connection (total of 7 pins)** Ground connection.
VDD	36, 73, 144	PWR	**Power Connection (total of 3 pins)** Power for the DRAM and system interface signals. These pins should be supplied with 3.3V.
VSS	19, 54, 89, 128	GND	**Ground Connection (total of 4 pins)** Ground connection.

3.0 Functional Description

This chapter discusses the detailed operations of the CS9211 in two categories: system-level and the operations/programming of the major functional blocks.

3.1 SYSTEM INTERCONNECTIONS

The system-level discussion topics revolve around events that affect the device as a whole unit and how the CS9211 connects/interfaces with other system devices (i.e., CS5530A, panel, memory, and crystal oscillator).

3.1.1 CS550A Connections

The CS9211 graphics companion connects to the TFT graphics data port of the CS550A I/O companion chip, as shown in Figure 3-1. In order for this interface to function, the CS550A must be in the “Limited ISA Mode”, not the “ISA Master Mode”, as discussed in the CS550A data book.

Register programming and internal memory loading commands are delivered to the CS9211 by means of a GPIO interface. The GPIOs can come from any device capable of controlling those signals, as described in Section 3.2.1 "Serial Interface" on page 17. For example, National’s SuperI/O (PC97317) also produces compatible GPIO signals.

The CS9211 reformats the incoming pixel data stream and produces an output data stream that is directly compatible with the attached LCD panel.

Timing and power sequence control signals are delivered to the CS9211 from the CS550A. Various “pass-through” or “internal/external” selection modes of the CS9211 allow those external signals to be used or modified internally, before being passed on to the panel, or ignored completely, in which case they would be generated internally.

The CS9211 receives a pixel data stream from the CS550A. The chief function of the CS9211 is to reformat this received input stream into an output stream suitable for display on the LCD panels it supports.

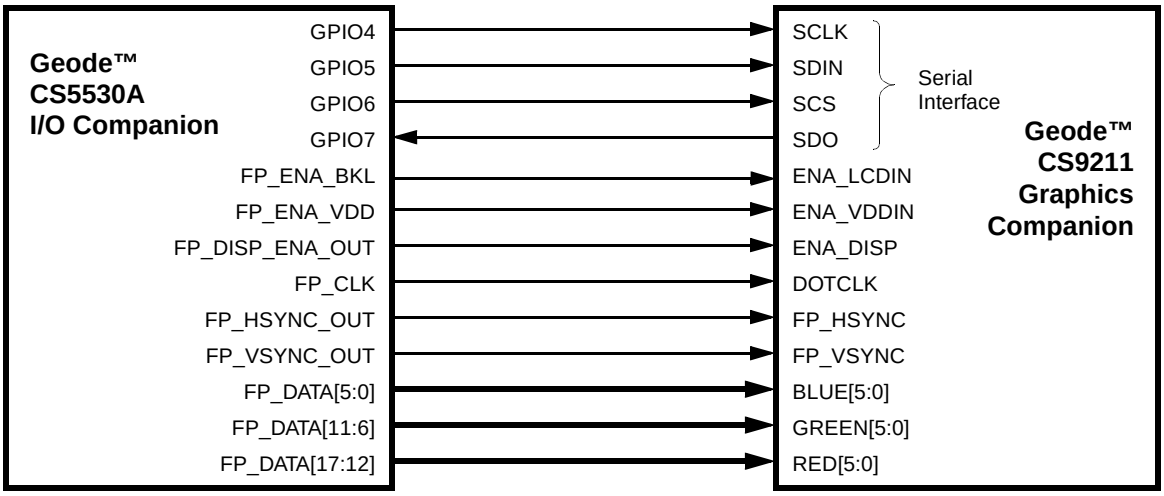


Figure 3-1. CS550A and CS9211 Signal Connections

Functional Description (Continued)

3.1.2 Panel Connections

As illustrated in Figure 3-3, the connections between the CS9211 and the LCD panel being driven are simple. There are three groups of interconnect: Power Control, Timing, and Data. Because of the wide variety of LCD panels currently used in the industry, this interface is discussed briefly and generically.

Power control signals enable the panel's backlight, main power, and contrast voltage. In some cases, these signals may be directly connected to the panel being used; in other cases, external circuitry such as a power FET, may be required. Consult the data sheet of the panel being used in the design for details.

Timing signals are connected directly to the panel. Different panel manufacturers use various nomenclatures to identify the timing signals, some of which are shown (separated by the "/" character) in Figure 3-3.

The output of the CS9211 is a 24-bit data bus that is artificially split into two 12-bit data buses by the CS9211's adopted nomenclature (UD/LD). The output data presented on these buses "moves" from pin to pin depending on the type of panel being used, as determined by the contents of several of the CS9211's internal registers. These output buses should be thought of as one 24-bit bus for ease of the designer's understanding and to avoid confusion with panels which have a UD/LD-type data bus nomenclature.

3.1.3 Memory Connections

The interface between the CS9211 and the frame buffer memory (if used) is straightforward. Signal names used in the CS9211 match up with those used by the standard EDO DRAM and SDRAM devices. Note that the frame buffer memory is only required for DSTN panels. If the memory is not required, the memory interface signals from the CS9211 may remain unconnected.

If a DSTN panel is used, the CS9211 must be connected to an external frame buffer RAM, which may be either EDO DRAM or SDRAM. The external frame buffer is not required if an SSTN panel is used. Pixel data is received by the pixel port, formatted by a dither block and programmable FRM, and stored in the CS9211 frame buffer. The formatted pixel data is subsequently read from the frame buffer and used to refresh half the DSTN panel, while the other half receives "live" data from the CS550A.

3.1.4 Crystal Oscillator Interface

The CS9211 requires a 14.318 MHz input clock to generate power sequencing signals to the panel. The input frequency should be 14.318 MHz. The clock may come from a compatible clock source anywhere in the design, or from a dedicated crystal oscillator tank circuit. The recommended oscillator tank circuit is shown in Figure 3-2.

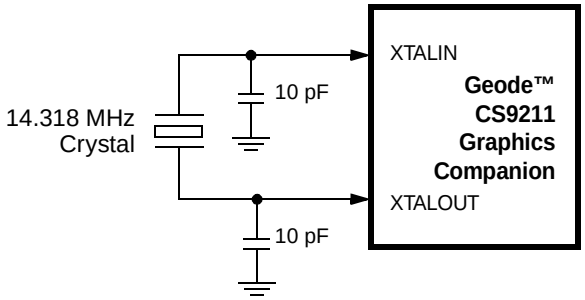


Figure 3-2. Oscillator Tank Circuit

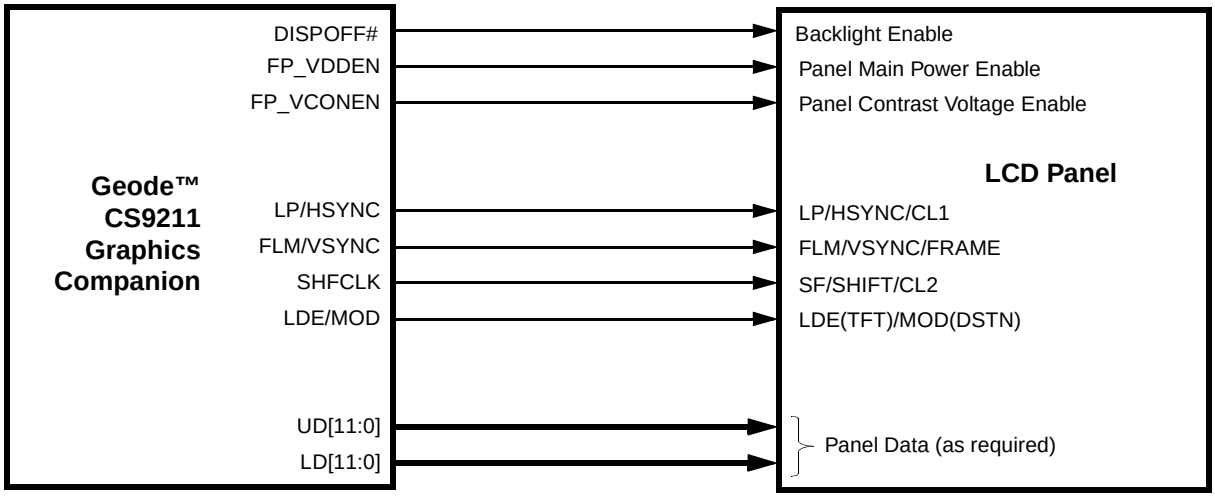


Figure 3-3. CS9211 and Flat Panel Signal Connections

Functional Description (Continued)

3.2 FUNCTIONAL BLOCKS

The block diagram of the CS9211, along with the basic system interconnections are shown in Figure 3-4. Details of each block will be discussed in this section.

The CS9211 interfaces directly to industry standard 8-, 16- and 24-bit color or monochrome single or dual-scan STN flat panels (not all combinations are supported). It can also support 18-bit active matrix thin-film-transistor (TFT) with one or two pixels per clock.

The digital RGB or video data that is supplied by the CS5530A is converted into a suitable format to drive the supported panels. The heart of the device is the Frame Rate Modulator (FRM), which provides the ability to display various intensities of each primary color. Dithering logic is included to further increase the apparent number of colors that can be displayed. To support the DSTN panels, a memory controller that interfaces to external EDO DRAM or SDRAM (used as a frame buffer) is built into the CS9211. A configurable timing generator provides timing pulses tailored to the panel being driven. The CS9211 supports automatic power sequence of panel power supplies. The device contains a CRC generator which may be used for self-validation during silicon validation.

Each pixel on an SSTN or DSTN LCD panel consists of three primary color components: red, green, and blue. Each primary color component, for a given pixel, can be turned on or off; there are no intermediate intensities. A total of eight colors can be generated for a given pixel through various combinations of turning each color component on or off. In order to generate more colors, frame rate modulation and dithering are used. The CS9211 is capable of generating 256K different colors, based on the 18-bit RGB pixel inputs.

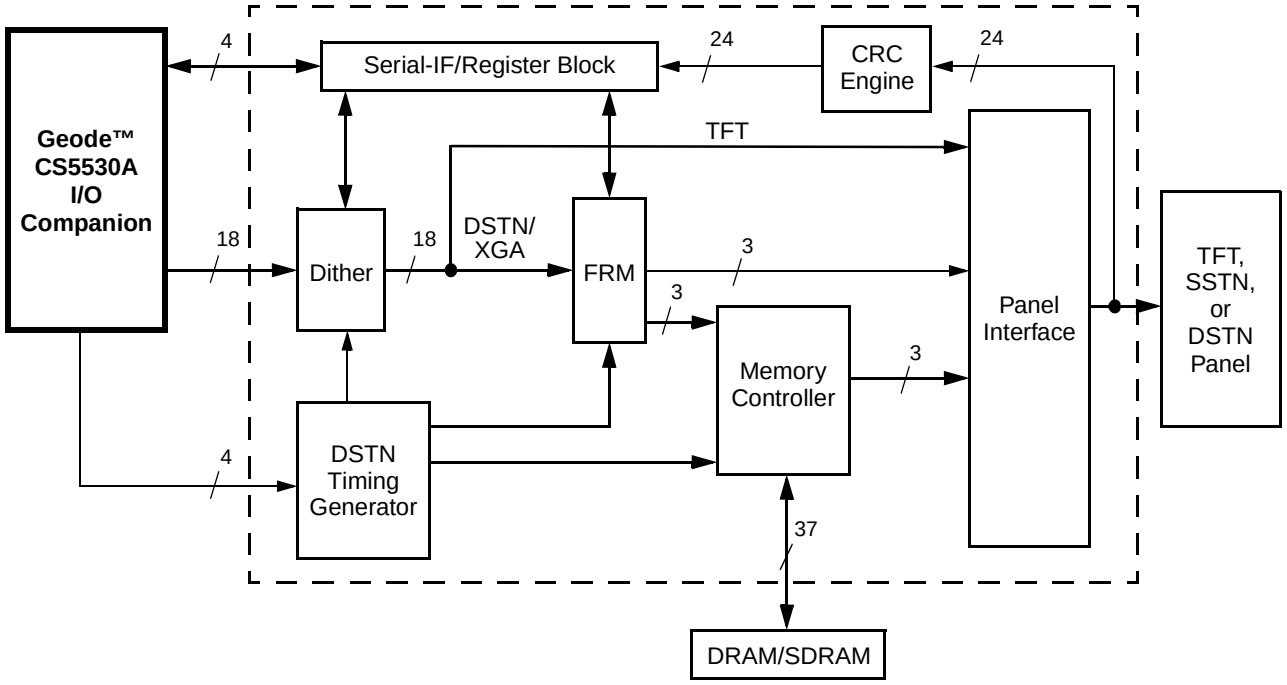


Figure 3-4. CS9211 Block Diagram

Functional Description (Continued)

3.2.1 Serial Interface

Two commands are defined for the serial interface, a read command and a write command. The read and write protocols are summarized in Table 3-1. Figure 3-5 on page 18 shows the write cycle timing, and Figure 3-6 on page 18 shows the read cycle timing. In order for the CS9211 to properly receive commands through the serial interface, the DOTCLK input signal must be active.

The protocol begins with the assertion of the SCS input, followed by activity on the SCLK (serial command clock) and SDIN (serial data input) lines. The serial data must be in the following order: one start bit (value = X), one control bit (value = 1), 12 address bits, a read/write command bit (1 = Write, 0 = Read), and 32 data bits. In the case of a read, seven (7) idle clock pulses must occur between the read command and the beginning of the 32 bits of data transmission on the SDO line. After the last bit of the serial data transfer, SCS should be deasserted.

The CS9211 samples the serial interface input signals on the rising edge of SCLK. Therefore, data driven onto the SDIN input should change on the falling edge of SCLK. Data driven by the CS9211 onto the SDO output changes on the rising edge of SCLK. Therefore data being read should be sampled on the falling edge of SCLK.

3.2.1.1 Write Transfer Sequence (52 clocks)

1) Assert SCS input.
2) One SCLK period “don’t care” transfer (i.e., clock toggle).
3) Write a 1 to SDIN.
4) Next, the address is transmitted with the LSB (Address[0]) first... MSB (Address[11]) last.
5) The Write bit = 1.
6) The data is transmitted LSB (Data[0]) first... MSB (Data[31]) last, on the positive edges of the next 32 SCLKS.
7) Deassert SCS (one clock period) and toggle SCLK for four clock periods.

3.2.1.2 Read Transfer Sequence (56 clocks)

1) Assert SCS input.
2) One SCLK period “don’t care” transfer (i.e., clock toggle).
3) Write a 1 to SDIN.
4) Next the address is transmitted with the LSB (Address[0]) first ... MSB (Address[11]) last.
5) The Read bit = 0.
6) Seven SCLK periods of “don’t care” transfer (i.e., clock toggles).
7) The data is transmitted on SDO with the LSB (Data[0]) first ... MSB (Data[31]) last, on the positive edges of the next 32 SCLK .
8) Deassert SCS (one clock period) and toggle SCLK for one clock period.

Table 3-1. Serial Interface Write/Read Sequences

Cycle(s)	Write Sequence with SCS = “1”		Cycle(s)	Read Sequence with SCS = “1”	
1	1 Start bit	SDIN = Don’t care	1	1 Start bit	SDIN = Don’t care
1	1 Control bit	SDIN = 1	1	1 Control bit	SDIN = 1
12	12 Address bits	SDIN = 4xx	12	12 Address bits	SDIN = 4xx
1	1 Write bit	SDIN = 1	1	1 Read bit	SDIN = 0
32	32 data bits	ex: SDIN = A8A8_A8A8h	7	7 Idle SCLKs	ex: SDIN = Don’t care
			32	32 Read data bits	ex: SDO = A8A8_A8A8h

Functional Description (Continued)

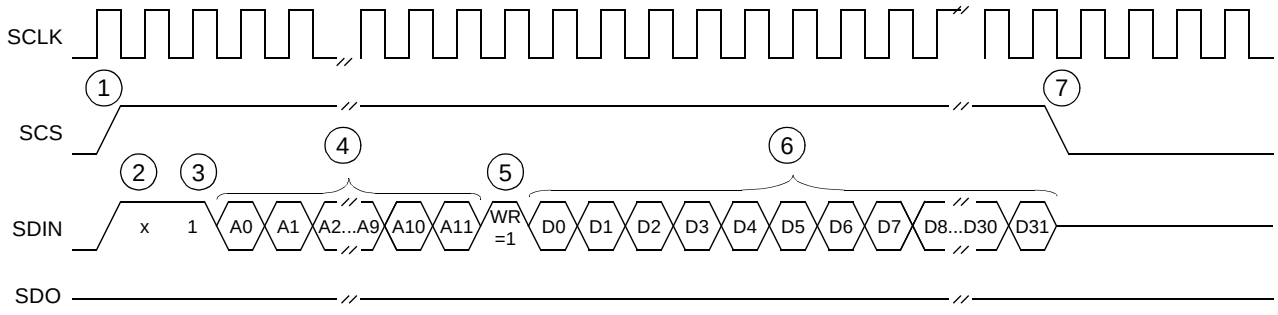


Figure 3-5. Serial Interface Write Cycle Timing Diagram

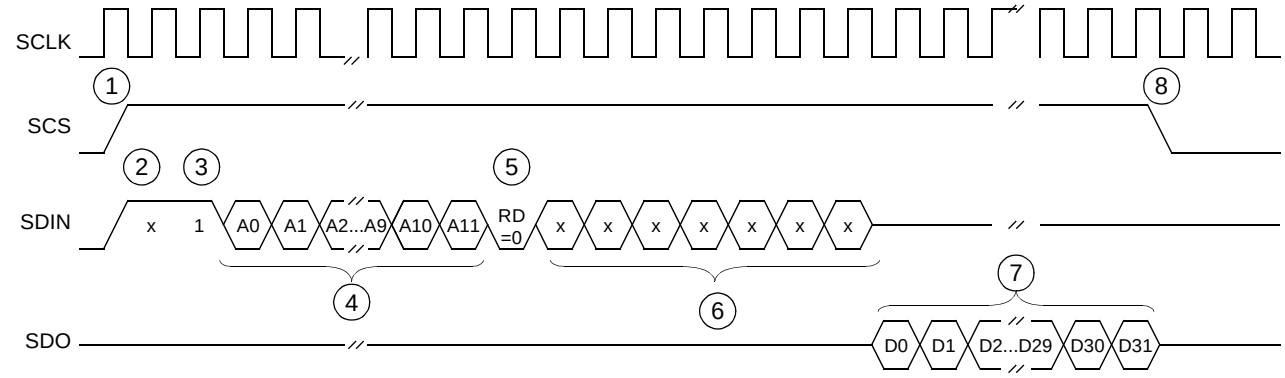


Figure 3-6. Serial Interface Read Cycle Timing Diagram

Functional Description (Continued)

3.2.2 Mode Selection

The CS9211 can be configured for various modes depending on the type of LCD panel being connected. The panel type and mode selection is through Offset 404h[21:16] as shown in Table 3-2 on page 20 and described below.

- DSTN or TFT and Color or Monochrome:
  - — DSTN or TFT: Allows a common connector to be used for TFT LCD panels and DSTN LCD panels. The system software can configure the CS9211 to operate in a pass-through mode that presents the digital pixel (RGB) input data on the UD/LD output pins to drive a TFT panel on the common connector. The input data is latched internally before being presented at the output pins to better control the timing of the panel interface signals.
  - — Color or Monochrome: Monochrome must be selected for 8-bit DSTN Mode.
- 8-Bit DSTN Mode (Monochrome Only):
  - — Supports DSTN panels with 640x480 pixel resolution.
  - — Register programming: Offset 404h[21:16] = 00_1_000.
- 8-Bit single scan Color STN Mode:
  - — Supports single scan STN panels with 640x480 color pixel resolution.
  - — Register programming: Offset 404h[21:16] = 00_0_011.
- 16-Bit Color DSTN Mode:
  - — Supports DSTN panels with 640x480 or 800x600 color pixel resolutions.
  - — Register programming: Offset 404h[21:16] = 00_0_001.
- 24-Bit Color DSTN Mode:
  - — Supports DSTN panels with 1024x768 color pixel resolution.
  - — Register programming: Offset 404h[21:16] = 00_0_010.
- TFT One Pixel per Clock Mode:
  - — Supports all TFT panels with up to 18-bit interface.
  - — Register programming: Offset 404h[21:16] = 01_0_000.
- TFT Two Pixel per Clock Mode:
  - — Supports 18-bit/24-bit 2pixel/CLK TFT panels.
  - — Register programming: Offset 404h[21:16] = 01_0_001.

3.2.2.1 TFT Mode

To enable TFT mode, set Offset 404h[21:20] = 01 (see Table 3-2 on page 20). When TFT mode has been selected, the output from the dither block is fed directly onto the panel data pins UD[11:0] and LD[11:0], in accordance with Table 3-4 on page 21, and in sync with the TFT timing signals HSYNC, VSYNC, and LDE. These three timing signals are enabled when Offset 404h[26:24] = 111 (see Table 3-3 on page 20). The TFT panel type must be selected according to Table 3-2. The shift clock output (SHFCLK) varies for each panel type (refer to Table 3-7 on page 24). The pixel data format on the LD/UD pins varies based on the type of TFT panel selected as indicated in Table 3-4. Certain timing selections must be made according to Table 3-8 "Panel Output Timing Selection Bits" on page 24 (see the discussion in Section 3.2.3 "Timing Signals" on page 22).

3.2.2.2 STN Mode

This mode is for either SSTN or DSTN panels. To enable STN mode, set Offset 404h[21:20] = 00 (see Table 3-2). When STN mode has been selected, the output from the dither block is sent through the FRM and the memory controller (memory controller: DSTN only), and continues to the panel data pins. The CS9211 will shift out the data on the positive edge of the shift clock (SHFCLK). The shift clock output (SHFCLK) varies for each panel type as shown in Table 3-7 on page 24. The pixel data format on the LD/UD pins varies based on the type of STN panel selected, as indicated in Table 3-4. Certain timing selections must be made according to Table 3-8 "Panel Output Timing Selection Bits" on page 24 (see the discussion in Section 3.2.3 "Timing Signals" on page 22).

3.2.2.3 Output Data Mapping

The output of the CS9211 is a 24-bit data bus that is artificially split into two 12-bit data buses by the CS9211's adopted nomenclature (UD/LD). The output data presented on these buses "moves" from pin to pin depending on the type of panel being used, as determined by the contents of Offset 404h[21:16] (see Table 3-2).

The mapping is shown in Table 3-4 on page 21. These output buses should be thought of as one 24-bit bus (perhaps named OUT[23:0]) for ease of the designer's understanding and to avoid confusion with panels that have a UD/LD-type data bus nomenclature.

Functional Description (Continued)

Table 3-2. Panel Mode Selection Bits

Bit	Name	Description
Offset 404h-407h		**Panel Timing Register 2 (R/W)** **Reset Value = 00000000h**
21:20	DSTN_TFT	**Panel Type Select**: Selects panel type. The selection of the panel type in conjunction with the PIX_OUT (bits [18:16]) setting determines how pixel data is mapped on the output LD/UD pins. This bit also determines the generation of SHFCLK and other panel timing interface signals. 00 = SSTN/DSTN panel 01 = TFT panel 10 = Reserved 11 = Reserved
19	COLOR_MONO	**Color/Mono Select**: Selects color or monochrome LCD panel. 0 = Color; 1 = Monochrome.
18:16	PIX_OUT	**Pixel Output Format**: These bits define the pixel output format. The selection of the pixel output format in conjunction with the panel type selection (bits [21:20]) and the color/monochrome selection (bits [19]) determines how the pixel data is formatted before being sent on to the LD/UD pins. These settings also determine the SHFCLK period for the specific panel. 000 = 8-bit DSTN panel or up to 24-bit TFT panel with one pixel per clock. Option 1: Mono 8-bit DSTN (bits [21:20] = 00 and bit 19 = 1) (Color 8-bit DSTN is not supported) SHFCLK = 1/4 of DOTCLK Option 2: Color TFT with 1 pixel/clock (bits [21:20] = 01 and bit 19 = 0) SHFCLK = DOTCLK 001 = 16-bit DSTN panel or 18/24-bit TFT XGA panel with two pixels per clock. Option 1: Color 16-bit DSTN (bits [21:20] = 00 and bit 19 = 0) SHFCLK = 1/(3:2:3) of DOTCLK Option 2: Mono 16-bit DSTN (bits [21:20] = 00 and bit 19 = 1) SHFCLK = 1/8 of DOTCLK Option 3: Color 18/24 bit TFT (bits [21:20] = 01 and bit 19 = 0) SHFCLK = 1/2 of DOTCLK 010 = 24-bit DSTN panel Color 24-bit DSTN (bits [21:20] = 00 and bit 19 = 0) (Mono 24-bit DSTN is not supported) SHFCLK = 1/4 of DOTCLK 011 = 8-bit SSTN panel Color 8-bit SSTN (bits [21:20] = 00 and bit 19 = 0) SHFCLK = 1/(3:2:3) of DOTCLK 100, 101, 110, and 111 = Reserved

Table 3-3. Panel Interface Pin Function Selection Bits

Bit	Name	Description
Offset 404h-407h		**Panel Timing Register 2 (R/W)** **Reset Value = 00000000h**
26	LP_HSYNC_SEL	**LP/HSYNC Select**: Selects the function of LP/HSYNC (pin 31). Set this bit based on the panel type connected. For DSTN or SSTN panels, set this bit to 0. For TFT panels, set this bit to 1. 0 = LP (output for DSTN/SSTN panel). 1 = HSYNC (output for TFT panel).
25	LDE_SEL	**LDE Select**: Always set this bit to 1. 0 = Reserved 1 = LDE (output for TFT panel).
24	FLM_VSYNC_SEL	**FLM/VSYNC Select**: Selects function of FLM/VSYNC (pin 33). Set this bit based on the panel type connected. For DSTN or SSTN panels, set this bit to 0. For TFT panels, set this bit to 1. 0 = FLM (output for DSTN/SSTN panel). 1 = VSYNC (output for TFT panel).

Functional Description (Continued)

Table 3-4. Output Data Mapping

Pin Name	DSTN 24-Bit	DSTN 16-Bit	STN 8-Bit	DSTN 8-Bit (Mono)	TFT 9-Bit	TFT 18-Bit	TFT 9+9-Bit	TFT 12+12-Bit
LD0	UD9			UD0(pix1)				BB0
LD1	UD10			UD1(pix2)			BB0	BB1
LD2	UD11			UD2(pix3)		B0	BB1	BB2
LD3	UD6			UD3(pix4)		B1	BB2	BB3
LD4	UD7	UD0	D0			B2		GB0
LD5	UD8	UD1	D1		B0	B3	GB0	GB1
LD6	UD3	UD2	D2		B1	B4	GB1	GB2
LD7	UD4	UD3	D3		B2	B5	GB2	GB3
LD8	UD5			LD0(pix1)				RB0
LD9	UD0			LD1(pix2)			RB0	RB1
LD10	UD1	UD4	D4	LD2(pix3)		G0	RB1	RB2
LD11	UD2	UD5	D5	LD3(pix4)		G1	RB2	RB3
UD0	LD9	UD6	D6			G2		BA0
UD1	LD10	UD7	D7		G0	G3	BA0	BA1
UD2	LD11	LD0			G1	G4	BA1	BA2
UD3	LD6	LD1			G2	G5	BA2	BA3
UD4	LD7							GA0
UD5	LD8						GA0	GA1
UD6	LD3	LD2				R0	GA1	GA2
UD7	LD4	LD3				R1	GA2	GA3
UD8	LD5	LD4				R2		RA0
UD9	LD0	LD5			R0	R3	RA0	RA1
UD10	LD1	LD6			R1	R4	RA1	RA2
UD11	LD2	LD7			R2	R5	RA2	RA3
SHFCLK	CL2/	CL2	CP	CP	CLK	CLK	CLK	CLK
LP/HSYN	CL1	CL1	LOAD	LOAD	HSYNC	HSYNC	HSYNC	HSYNC
FLM/VSYNC	FLM	FLM	FRM	FRM	VSYNC	VSYNC	VSYNC	VSYNC
MOD/LDE	-NA-	-NA-			LDE	LDE	LDE	LDE
FP_VDDEN					ENLVDD	ENLVDD	ENLVDD	ENLVDD
FP_VCONEN					ENLVEE	ENLVEE	ENLVEE	ENLVEE
DISPOFF#	DISPOFF	DISPOFF	DISPON		BKLTON	BKLTON	BKLTON	BKLTON

Functional Description (Continued)

3.2.3 Timing Signals

The CS9211 provides features that allow control over the timing pulses coming from the CS550A (or other source) and over those which drive the panel. These pulses may be inverted, positioned, and otherwise modified as explained in this section.

3.2.3.1 Input Timing Signals

The internal logic of the CS9211 is designed to operate from the leading edge of the incoming VSYNC and HSYNC pulses. This internal logic is triggered from the rising edge of the input pulses after inversion (or not) by Offset 400h bits 30 and 29, as shown in Figure 3-7. The purpose of the Offset 400h[30:29] is to make the leading edge of the input pulses (be it a rising or falling edge) appear as a rising edge to the internal logic, thereby triggering the internal logic at the leading edge of the input pulses. In Figure 3-7, when the FP_xSYNC_POL bit is 1 (POL = 1), the inverting buffer will be enabled; when the FP_xSYNC_POL bit is 0 (POL = 0), the non-inverting buffer will be enabled. (The terminology FP_xSYNC_POL refers to the fact that this holds true for both the HSYNC and VSYNC pulses).

Two bits (Offset 400h[30:29]) are used to match the CS9211 to the polarity of the incoming HSYNC and VSYNC signals, as shown in Table 3-5. These bits should be set as indicated to match the polarity of the incoming timing pulses to the CS9211's internal logic needs.

The internal logic following the HSYNC input may be bypassed by programming Offset 400h[27] = 0. In this case, the input HSYNC, after possible inversion by Offset 400[29], is passed directly onto the output pin of the CS9211. If Offset 400h[27] = 1, then the incoming HSYNC pulse may be modified by Offset 400h[7:0] before being passed to the output HSYNC pin.

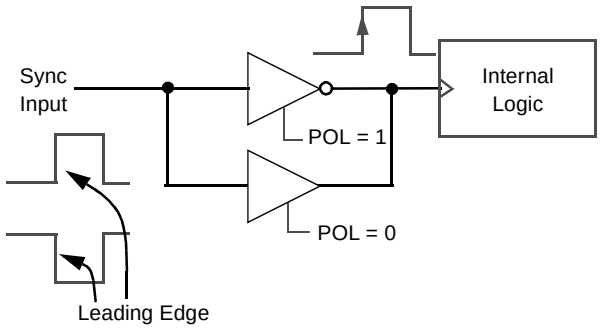


Figure 3-7. Input Timing Pulse Polarity Selection

Table 3-5. Input Timing Control Bits

Bit	Name	Description
Offset 400h-403h		**Panel Timing Register 1 (R/W)** **Reset Value = 0000000h**
30	FP_VSYNC_POL	**FP_VSYNC Input Polarity**: Selects positive or negative polarity of the FP_VSYNC input (pin 99). Program this bit to match the polarity of the incoming FP_VSYNC signal. Note that bit 23 of Offset 404h independently controls the polarity of the output VSYNC. 0 = FP_VSYNC is normally low, transitioning high during sync interval (**Default**). 1 = FP_VSYNC is normally high, transitioning low during sync interval.
29	FP_HSYNC_POL	**FP_HSYNC Input Polarity**: Selects positive or negative polarity of the FP_HSYNC input (pin 97). Program this bit to match the polarity of the incoming FP_HSYNC signal. Note that bit 22 of Offset 404h independently controls the polarity of the output HSYNC. 0 = FP_HSYNC is normally low, transitioning high during sync interval (**Default**). 1 = FP_HSYNC is normally high, transitioning low during sync interval.
27	HSYNC_SRC	**TFT Horizontal Sync Source**: Selects an internally generated or external pass-through source of the TFT horizontal sync output on pin 31. The internally generated HSYNC pulse will be triggered by the input HSYNC, but the output polarity, and leading and trailing edge positions are controlled by registers 404h[22] and 400h[7:0] respectively. The external mode will pass the input HSYNC pulse directly to the output pin. 0 = Pass the input HSYNC directly onto the output LP/HSYNC pin (pin 31) (**Default**). 1 = Internally generate the output HSYNC using the leading/trailing edge bits [7:0] and the polarity bit (Offset 404h[22]).
7:5	HSYNC_LEADING_EDGE	**Horizontal Sync Leading Edge Position**: Selects the position of the leading edge of the output HSYNC pulse with respect to the rising edge of the modified input HSYNC pulse. The modified input HSYNC pulse is that which has been inverted, or not inverted, by bit 29. The position is programmable in steps of 1 DOTCLK, starting at 2 DOTCLOCKS and extending up to 8. Bit 27 must be set in order for bits [7:5] to be recognized. Note that there are combinations of bits [7:5] and [4:0] that can result in a zero- or negative-length pulse, for example if the trailing edge is positioned before the leading edge. In this case, the output pulse will not be generated. 000 = No delay from the input HSYNC (**Default**). 001-111 = Position the HSYNC leading edge by 2 to 8 DOTCLKs with respect to the input HSYNC rising edge. Note that there is no setting for a position of 1 DOTCLOCK.

Functional Description (Continued)

3.2.3.2 Output Timing Signals

There are two separate pass-through bits to select internal or external generation of the output timing signals. The PASS_THRU bit, Offset 404h[30] is global and affects whether Offset 400h[7:0], Offset 404h[29], and Offset 404h[27:24] control bits will apply or not. The second pass-through is the HSYNC_SRC bit, Offset 400h[27], and it determines if the incoming FP_HSYNC pulse will be passed through unmodified or not. See Table 3-8 on page 24 for descriptions on these bits.

HSYNC

Two groups of bits (Offset 400h[7:5] and Offset 400h[4:0]) control the positions of the leading and trailing edges of the output HSYNC pulse, also called LP (Latch Pulse), LINE, or CL1 for some panels. These two groups are effective only if HSYNC_SRC, Offset 400h[27], is set to 1.

Regardless of the input or output polarity, the two groups of bits move the leading and trailing edges of the output HSYNC pulse with respect to the leading edge of the input HSYNC pulse, as shown in Figure 3-8. Note the difference between the terms “leading edge” and “rising edge”, and “trailing edge” and “falling edge”.

Offset 400h[7:5] controls the position of the leading edge of the output HSYNC pulse with respect to the leading edge of the input HYSNC pulse. The leading edge of the output pulse may be delayed with respect to the leading edge of the input HYSNC pulse in increments of one DOTCLK. Table 3-6 details the amount of delay in DOTCLK increments for each setting of Offset 400h[7:5]; note that there is a skip in the otherwise logical order of increasing delays from 000 to 001.

Offset 400h[4:0] controls the position of the trailing edge of the output HSYNC pulse with respect to the leading edge of the input HYSNC pulse. The trailing edge of the output pulse may be delayed with respect to the leading edge of the input HYSNC pulse in increments of one DOTCLK. Table 3-6 details the amount of delay in DOTCLK increments for each setting of Offset 400h[4:0]; note that a setting of 00000 will result in no output pulse. Note also that with this scheme it is possible to erroneously program an output pulse whose trailing edge occurs before the leading edge! In such a case there will be no output pulse.

The polarity of the HSYNC output pulse may be controlled by Offset 404h[22], only if Offset 404h[26] = 1.

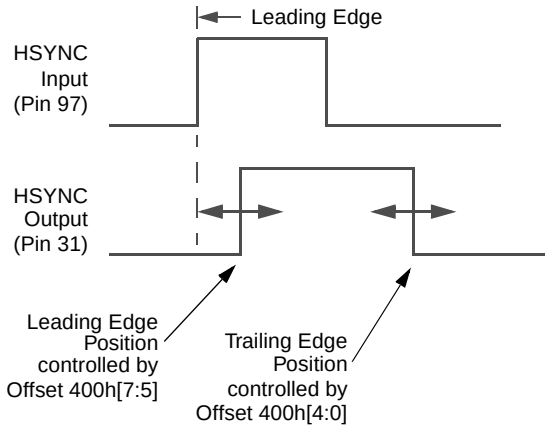


Figure 3-8. Control of HSYNC Output

Table 3-6. HSYNC Edge Position Control

HSYNC Leading Edge			HSYNC Trailing Edge							
Offset 400h[7:5]	No. of DOTCLK Delays		Offset 400h[4:0]	No. of DOTCLK Delays	Offset 400h[4:0]	No. of DOTCLK Delays	Offset 400h[4:0]	No. of DOTCLK Delays	Offset 400[4:0]	No. of DOTCLK Delays
000	0		00000	No Pulse	01000	8	10000	16	11000	24
001	2		00001	1	01001	9	10001	17	11001	25
010	3		00010	2	01010	10	10010	18	11010	26
011	4		00011	3	01011	11	10011	19	11011	27
100	5		00100	4	01100	12	10100	20	11100	27
101	6		00101	5	01101	13	10101	21	11101	29
110	7		00110	6	01110	14	10110	22	11110	30
111	8		00111	7	01111	15	10111	23	11111	31

Functional Description (Continued)

Frame Pulse (VSYNC)

VSYNC pulses are provided to the attached panel in one of two ways, either externally or internally. If the PASS_THRU mode is set (Offset 404h[30] = 1), the input FP_VSYNC (pin 99) is passed through unchanged to the output pin FLM/VSYNC (pin 33).

If the PASS-THRU mode is not set (Offset 404h[30] = 0), then the VSYNC/FLM pulse is generated internally in response to the input FP_VSYNC pulse. The manner in which the internal VSYNC/FLM pulse is generated depends on the mode set by Offset 404h[21:16].

If an SSTN panel is chosen, then the output FLM pulse is generated in response to each incoming FP_VSYNC.

If a DSTN panel is chosen, then the counter VPAN_SIZE (Offset 400h[26:16]) comes into play (see Table 3-8). The first FLM (First Line Marker) is generated at the beginning of the first line. Then the CS9211 counts the number of lines. A second FLM is generated when half number of total lines has been reached. This is required because in DSTN panels, both halves of the panel are receiving new lines of data simultaneously, thus a new FLM pulse is required when both halves of the panel have been simultaneously refreshed.

The polarity of the output VSYNC pulse may be inverted by Offset 404h[23] only if Offset 404h[24] = 1.

Shift Clock

Table 3-7 shows the relationship between the output shift clock (SHFCLK) and the input DOTCLK. This relationship varies depending on the panel type as selected by Offset 404h[21:18].

One additional bit exists to allow more control over the output shift clock. The Panel Shift Clock Retrace Activity Control bit at Offset 404h[27] allows the shift clock to be active only during active data transfer or free running as required by some panel types. In case of STN (DSTN/SSTN) modes, the panel shift clock retrace activity control bit does not have any effect.

Table 3-7. Input DOTCLK vs. Panel SHFCLK

Panel Clock	DSTN 24-Bit	DSTN 16-Bit	STN 8-Bit	TFT 9-Bit	TFT 18-Bit	TFT 9+9-Bit	TFT 12+12-Bit
SHFCLK	DOTCLK/4	DOTCLK/(3:2:3)	DOTCLK/(3:2:3)	DOTCLK	DOTCLK	DOTCLK/2	DOTCLK/2

Table 3-8. Panel Output Timing Selection Bits

Bit	Name	Description
Offset 400h-403h		**Panel Timing Register 1 (R/W)** — **Reset Value = 0000000h**
29	FP_HSYNC_POL	**FP_HSYNC Input Polarity**: Selects positive or negative polarity of the FP_HSYNC input (pin 97). Program this bit to match the polarity of the incoming FP_HSYNC signal. Note that bit 22 of Offset 404h independently controls the polarity of the output HSYNC. 0 = FP_HSYNC is normally low, transitioning high during sync interval (**Default**). 1 = FP_HSYNC is normally high, transitioning low during sync interval.
26:16	PAN_VSIZE	**Panel Vertical Size**: This field represents the panel vertical size in terms of scan lines. The value programmed should be equal to the panel size that is being connected. This can be used only for DSTN/STN modes. Example: 640x480 = 1E0h, 800x600 = 258h, and 1024x768 = 300h.
7:5	HSYNC_LEADING_EDGE	**Horizontal Sync Leading Edge Position**: Selects the position of the leading edge of the output HSYNC pulse with respect to the rising edge of the modified input HSYNC pulse. The modified input HSYNC pulse is that which has been inverted, or not inverted, by bit 29. The position is programmable in steps of 1 DOTCLK, starting at 2 DOTCLOCKS and extending up to 8. Bit 27 must be set in order for bits [7:5] to be recognized. Note that there are combinations of bits [7:5] and [4:0] that can result in a zero- or negative-length pulse, for example if the trailing edge is positioned before the leading edge. In this case, the output pulse will not be generated. 000 = No delay from the input HSYNC (**Default**). 001-111 = Position the HSYNC leading edge by 2 to 8 DOTCLKs with respect to the input HSYNC rising edge. Note that there is no setting for a position of 1 DOTCLOCK.

Functional Description (Continued)

Table 3-8. Panel Output Timing Selection Bits (Continued)

Bit	Name	Description
4:0	HSYNC_TRAILING_EDGE	**Horizontal Sync Trailing Edge Position**: Selects the position of the trailing edge of the output HSYNC pulse with respect to the rising edge of the modified input HSYNC pulse. The modified input HSYNC pulse is that which has been inverted, or not inverted, by bit 29. The position is programmable in steps of 1 DOTCLK, starting at 1 DOTCLOCK and extending up to 31. Bit 27 must be set in order for bits [4:0] to be recognized. Note that there are combinations of bits [7:5] and [4:0] that can result in a zero- or negative-length pulse, for example if the trailing edge is positioned before the leading edge. In this case, the output pulse will not be generated. 00000 = Does not generate the HSYNC pulse if bit 27 = 0. (**Default**). 00001 - 11111 = The HSYNC trailing edge position can be varied from 1 to 31 DOTCLKs with respect to the input HYSNC rising edge.
Offset 404h-407h		**Panel Timing Register 2 (R/W)** **Reset Value = 00000000h**
30	PASS_THRU	**Pass-Through**: Activates the Pass-Through mode. In Pass-Through mode, the input timing and the pixel data are passed directly onto the panel interface timing and the panel data pins to drive the panel; the internal CS9211 logic and timing is not used. In normal mode, Offset 400h[7:0], 404h[29], and 404h[27:24] are effective. 0 = Normal mode; output timing uses the logic and timing from the CS9211. 1 = Pass-Through mode; CS9211 internal timing logic functions are not used.
29	LDE_POL_SEL	**Display Timing Strobe Polarity Select**: Selects the polarity of the LDE pin (pin 32). This can be used for some TFT panels that require an active low timing LDE. 0 = LDE signal is active low (**Default**). 1 = LDE signal is active high.
27	PSH_CLK_CTL	**Panel Shift Clock Retrace Activity Control**: Programs the shift clock (SHFCLK, pin 30) to be either free running or active only during the display period. Some TFT panels recommend keeping the shift clock running during the retrace time. This bit has no effect in DSTN or SSTN modes. 0 = Shift clock is active only during active display period. 1 = Shift clock is free running during the entire frame period.
26	LP_HSYNC_SEL	**LP/HSYNC Select**: Selects the function of LP/HSYNC (pin 31). Set this bit based on the panel type connected. For DSTN or SSTN panels, set this bit to 0. For TFT panels, set this bit to 1. 0 = LP (output for DSTN/SSTN panel). 1 = HSYNC (output for TFT panel).
23	VSYNC_POL	**Vertical Sync Output Polarity**: Selects polarity of the output VSYNC signal (pin 33). This bit is effective only for TFT panels; for this bit to function, bit 24 must be set to 1. Note that Offset 400h[30] selects the polarity of the input HSYNC, whereas bit 23 selects the polarity of the output VSYNC. 0 = VSYNC output is active high. 1 = VSYNC output is active low.
22	HSYNC_POL	**Horizontal Sync Output Polarity**: Selects polarity of output HSYNC signal (pin 31). This bit is effective only for TFT panels; for this bit to function, bit 26 must be set to 1. Note that Offset 400h[29] selects the polarity of the input VSYNC, whereas bit 22 selects the polarity of the output HSYNC. 0 = HSYNC output is active high. 1 = HSYNC output is active low.
13	CONT_LPS	**Continuous Line Pulses**: This bit selects whether line pulses are continuously output or are output only during the active display time. In most cases, DSTN panels require continuous line pulses (LPs). This bit will have no effect if the CS9211 is set to TFT mode. 0 = Continuous line pulses. 1 = Line pulses during the display time only.

Functional Description (Continued)

3.2.4 Frame Rate Modulation

The Frame Rate Modulation (FRM) scheme is the heart of the CS9211. Frame Rate Modulation cannot be turned off but it can be modified through certain programming registers and internal memories.

Each pixel on an LCD panel consists of three primary color components: red, green, and blue. Each primary color component, for a given pixel, can either be turned on or turned off; there are no intermediate intensities. A total of eight colors can be generated for a given pixel through various combinations of turning each color component on or off. In order to generate more colors, Frame Rate Modulation (and dithering) is used. The idea behind Frame Rate Modulation is to turn each primary color component of a pixel on and off a certain fraction of the time to create the perception of intensities between fully off and fully on.

For example, imagine a pixel whose blue and green color components are always off. If the pixel's red color component was also always off, the pixel would be black. If the pixel's red color component was always on, the pixel would be the brightest red. If the red color component was blinking on and off for equal intervals, then the pixel would look about half as bright as the brightest red. Use of intervals other than 50%-on/50%-off will yield other intensities between black and fully bright. Assuming the blink rate is sufficiently fast, a viewer's eye would integrate the intensity of a modulated pixel to perceive intensities between fully off (black) and fully on (bright red).

The FRM algorithm in the CS9211 uses 64-frame-long sequences to determine when to turn the red, green, and blue pixel color components on and off. (A frame is one complete image on a panel.) The sequence repeats itself every 64 frames. The CS9211 contains one 64-bit x 32-bit FRM memory for each of the three primary pixel colors, red, green, and blue. These three memories can be programmed simultaneously or individually. Each of the three memories holds up to 32 different modulation sequences, therefore 32 different intensities for each primary color component can be generated by Frame Rate Modulation. The memory values can be set to provide any intensity variation to accommodate the properties of different LCD panels, but for best results, successive values should increase monotonically.

The number of discrete intensities is chosen with Offset 40Ch[6:4] (see Table 3-9). These bits determine how many of the most significant bits of each pixel value for each color component will be used by the FRM algorithm to generate the base intensities. FRM can use 5-bit to 1-bit schemes in order to share the 6-bit input. If a 5-bit FRM scheme is used, there are 2^5 (32) base intensities (prior to dithering). If a 1-bit scheme is used, only 2^1 (2) intensities are available, with the first 16 intensities having one bit sequence and the next 16 intensities using the other bit sequence.

Table 3-9. Frame Rate Modulation Control Bit

Bit	Name	Description
Offset 40Ch-40Fh		**Dither and Frame Rate Control Register (R/W)** **Reset Value = 00000000h**
6:4	NO_OF_FRM INTENSITIES	**Number Of FRM Intensities**: The value set by bits [6:4] is the number of intensities that will exist due to Frame Rate Modulation, prior to dithering. This field selects how many of the incoming most significant data bits (per color) are used to generate the FRM intensities. 000 = 2 FRM intensities (selects 1 MS (most-significant) bit for use by FRM). 001 = 4 FRM intensities (selects 2 MS bits for use by FRM). 010 = 8 FRM intensities (selects 3 MS bits for use by FRM). 011 = 16 FRM intensities (selects 4 MS bits for use by FRM). 100 = 32 FRM intensities (selects 5 MS bits for use by FRM). 101, 110, 111 = Reserved.

Functional Description (Continued)

Table 3-10 is an example of one of the three 32 x 64 FRM-Sequence tables that is addressed by the most significant bit of the incoming pixel value. The ”n” most-significant bits (as chosen by Offset 40Ch[6:4]) of each color component of each incoming pixel looks up one of the 64-bit words from this table. The number of 1’s in each 64-bit word determines how bright the pixel will be when that word is chosen. A word with all zeros will never illuminate the given pixel in that color, therefore the pixel will be black. A word with only one “1” will illuminate the given pixel one frame out of 64, so the pixel will be as dim as possible without being off entirely. A word with 10 “1”s will illuminate the given pixel 10 frames out of 64. A word with 64 “1”s will illuminate the given pixel in each of the 64 frames, so that pixel will be as bright as possible.

The Freq (frequency ratio) indicates the number of 0 to 1 transitions within 64 frames. This value multiplied by the refresh rate will give the frequency of frame rate modulation of a particular intensity. Higher frequency frame rate modulation will result in better picture quality. The Int (intensity) column indicates the duty cycle of the primary color.

The intensity level of this FRM table starts from 0/64 and gradually increases to 16/64 instead of jumping directly to 16/64. It seems that the human eye is less sensitive to frequency variation at low intensity. As the intensity level increases, it increases slowly from 16/64 to 48/64 to create a smooth transition of intensities. The full scale intensity level is truncated at 48/64 intentionally; above this point the differences between levels start to become visible. There is a trade-off between maximum intensity level and smooth gradations of color.

The generation of FRM tables suitable for driving a particular display panel in a particular application requires a good understanding of human vision and significant experimentation. Good candidate patterns for these tables will have 1’s separated by equal numbers of 0’s throughout the word, instead of clumping all the 1’s together in a particular location. Successive values should increase monotonically. All three tables may be identically or individually programmed.

Table 3-10. Example FRM RAM Table for One Color Component

Col	Frame Count from 0 to 63	Freq	Int
0	00000000,00000000,00000000,00000000,00000000,00000000,00000000,00000000	0/64	0/64
1	00000000,00000000,00000000,00000000,00000000,00000000,00000000,00000000	0/64	0/64
2	00000001,00000001,00000001,00000001,00000001,00000001,00000001,00000001	8/64	8/64
3	00000010,00001000,00010000,01000001,00000010,00001000,00010000,01000001	10/64	10/64
4	00010001,00010001,00010001,00010001,00010001,00010001,00010001,00010001	16/64	16/64
5	00010010,01001001,00100100,10010010,01001001,00100100,10010010,01001001	21/64	21/64
6	00100100,10010100,10010010,01010010,01001010,01001001,00101001,00100101	23/64	23/64
7	00100101,00100101,00100101,00100101,00100101,00100101,00100101,00100101	24/64	24/64
8	00100101,00101001,01001001,01001010,01010010,10010010,10010100,10100101	25/64	25/64
9	00101001,01001010,01010010,10010101,00101001,01001010,01010010,10010101	26/64	26/64
10	00101001,01010010,10100101,00101010,01010100,10100101,01001010,10010101	27/64	27/64
11	00101010,01010101,00101010,01010101,00101010,01010101,00101010,01010101	28/64	28/64
12	00101010,10010101,01010010,10101010,01010101,01001010,10101001,01010101	29/64	29/64
13	00101010,10101010,01010101,01010101,00101010,10101010,01010101,01010101	30/64	30/64
14	00101010,10101010,10101010,10101010,01010101,01010101,01010101,01010101	31/64	31/64
15	01010101,01010101,01010101,01010101,01010101,01010101,01010101,01010101	32/64	32/64
16	01010101,01010101,01010101,01010101,10101010,10101010,10101010,10101011	31/64	33/64
17	01010101,01010101,10101010,10101011,01010101,01010101,10101010,10101011	30/64	34/64
18	01010101,01101010,10101101,01010101,10101010,10110101,01010110,10101011	29/64	35/64
19	01010101,10101011,01010101,10101011,01010101,10101011,01010101,10101011	28/64	36/64
20	01010110,10101101,01011010,11010101,10101011,01011010,10110101,01101011	27/64	37/64
21	01010110,10110101,10101101,01101011,01010110,10110101,10101101,01101011	26/64	38/64
22	01011010,11010110,10110110,10110101,10101101,01101101,01101011,01011011	25/64	39/64
23	01011011,01011011,01011011,01011011,01011011,01011011,01011011,01011011	24/64	40/64
24	01011011,01101011,01101101,10101101,10110101,10110110,11010110,11011011	23/64	41/64
25	01011011,01101101,10110110,11011011,01011011,01101101,10110110,11011011	22/64	42/64
26	01101101,10110110,11011011,01101101,10110110,11011011,01101101,10110111	21/64	43/64
27	01101101,10110111,01101101,10110111,01101101,10110111,01101101,10110111	20/64	44/64
28	01101101,11011011,01110110,11011101,10111011,01101110,11011011,10110111	19/64	45/64
29	01101110,11011101,10111011,01110111,01101110,11011101,10111011,01110111	18/64	46/64
30	01101110,11101110,11011101,11011101,10111011,10111011,01110111,01110111	17/64	47/64
31	01110111,01110111,01110111,01110111,01110111,01110111,01110111,01110111	16/64	48/64

Functional Description (Continued)

3.2.4.1 Removal of Flickering

One side effect of frame rate modulation is flickering. If a large group of pixels on an LCD panel were the exact same intensity, and all of the pixels in this large group were blinking on and off together in synchronization, the flickering effect would be detectable by the human eye. The CS9211 removes detectable flickering by de-synchronizing adjacent pixels so that they do not blink on and off at the same time.

The de-synchronization is implemented by using two linear feedback shift registers (LFSR) to randomize the switching sequences of each individual pixel on the display. A 15-bit LFSR, which is advanced every pixel clock, is used to generate global randomization. A 9-bit LFSR, which is advanced every HSYNC, is used to generate local randomization. Both LFSRs are reset every frame. The addition of the lower 6 bits of these two LFSRs gives each pixel a pseudo-randomized index into the chosen 64-bit word of the corresponding FRM RAM Table. Using this index and frame count, every pixel on the display starts the switching sequence from 1 of the 64 possible positions pseudo-randomly and completes one sequence in 64 frames.

In order to randomize the switching sequence further, each primary color FRM RAM Table has an independent 15-bit LFSR, with its own seed value. These seed values are fully programmable. The only side effect of this implementation is motion artifacts on the display, which is common in FRM implementations. As long as the refresh rate of the LCD panel is high, this effect should not be noticeable.

3.2.5 FRM Memory

The three 32 x 64 FRM memories are programmed through the serial interface. There is one separate FRM look-up table for each primary color (R, G, and B). Table 3-11 shows the registers used to program the FRM RAM tables. The FRM RAM tables can be programmed either individually or all together using the register Offset 418h[9:8]. Register Offset 418h[5:0] is used to select the initial FRM RAM index, which automatically increment with each read or write operation. Register Offset 41Ch[31:0] is used to access the actual FRM RAM data. Two 32-bit register accesses are required to fill one 64-bit FRM RAM location.

Table 3-11. FRM Memory Access Control Bits

Bit	Name	Description
Offset 418h-41Bh		**FRM Memory Index Register (R/W)** — **Reset Value = 00000000h**
9:8	RGB_SEL	**RGB Memory (FRM RAM) Select:** Allows reading or writing to individual R,G, and B memory FRM RAM locations or writing to all of them at the same time. 00 = Read from R FRM RAM but write to RGB FRM RAM. 01 = read or write to R FRM RAM. 10 = Read or write to G FRM RAM. 11 = Read or write to B FRM RAM. **Note:** All FRM RAMs can be accessed through the serial interface before the panel is powered up.
5:0	FRM_INDEX	**FRM Memory Index:** This auto-incrementing value represents the index to the FRM RAM. Each RAM is configured as 32x64, requiring two index values to update each row of FRM RAM. For example, the 00h index value will update the 32 LSB's of row "0" FRM RAM and the 01h index value will update the 32 MSB's of row "0" FRM RAM. To update the entire RAM location, the index is programmed only once with the starting value, "00". This is used inside the CS9211 to auto increment the FRM RAM locations for every FRM RAM data access using the Offset 41Ch.
Offset 41Ch-41Fh		**FRM Memory Data Register** — **Reset Value = 00000000h**
31:0	FRM_DATA	**FRM Memory Data Register**: This 32-bit data represents FRM RAM data to be read or written to the FRM RAM table in accordance to the RGB_SEL (Offset 418h[9:8]) and the index value (Offset 418h[5:0]).

Functional Description (Continued)

3.2.6 Dithering

Dithering creates intermediate color intensities by mixing available colors. Human vision sees an average of the intensities of adjacent pixels on a screen. Although dithering provides additional shades, it does so by sacrificing spatial resolution.

3.2.6.1 Theory Of Dithering

The number of colors that a given panel displays can be enhanced beyond the intensity combinations generated by frame rate modulation by way of a technique called dithering. The drawback is that fine spatial details are lost in this process, and boundaries between regions of differing color intensities become blurred.

For example, consider just the red color component of a 2x2 square of pixels. If the only two options for the red color component were to be turned on or off, there would be only two colors, black and the brightest red. However, if two of the pixels' red color components in the 2x2 square were turned on and two were turned off, the human eye would blend these adjacent pixels and the 2x2 pixel square would appear to be half as bright as the brightest red.

This process is illustrated in Figure 3-9. Suppose each pixel in a 2x2 square had 6 bits of data associated with it. The frame rate modulator is using the upper four most significant bits, so the lower two bits would be lost or truncated without the support of the dithering process. Consider the arbitrary 6-bit pixel value 38h = 11_1000; the upper four bits of 38h are 1110, which in hex is "E". Without dithering, pixel values 39h (11_1001), 3Ah (11_1010), and 3Bh (11_1011) would all be displayed the same as pixel value 38h (11_1000), since the upper four bits are the same for each value ("E"). Since pixel value 3Ch (11_1100) has a different set of upper four bits (1111 instead of 1110), 3Ch would appear brighter than 38h. So, without dithering, it would seem that the panel could accurately display only pixel values 38h and 3Ch. When the two LSBs are removed, these become values Eh and Fh, respectively.

Dithering provides a means of displaying the "missing" values 39h, 3Ah, and 3Bh, by displaying combinations of the values the panel is able to display in a 2x2 square. The average intensity of the pixels in the 2x2 square becomes the intensity of the 'missing' values, as illustrated in Figure 3-9. In order to leave room at the top of the intensity scale, value 3Bh is passed through unchanged, and values 38h, 39h, and 3Ah are modified by the dither algorithm.

One of four dither patterns are chosen by the two LSBs, bolded below the "Case n" text in Figure 3-9. A zero in the dither pattern (middle column of Figure 3-9) indicates the input value will be passed through unchanged. A one in the dither pattern indicates the displayed value should be decremented to the next available intensity value.

In Case 1) of Figure 3-9, all four pixels want to be value 38h, which is no problem for the panel since 38h (or Eh) is one of the values it can display directly. However, the dither pattern contains three ones, so three of the pixels in this square are dithered down to the next available brightness, "Dh". In Case 2), all four pixels want to be intensity 39. Two pixels are dithered down to intensity "Dh", and two are passed through unchanged as Eh. In Case 3) , selected by dither bits 10, only one pixel is dithered down to brightness Dh, and the other three pass through unchanged. In Case 4), the dither pattern contains all zeros, so the value Eh is passed through unchanged for all four pixels in the 2x2 square. Moving from Case 1 to Case 4, one less pixel is dithered down in each case In Case 5), the sequence begins again with the next-brightest intensity, Eh, being the one that is dithered-down to.

3.2.6.2 Pre-Programmed Dither Patterns (ROM)

The example discussed with reference to Figure 3-9 is 2-bit dithering. In 2-bit dithering, four patterns are used, as shown in Cases 1-4.

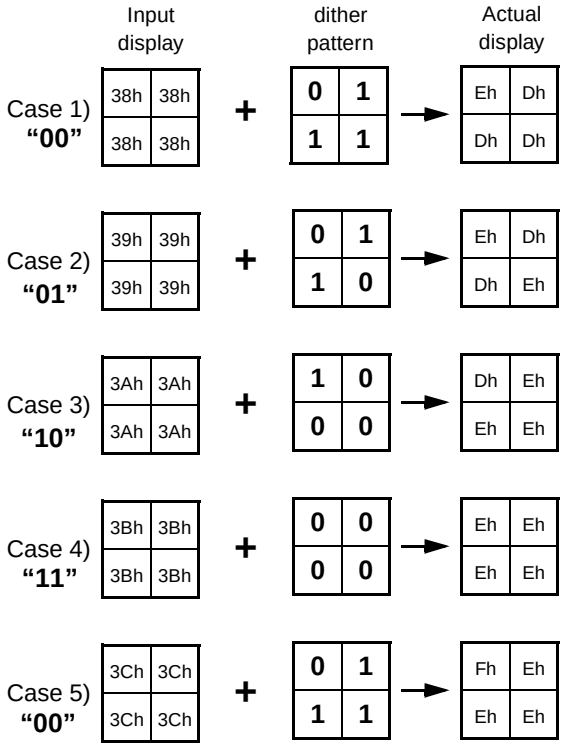


Figure 3-9. Effect of Two-Bit Dithering

Cases 1-4 can be redrawn as a single picture. Refer to the dark outlined 2x2 box contained within the 8x8 pixel pattern on the "2-bit scheme" in Figure 3-10. The numbers in the pixels indicate the value of the lower two bits: 00 = blank, 01 = "1", 10 = "2", and 11 = "3". When the value is "00", only the pixel shown as blank will retain the input color intensity. The other three pixels will be decremented to the next available intensity value. As the lower two bits of any intensity value increase from 00 to 01, the pixel labeled "1" will retain the input value and the other two will be decremented to the next available intensity. When the lower two bits are 10 ("2"), then the pixel labeled "2" will also retain the input value, and the remaining one pixel will be decremented to the next available intensity. When the lower two bits are 11 ("3"), then all four pixels retain the input value.

Functional Description (Continued)

Figure 3-10 shows the order in which pixels will be dithered down to the next available intensity, as the least significant bits increase from “0”, for 1-, 2-, 3-, and 4-bit dithering.

The values are given in hexadecimal. The CS9211 also supports 5-bit dithering but that pattern is not shown.

The patterns shown in Figure 3-10 are stored in the CS9211’s internal ROM. These patterns will be used when the dither ROM is selected by Offset 40Ch[12] = 0.

3.2.6.3 Controlling Dithering

Table 3-13 "Dithering Programming Bits" on page 32 indicates the register settings used to control the dithering process.

The incoming pixel data goes through the dithering logic. Dither logic is enabled by writing a “1” to Offset 40Ch[0]. If the dithering logic is disabled, then only FRM will be producing the color intensities. FRM cannot be turned off.

The first step in setting the registers is to decide how to split the incoming bits per pixel between bits used for FRM and bits used for dithering. Offset 40Ch[6:4, 3:1] determines these settings; these two groups of bits must be set to match each other.

Next, the user must decide whether to use the pre-programmed (ROM) internal dithering patterns or create new ones in the dither RAM. If RAM will be used, program Offset 40Ch[12] and Offset 424h[7:6] accordingly. If pre-programmed dither patterns (ROM) will be used, the dither RAM will go into a reduced power state when it is deselected by Offset 40Ch[12] = 0 and Offset 424h[7:6] = 00.

F	7	D	5	F	7	D	5
3	B	1	9	3	B	1	9
C	4	E	6	C	4	E	6
	8	2	A		8	2	A
F	7	D	5	F	7	D	5
3	B	1	9	3	B	1	9
C	4	E	6	C	4	E	6
	8	2	A		8	2	A

4-Bit Scheme

1	5	2	6	1	5	2	6
7	3		4	7	3		4
2	6	1	5	2	6	1	5
	4	7	3		4	7	3
1	5	2	6	1	5	2	6
7	3		4	7	3		4
2	6	1	5	2	6	1	5
	4	7	3		4	7	3

3-Bit Scheme

3	1	3	1	3	1	3	1
	2		2		2		2
3	1	3	1	3	1	3	1
	2		2		2		2
3	1	3	1	3	1	3	1
	2		2		2		2
3	1	3	1	3	1	3	1
	2		2		2		2

2-Bit Scheme

1		1		1		1	
	1		1		1		1
1		1		1		1	
	1		1		1		1
1		1		1		1	
	1		1		1		1
1		1		1		1	
	1		1		1		1

1-Bit Scheme

Figure 3-10. N-Bit Dithering Pattern Schemes

Functional Description (Continued)

3.2.7 User-defined Dither Patterns

The CS9211 allows the user to define custom dither patterns, should the pre-programmed patterns prove to be insufficient. As shown in Table 3-13, this memory is accessed through Offset 424h (control and address) and 428h (data).

The dither RAM structure is 32 columns x 64 rows, in which each column represents one 8x8 dither pattern matrix, like one of the matrices shown in Figure 3-10. The first row of the 8x8 matrix goes into rows 0 - 7 of the appropriate column, with the left-most bit going into row 0 or the column, and the right-most bit going into row 7 of the column. The second row goes into rows 8-15 of the same column, and so on until the eighth row of the 8x8 matrix goes into rows 48-63 of the column. This structure is illustrated in Figure 3-11.

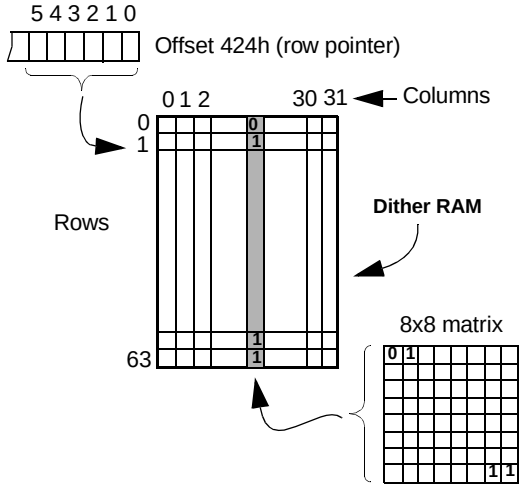


Figure 3-11. Dither Ram Structure

The dither RAM is loaded row by row, not column by column, so the user must write out each matrix in a column, then convert the resulting rows to the data to be loaded, via Offset 424h and 428h. Offset 424 points to the row to be loaded, and offset 428h supplies the data to the row.

Looking back at Figure 3-9, it is apparent that the dither patterns associated with Cases 1) and 3) are logical inverses of each other, thereby precluding the need to store both of them in the RAM. Data is read back from the dither RAM either inverted or non-inverted, according to the MSB of the dither bits. If the MSB of the dither bits is one, data will be read from the dither RAM as inverted data. The user who chooses to define custom dither patterns must maintain inverse dither pattern pairs or else their patterns will not work correctly.

Table 3-12 indicates which 8x8 matrices go into which columns of the dither RAM. The entries in Table 3-12 are a fractional form of notation employed to identify the matrix. As shown in Figure 3-10, the 8x8 matrices are made up of smaller matrices that are replicated to fill out the 8x8 matrix. The notations in Table 3-12 refer to the smaller matrices (sub-matrices) from which the 8x8 matrices are built.

The fractional notation in Table 3-12 identifies a smaller matrix (sub-matrix) by using a denominator which refers to the number of squares in the sub-matrix, and a numerator which refers to the number of “1” entries in a given matrix. Thus the notation “7/8” refers to a 2 x 4 matrix (from the 3-bit dithering scheme) which contains 7 ones.

Table 3-12 does not contain all possible ‘fractional’ entries for a given dithering scheme. For instance, in the 3-bit schemes, there is no entry for the “1/8” matrix. The “1/8” matrix (being a 2x4 matrix which contains a single 1) would be the logical inverse of the “7/8” matrix, hence, storing the 1/8 matrix is unnecessary. Similarly, the “2/8” matrix is the inverse of the “6/8” matrix, and the “3/8” matrix is the inverse of the “5/8” matrix. The matrices that are not stored directly are accessed when the most-significant dither bit is a 1. An exception is the “0/n” matrix, which contains no ones. It is stored in INVERSE FORM in column 0, since there is no stored “n/n” matrix to read the inverse of. The “I” after any fractional designation in the column 0 and 16 entries entries of Table 3-12 indicates this matrix should be stored in inverse form.

Table 3-12. Dither RAM Column Usage

Column	Number of Dither Bits				
	1	2	3	4	5
0	0/2 I	0/4 I	0/8 I	0/16 I	0/32 I
1					
2					31/32
3					
4				15/16	30/32
5					
6					29/32
7					
8			7/8	14/16	28/32
9					
10					27/32
11					
12				13/16	26/32
13					
14					25/32
15					
16		3/4 I	6/8 I	12/16 I	24/32 I
17					
18					23/32
19					
20				11/16	22/32
21					
22					21/32
23					
24			5/8	10/16	20/32
25					
26					19/32
27					
28				9/16	18/32
29					
30					17/32
31	1/2	2/4	4/8	8/16	16/32

Functional Description (Continued)

Table 3-13. Dithering Programming Bits

Bit	Name	Description
Offset 40Ch-40Fh		**Dither and Frame Rate Control Register (R/W)** **Reset Value = 00000000h**
12	DITHER_RAM_ROM_SEL	**Dither RAM or ROM Select**: This bit selects either internal ROM or internal RAM as the source of the dither patterns. 0 = Selects fixed (internal to CS9211) ROM for dither patterns (**Default**). 1 = Selects programmable (internal to CS9211) RAM for dither patterns. To update the dither RAM, this bit must = 1. **Note:** See Offset 424h[6].
6:4	NO_OF_FRM INTENSITIES	**Number Of FRM Intensities**: The value set by bits [6:4] is the number of intensities that will exist due to Frame Rate Modulation, prior to dithering. This field selects how many of the incoming most significant (MS) data bits (per color) are used to generate the FRM intensities . 000 = Two FRM intensities (selects 1 MS (most significant) bit for use by FRM). 001 = Four FRM intensities (selects 2 MS bits for use by FRM). 010 = Eight FRM intensities (selects 3 MS bits for use by FRM). 011 = Sixteen FRM intensities (selects 4 MS bits for use by FRM). 100 = Thirty two FRM intensities (selects 5 MS bits for use by FRM). 101, 110, 111 = Reserved.
3:1	DITH_BITS	**Dithering Bits Select**: This field is used to select the number of bits to be used for the dithering pattern. Dither bits are the least-significant bits of each pixel's color value. 000 = Reserved 001 = Selects 5 bits as dither bits. Number of FRM intensities should be 2 (i.e., bits [6:4] = 000). 010 = Selects 4 bits as dither bits. Number of FRM intensities should be 4 (i.e., bits [6:4] = 001). 011 = Selects 3 bits as dither bits. Number of FRM intensities should be 8 (i.e., bits [6:4] = 010). 100 = Selects 2 bits as dither bits. Number of FRM intensities should be 16 (i.e., bits [6:4] = 011). 101 = Selects 1 bit as a dither bit. Number of FRM intensities should be 32 (i.e., bits [6:4] = 100).
0	DITH_ENB	**Dithering Enable**: Enable/disable dithering. The dither bit must be enabled in order for dither RAM reads or writes to occur. When this bit is cleared, the internal dither RAM is powered down. 0 = Dither disable - The dithering function is turned off. When the dither is disabled, dither bits [3:1] do not have any effect and the dither RAM is not accessible. 1 = Dither enable. The dither functions with the number of dither bits as set in [3:1]
Offset 424h-427h		**Dither RAM Control and Address Register** **Reset Value = 00000000h**
7	DITHER_RAM_ACCESS	**Dither RAM Access Bit**: Allows reads and writes to and from dither RAM. 0 = Disable (Do not allow reads or writes). 1 = Enable (Allow reads and writes). To perform dither RAM reads and writes, bits 7 and 6 must be set to 1. In addition, Offset 40Ch bits 12 and 0 must be set to 1. If any of these bits are not set to 1, the RAM goes into power-down mode.
6	DITHER_RAM_UPDT	**Dither RAM Update**: This bit works in conjunction with bit 7. If this bit is enabled, it allows the data to update the RAM. 0 = Disable (do not allow dither RAM access). 1 = Enable (allow dither RAM access). To perform dither RAM reads and writes, bits 7 and 6 must be set to 1. In addition, Offset 40Ch bits 12 and 0 must be set to 1. If any of these bits are not set to 1, the RAM goes into power-down mode.
5:0	DITHER_RAM_ADDR	**Dither RAM Address**: This 6-bit field specifies the address to be used for the next access to the dither RAM. Each access to the data register automatically increments the RAM address register. If non-sequential access is made to the dither RAM, the address register must be reloaded before each non-sequential data block.
Offset 428h-42Bh		**RAM Data Register (R/W)** **Reset Value = 00000000h**
31:0	RAM_DATA	**RAM Data**: This 32-bit field contains the read or write data for the RAM access.

Functional Description (Continued)

3.2.8 CRC Signature

The CS9211 contains hardware logic that performs Cyclical Redundancy Checks (CRCs) on the panel data digital pipeline, using the polynomial $1 + x^3 + x^4 + x^{24}$. This feature is used for error detection during silicon and design validation and makes it possible to capture a unique 24-bit signature for any given mode setup. An error in the dither/FRM pixel pipeline will produce a different signature when compared to a known good signature value. Various logic blocks can be configured, as shown in Table 3-14. This allows the programmer to quickly and accurately test data processing without having to look for incorrect pixels on the screen. In the FRM block test, each frame will produce a different signature in a sequence, which repeats after 64 frames. The signature and the corresponding frame count can be read from the register Offset 42Ch. Table 3-15 shows the bit formats for the register that controls this feature, and Figure 3-12 shows a simple block diagram.

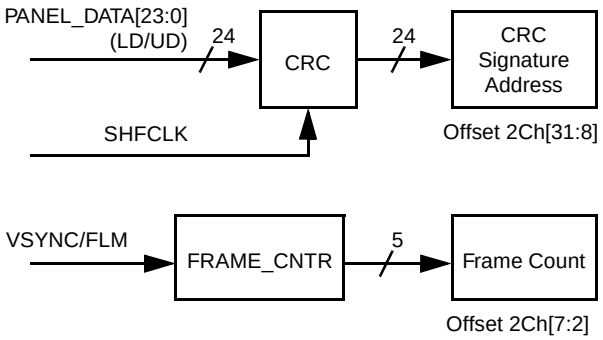


Figure 3-12. CRC Data Path

Table 3-14. Logic Functions Affecting the CRC

Dither Enable for TFT/DSTN/SSTN	Bypass Dither for TFT/DSTN/SSTN	FRM Enable for DSTN/SSTN	FRM Bypass for DSTN/SSTN	Bypass CS9211
Offset 40Ch[6:0] 000,001,1 001,010,1 010,011,1 011,100,1 100,101,1 101,XXX,X	Offset 40Ch[6:0] 101,XXX,X	Changes with the Frame Count (0 to 31) Note: Generates the signature (Offset 42Ch[31:8]) for a given frame count (Offset 42Ch[7:2])	LFSR = 00 FRM_RAM Contents = all 0's	Offset 404h[30] = 1

Table 3-15. Panel CRC Signature Register

Bit	Name	Description
Offset 42Ch-42Fh		**Panel CRC Signature Register (R/W)** **Reset Value = xxxxxxxxh**
31:8	SIG_DATA	**Signature Address (Read Only)**: 24-bit signature data for dither logic or FRM logic.
7:2	FRAME_CNT	**Frame Count**: Represents the frame count, which is an index for the generated signature for that frame.
1	SGFR	**Signature Free Run**: The value of this bit during the first cycle of a frame determines whether a signature will be generated for that frame. If this bit is kept high, with signature enabled (bit 0 = 1), the signature generator captures data continuously across multiple frames. Changing this bit from high-to-low causes the signature generation process to stop after the current frame. 0 = Do not capture signature during next frame. 1 = Capture signature during next frame.
0	SIG_EN	**Signature Enable**: Enables/disables signature capture. 0 = Disable; 1 = Enable.

Functional Description (Continued)

Table 3-16 provides the mapping for the panel data bits as inputs to the CRC.

Where:

RU1/BU1/GU1 -> pixel 1
RU2/GU2/BU2 -> pixel 2

and so on for the Upper Display from line 1 to line 240 of a 640x480 panel, and

RL1/GL1/BL1 -> pixel 1
RL2/GL2/BL2 -> pixel 2

and so on for the Lower Display from line 241 to line 480.

Panel selection is done through the register bits at Offset 404h[18:16]. The selection of these bits generates the desired SHFCLK from the pixel clock, based on the panel type selected, and steers the internal pixel bus onto the panel interface data pins (the LD and UD groups in Table 3-4). All unused pins are driven with 0's.

This panel data is sent to the CRC signature generator.

The CRC value varies for each panel configuration for a fixed on-screen image.

Table 3-16. Mapping of Panel Data as CRC Input

CRC Input (LD/UD)	DSTN 24-Bit, Offset 404h[18:16] = 010	DSTN 16-Bit, Offset 404h[18:16] = 001			SSTN 8-Bit, Offset 404h[18:16] = 011			TFT, Offset 404h[18:16] = 010
		1st Input to CRC	2nd Input to CRC	3rd Input to CRC	1st Input to CRC	2nd Input to CRC	3rd Input to CRC	
bit[0]	BU4	0	0	0	0			0
bit[1]	GU4	0	0	0	0			0
bit[2]	RU4	0	0	0	0			B0
bit[3]	BU3	0	0	0	0			B1
bit4]	GU3	GU3	RU6	BU8	G3	R6	B8	B2
bit[5]	RU3	RU3	BU5	GU8	R3	B5	G8	B3
bit[6]	BU2	BU2	GU5	RU8	B2	G5	R8	B4
bit[7]	GU2	GU2	RU5	BU7	G2	R5	B7	B5
bit[8]	RU2	0	0	0	0			0
bit[9]	BU1	0	0	0	0			0
bit[10]	GU1	RU2	BU4	GU7	R2	B4	G7	G0
bit[11]	RU1	BU1	GU4	RU7	B1	G4	R7	G1
bit[12]	BL4	GU1	RU4	BU6	G1	R4	B6	G2
bit[13]	GL4	RU1	BU3	GU6	R1	B3	G6	G3
bit[14]	RL4	GL3	RL6	BL8	0			G4
bit[15]	BL3	RL3	BL5	GL8	0			G5
bit[16]	GL3	0	0	0	0			0
bit[17]	RL3	0	0	0	0			0
bit[18]	BL2	BL2	GL5	RL8	0			R0
bit[19]	GL2	GL2	RL5	BL7	0			R1
bit[20]	RL2	RL2	BL4	GL7	0			R2
bit[21]	BL1	BL1	GL4	RL7	0			R3
bit[22]	GL1	GL1	RL4	BL6	0			R4
bit[23]	RL1	RL1	BL3	GL6	0			R5

Functional Description (Continued)

3.2.9 Simultaneous Display

The problem with displaying pixel data to both a CRT screen and a DSTN panel at the same time is that horizontal scan lines in both the upper and lower halves of a DSTN panel screen must be written at the same time. This differs from the order that pixel data is written to a CRT screen, where the pixel data for one horizontal scan line at a time is written to the screen, starting with the scan line at the top of the screen and ending at the bottom of the screen.

Designs which incorporate the CS9211 are able to support simultaneous display with a DSTN panel and CRT. The CS9211 stores DSTN pixel data in the external frame buffers, and then reorders the pixel data stream to include pixel data for both the upper and lower halves of the screen before sending the data out to the panel. The data in the frame buffer has already been frame-rate-modulated and/or dithered, if necessary, and packed as three bits per pixel.

Simultaneous display is supported only with the panel and CRT in the same mode and refresh rate. In this mode, the refresh rate should be set as high as possible while maintaining compatibility with established monitor timing standards.

3.2.10 Maximum Frequency

The CS9211 will operate at a DOTCLK frequency of up to 65 MHz. There is no minimum frequency for the CS9211 device; however, many flat panels have signal timings that require minimum frequencies. Refer to the flat panel display manufacturer's specifications as appropriate.

3.2.11 Memory Controller

To support DSTN panels, the CS9211 memory interface must be connected to a DRAM in either EDO (Extended Data Out) or SDRAM format. This DRAM is used to store a DSTN-formatted copy of the frame buffer. Pixel data is received by the pixel port, formatted by the Frame Rate Modulator and dither block, and then stored in the frame buffer. The formatted pixel data is subsequently read from the memory and used to refresh the DSTN panel. Table 3-17 shows the registers associated with programming the memory controller.

Table 3-17. Memory Controller Programming Registers

Bit	Name	Description
Offset 404h-407h		**Panel Timing Register 2 (R/W)** — **Reset Value = 00000000h**
31	HIGH_RESOL_MCLK	**High Resolution MCLK**: Selects the MCLK frequency in terms or the DOTCLK frequency. This bit should be programmed as "0" for all the DSTN panels with resolutions up to 800x600, where the memory clock is the same as the DOTCLK. This should be set to "1" for the 1024x768 DSTN panel to run the memory clock at two-thirds the rate of the DOTCLK. 0 = Memory clock runs at the same frequency as DOTCLK. 1 = Memory clock runs at two-thirds the frequency of the DOTCLK.
Offset 420h-423h		**Memory Control Register** — **Reset Value = 1EF80008h**
4	EDO_LATE	**EDO DRAM Late Latch Bit**: When this bit is set, the data is latched into the CS9211, one clock after the data arrives from the DRAM. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. This bit is effective only if EDO RAM is used, as selected by bit 0 = 0. 0 = Latch the data with no delay. 1 = Latch the data with a delay of one clock.
3	EDO_EDGE_SEL	**EDO Data Latch Edge Select**: This bit controls which clock edge is used to latch data. When this bit is set, the data from the DRAM is latched into the CS9211 on the negative edge of the memory clock. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. This bit is effective only if EDO RAM is used, as selected by bit 0 = 0. 0 = Latch on positive (rising) edge. 1 = Latch on negative (falling) edge.
2	SDRAM_LD	**SDRAM Load Bit**: SDRAM Load Mode Register. When enabled, this bit activates RAM refresh. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = Disable; 1 = Enable.
1	SDRAM_CLK_INVERT	**SDRAM Clock**: Inverts the clock to the SDRAM interface. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = Use inverted clock. 1 = Use non-inverted clock.
0	SDRAM_EDO	**SDRAM or EDO**: Selects external frame buffer memory type. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = EDO; 1 = SDRAM.

Functional Description (Continued)

3.2.12 Power Sequence Control

The CS9211 contains a power-sequence controller that manages the application of the power and control voltages to the panel in a specified order compatible with most panel types. Table 3-18 shows the register control bits for power sequencing and Figure 3-13 on page 37 identifies the power sequence and the various delays.

Four panel power control functions are managed by the CS9211's power sequence controller. With reference to Figure 3-13, these are:

1) FP_VDDEN, Flat Panel VDD Enable: This signal is designed to enable the basic panel power VDD. It is intended that this signal be connected to a power FET or similar switching device (either internal to the panel or not) that supplies VDD to the panel, when enabled by this signal. It should not be used as the source of VDD to the panel.

2) Data and Control Signal: Activity on the data and control lines to the panel is managed as part of the power control sequence.

3) FP_VCONEN, Flat Panel Voltage Contrast Enable: This signal is designed to enable the contrast voltage to the panel. It is intended that this signal be connected to a power FET or similar switching device (either internal to the panel or not) that supplies the contrast voltage to the panel, when enabled by this signal. It should not be used as the source of contrast voltage to the panel.

4) DISPOFF#, Disable Backlight Off: This signal is intended to control the backlight of the panel. It is an active-low signal; when asserted (low), it turns the backlight off.

3.2.12.1 External Power Sequencing

Offset 408h[27] selects whether power sequencing will be controlled externally or internally. If external sequencing is selected, then Offset 408h[24:18] do not have any effect.

When external power sequencing is selected, output FP_VDDEN directly follows input ENA_VDDIN, and FP_VCONEN follows input ENA_LCDIN. The DISPOFF# signal may be directly controlled by writing to Offset 408h[25].

3.2.12.2 Internal Power Sequencing

Offset 408h[27] selects whether power sequencing will be controlled externally or internally. If internal sequencing is selected, then the four functions listed above are controlled automatically by the CS9211.

When operating using internal power sequencing, a power-up or down sequence is initiated by writing to the Panel Power Control bit at Offset 408h[24]. When the Panel Power Control bit is low and written high, a panel power-up sequence will occur, following the order given in Figure 3-13 and the timings as selected by Offset 408h[23:21]. If the Panel Power Control bit is high and written low, a panel power-down sequence will occur, following the order given in Figure 3-13 and with the timings as selected by Offset 408h[20:18].

The Panel Power Control bit may be read at any time in order to determine the assumed state of the panel. If the bit is high, it is assumed that a low-to-high transition has previously occurred and the panel is on. If the bit is low, it is assumed that either the bit has never been set high or a high-to-low transition of the bit has previously occurred; in either case the panel is off.

The length of each of the phase delays during the power-up and down sequences may be set to one of two values (32 ms or 128 ms) by Phase Control bits at Offset 408h[23:18]. The delay controlled by each of these bits is diagrammed in Figure 3-13.

Table 3-18. Power Sequence Control Bits

Bit	Name	Description
Offset 408h-40Bh		**Power Management Register (R/W)** — **Reset Value = 00000000h**
27	PWR_SEQ_SEL	**Power Sequence Select**: Selects whether to use internal or external power sequence. The power sequence controls the order in which FP_VDDEN, FP_VCONEN, the data and control signals, and DISPOFF# become active during power-up, and inactive during power-down. 0 = Use internal power sequencing (phase timing is controlled by bits [24:18]. 1 = Use external power sequencing (phase timing is controlled by signals generated from CS550A).
25	DISPOFF_CNTL	**Display Off Control Source**: Selects how DISPOFF# is controlled. Independent control may be used to disable the backlight to save power, even if the panel is otherwise on. 0 = DISPOFF# is controlled by with the power-up/down sequence, internal or external mode. 1 = DISPOFF# immediately turns the backlight off.
24	PWR_CNTL	**Panel Power Control**: Initiates the internal power-up or power-down sequence. When the bit is set from high-to-low, the internal power-down sequence is initiated with the timings as selected by Offset 408h[20:18]. When the bit is set from low-to-high, the internal power-up sequence is initiated with the timings as selected by Offset 408h[23:21]. This bit may be read to determine the power status (i.e., on or off) of the panel. This bit functions as described only if the internal power sequence has been selected by bit [27]. 0 = Powered down; 1 = Powered up.

Functional Description (Continued)

Table 3-18. Power Sequence Control Bits (Continued)

Bit	Name	Description
23	PWRUP_PHASE_2	**Panel Power-Up Phase 2**: Selects the interval between enabling FP_VDDEN to enabling panel data and control signals. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
22	PWRUP_PHASE_1	**Panel Power-Up Phase 1**: Selects the interval between enabling the panel data signals to enabling FP_VCONEN. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
21	PWRUP_PHASE_0	**Panel Power-Up Phase 0**: Selects the interval between disabling FP_VCONEN to disabling DISPOFF#. This bit is ineffective if independent DISPOFF# control is selected by bit 25. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
20	PWRDN_PHASE_0	**Panel Power-Down Phase 0**: Selects the interval between disabling panel DISPOFF# to disabling FP_VCONEN. See Figure 3-13 on page 37. This bit is ineffective if independent DISPOFF# control is selected by bit 25. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
19	PWRDN_PHASE_1	**Panel Power-Down Phase 1**: Selects the interval between disabling FP_VCONEN to disabling the panel data signals. See Figure 3-13 "Panel Power Sequence" on page 37. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
18	PWRDN_PHASE_2	**Panel Power-Down Phase 2**: Selects the interval between disabling the panel data signals to disabling panel FP_VDDEN. See Figure 3-13 "Panel Power Sequence" on page 37. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.

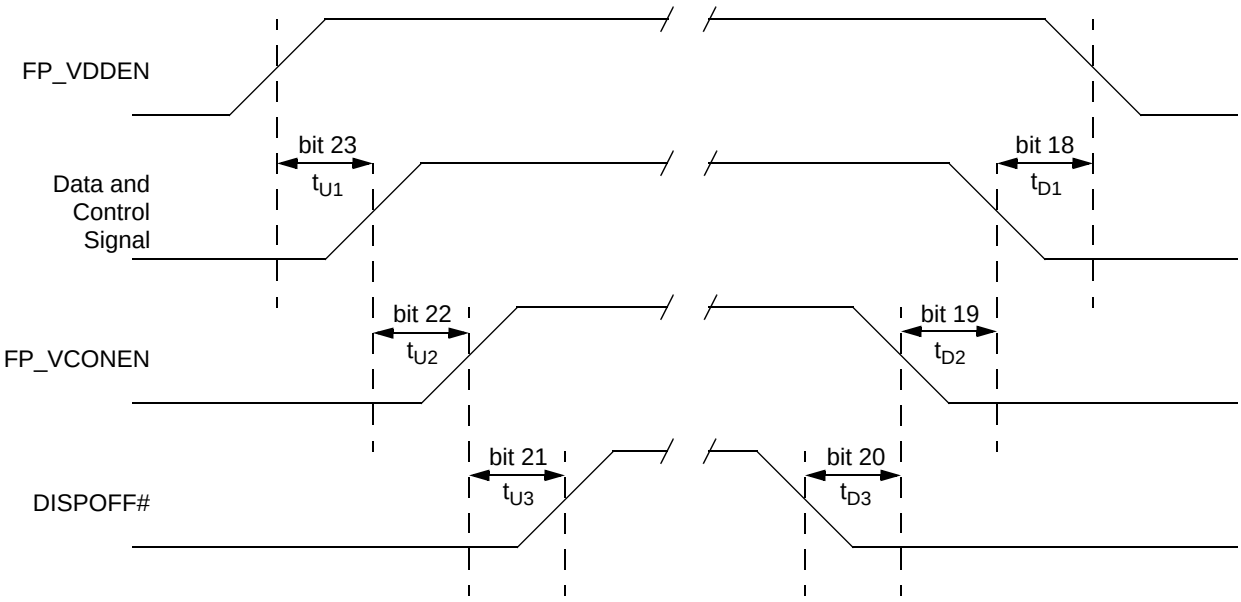


Figure 3-13. Panel Power Sequence

Functional Description (Continued)

3.2.13 General Purpose I/O Pins

The CS9211 provides eight GPIO (General Purpose I/O) pins. There are two 32-bit registers used for programming the GPIO pins:

- GPIO Control Register (Offset 438h):
  - — TYPE Bits [7:0] - Allows for setting each GPIO pin's direction (i.e., input or output).
  - — MODE Bits [15:8] - Selects pins mode (i.e., normal mode or weak pull-up/down mode).
  - — PUPD Bits [23:16] - Enables selected pull-up/down mode (as long as corresponding MODE bit is enabled and TYPE bit is set as an output).
- GPIO Data Register (Offset 434h)
  - — DATA Bits [7:0] - Contain direct values of the GPIO pins. Write operations to the corresponding GPIO pins should be done only for bits defined as outputs. Reads from the data register will read the last written value if the pin is an output.
  - — STS Bits [15:8] are read only status bits. The valid GPIO pins' status can be read from those pins.

Table 3-19 "GPIO Pin Programming Registers" on page 38 gives the bit formats of the registers used for programming the GPIO pins.

Table 3-19. GPIO Pin Programming Registers

Bit	Name	Description
Offset 434h-437h		**GPIO Data Register (R/W)** — **Reset Value = xxxxxx00h**
31:16	RSVD	**Reserved (Read Only)**
15	GPIO7_STS	**GPIO7 Pin State (Read Only)**: Reports the value of pin GPIO7 when it is configured as an input.
14	GPIO6_STS	**GPIO6 Pin State (Read Only)**: Reports the value of pin GPIO6 when it is configured as an input.
13	GPIO5_STS	**GPIO5 Pin State (Read Only)**: Reports the value of pin GPIO5 when it is configured as an input.
12	GPIO4_STS	**GPIO4 Pin State (Read Only)**: Reports the value of pin GPIO4 when it is configured as an input.
11	GPIO3_STS	**GPIO3 Pin State (Read Only)**: Reports the value of pin GPIO3 when it is configured as an input.
10	GPIO2_STS	**GPIO2 Pin State (Read Only)**: Reports the value of pin GPIO2 when it is configured as an input.
9	GPIO1_STS	**GPIO1 Pin State (Read Only)**: Reports the value of pin GPIO1 when it is configured as an input.
8	GPIO0_STS	**GPIO0 Pin State (Read Only)**: Reports the value of pin GPIO0 when it is configured as an input.
7	GPIO7_DATA	**GPIO7 Pin Configuration**: Reflects the level of GPIO7. 0 = Low, 1 = High. (Note)
6	GPIO6_DATA	**GPIO6 Pin Configuration**: Reflects the level of GPIO6. 0 = Low, 1 = High. (Note)
5	GPIO5_DATA	**GPIO5 Pin Configuration**: Reflects the level of GPIO5. 0 = Low, 1 = High. (Note)
4	GPIO4_DATA	**GPIO4 Pin Configuration**: Reflects the level of GPIO4. 0 = Low, 1 = High. (Note)
3	GPIO3_DATA	**GPIO3 Pin Configuration**: Reflects the level of GPIO3. 0 = Low, 1 = High. (Note)
2	GPIO2_DATA	**GPIO2 Pin Configuration**: Reflects the level of GPIO2. 0 = Low, 1 = High. (Note)
1	GPIO1_DATA	**GPIO1 Pin Configuration**: Reflects the level of GPIO1. 0 = Low, 1 = High. (Note)
0	GPIO0_DATA	**GPIO0 Pin Configuration**: Reflects the level of GPIO0. 0 = Low, 1 = High. (Note)
Note: Bits [7:0] contain the direct values of the GPIO pins. Write operations can be done only for GPIOs that are defined as outputs. Reads from these bits read the last written value if the GPIO pin is configured as an output. The direction of the GPIO pins is controlled through Offset 438h[7:0].		
Offset 438h-43Bh		**GPIO Control Register (R/W)** — **Reset Value = 00000000h**
31:24	RSVD	**Reserved**: Set to 0.
23	GPIO7_PUPD	**GPIO7 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
22	GPIO6_PUPD	**GPIO6 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
21	GPIO5_PUPD	**GPIO5 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
20	GPIO4_PUPD	**GPIO4 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
19	GPIO3_PUPD	**GPIO3 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
18	GPIO2_PUPD	**GPIO2 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
17	GPIO1_PUPD	**GPIO1 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
16	GPIO0_PUPD	**GPIO0 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
15	GPIO7_MODE	**GPIO7 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
14	GPIO6_MODE	**GPIO6 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
13	GPIO5_MODE	**GPIO5 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
12	GPIO4_MODE	**GPIO4 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
11	GPIO3_MODE	**GPIO3 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
10	GPIO2_MODE	**GPIO2 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.

Functional Description (Continued)

Table 3-19. GPIO Pin Programming Registers (Continued)

Bit	Name	Description
9	GPIO1_MODE	**GPIO1 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
8	GPIO0_MODE	**GPIO0 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
7	GPIO7_TYPE	**GPIO7 Pin Type**: 0 = Input; 1 = Output.
6	GPIO6_TYPE	**GPIO6 Pin Type**: 0 = Input; 1 = Output.
5	GPIO5_TYPE	**GPIO5 Pin Type**: 0 = Input; 1 = Output.
4	GPIO4_TYPE	**GPIO4 Pin Type**: 0 = Input; 1 = Output.
3	GPIO3_TYPE	**GPIO3 Pin Type**: 0 = Input; 1 = Output.
2	GPIO2_TYPE	**GPIO2 Pin Type**: 0 = Input; 1 = Output.
1	GPIO1_TYPE	**GPIO1 Pin Type**: 0 = Input; 1 = Output.
0	GPIO0_TYPE	**GPIO0 Pin Type**: 0 = Input; 1 = Output.
Note: To enable the pull-up or pull-down mode function, the corresponding GPIO pin's MODE bit must be set to 1, and the corresponding TYPE bit must enable it as an output (i.e., be set to 1).		

4.0 Register Descriptions

Table 4-1 provides a summary of the Configuration Registers, followed by descriptions of the individual registers and their bit formats. These registers are accessed using the serial interface, as described in Section 3.2.1 “Serial Interface” on page 17. Note that all configuration registers are memory mapped.

Table 4-1. Configuration Registers Summary

Offset	Access	Name / Function	Reset Value	Reference (Table 4-2)
400h-403h	R/W	**Panel Timing Register 1** Configures the flat panel horizontal and vertical timing characteristics	00000000h	Page 41
404h-407h	R/W	**Panel Timing Register 2** Configures the flat panel horizontal and vertical timing characteristics	00000000h	Page 41
408h-40Bh	R/W	**Power Management Register** Configures the power management features of the LCD controller	00000000h	Page 43
40Ch-40Fh	R/W	**Dither and Frame Rate Control Register** Configures dithering and frame rates	00000000h	Page 44
410h-413h	R/W	**Blue LFSR Seed** 15-bit value that specifies the seed value for the FRM conversion of the Blue component of each pixel	00000000h	Page 45
414h-417h	R/W	**Green LFSR Seed** 15-bit value that specifies the seed value for the FRM conversion of the Green component of each pixel **Red LFSR Seed** 15-bit value that specifies the seed value for the FRM conversion of the Red component of each pixel	00000000h	Page 45
418h-41Bh	R/W	**FRM Memory Index Register**	00000000h	Page 45
41Ch-41Fh	R/W	**FRM Memory Data Register** (32 x 64 Bits)	00000000h	Page 45
420h-423h	R/W	**Memory Control Register** Selects the memory type, SDRAM or EDO DRAM	1EF80008h	Page 45
424h-427h	R/W	**Dither RAM Control and Address Register** Provides the dither RAM address. The value programmed is used to initialize the Dither RAM address counter. Subsequent accesses to the Dither RAM Data Register cause the address counter to increment.	00000000h	Page 46
428h-42Bh	R/W	**Dither RAM Data Register** Provides the Dither RAM data. The data can be read or written to the dither RAM via this register. Prior to accessing the data register, an appropriate address should be loaded to the Dither RAM Address Register (Offset 424h). Subsequent accesses to the data register cause the internal address counter to increment for the next cycle.	00000000h	Page 46
42Ch-42Fh	R/W	**Panel CRC (Cyclical Redundancy Check) Signature Register** When CRC is enabled, the CRC logic writes the generated signature to this register. The value can be compared with the software simulation results or a previously generated signature for the same image and settings.	xxxxxxxxh	Page 46
430h-433h	RO	**Device and Revision ID Register** Reads the CS9211’s device ID and revision ID.	92110302h	Page 46
434h-437h	R/W	**GPIO Data Register** Status and levels of GPIO pins.	xxxxxxxxh	Page 46
438h-43Bh	R/W	**GPIO Control Register** Configuration of each GPIO pin as an input or output, and in normal or weak pull-up/down modes.	xxxxxxxxh	Page 47

Register Descriptions (Continued)

Table 4-2. Configuration Registers

Bit	Name	Description
Offset 400h-403h		**Panel Timing Register 1 (R/W)** **Reset Value = 0000000h**
31	RSVD	**Reserved**: This bit is not defined.
30	FP_VSYNC_POL	**FP_VSYNC Input Polarity**: Selects positive or negative polarity of the FP_VSYNC input signal (pin 99). Program this bit to match the polarity of the incoming FP_VSYNC signal. Note that Offset 404h[23] independently controls the polarity of the VSYNC output signal (pin 33). 0 = FP_VSYNC is normally low, transitioning high during sync interval (**Default**). 1 = FP_VSYNC is normally high, transitioning low during sync interval.
29	FP_HSYNC_POL	**FP_HSYNC Input Polarity**: Selects positive or negative polarity of the FP_HSYNC input (pin 97). Program this bit to match the polarity of the incoming FP_HSYNC signal. Note that Offset 404h[22] independently controls the polarity of the HSYNC output signal (pin 31). 0 = FP_HSYNC is normally low, transitioning high during sync interval (**Default**). 1 = FP_HSYNC is normally high, transitioning low during sync interval.
28	RSVD	**Reserved**: This bit is not defined.
27	HSYNC_SRC	**TFT Horizontal Sync Source**: Selects an internally generated or external pass-through source of the TFT horizontal sync output on pin 31. The internally generated HSYNC pulse will be triggered by the input HSYNC, but the output polarity, and leading and trailing edge positions are controlled by registers 404h[22] and 400h[7:0] respectively. The external mode will pass the input HSYNC pulse directly to the output pin. 0 = Pass the input HSYNC directly onto the output LP/HSYNC pin (pin 31) (**Default**). 1 = Internally generate the output HSYNC using the leading/trailing edge bits [7:0] and the polarity bit (Offset 404h[22]).
26:16	PAN_VSIZE	**Panel Vertical Size**: This field represents the panel vertical size in terms of scan lines. The value programmed should be equal to the panel size that is being connected. This can be used only for DSTN/STN modes. Example: 640x480 = 1E0h, 800x600 = 258h, and 1024x768 = 300h.
15:8	RSVD	**Reserved**: These bits are not defined.
7:5	HSYNC_LEADING_EDGE	**Horizontal Sync Leading Edge Position**: Selects the position of the leading edge of the output HSYNC pulse with respect to the rising edge of the modified input HSYNC pulse. The modified input HSYNC pulse is that which has been inverted, or not inverted, by bit 29. The position is programmable in steps of 1 DOTCLK, starting at 2 DOTCLOCKS and extending up to 8. Bit 27 must be set in order for bits [7:5] to be recognized. Note that there are combinations of bits [7:5] and [4:0] that can result in a zero- or negative-length pulse, for example if the trailing edge is positioned before the leading edge. In this case, the output pulse will not be generated. 000 = No delay from the input HSYNC (**Default**). 001-111 = Position the HSYNC leading edge by 2 to 8 DOTCLKs with respect to the input HSYNC rising edge. Note that there is no setting for a position of 1 DOTCLOCK.
4:0	HSYNC_TRAILING_EDGE	**Horizontal Sync Trailing Edge Position**: Selects the position of the trailing edge of the output HSYNC pulse with respect to the rising edge of the modified input HSYNC pulse. The modified input HSYNC pulse is that which has been inverted, or not inverted, by bit 29. The position is programmable in steps of 1 DOTCLK, starting at 1 DOTCLOCK and extending up to 31. Bit 27 must be set in order for bits [4:0] to be recognized. Note that there are combinations of bits [7:5] and [4:0] that can result in a zero- or negative-length pulse, for example if the trailing edge is positioned before the leading edge. In this case, the output pulse will not be generated. 00000 = Does not generate the HSYNC pulse if bit 27 = 0. (**Default**). 00001 - 11111 = The HSYNC trailing edge position can be varied from 1 to 31 DOTCLKs with respect to the input HYSNC rising edge.

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
Offset 404h-407h		**Panel Timing Register 2 (R/W)** — **Reset Value = 00000000h**
31	HIGH_RESOL_MCLK	**High Resolution MCLK**: Selects the MCLK frequency in terms or the DOTCLK frequency. This bit should be programmed as “0” for all the DSTN panels with resolutions up to 800x600, where the memory clock is the same as the DOTCLK. This should be set to “1” for the 1024x768 DSTN panel to run the memory clock at two-thirds the rate of the DOTCLK. 0 = Memory clock runs at the same frequency as DOTCLK. 1 = Memory clock runs at two-thirds the frequency of the DOTCLK.
30	PASS_THRU	**Pass-Through**: Activates the Pass-Through mode. In Pass-Through mode, the input timing and the pixel data are passed directly onto the panel interface timing and the panel data pins to drive the panel; the internal CS9211 logic and timing is not used. In normal mode, Offset 400h[7:0], 404h[29], and 404h[27:24] are effective. 0 = Normal mode; output timing uses the logic and timing from the CS9211. 1 = Pass-Through mode; CS9211 internal timing logic functions are not used.
29	LDE_POL_SEL	**Display Timing Strobe Polarity Select**: Selects the polarity of the LDE pin (pin 32). This can be used for some TFT panels that require an active low timing LDE. 0 = LDE signal is active low (**Default**). 1 = LDE signal is active high.
28	RSVD	**Reserved**: This bit is not defined.
27	PSH_CLK_CTL	**Panel Shift Clock Retrace Activity Control**: Programs the shift clock (SHFCLK, pin 30) to be either free running or active only during the display period. Some TFT panels recommend keeping the shift clock running during the retrace time. This bit has no effect in DSTN or SSTN modes. 0 = Shift clock is active only during active display period. 1 = Shift clock is free running during the entire frame period.
26	LP_HSYNC_SEL	**LP/HSYNC Select**: Selects the function of LP/HSYNC (pin 31). Set this bit based on the panel type connected. For DSTN or SSTN panels, set this bit to 0. For TFT panels, set this bit to 1. 0 = LP (output for DSTN/SSTN panel). 1 = HSYNC (output for TFT panel).
25	LDE_SEL	**LDE Select**: Always set this bit to 1. 0 = Reserved 1 = LDE (output for TFT panel).
24	FLM_VSYNC_SEL	**FLM/VSYNC Select**: Selects function of FLM/VSYNC (pin 33). Set this bit based on the panel type connected. For DSTN or SSTN panels, set this bit to 0. For TFT panels, set this bit to 1. 0 = FLM (output for DSTN/SSTN panel). 1 = VSYNC (output for TFT panel).
23	VSYNC_POL	**Vertical Sync Output Polarity**: Selects positive or negative polarity of the VSYNC output signal (pin 33). This bit is effective only for TFT panels; for this bit to function, bit 24 must be set to 1. Note that Offset 400h[30] independently controls the polarity of the FP_VSYNC input signal (pin 99). 0 = VSYNC output is active high. 1 = VSYNC output is active low.
22	HSYNC_POL	**Horizontal Sync Output Polarity**: Selects polarity of output HSYNC signal (pin 31). This bit is effective only for TFT panels; for this bit to function, bit 26 must be set to 1. Note that Offset 400h[29] selects independently controls the polarity of the FP_HSYNC input signal (pin 97). 0 = HSYNC output is active high. 1 = HSYNC output is active low.
21:20	DSTN_TFT	**Panel Type Select**: Selects panel type. The selection of the panel type in conjunction with the PIX_OUT (bits [18:16]) setting determines how pixel data is mapped on the output LD/UD pins. This bit also determines the generation of SHFCLK and other panel timing interface signals. 00 = SSTN/DSTN panel 01 = TFT panel 10 = Reserved 11 = Reserved
19	COLOR_MONO	**Color/Mono Select**: Selects color or monochrome LCD panel. 0 = Color; 1 = Monochrome.

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
18:16	PIX_OUT	**Pixel Output Format**: These bits define the pixel output format. The selection of the pixel output format in conjunction with the panel type selection (bits [21:20]) and the color/monochrome selection (bits [19]) determines how the pixel data is formatted before being sent on to the LD/UD pins. These settings also determine the SHFCLK period for the specific panel. 000 = 8-bit DSTN panel or up to 24-bit TFT panel with one pixel per clock. Option 1: Mono 8-bit DSTN (bits [21:20] = 00 and bit 19 = 1) (Color 8-bit DSTN is not supported) SHFCLK = 1/4 of DOTCLK Option 2: Color TFT with 1 pixel/clock (bits [21:20] = 01 and bit 19 = 0) SHFCLK = DOTCLK 001 = 16-bit DSTN panel or 18/24-bit TFT XGA panel with two pixels per clock. Option 1: Color 16-bit DSTN (bits [21:20] = 00 and bit 19 = 0) SHFCLK = 1/(3:2:3) of DOTCLK Option 2: Mono 16-bit DSTN (bits [21:20] = 00 and bit 19 = 1) SHFCLK = 1/8 of DOTCLK Option 3: Color 18/24 bit TFT (bits [21:20] = 01 and bit 19 = 0) SHFCLK = 1/2 of DOTCLK 010 = 24-bit DSTN panel Color 24-bit DSTN (bits [21:20] = 00 and bit 19 = 0) (Mono 24-bit DSTN is not supported) SHFCLK = 1/4 of DOTCLK 011 = 8-bit SSTN panel Color 8-bit SSTN (bits [21:20] = 00 and bit 19 = 0) SHFCLK = 1/(3:2:3) of DOTCLK 100, 101, 110, and 111 = Reserved
15:14	RSVD	**Reserved**: This bit is not defined.
13	CONT_LPS	**Continuous Line Pulses**: This bit selects whether line pulses are continuously output or are output only during the active display time. In most cases, DSTN panels require continuous line pulses (LPs). This bit will have no effect if the CS9211 is set to TFT mode. 0 = Continuous line pulses. 1 = Line pulses during the display time only.
12:0	RSVD	**Reserved**: These bits are not defined.
Offset 408h-40Bh		**Power Management Register (R/W)** **Reset Value = 00000000h**
31:28	RSVD	**Reserved**: These bits are not defined.
27	PWR_SEQ_SEL	**Power Sequence Select**: Selects whether to use internal or external power sequence. The power sequence controls the order in which FP_VDDEN, FP_VCONEN, the data and control signals, and DISPOFF# become active during power-up, and inactive during power-down. 0 = Use internal power sequencing (phase timing is controlled by bits [24:18]. 1 = Use external power sequencing (phase timing is controlled by signals generated from CS5530/CS550A).
26	RSVD_0	**Reserved.:** This bit should always be set to zero.
25	DISPOFF_CNTL	**Display Off Control Source**: Selects how DISPOFF# is controlled. Independent control may be used to disable the backlight to save power, even if the panel is otherwise on. 0 = DISPOFF# is controlled by with the power-up/down sequence, internal or external mode. 1 = DISPOFF# immediately turns the backlight off.
24	PWR_CNTL	**Panel Power Control**: Initiates the internal power-up or power-down sequence. When the bit is set from high-to-low, the internal power-down sequence is initiated with the timings as selected by Offset 408h[20:18]. When the bit is set from low-to-high, the internal power-up sequence is initiated with the timings as selected by Offset 408h[23:21]. This bit may be read to determine the power status (i.e., on or off) of the panel. This bit functions as described only if the internal power sequence has been selected by bit [27]. 0 = Powered down; 1 = Powered up.
23	PWRUP_PHASE_2	**Panel Power-Up Phase 2**: Selects the interval between enabling FP_VDDEN to enabling panel data and control signals. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
22	PWRUP_PHASE_1	**Panel Power-Up Phase 1**: Selects the interval between enabling the panel data signals to enabling FP_VCONEN. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
21	PWRUP_PHASE_0	**Panel Power-Up Phase 0**: Selects the interval between disabling FP_VCONEN to disabling DISPOFF#. This bit is ineffective if independent DISPOFF# control is selected by bit 25. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
20	PWRDN_PHASE_0	**Panel Power-Down Phase 0**: Selects the interval between disabling panel DISPOFF# to disabling FP_VCONEN. See Figure 3-13 on page 37. This bit is ineffective if independent DISPOFF# control is selected by bit 25. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
19	PWRDN_PHASE_1	**Panel Power-Down Phase 1**: Selects the interval between disabling FP_VCONEN to disabling the panel data signals. See Figure 3-13 on page 37. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
18	PWRDN_PHASE_2	**Panel Power-Down Phase 2**: Selects the interval between disabling the panel data signals to disabling panel FP_VDDEN. See Figure 3-13 "Panel Power Sequence" on page 37. 0 = 32 ms ±1.0 ms; 1 = 128 ms ±4.0 ms.
17:0	RSVD	**Reserved**: These bits are not defined.
Offset 40Ch-40Fh		**Dither and Frame Rate Control Register (R/W)** **Reset Value = 00000000h**
31:16	RSVD	**Reserved**: These bits are not defined
15:13	REF_CYC	**Refresh Cycle Select Bits**: Selects the number of refresh cycles for the SDRAM. These cycles occur during the retrace time at the end each line. 000 = Generate three refresh cycles for the external frame buffer. 001 = Generate one refresh cycle for the external frame buffer. 010 = Generate five refresh cycles for the external frame buffer. Others = Reserved.
12	DITHER_RAM_ROM_SEL	**Dither RAM or ROM Select**: This bit selects either internal ROM or internal RAM as the source of the dither patterns. 0 = Selects fixed (internal to CS9211) ROM for dither patterns (**Default**). 1 = Selects programmable (internal to CS9211) RAM for dither patterns. To update the dither RAM, this bit must = 1. **Note:** See Offset 424h[6].
11	GRAY_SCALE_SEL	**Gray Scale Selection:** This bit chooses two methods of converting an incoming color pixel stream to shades of gray for display on monochrome panels. This bit is ignored if Offset 404h[19] is set to 0 (color mode). 0 = Green color only - Only the green pixel data input is used to generate the gray shades. 1 = NTSC weighting - Red, blue and green pixel color inputs are used to generate the gray shades for the monochrome panel.
10	NEG_IMG	**Negative Image**: This bit converts the black to white and white to black and all colors in between to their logical inverse to provide a negative image of the original image. It acts as though the incoming data stream were logically inverted (1 becomes 0 and 0 becomes 1). 0 = Normal display mode; 1 = Negative image display mode.
9:7	RSVD	**Reserved**: This bit is not defined.
6:4	NO_OF_FRM INTENSITIES	**Number Of FRM Intensities**: The value set by bits [6:4] is the number of intensities that will exist due to Frame Rate Modulation, prior to dithering. This field selects how many of the incoming most significant (MS) data bits (per color) are used to generate the FRM intensities. 000 = 2 FRM intensities (selects 1 MS (most significant) bit for use by FRM). 001 = 4 FRM intensities (selects 2 MS bits for use by FRM). 010 = 8 FRM intensities (selects 3 MS bits for use by FRM). 011 = 16 FRM intensities (selects 4 MS bits for use by FRM). 100 = 32 FRM intensities (selects 5 MS bits for use by FRM). 101, 110, 111 = Reserved.
3:1	DITH_BITS	**Dithering Bits Select**: This field is used to select the number of least-significant (LS) bits to be used for the dithering pattern. Dither bits are the least-significant bits of each pixel's color value. 000 = Reserved 001 = Selects 5 LS bits as dither bits. Number of FRM intensities should be 2 (i.e., bits [6:4] = 000). 010 = Selects 4 LS bits as dither bits. Number of FRM intensities should be 4 (i.e., bits [6:4] = 001). 011 = Selects 3 LS bits as dither bits. Number of FRM intensities should be 8 (i.e., bits [6:4] = 010). 100 = Selects 2 LS bits as dither bits. Number of FRM intensities should be 16 (i.e., bits [6:4] = 011). 101 = Selects LS 1 bit as a dither bit. Number of FRM intensities should be 32 (i.e., bits [6:4] = 100).

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
0	DITH_ENB	**Dithering Enable**: Enable/disable dithering. The dither bit must be enabled in order for dither RAM reads or writes to occur. When this bit is cleared, the internal dither RAM is powered down. 0 = Dither disable - The dithering function is turned off. When the dither is disabled, dither bits [3:1] do not have any effect and the dither RAM is not accessible. 1 = Dither enable. The dither functions with the number of dither bits as set in [3:1]
Offset 410h-413h		**BLUE LFSR SEED Register (R/W)** — **Reset Value = 00000000h**
31:15	RSVD	**Reserved**: These bits are not defined.
14:0	BSEED	**Blue LFSR Seed[14:0]:** 15-bit value that specifies the seed value for the FRM conversion of the Blue component of each pixel
Offset 414h-417h		**Red and Green LFSR Seed Register (R/W)** — **Reset Value = 00000000h**
31	RSVD	**Reserved**: This bit is not defined.
30:16	GSEED	**Green LFSR Seed[14:0]:** 15-bit value that specifies the seed value for the FRM conversion of the Green component of each pixel
15	RSVD	**Reserved**: This bit is not defined.
14:0	RSEED	**Red LFSR Seed[14:0]:** 15-bit value that specifies the seed value for the FRM conversion of the Red component of each pixel
Offset 418h-41Bh		**FRM Memory Index Register (R/W)** — **Reset Value = 00000000h**
31:10	RSVD	**Reserved**: These bits are not defined.
9:8	RGB_SEL	**RGB Memory (FRM RAM) Select:** Allows reading or writing to individual R,G, and B memory FRM RAM locations or writing to all of them at the same time. 00 = Read from R FRM RAM but write to RGB FRM RAM. 01 = read or write to R FRM RAM. 10 = Read or write to G FRM RAM. 11 = Read or write to B FRM RAM. **Note:** All FRM RAMs can be accessed through the serial interface before the panel is powered up.
7:6	RSVD	**Reserved**: These bits are not defined.
5:0	FRM_INDEX	**FRM Memory Index:** This auto-incrementing value represents the index to the FRM RAM. Each RAM is configured as 32x64, requiring two index values to update each row of FRM RAM. For example, the 00h index value will update the 32 LSB's of row "0" FRM RAM and the 01h index value will update the 32 MSB's of row "0" FRM RAM. To update the entire RAM location, the index is programmed only once with the starting value, "00". This is used inside the CS9211 to auto increment the FRM RAM locations for every FRM RAM data access using the Offset 41Ch.
Offset 41Ch-41Fh		**FRM Memory Data Register** — **Reset Value = 00000000h**
31:0	FRM_DATA	**FRM Memory Data Register**: This 32-bit data represents FRM RAM data to be read or written to the FRM RAM table in accordance to the RGB_SEL (Offset 418h[9:8]) and the index value (Offset 418h[5:0]).
Offset 420h-423h		**Memory Control Register** — **Reset Value = 1EF80008h**
31:5	RSVD	**Reserved**: These bits are not defined.
4	EDO_LATE	**EDO DRAM Late Latch Bit**: When this bit is set, the data is latched into the CS9211, one clock after the data arrives from the DRAM. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. This bit is effective only if EDO RAM is used, as selected by bit 0 = 0. 0 = Latch the data with no delay. 1 = Latch the data with a delay of one clock.
3	EDO_EDGE_SEL	**EDO Data Latch Edge Select**: This bit controls which clock edge is used to latch data. When this bit is set, the data from the DRAM is latched into the CS9211 on the negative edge of the memory clock. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. This bit is effective only if EDO RAM is used, as selected by bit 0 = 0. 0 = Latch on positive (rising) edge. 1 = Latch on negative (falling) edge.
2	SDRAM_LD	**SDRAM Load Bit**: SDRAM Load Mode Register. When enabled, this bit activates RAM refresh. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = Disable; 1 = Enable.

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
1	SDRAM_CLK _INVERT	**SDRAM Clock**: Inverts the clock to the SDRAM interface. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = Use inverted clock. 1 = Use non-inverted clock.
0	SDRAM_EDO	**SDRAM or EDO**: Selects external frame buffer memory type. Since SSTN and TFT panels do not use any frame buffer, this bit is used only for DSTN panels. 0 = EDO; 1 = SDRAM.
Offset 424h-427h		**Dither RAM Control and Address Register** — **Reset Value = 00000000h**
31:8	RSVD	**Reserved**: Set to 0.
7	DITHER_ RAM_ACCESS	**Dither RAM Access Bit**: Allows reads and writes to and from dither RAM. 0 = Disable (Do not allow reads or writes). 1 = Enable (Allow reads and writes). To perform dither RAM reads and writes, bits 7 and 6 must be set to 1. In addition, Offset 40Ch bits 12 and 0 must be set to 1. If any of these bits are not set to 1, the RAM goes into power-down mode.
6	DITHER_ RAM_UPDT	**Dither RAM Update**: This bit works in conjunction with bit 7. If this bit is enabled, it allows the data to update the RAM. 0 = Disable (do not allow dither RAM access). 1 = Enable (allow dither RAM access). To perform dither RAM reads and writes, bits 7 and 6 must be set to 1. In addition, Offset 40Ch bits 12 and 0 must be set to 1. If any of these bits are not set to 1, the RAM goes into power-down mode.
5:0	DITHER_ RAM_ADDR	**Dither RAM Address**: This 6-bit field specifies the address to be used for the next access to the dither RAM. Each access to the data register automatically increments the RAM address register. If non-sequential access is made to the dither RAM, the address register must be reloaded before each non-sequential data block.
Offset 428h-42Bh		**Dither RAM Data Register (R/W)** — **Reset Value = 00000000h**
31:0	DITHER_RAM_ DATA	**RAM Data**: This 32-bit field contains the read or write data for the RAM access.
Offset 42Ch-42Fh		**Panel CRC Signature Register (R/W)** — **Reset Value = xxxxxxxxh**
31:8	SIG_DATA	**Signature Address (Read Only)**: 24-bit signature data for dither logic or FRM logic.
7:2	FRAME_CNT	**Frame Count**: Represents the frame count, which is an index for the generated signature for that frame.
1	SGFR	**Signature Free Run**: The value of this bit during the first cycle of a frame determines whether a signature will be generated for that frame. If this bit is kept high, with signature enabled (bit 0 = 1), the signature generator captures data continuously across multiple frames. Changing this bit from high-to-low causes the signature generation process to stop after the current frame. 0 = Do not capture signature during next frame. 1 = Capture signature during next frame.
0	SIG_EN	**Signature Enable**: Enables/disables signature capture. 0 = Disable; 1 = Enable.
Offset 430h-433h		**Device and Revision ID Register (RO)** — **Reset Value = 92110303h**
31:16	DEV_ID	**Device ID (Read Only)**: This 16-bit field contains the data that represents the device ID.
15:0	REV_ID	**Revision ID (Read Only)**: This 16-bit field contains the data that represents the revision ID.
Offset 434h-437h		**GPIO Data Register (R/W)** — **Reset Value = xxxxxx00h**
31:16	RSVD	**Reserved (Read Only)**
15	GPIO7_STS	**GPIO7 Pin State (Read Only)**: Reports the value of pin GPIO7 when it is configured as an input.
14	GPIO6_STS	**GPIO6 Pin State (Read Only)**: Reports the value of pin GPIO6 when it is configured as an input.
13	GPIO5_STS	**GPIO5 Pin State (Read Only)**: Reports the value of pin GPIO5 when it is configured as an input.
12	GPIO4_STS	**GPIO4 Pin State (Read Only)**: Reports the value of pin GPIO4 when it is configured as an input.
11	GPIO3_STS	**GPIO3 Pin State (Read Only)**: Reports the value of pin GPIO3 when it is configured as an input.
10	GPIO2_STS	**GPIO2 Pin State (Read Only)**: Reports the value of pin GPIO2 when it is configured as an input.
9	GPIO1_STS	**GPIO1 Pin State (Read Only)**: Reports the value of pin GPIO1 when it is configured as an input.
8	GPIO0_STS	**GPIO0 Pin State (Read Only)**: Reports the value of pin GPIO0 when it is configured as an input.
7	GPIO7_DATA	**GPIO7 Pin Configuration**: Reflects the level of GPIO7. 0 = Low, 1 = High. (Note)
6	GPIO6_DATA	**GPIO6 Pin Configuration**: Reflects the level of GPIO6. 0 = Low, 1 = High. (Note)

Register Descriptions (Continued)

Table 4-2. Configuration Registers (Continued)

Bit	Name	Description
5	GPIO5_DATA	**GPIO5 Pin Configuration**: Reflects the level of GPIO5. 0 = Low, 1 = High. (Note)
4	GPIO4_DATA	**GPIO4 Pin Configuration**: Reflects the level of GPIO4. 0 = Low, 1 = High. (Note)
3	GPIO3_DATA	**GPIO3 Pin Configuration**: Reflects the level of GPIO3. 0 = Low, 1 = High. (Note)
2	GPIO2_DATA	**GPIO2 Pin Configuration**: Reflects the level of GPIO2. 0 = Low, 1 = High. (Note)
1	GPIO1_DATA	**GPIO1 Pin Configuration**: Reflects the level of GPIO1. 0 = Low, 1 = High. (Note)
0	GPIO0_DATA	**GPIO0 Pin Configuration**: Reflects the level of GPIO0. 0 = Low, 1 = High. (Note)
Note: Bits [7:0] contain the direct values of the GPIO pins. Write operations can be done only for GPIOs that are defined as outputs. Reads from these bits read the last written value if the GPIO pin is configured as an output. The direction of the GPIO pins is controlled through Offset 438h[7:0].		
Offset 438h-43Bh	**GPIO Control Register (R/W)**	**Reset Value = 000000h**
31:24	RSVD	**Reserved**: Set to 0.
23	GPIO7_PUPD	**GPIO7 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
22	GPIO6_PUPD	**GPIO6 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
21	GPIO5_PUPD	**GPIO5 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
20	GPIO4_PUPD	**GPIO4 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
19	GPIO3_PUPD	**GPIO3 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
18	GPIO2_PUPD	**GPIO2 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
17	GPIO1_PUPD	**GPIO1 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
16	GPIO0_PUPD	**GPIO0 Pin Pull-up or Pull-down Mode**: 0 = Pull-down mode; 1 = Pull-up mode. (Note)
15	GPIO7_MODE	**GPIO7 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
14	GPIO6_MODE	**GPIO6 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
13	GPIO5_MODE	**GPIO5 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
12	GPIO4_MODE	**GPIO4 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
11	GPIO3_MODE	**GPIO3 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
10	GPIO2_MODE	**GPIO2 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
9	GPIO1_MODE	**GPIO1 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
8	GPIO0_MODE	**GPIO0 Pin Mode**: 0 = Normal mode; 1 = Weak pull-up or weak pull-down mode.
7	GPIO7_TYPE	**GPIO7 Pin Type**: 0 = Input; 1 = Output.
6	GPIO6_TYPE	**GPIO6 Pin Type**: 0 = Input; 1 = Output.
5	GPIO5_TYPE	**GPIO5 Pin Type**: 0 = Input; 1 = Output.
4	GPIO4_TYPE	**GPIO4 Pin Type**: 0 = Input; 1 = Output.
3	GPIO3_TYPE	**GPIO3 Pin Type**: 0 = Input; 1 = Output.
2	GPIO2_TYPE	**GPIO2 Pin Type**: 0 = Input; 1 = Output.
1	GPIO1_TYPE	**GPIO1 Pin Type**: 0 = Input; 1 = Output.
0	GPIO0_TYPE	**GPIO0 Pin Type**: 0 = Input; 1 = Output.
Note: To enable the pull-up or pull-down mode function, the corresponding GPIO pin's MODE bit must be set to 1, and the corresponding TYPE bit must enable it as an output (i.e., be set to 1).		

5.0 Electrical Specifications

This section provides information on absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in the Electrical Specifications are with respect to V_{SS} unless otherwise noted.

5.1 TEST MODES

The CS9211 can be forced into different test modes. Table 5-1 summarizes the test mode selection process.

5.1.1 NAND Tree Mode

The NAND tree mode is used to test input and bi-directional pins which will be part of the NAND tree chain. The NAND tree chain starts on pin 3 (UD11) and ends on pin 143 (MA2) where the output of the chain is captured. The following pins are not included in the NAND chain:

— All supply pins
— MBIST_EN (pin 45)
— SCAN_EN (pin 46)
— TEST_SE (pin 47)
— XTALIN (pin 48)
— XTALOUT (pin 49)

Table 5-1. Test Mode Selection

Mode	SCAN_EN (Pin 46)	TEST_SE (Pin 47)
NAND tree test	0	1

Table 5-2. NAND Tree Test Mode Pins

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
UD10	4	FLM/VSYNC	33	BLUE4	84	MD5	115
UD9	5	FP_VDDEN	34	RED3	85	MD9	116
UD8	6	FP_VCONEN	35	RED4	86	MD6	117
UD7	7	DISPOFF#	39	GREEN2	87	MD8	118
UD6	8	SCLK	40	BLUE5	88	MD7	119
UD5	9	SDIN	41	GREEN1	92	DQML	120
UD4	10	SDO	42	GREEN0	93	DQMH	121
UD3	11	SCS	43	GREEN3	94	WE#	122
UD2	12	RESET#	44	ENA_DISP	95	MCLK	123
UD1	13	GPIO7	63	RED5	96	CASH#	124
UD0	14	GPIO6	64	FP_HSYNC	97	CAS#/CASL#	127
LD11	15	GPIO5	65	GREEN4	98	CKE	129
LD10	16	GPIO4	66	FP_VSYNC	99	RAS#	130
LD9	20	GPIO3	67	GREEN5	100	CS#	131
LD8	21	GPIO2	68	ENA_LCDIN	101	MA9	132
LD7	22	GPIO1	69	MD15	102	OE#/BA	133
LD6	23	GPIO0	70	MD0	103	MA8	134
LD5	24	DOTCLK	75	MD14	104	MA10	135
LD4	25	RED0	76	MD1	105	MA0	136
LD3	26	ENA_VDDIN	77	MD13	106	MA7	137
LD2	27	RED2	78	MD2	107	MA1	138
LD1	28	RED1	79	MD12	110	MA6	139
LD0	29	BLUE0	80	MD3	111	MA5	140
SHFCLK	30	BLUE3	81	MD11	112	MA4	141
LP/HSYNC	31	BLUE1	82	MD4	113	MA3	142
LDE/MOD	32	BLUE2	83	MD10	114	MA2	143

Electrical Specifications (Continued)

5.2 ABSOLUTE MAXIMUM RATINGS

Table 5-3 lists absolute maximum ratings for the CS9211. Stresses beyond the listed ratings may cause permanent damage to the device. Exposure to conditions beyond these limits may (1) reduce device reliability and (2) result in premature failure even when there is no immediate apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced life and reliability. These are stress ratings only and do not imply that operation under any conditions other than those listed under Table 5-4 is possible.

5.3 OPERATING CONDITIONS

Table 5-4 lists the recommended operating conditions for the CS9211.

Table 5-3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Operating Case Temperature		130	°C	Power Applied
Storage Temperature	–40	150	°C	No Bias
Supply Voltage		4.0	V	

Table 5-4. Operating Conditions

Symbol	Parameter		Min	Max	Units	Comments
T_C	Operating Case Temperature		0	85	°C	
V_{DD}	Supply Voltage		3.14	3.46	V	3.3V nominal
V_{IH}	High-Level Input Voltage		2.0	5.25	V	
V_{IL}	Low-Level Input Voltage		–0.3	0.8	V	
I_{OH}	High-Level Output Current (for each driver type)	4	–4		mA	V_{OH} = 2.0V V_{DD} = 3.0V
		8	–8			
		12	–12			
I_{OL}	Low-Level Output Current (for each driver type)	4	4		mA	V_{OL} = 2.0V V_{DD} = 3.0V
		8	8			
		12	12			

Electrical Specifications (Continued)

5.4 DC CHARACTERISTICS

Table 5-5 lists the DC characteristics for the CS9211. All DC parameters and current measurements in this section were measured under the operating conditions listed in Table 5-4 "Operating Conditions" on page 49, unless otherwise noted.

Table 5-5. DC Characteristics

Symbol	Parameter	Min	Max	Units	Comments
I_{CC}	Supply Current (dynamic)		140	mA	V_{DD} nominal, (Note 1)
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA, (Note 2)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA, (Note 3)
I_{DD}	Static I_{DD}		550	µA	All Inputs are forced low
I_{IH}	High-Level Input Leakage Current	–10	–10	µA	$V_{IH} = V_{DD}$
	Input with internal pull-ups	–200	10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level Input Leakage Current	–10	10	µA	V_{IL} = 0V
	Input with internal pull-ups	–200	200	µA	V_{IL} = 0V
IO_{ZH}	High-Level I/O Leakage Current	–10	10	µA	$V_{IH} = V_{DD}$
IO_{SL}	Low-Level I/O Leakage Current	–10	10	µA	V_{IL} = 0V
C_{IN}	Input Capacitance		10	pF	

1) V_{DD} = 3.3V±5%, T_{CASE} = 0°C to 85°C, unless otherwise specified.
2) I_{OL} is specified for a standard buffer.
3) I_{OH} is specified for a standard buffer.

Electrical Specifications (Continued)

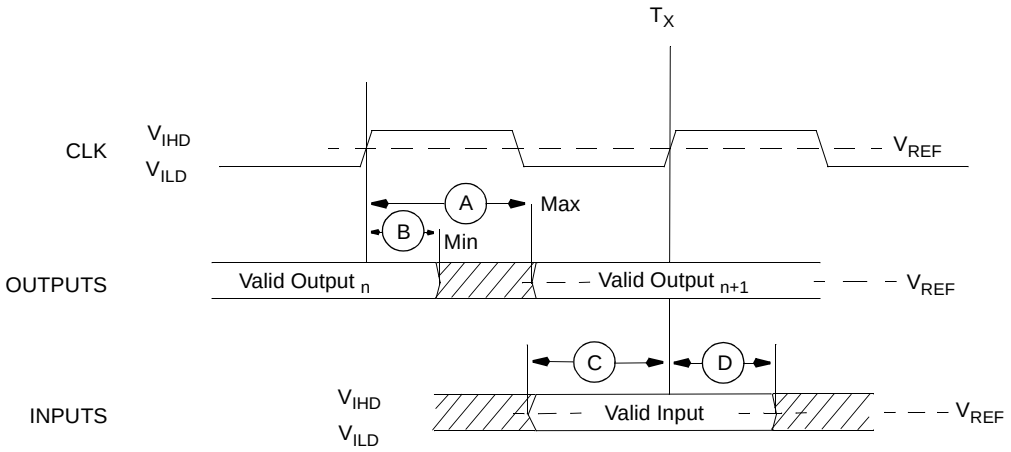
5.5 AC CHARACTERISTICS

The following tables list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. The rising-clock-edge reference level V_{REF} and other reference levels are shown in Table 5-6. Input or output signals must cross these levels during testing.

Input setup and hold times, illustrated in Figure 5-1, are specified minimums that define the smallest acceptable sampling window for which a synchronous input signal must be stable for correct operation. The output delay time has a minimum and a maximum, also illustrated in Figure 5-1.

Table 5-6. Drive Level and Measurement Points for Switching Characteristics

Symbol	Voltage (V)
V_{REF}	1.5
V_{IHD}	3.0
V_{ILD}	0.0



Legend: A = Maximum Output Delay Specification
B = Minimum Output Delay Specification
C = Minimum Input Setup Specification
D = Minimum Input Hold Specification

Figure 5-1. Drive Level and Measurement Points for Switching Characteristics

Electrical Specifications (Continued)

5.5.1 Pixel Port Timing

Table 5-7. Pixel Port Interface Timing

Symbol	Parameter	Min	Max	Unit	Comments (Note 1)
t_D	DOTCLK period	15.4	---	ns	65 MHz max speed
t_{DHP}	DOTCLK high pulse width	5	---	ns	40-60% duty cycle at 65 MHz
t_{DIS}	RED[5:0], GREEN[5:0], BLUE[5:0] setup to rising DOTCLK	0.1	5.2	ns	
t_{DIH}	RED[5:0], GREEN[5:0], BLUE[5:0] hold from rising DOTCLK	0.1	5.2	ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

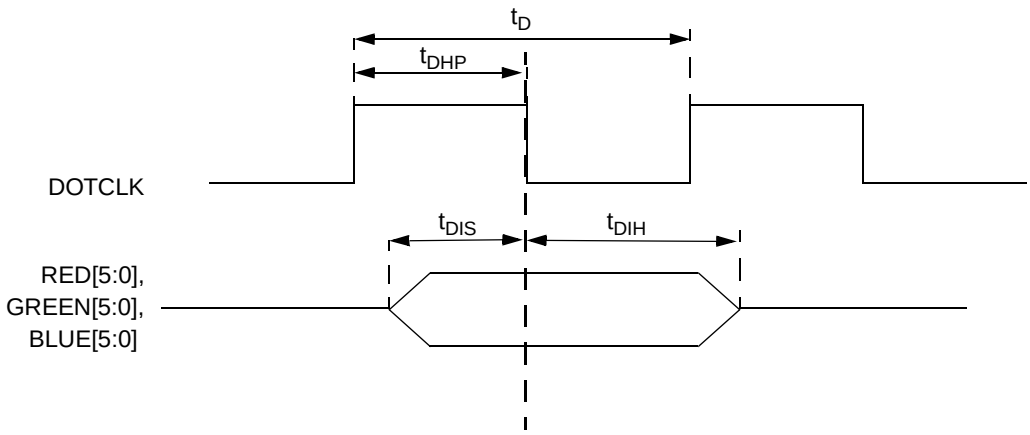


Figure 5-2. Pixel Port Interface Signals

Electrical Specifications (Continued)

5.5.2 Serial Interface Timing

Table 5-8. Serial Interface Timing

Symbol	Parameter	Min	Max	Unit	Comments (Note 1)
t_S	SCLK period	50		ns	
t_{SHP}	SCLK high pulse width	20	t_S – 12	ns	
t_{SIS}	SCS, SDIN setup to rising SCLK	25		ns	
t_{SIH}	SCS, SDIN hold from rising SCLK	20		ns	
t_{SOV}	SDO valid from rising SCLK		10	ns	
t_{SOH}	SDO hold from rising SCLK		10	ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

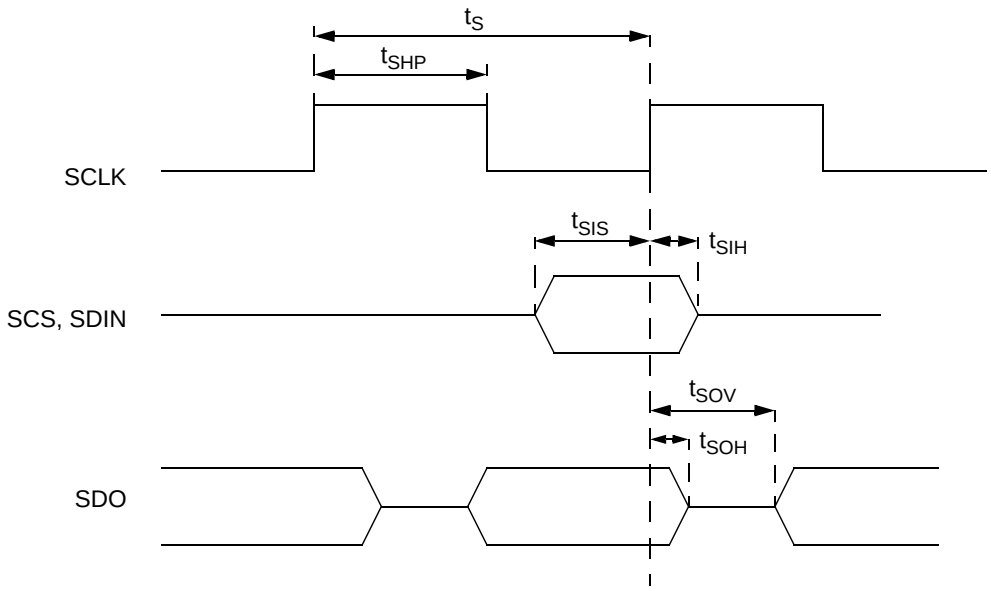


Figure 5-3. Serial Interface Signals

Electrical Specifications (Continued)

5.5.3 Flat Panel Timing

Table 5-9. Flat Panel Interface Timing (50 pF Output Load)

Symbol	Parameter	DSTN Mode		TFT Mode		Units	Comments (Note 1)
		Min	Max	Min	Max		
t_P	SHFCLK period	50	---	30	---	ns	
t_{PT}	SHFCLK rise/fall transition time		4		3	ns	
t_{PHP}	SHFCLK high pulse width	15	---	5	---	ns	
t_{PLP}	SHFCLK low pulse width	15	---	5	---	ns	
t_{POS}	Panel output setup to falling SHFCLK (Data setup time to the Panel)	10	---	3	---	ns	
t_{POH}	Panel output hold from falling SHFCLK (Data hold time to the panel)	10	---	7	---	ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

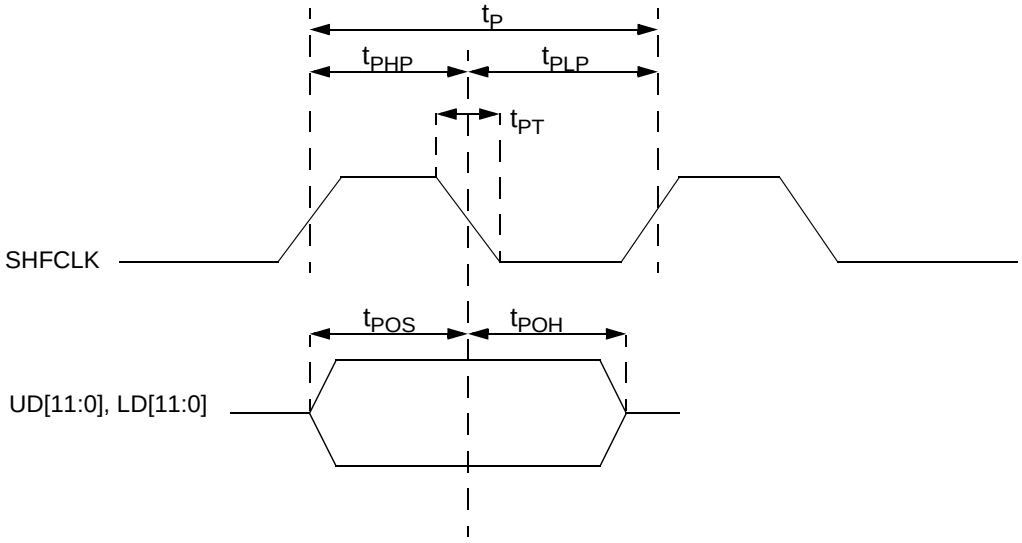


Figure 5-4. Flat Panel Interface Signals

Electrical Specifications (Continued)

5.5.4 Memory Interface Timing

Table 5-10. EDO DRAM Interface Timing

Symbol	Parameter	Min (Note 1)	Max ((Note 1))	Unit	Comments (Note 2)
t_{OWS}	OE# and WE# setup to falling RAS#	3*tD–5		ns	
t_{OWH}	OE# and WE# hold from rising RAS#	3*tD–2		ns	
t_{RP}	RAS# precharge time	3*tD–2		ns	
t_{RCD}	Falling RAS# to falling CASH#, CASL#	tD–1		ns	
t_{CAS}	CASH# and CASL# low pulse width	tD/2–6		ns	
t_{CP}	CASH# and CASL# precharge time	tD/2–6		ns	
t_{ASR}	MA[10:0] setup to falling RAS#	3*tD–2		ns	
t_{RAH}	MA[10:0] hold from falling RAS#	tD–1.5		ns	
t_{ASC}	MA[10:0] setup to falling CASH#, CASL#	tD/2–6		ns	
t_{CAH}	MA[10:0] hold from falling CASH#, CASL#	tD/2–6		ns	
t_{DS}	MD[15:0] write data setup to falling CASH#, CASL#	tD/2–10		ns	
t_{DH}	MD[15:0] write data hold from falling CASH#, CASL#	tD/2–2		ns	
t_{DV}	MD[15:0] read data valid from falling CASH#, CASL#		2*tD–10	ns	

1. 2X Refresh Mode (min tD = 25 ns). tD = DOT clock (DOTCLK) period.
2. All AC tests, unless otherwise specified, are at: VDD = 3.14 to 3.46 (3.3V nominal), TC = 0°C to 85°C, and CL = 50 pF.

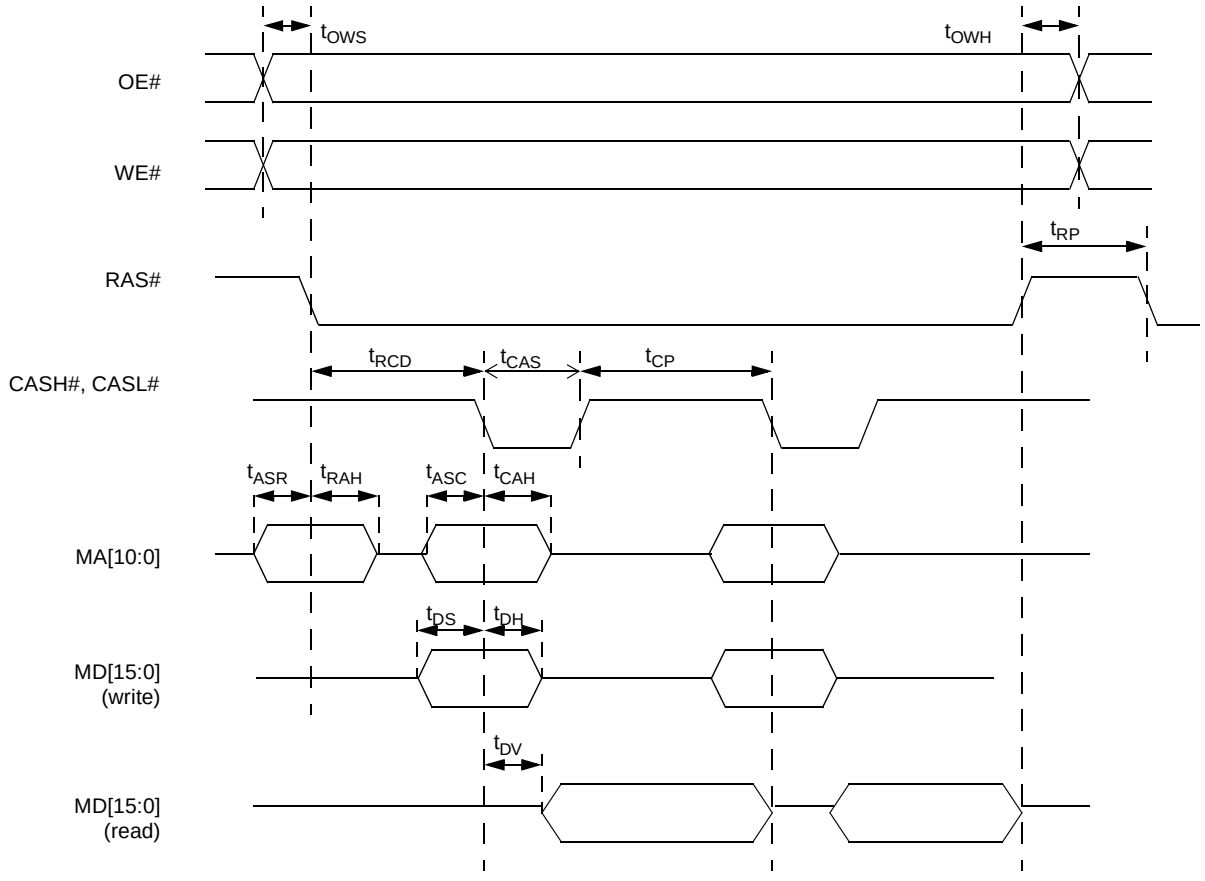


Figure 5-5. EDO DRAM Interface Signals

Electrical Specifications (Continued)

Table 5-11. SDRAM Read Timing

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
t_1	Clock Cycle Time	20		ns	
t_2	CS# Setup Time	2		ns	
t_3	CS# Hold Time	1		ns	
t_4	RAS# Setup Time	2		ns	
t_5	RAS# Hold Time	1		ns	
t_6	CAS# Setup Time	2		ns	
t_7	CAS# Hold Time	1		ns	
t_8	WE# Setup Time	2		ns	
t_9	WE# Hold Time	1		ns	
t_{10}	Address (MA) Setup Time	2		ns	
t_{11}	Address (MA) Hold Time	1		ns	
t_{12}	DQM Setup Time	2		ns	
t_{13}	DQM Hold Time	1		ns	
t_{14}	Data-In Setup Time	0.1	2	ns	
t_{15}	Data-In Hold Time	0.1	2	ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

Table 5-12. SDRAM Write Timing

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
t_1	Clock Cycle Time	20		ns	
t_2	CS# Setup Time	2		ns	
t_3	CS# Hold Time	1		ns	
t_4	RAS# Setup Time	2		ns	
t_5	RAS# Hold Time	1		ns	
t_6	CAS# Setup Time	2		ns	
t_7	CAS# Hold Time	1		ns	
t_8	WE# Setup Time	2		ns	
t_9	WE# Hold Time	1		ns	
t_{10}	Address (MA) Setup Time	2		ns	
t_{11}	Address (MA) Hold Time	1		ns	
t_{12}	DQM Setup Time	2		ns	
t_{13}	DQM Hold Time	1		ns	
t_{14}	Data-Out Setup Time	2		ns	
t_{15}	Data-Out Hold Time	1		ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

Electrical Specifications (Continued)

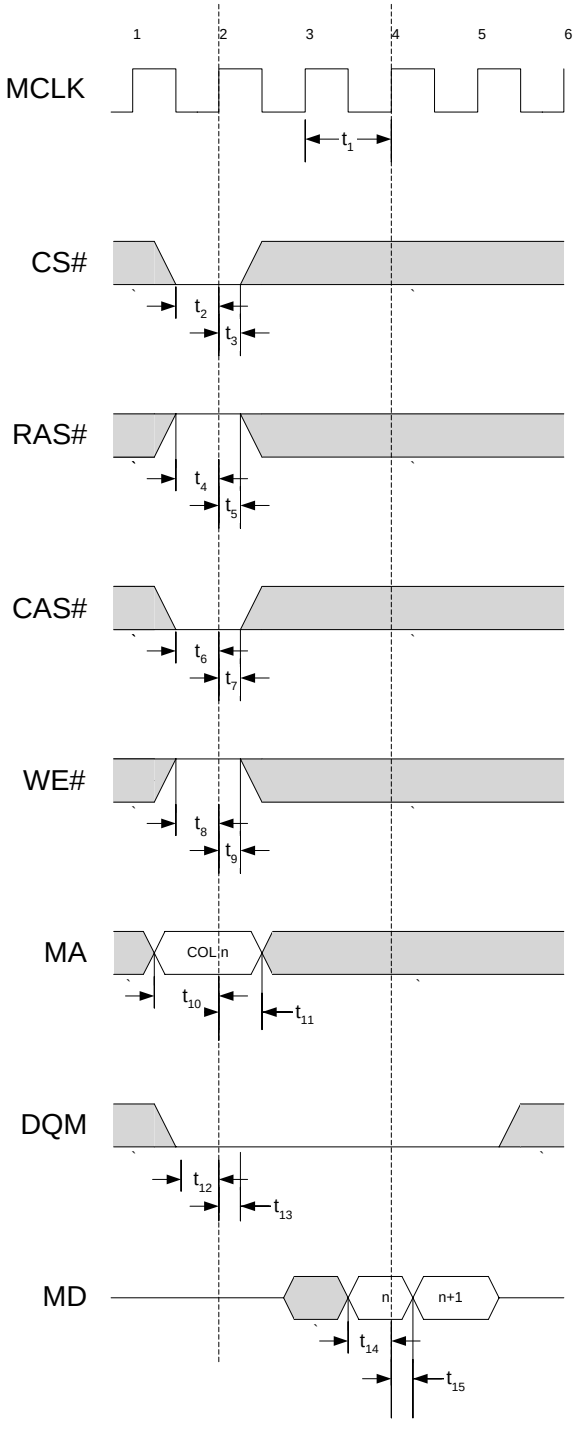


Figure 5-6. SDRAM Read Timing

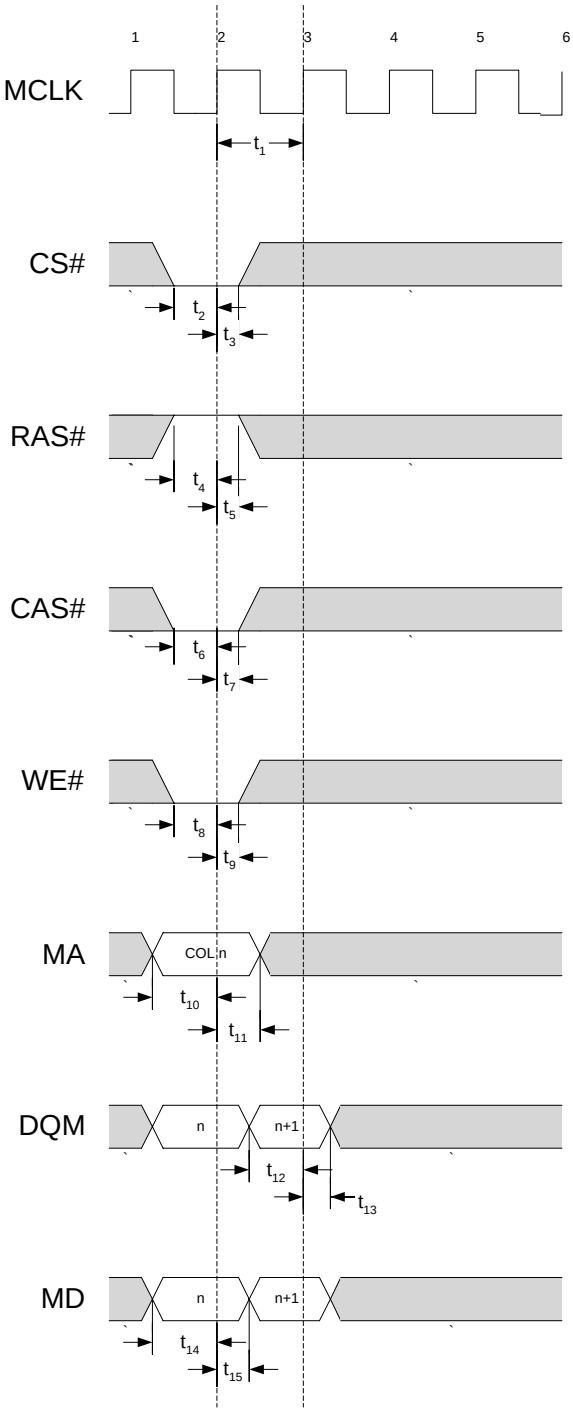


Figure 5-7. SDRAM Write Timing

Electrical Specifications (Continued)

5.5.5 Panel Timings

Table 5-13. DSTN Color Panel Timing Characteristics

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
T_{P1}	SHFCLK period	50	---	ns	
T_{P2}	SHFCLK high time	15	---	ns	
T_{P3}	SHFCLK low time	15	---	ns	
T_{P4}	SHFCLK rise time	-	4	ns	
T_{P5}	SHFCLK fall time		4	ns	
T_{P6}	Valid data to SHFCLK falling edge (data setup time)	10		ns	
T_{P7}	SHFCLK falling edge to valid data (data hold time)	10		ns	
T_{P8}	LP pulse width	150	---	ns	
T_{P9}	FLM setup time	120	---	ns	
T_{P10}	FLM hold time (valid FLM time after falling edge of LP)	300	--	ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

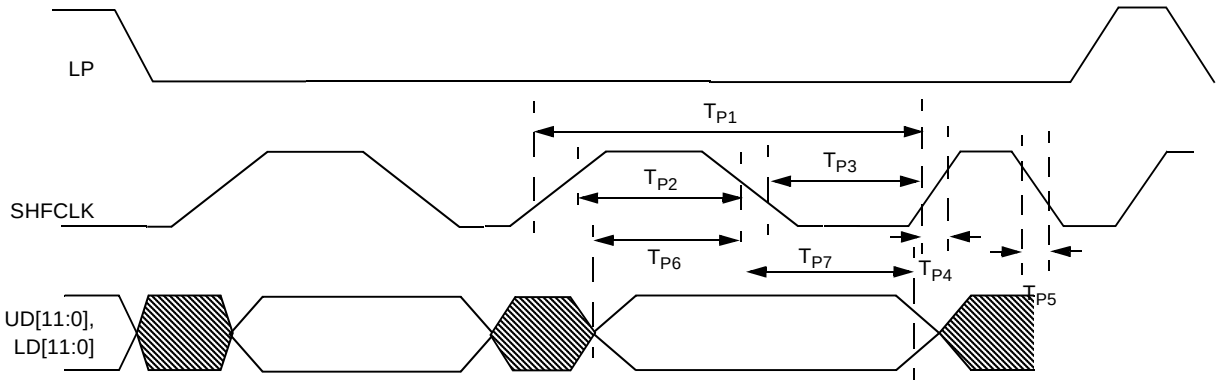


Figure 5-8. DSTN Color Panel Output Timing; LP and SHFCLK Relationship

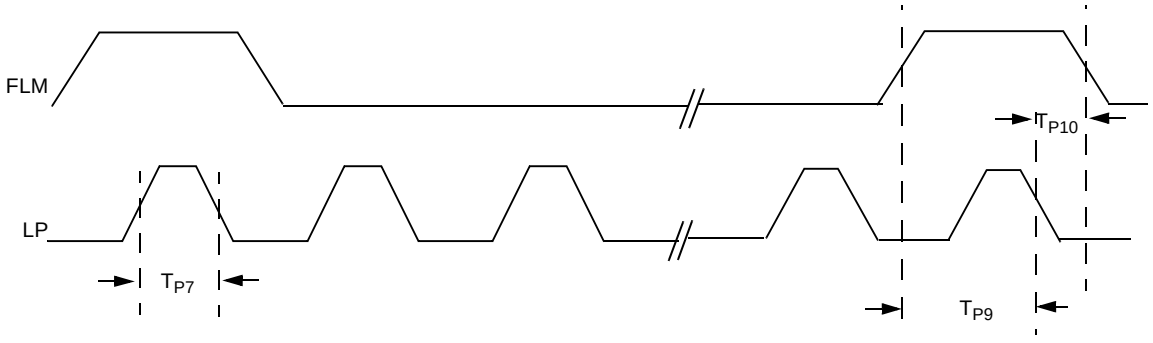


Figure 5-9. DSTN Color Panel Output Timing; FLM and LP Relationship

Electrical Specifications (Continued)

Table 5-14. Active Matrix TFT Color Panel Timing Characteristics

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
T_{P1}	SHFCLK period	30		ns	
T_{P2}	SHFCLK high time	5		ns	
T_{P3}	SHFCLK low time	5		ns	
T_{P4}	SHFCLK rise time		3	ns	
T_{P5}	SHFCLK fall time		3	ns	
T_{P6}	Valid data to SHFCLK falling edge (Data setup time)	3		ns	
T_{P7}	UD[11:0] and LD[11:0] hold time (Data hold time)	5		ns	
T_{P8}	HSYNC width	500		ns	
T_{P9}	LDE active to SHFCLK inactive (LDE setup time)	3		ns	
T_{P10}	SHFCLK inactive to LDE inactive (LDE Hold time)	7		ns	

1. All AC tests, unless otherwise specified, are at: V_{DD} = 3.14 to 3.46 (3.3V nominal), T_C = 0°C to 85°C, and C_L = 50 pF.

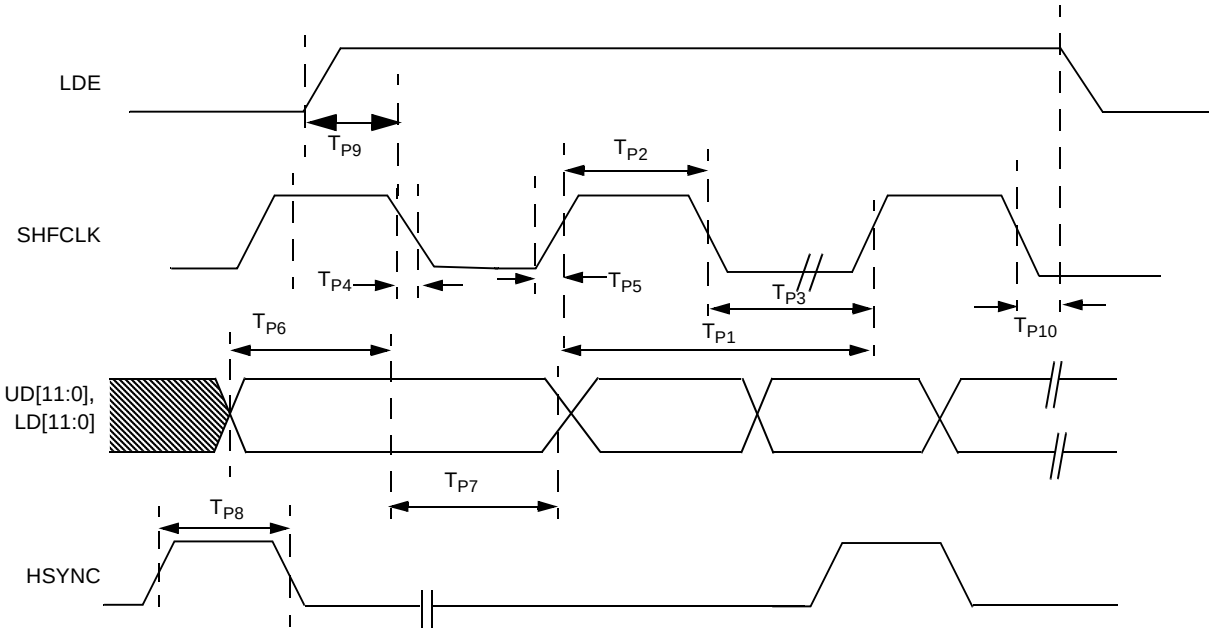
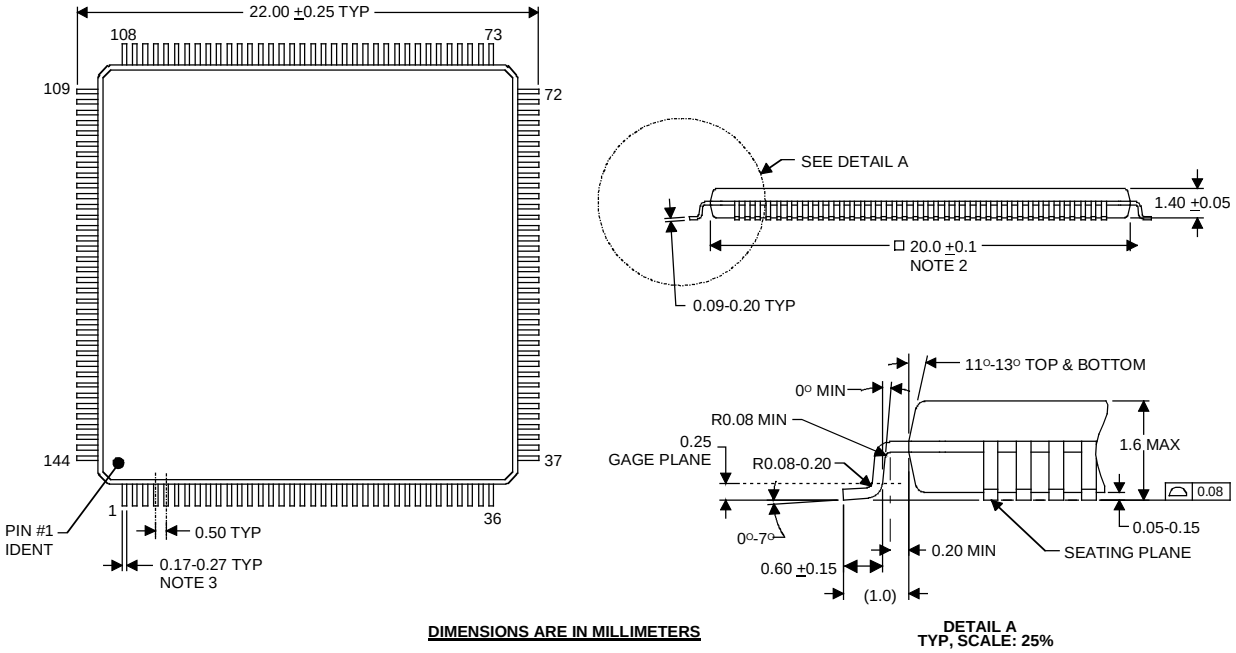


Figure 5-10. Active Matrix TFT Color Panel Output Timing

6.0 Mechanical Package Outline



DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON ALLOY 42 / COPPER

2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION
   MAXIMUM ALLOWABLE MODE PROTRUSION 0.25mm PER SIDE.

3. DIMESION DOES NOT INCLUDE MOLD PROTRUSION
   ALLOWABLE BAMBAR PROTRUSION SHALL BE 0.08

4. REFERENCE JEDEC REGISTRATION MO-136, VARIATION BT,
   DATED SEP/93

Figure 6-1. 144-Pin LQFP (Low-Profile Quad Flat Pack)

Appendix A Support Documentation

A.1 REVISION HISTORY

This document is a report of the revision/creation process of the data book for the Geode™ CS9211 graphics companion. Any revisions (i.e., additions, deletions, parameter corrections, etc.) are recorded in the table(s) below.

Revision # (PDF Date)	Revisions / Comments
0.1 (9/24/99)	First release for web posting.
0.2 (12/1/99)	Second preliminary release for web posting. Added table of contents and two new chapters (functional and registers).
0.3 (2/9/00)	Edited Section 4.0 “Register Descriptions” (see Rev 0.3 for details).
0.4 (7/11/00)	Engineering edits. Complete proofreading and corrections.
1.0 (8/10/00)	TME edits (see Rev 1.0 for details). Released for posting.
2.0 (10/3/00)	Engineering edits. See Rev 2.0 for details.
2.1 (10/27/00)	Changes made in Section 5.0 “Electrical Specifications” only: Changed V_{DD} in Table 5-4 through Table 5-13 (with the exception of Table 5-6). Changed V_{IHD} and V_{ILD} voltages in Table 5-6 "Drive Level and Measurement Points for Switching Characteristics".

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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