FAIRCHILD SEMICONDUCTOR™

December 1991
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74ACTQ16543
16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ACTQ16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The ACTQ16543 utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

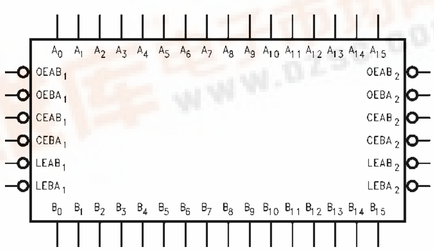
- Utilizes Fairchild FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Independent registers for A and B buses
- Separate controls for data flow in each direction
- Back-to-back registers for storage
  Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the ACTQ543
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250pF loads

Ordering Code:

Order Number	Package Number	Package Description
74ACTQ16543SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACTQ16543MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Pin Descriptions

Pin Names	Descriptions
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B 3-STATE Outputs

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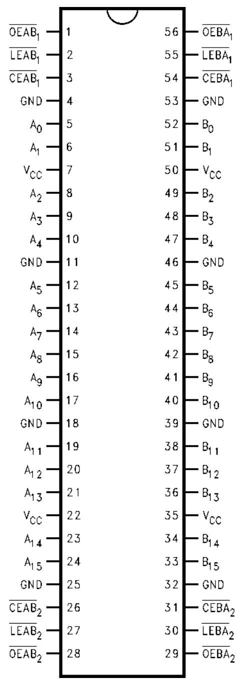
Connection Diagram

Pin Assignment for SSOP and TSSOP



Functional Description

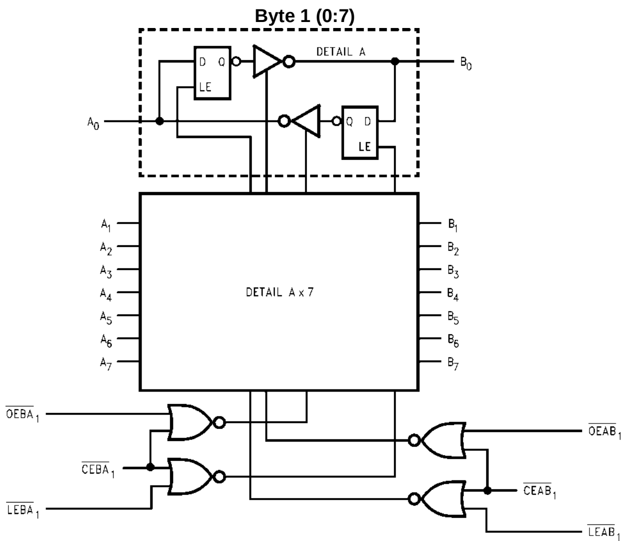
The ACTQ16543 contains sixteen non-inverting transceivers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}_n$) input must be LOW in order to enter data from A_0–A_{15} or take data from B_0–B_{15}, as indicated in the Data I/O Control Table. With $\overline{CEAB}_n$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}_n$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}_n$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}_n$ and $\overline{OEAB}_n$ both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$ inputs.

Data I/O Control Table

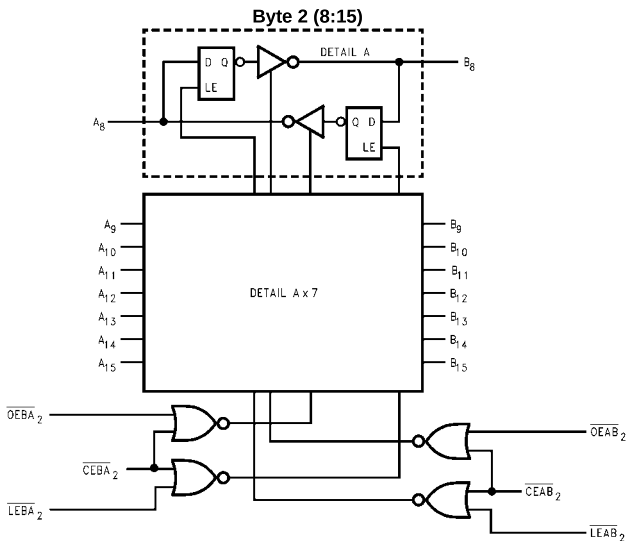
Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control
is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin	±50 mA
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = +25°C Guaranteed Limits	T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
	Output Voltage	5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
	Output Voltage	5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±5.0	μA	$V_I = V_{IL}$, V_{IH}; $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)				−75	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8		V	Figure 1, Figure 2 (Note 5)(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8		V	Figure 1, Figure 2 (Note 5)(Note 6)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5		V	Figure 1, Figure 2 (Note 4)(Note 6)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8		V	Figure 1, Figure 2 (Note 4)(Note 6)
V_{IHD}	Minimum HIGH Dynamic Input Voltage Level	5.0	1.7	2.0		V	(Note 4)(Note 7)
V_{ILD}	Maximum LOW Dynamic Input Voltage Level	5.0	1.2	0.8		V	(Note 4)(Note 7)

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

Note 4: Worst case package.

DC Electrical Characteristics (Continued)

Note 5: Maximum number of outputs that can switch simultaneously is n. (n – 1) outputs are switched LOW and one output held LOW.

Note 6: Maximum number of outputs that can switch simultaneously is n. (n – 1) outputs are switched HIGH and one output held HIGH.

Note 7: Maximum number of data inputs (n) switching. (n – 1) inputs switching 0V to 3V Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to $B_n$or B_n to A_n	5.0	3.8 3.5	5.9 5.5	8.3 7.9	3.0 2.6	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}_n$, $\overline{LEAB}_n$ to A_n, B_n	5.0	4.7 3.9	6.9 6.3	9.8 9.0	3.4 3.1	10.8 9.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	4.2 4.9	6.3 7.3	9.2 10.3	3.0 3.6	9.9 10.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	2.8 2.6	5.2 5.0	8.0 7.6	2.1 2.0	8.3 8.1	ns

Note 8: Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0		3.0	3.0	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0		1.5	1.5	ns
t_W	Latch Enable, B to A Pulse Width, LOW	5.0		4.0	4.0	ns

Note 9: Voltage Range 5.0 is 5.0V ±0.5V

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = -40$ to $+85°C$, V_{CC} = Com, C_L = 50 pF, 16 Outputs Switching (Note 10)			$T_A = -40$ to $+85°C$, V_{CC} = Com, C_L = 250 pF (Note 11)		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	4.5 3.7		11.1 9.6	5.8 5.1	14.3 13.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}_n$, $\overline{LEAB}_n$ to A_n, B_n	4.3 3.7		11.3 9.7	6.2 5.8	16.3 14.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	4.0 4.3		10.7 11.3	(Note 12)		ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	3.0 2.8		8.0 7.6	(Note 13)		ns
t_{OSHL} (Note 14)	Pin to Pin Skew HL Data to Output			1.1			ns
t_{OSLH} (Note 14)	Pin to Pin Skew LH Data to Output			1.4			ns
t_{OSHL} (Note 14)	Pin to Pin Skew Latch to Output			2.6			ns
t_{OSLH} (Note 14)	Pin to Pin Skew Latch to Output			1.0			ns
t_{OST} (Note 14)	Pin to Pin Skew Data to Output			1.0			ns
t_{OST} (Note 14)	Pin to Pin Skew Latch to Output			2.2			ns

Note 10: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 12: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 13: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation.Capacitance	95.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

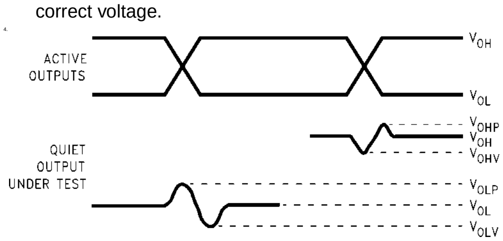
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.



V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
6. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV}on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case for active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability on the measurements.

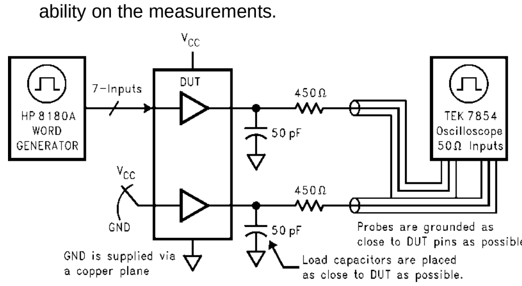
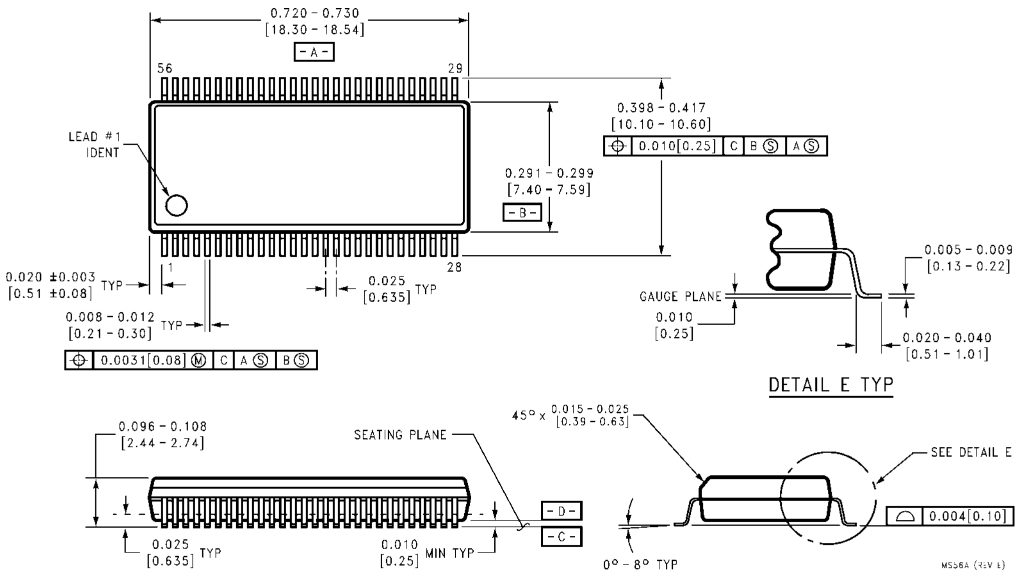


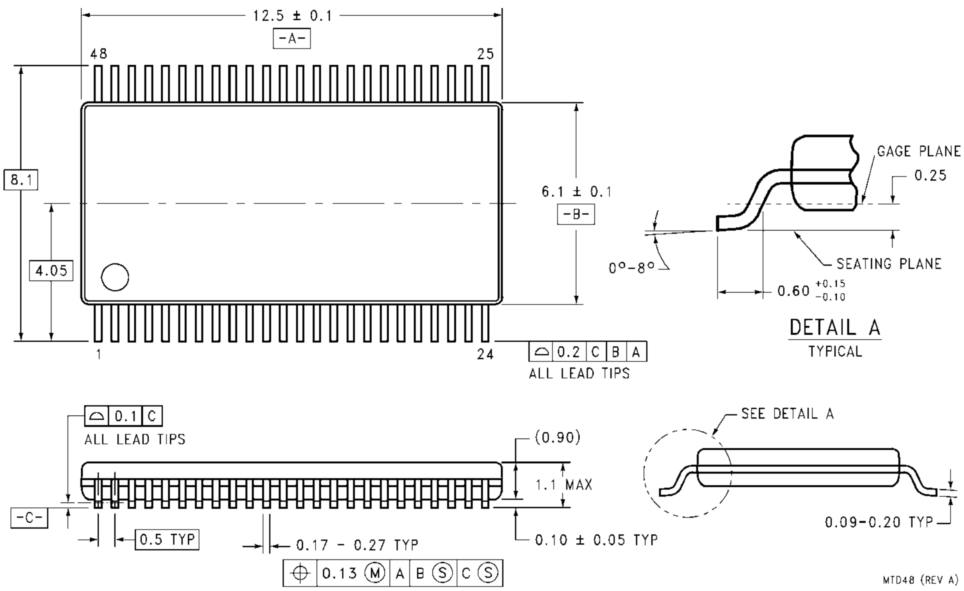
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (SSOP), JEDEC MO-153, 6.1mm Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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