捷多邦,专业PCB打样工厂,24小时加**省**UT**4**LVC1G123 SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

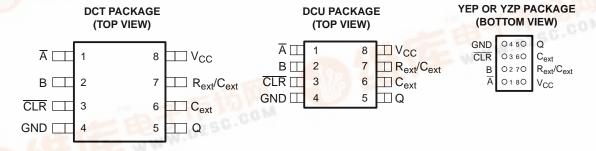
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FEATURES

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- Available in the Texas Instruments
 NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{nd} of 8 ns at 3.3 V
- Supports Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on A and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs

- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G123 is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the \overline{B} input goes high. In the second method, the \overline{B} input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the \overline{B} input is high, and the clear (\overline{CLR}) input goes high.

ORDERING INFORMATION

TA	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1G123YEPR	20
	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G123YZPR	D8_
–40°C to 85°C	SSOP - DCT	Reel of 3000	SN74LVC1G123DCTR	C23
	550F = DC1	Reel of 250	SN74LVC1G123DCTT	023_
	Vescop pour	Reel of 3000	SN74LVC1G123DCUR	Coo
	VSSOP – DCU	Reel of 250	SN74LVC1G123DCUT	C23_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
 DCU: The actual top-side marking has one additional character that designates the assembly/test site.
 YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

Popplease be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DECSCRIPTION/ORDERING INFORMATION (CONTINUED)

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\overline{A}) or high-level-active (B) input. Pulse duration can be reduced by taking \overline{CLR} low. \overline{CLR} can be used to override \overline{A} or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

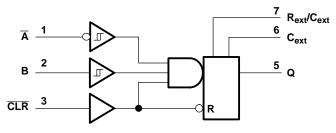
NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE

	INPUTS	OUTPUTS	
CLR	Ā	В	Q
L	Х	Х	L
X	Н	X	L ⁽¹⁾
X	Χ	L	L ⁽¹⁾
Н	L	\uparrow	Л
Н	\downarrow	Н	Л
1	L	Н	Л

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

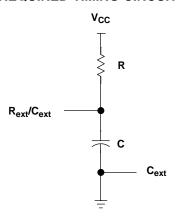
LOGIC DIAGRAM (POSITIVE LOGIC)



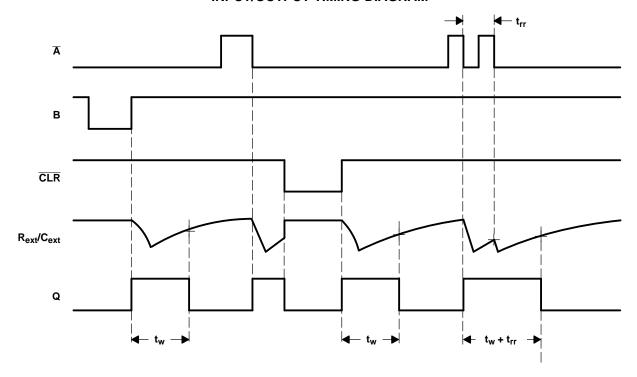


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REQUIRED TIMING CIRCUIT



INPUT/OUTPUT TIMING DIAGRAM





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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in th	e high-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in th	e high or low state (2)(3)	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current		-50	mA	
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package		227	°C/W
		YEP/YZP package		102	
T _{stg}	Storage temperature range	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



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Recommended Operating Conditions(1)

			MIN	MAX	UNIT
	O mark contracts	Operating	1.65	5.5	.,
V_{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
.,	High level inner value	V _{CC} = 2.3 V to 2.7 V	1.7		V
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
.,	Laur laural imputuralta na	V _{CC} = 2.3 V to 2.7 V		0.7	\ /
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V _I	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I _{OH}	High-level output current	V 2.V		-16	mA
		$V_{CC} = 3 V$		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 2.V		16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
D (2)	Cutamal timin a maintain a	V _{CC} = 2 V	5 k		0
R _{ext} ⁽²⁾	External timing resistance	V _{CC} ≥ 3 V	1 k		Ω
T _A	Operating free-air temperature		-40	85	°C

 ⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
 (2) R_{ext}/C_{ext} is an I/O and must not be connected directly to GND or V_{CC}.



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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TES	T CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
		$I_{OH} = -100 \ \mu A$		1.65 V to 5.5 V	V _{CC} - 0.1			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
.,		$I_{OH} = -8 \text{ mA}$		2.3 V	1.9			V
V _{OH}		I _{OH} = -16 mA		2.1/	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$		4.5 V	3.8			
		$I_{OL} = 100 \mu A$		1.65 V to 5.5 V			0.1	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
\/		$I_{OL} = 8 \text{ mA}$		2.3 V			0.3	V
V _{OL}		I _{OL} = 16 mA		3 V			0.4	V
		I _{OL} = 24 mA	3 V			0.55		
		$I_{OL} = 32 \text{ mA}$		4.5 V			0.55	
	R _{ext} /C _{ext} ⁽²⁾	B = GND,	$\overline{A} = \overline{CLR} = V_{CC}$	1.65 V to 5.5 V			±0.25	
I _I	Ā, B, CLR	V _I = 5.5 V or GND		1.05 V 10 5.5 V			±1	μΑ
I _{off}	Ā, B, Q, CLR	V_I or $V_O = 5.5 \text{ V}$		0			±10	μΑ
I _{CC}	Quiescent	$V_I = V_{CC}$ or GND,	I _O = 0	5.5 V			20	μΑ
				1.65 V			165	
				2.3 V			220	
I _{CC}	Active state	$V_I = V_{CC}$ or GND,	$R_{ext}/C_{ext} = 0.5 V_{CC}$	3 V			280	μΑ
				4.5 V			650	
				5.5 V			975	
C _i		$V_I = V_{CC}$ or GND		3.3 V		3		pF

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	PARAMETE	R TEST CO		TEST CONDITIONS		V_{CC} = 1.8 V \pm 0.15 V		V_{CC} = 2.5 V \pm 0.2 V		V_{CC} = 3.3 V \pm 0.3 V		V _{CC} = 5 V ± 0.5 V	
					MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
+ 101	Pulse duration	CLR			8		4		3		2.5		20
t _w IN	Puise duration	Ā or B trigger			8		4		3		2.5		ns
			D - 1 kO	C _{ext} = 100 pF						5.5		4.5	ns
	Pulse retrigger time		$\kappa_{\rm ext} = 1 \kappa \Omega$	$C_{\text{ext}} = 100 \text{ pF}$ $C_{\text{ext}} = 100 \mu\text{F}$						1.4		1.1	μs
t _{rr}	ruise retiligger tillle		D Eko	C _{ext} = 100 pF		75		45					ns
			$R_{\text{ext}} = 5 \text{ k}\Omega$	$C_{\text{ext}} = 100 \text{ pF}$ $C_{\text{ext}} = 100 \mu\text{F}$		1.8		1.4					μs

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		_C = 1.8 ' : 0.15 V	V	V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.5	5 V 5 V	UNIT
	(INFO1)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Ā or B		7	18.5	52	4	17	3	11.5	2	7.6	
t _{pd}	CLR	Q	5	12.4	34	3	11.5	2	8	1.5	5.5	ns
	CLR trigger		7	17.4	54	4	15.5	3	10.5	2	7	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) This test is performed with the terminal in the off-state condition.



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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	0.45.1		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT			
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN	TYP ⁽	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNII
	Ā or B			6	18.6	57	3	18.5	2	12.5	1.5	8.2	
t _{pd}	CLR	Q		4	11.6	36.5	2	12.5	1.5	8.6	1.5	6	ns
	CLR trigger			5	17.3	59	2.5	17	2	11.5	1.5	7.5	
			C_{ext} = 28 pF, R_{ext} = 2 k Ω		225	600	190	220	170	200	150	180	ns
t _w OUT ⁽²⁾		Q	$C_{\text{ext}} = 0.01 \mu\text{F},$ $R_{\text{ext}} = 10 \text{k}\Omega$		100	110	100	110	100	110	100	110	μs
			$C_{ext} = 0.1 \mu F,$ $R_{ext} = 10 k\Omega$		1	1.1	1	1.1	1	1.1	1	1.1	ms

Operating Characteristics

 $T_A = 25^{\circ}C$

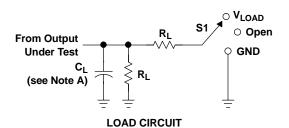
	PARAMETER	TEST CONDITIONS		V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT
Cod	Power dissipation	$\overline{A} = \text{low}, B = \text{high},$	$R_{\text{ext}} = 1 \text{ k}\Omega,$ No C_{ext}			35	37	pF
Cpd	capacitance	CLR = 10 MHz	$R_{\text{ext}} = 5 \text{ k}\Omega,$ No C_{ext}	41	40			þΓ

⁽¹⁾ $T_A = 25^{\circ}C$ (2) $t_w = Duration of pulse at Q output$

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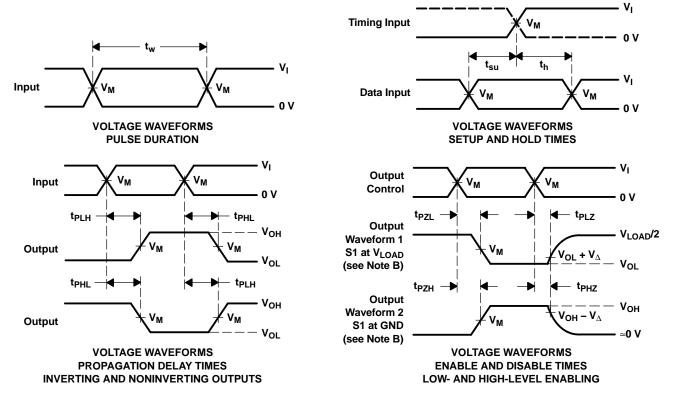


PARAMETER MEASUREMENT INFORMATION



TEST	S 1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INF	PUTS	.,	.,		_	.,
V _{CC}	V_{l}	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_{\Delta}$
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 ΜΩ	0.15 V
2.5 V \pm 0.2 V	v_{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V \pm 0.5 V	V_{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 Μ Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

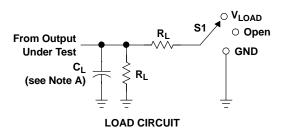
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



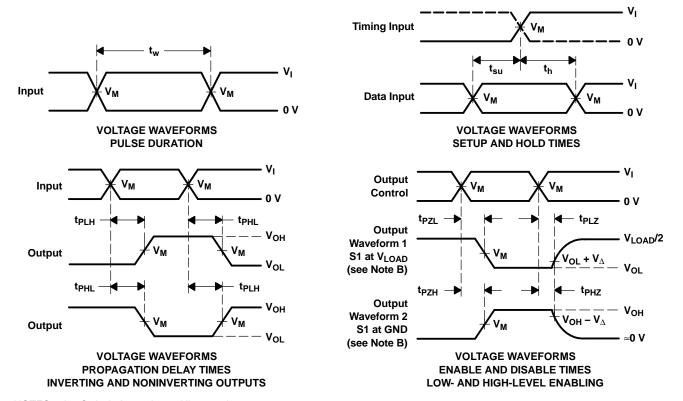
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL} t _{PLZ} /t _{PZL}	Open V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INPUTS		.,	.,	•	_	
V _{CC}	V_{l}	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	v_{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



APPLICATION INFORMATION(1)

OUTPUT PULSE DURATION

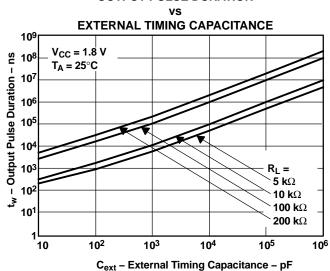


Figure 3.

OUTPUT PULSE DURATION

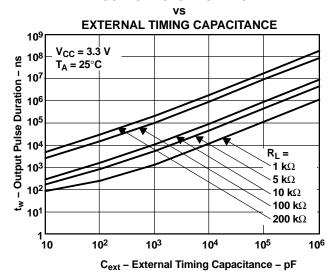


Figure 4.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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OUTPUT PULSE DURATION

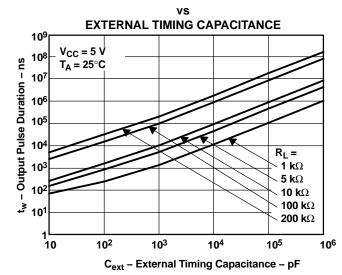


Figure 5.

OUTPUT PULSE DURATION CONSTANT

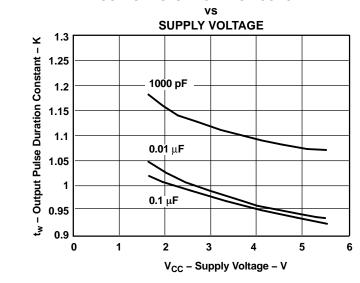
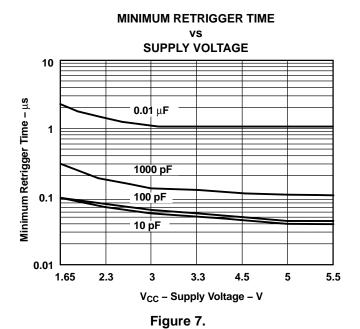


Figure 6.



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PACKAGE OPTION ADDENDUM

6-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVC1G123DCURE4	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCUTE4	ACTIVE	US8	DCU	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTT	ACTIVE	SM8	DCT	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUR	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUT	ACTIVE	US8	DCU	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123YEPR	ACTIVE	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G123YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

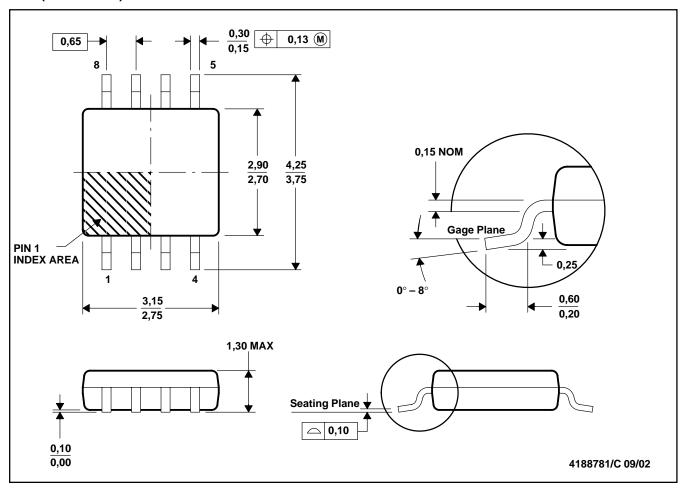
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

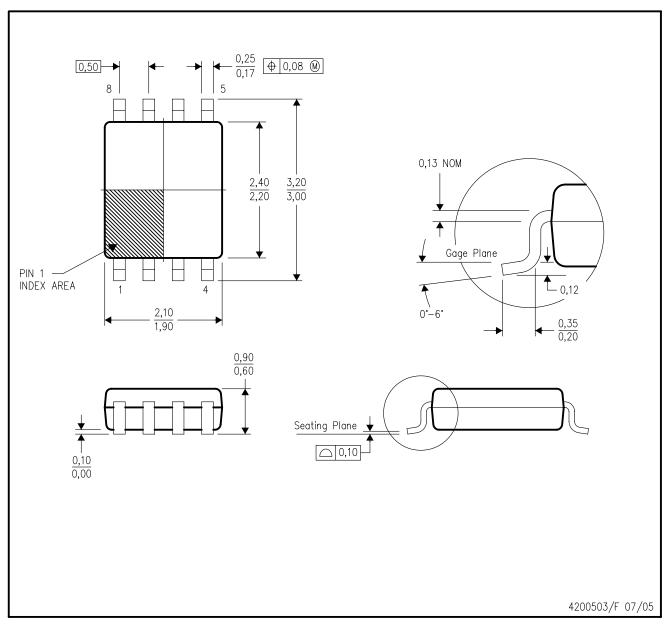


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



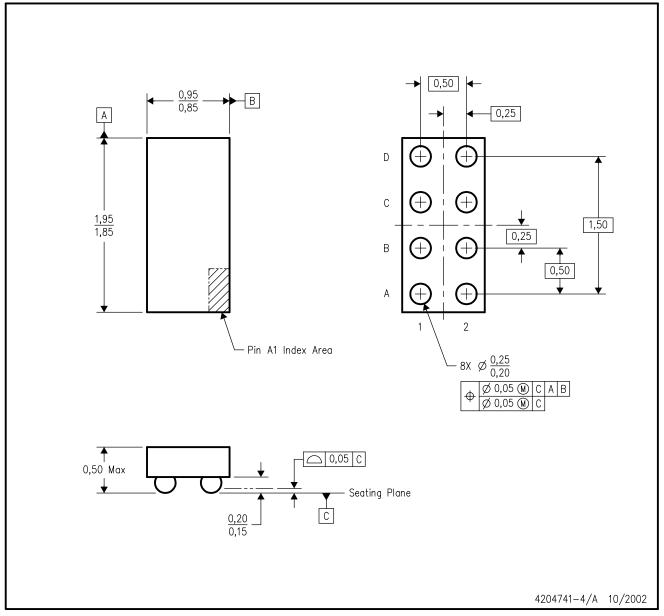
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



NOTES:

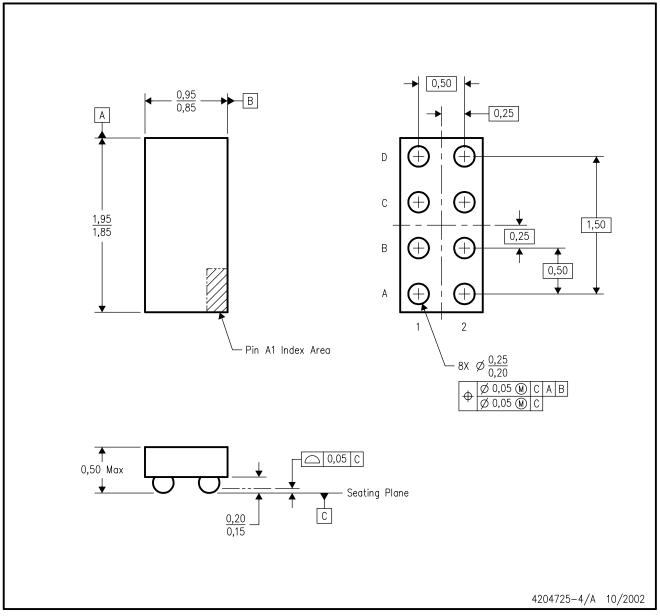
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead—free. Refer to the 8 YEP package (drawing 4204725) for tin—lead (SnPb).

NanoFree is a trademark of Texas Instruments.



YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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