

SONY

CXA1646Q/CXA1767Q

Electronic Volume

Description

The CXA1646Q/CXA1767Q is a serial control electronic volume IC for car stereos.

Features

- Loudness
- Volume control
(1dB-step from 0dB to -87dB, -∞dB)
- Balance
- Tone control
(2dB-step 2 band from -14dB to +14dB)
- Fader
(2dB-step to -20dB, -25dB, -35dB, -45dB, -60dB, -∞dB)
- Input selector (4 channels)
- Serial data control (DATA, CLK, CE)
- Single 8V power supply
- Zero-cross detection circuit

Structure

Bipolar IC

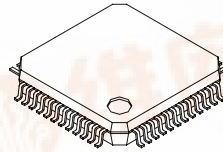
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	13	V
• Operating temperature	Topr	-40 to +85	°C
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power dissipation	Pd	350	mW (Ta = 85°C, 1646Q)
		240	mW (Ta = 85°C, 1767Q)

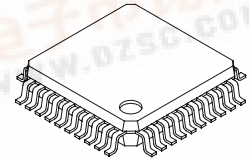
Recommended Operating Condition

Supply voltage	Vcc	6 to 12	V
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CXA1646Q
48 pin QFP (Plastic)

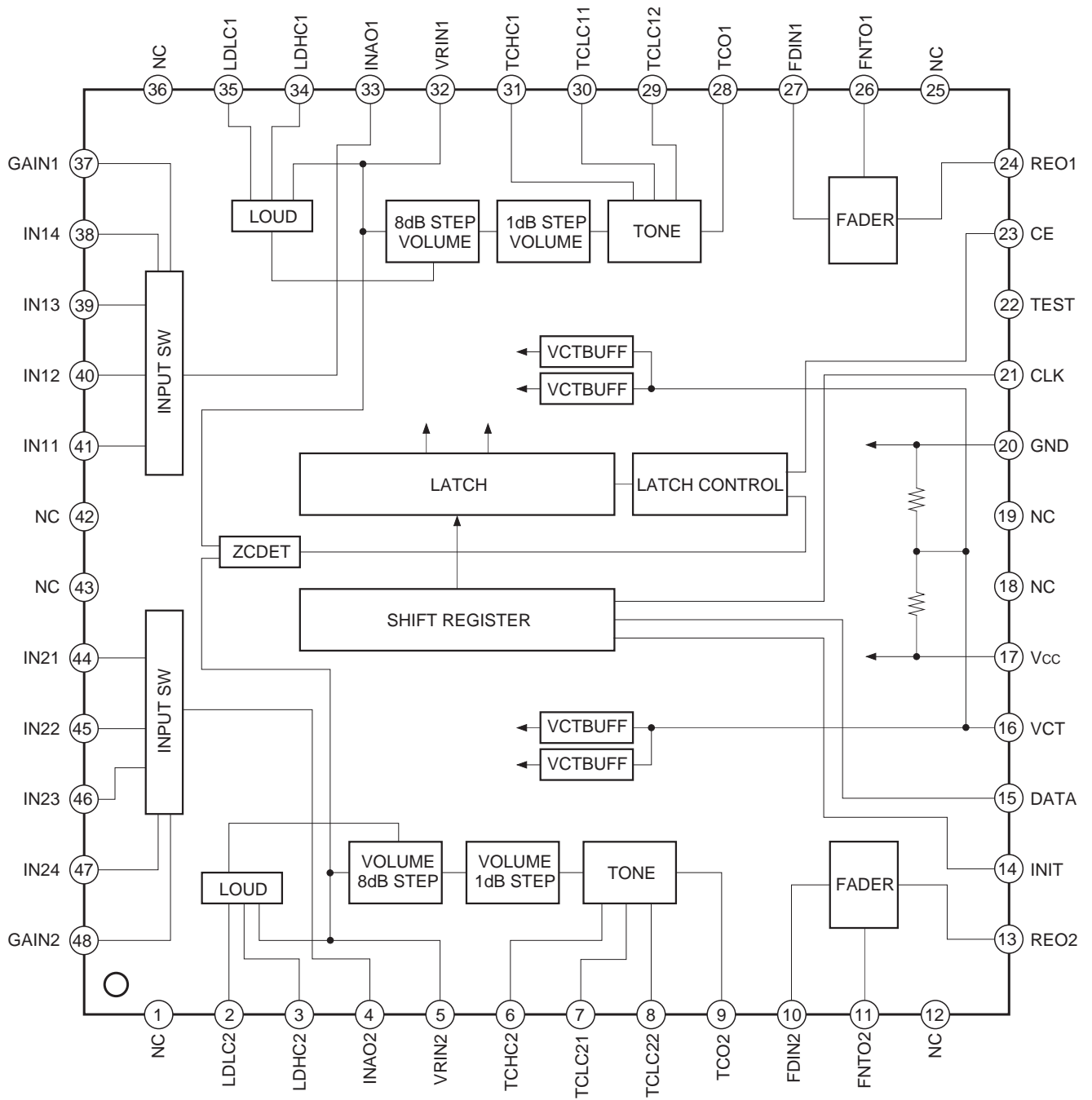


CXA1767Q
40 pin QFP (Plastic)

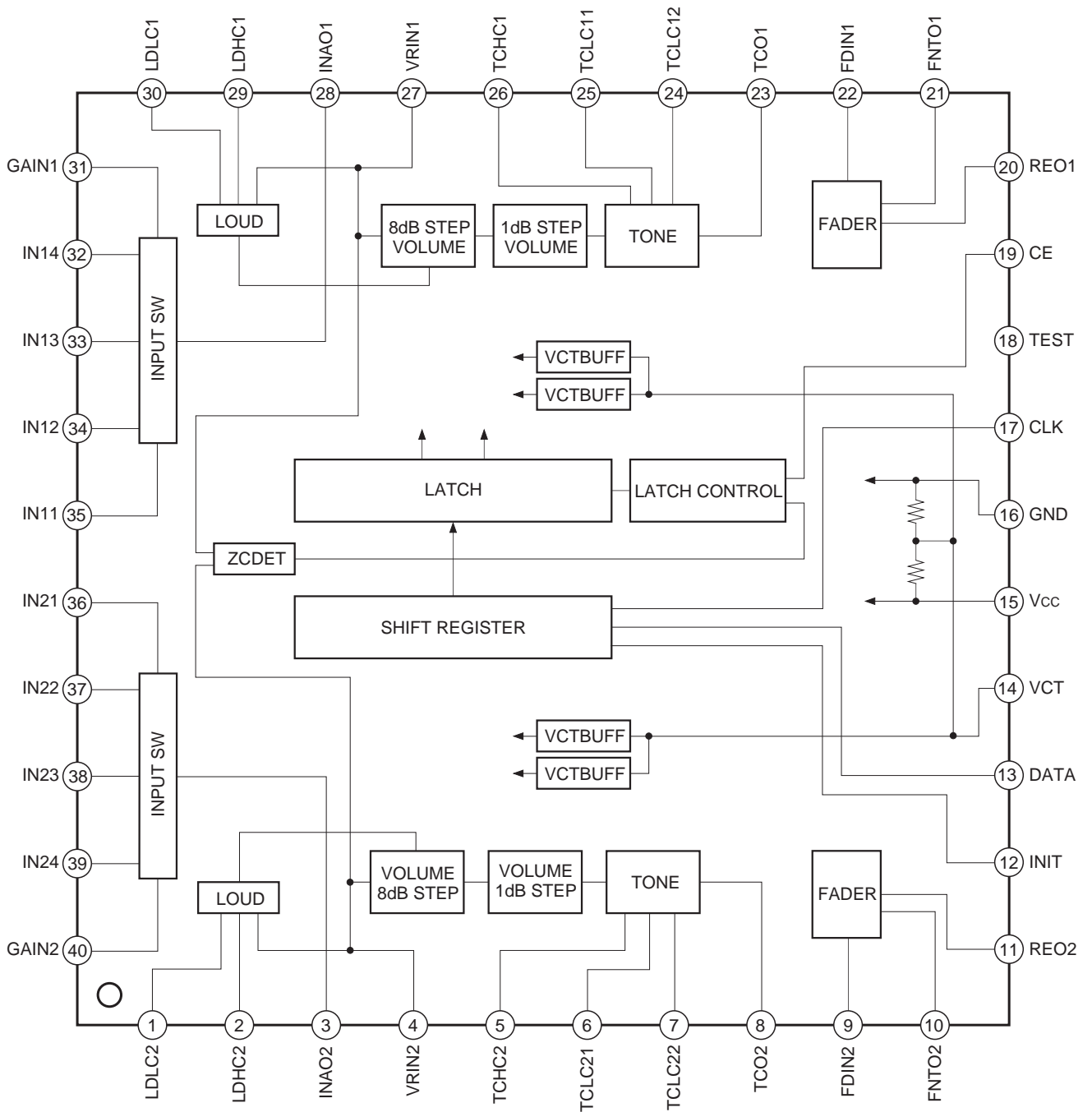


Block Diagram and Pin Configuration

CXA1646Q

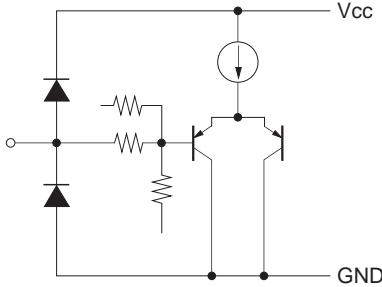
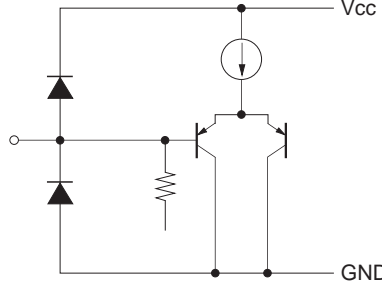
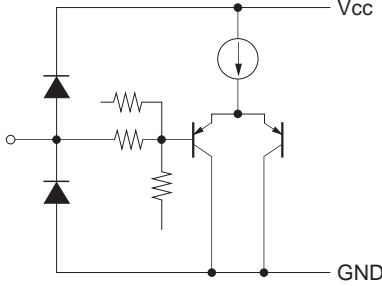
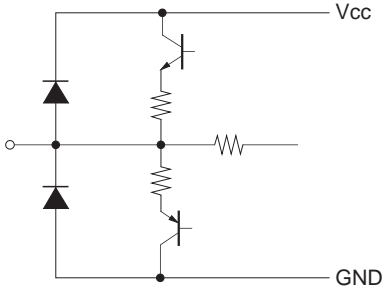


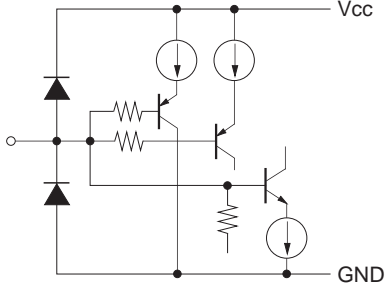
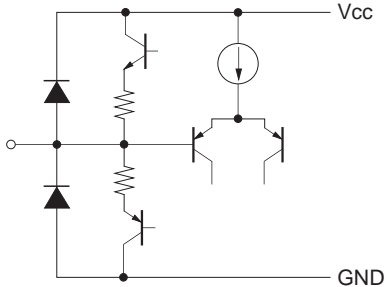
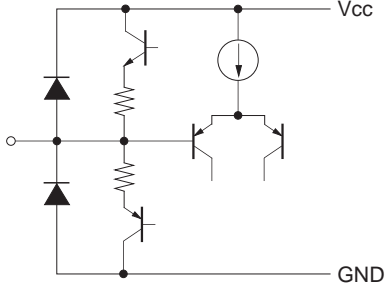
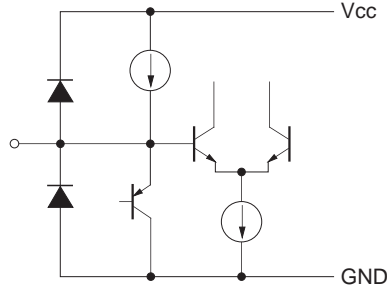
CXA1767Q

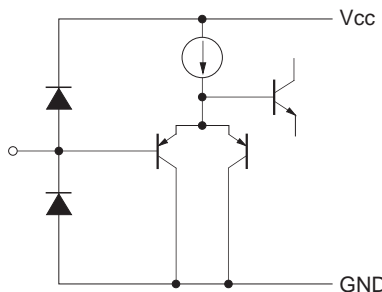
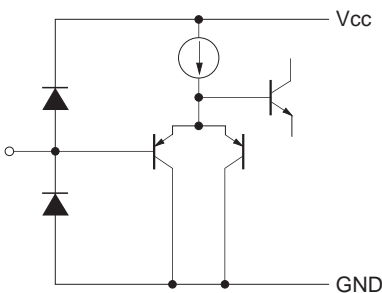
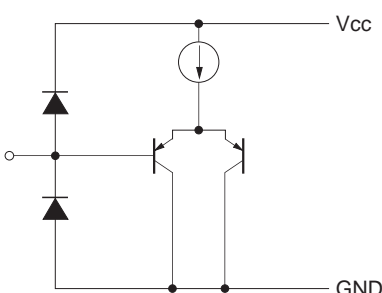


Pin Description (Pin No. in the parenthesis is for CXA1767Q.)

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
2 (1) 35 (30)	LDLC2 LDLC1	5.28kΩ VCT		Sets loudness low cut-off frequency.
3 (2) 34 (29)	LDHC2 LDHC1	7.97kΩ VCT		Sets loudness high cut-off frequency.
4 (3) 33 (28)	INAO2 INAO1	— VCT		Input selector output
5 (4) 32 (27)	VRIN2 VRIN1	50kΩ VCT		Volume input

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
6 (5) 31 (26)	TCHC2 TCHC1	5kΩ VCT		Sets tone high frequency.
7 (6) 30 (25)	TCLC21 TCLC11	8kΩ VCT		Sets tone low frequency.
8 (7) 29 (24)	TCLC22 TCLC12	8kΩ VCT		Sets tone low frequency.
9 (8) 28 (23)	TCO2 TCO1	— VCT		Tone control output

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
10 (9) 27 (22)	FDIN2 FDIN1	24kΩ VCT		Fader input
11 (10) 26 (21)	FNT02 FNT01	— VCT		Front output
13 (11) 24 (20)	REO2 REO1	— VCT		Rear output
14 (12)	INIT	— —		System reset

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
15 (13)	DATA	$\approx \infty$		Serial data input
16 (14)	VCT	$\frac{1}{2} V_{CT}$		$\frac{1}{2} V_{CC}$
17 (15)	Vcc	Vcc		+power supply
20 (16)	GND	GND		GND
21 (17)	CLK	$\approx \infty$		Serial clock
22 (18)	TEST	—		Test. Leave open.
23 (19)	CE	$\approx \infty$		Latch enable

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
37 (31) 48 (40)	GAIN1 GAIN2	10kΩ VCT		Sets input amplifier gain to 6dB by connecting to VCT. 0dB at open.
38 (32) 39 (33) 40 (34) 41 (35) 44 (36) 45 (37) 46 (38) 47 (39)	IN14 IN13 IN12 IN11 IN21 IN22 IN23 IN24	50kΩ VCT		Signal input

Reset

Reset is performed by lowering the INIT pin below 1V when CLK is High. Reset is disabled when CLK is Low. The following table shows the reset status.

Mode	Set value
INPUT	1
VRC1	-∞
VRF1	-7dB
VRC2	-∞
VRF2	-7dB
LOUD	OFF
TONE BASS	0dB
TONE TREBLE	0dB
FADER	0dB, REAR

Data Format

(a) Data allocation

FAST BIT	D1 D2	NOP	MSB
	D3 D4	ISW	
	D5	LOUD	
	D6 D7 D8 D9	VRC1	
	D10 D11 D12	VRF1	
	D13 D14 D15 D16	VRC2	
	D17 D18 D19	VRF2	
	D20 D21 D22 D23	TONE BASS	
	D24 D25 D26 D27	TONE TREBLE	
	D28 D29 D30 D31	FADER	
LAST BIT	D32	FADER SELECT	LSB

(b) Set table

• NOP

Set value	D1	D2
—	0	0

• ISW

Set value	D1	D2
IN14/IN24	1	1
IN13/IN23	1	0
IN12/IN22	0	1
IN11/IN21	0	0

• LOUD

Set value	D5
ON	1
OFF	0

• VRC1/VRC2

Set value	D6/D13	D7/D14	D8/D15	D9/D16
0	1	1	1	1
-8	1	1	1	0
-16	1	1	0	1
-24	1	1	0	0
-32	1	0	1	1
-40	1	0	1	0
-48	1	0	0	1
-56	1	0	0	0
-64	0	1	1	1
-72	0	1	1	0
-80	0	1	0	1
-∞	0	1	0	0
-∞	0	0	0	0

• VRF1/VRF2

Set value	D10/D17	D11/D18	D12/D19
0	1	1	1
-1	1	1	0
-2	1	0	1
-3	1	0	0
-4	0	1	1
-5	0	1	0
-6	0	0	1
-7	0	0	0

• **TONE BASS/TREBLE**

Set value	D20/D24	D21/D25	D22/D26
14	1	1	1
12	1	1	0
10	1	0	1
8	1	0	0
6	0	1	1
4	0	1	0
2	0	0	1
0	0	0	0

• **BOOST/CUT**

Set value	D23/D27
BOOST	1
CUT	0

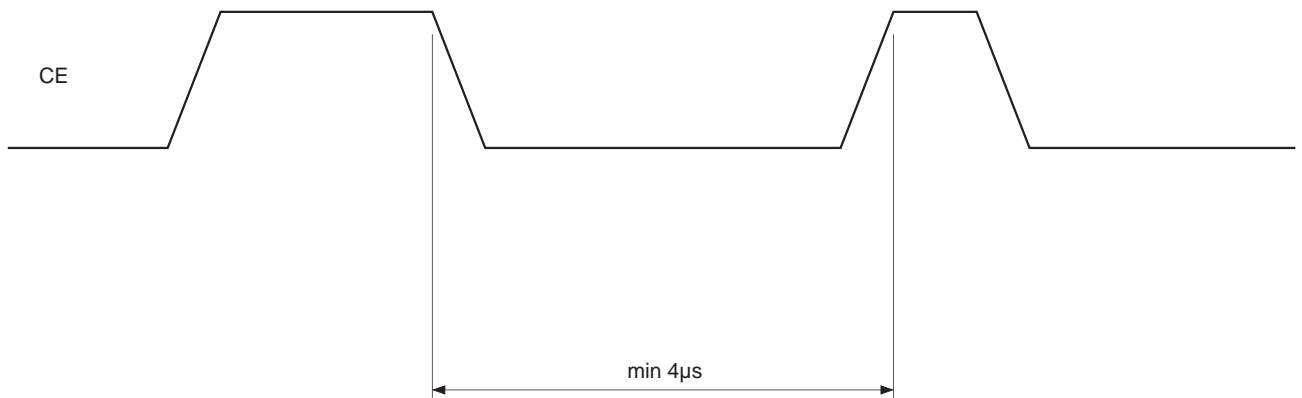
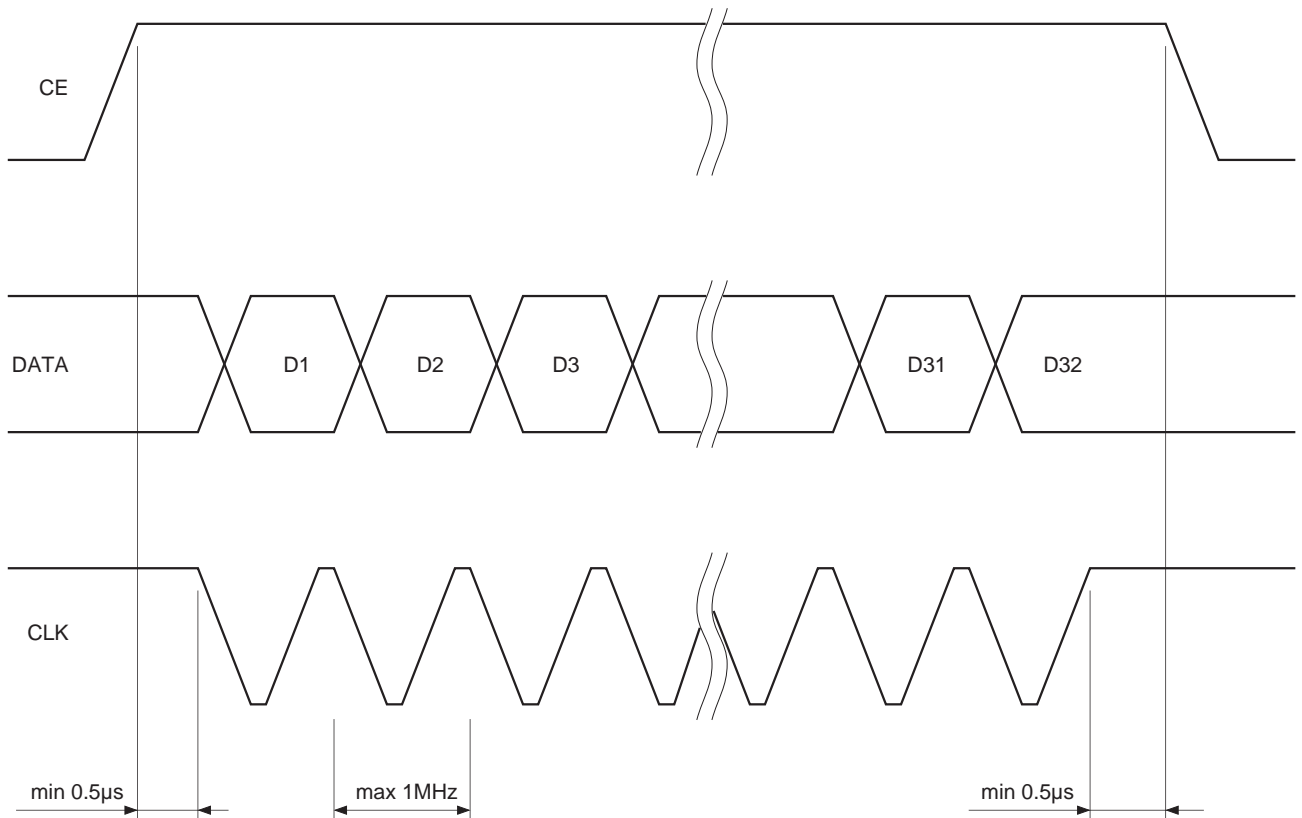
• **FADER**

Set value	D28	D29	D30	D31
-∞	1	1	1	1
-60	1	1	1	0
-45	1	1	0	1
-35	1	1	0	0
-25	1	0	1	1
-20	1	0	1	0
-18	1	0	0	1
-16	1	0	0	0
-14	0	1	1	1
-12	0	1	1	0
-10	0	1	0	1
-8	0	1	0	0
-6	0	0	1	1
-4	0	0	1	0
-2	0	0	0	1
0	0	0	0	0

• **FADER SELECT**

Set value	D32
Attenuation of front signal	1
Attenuation of rear signal	0

• DATA TIMING

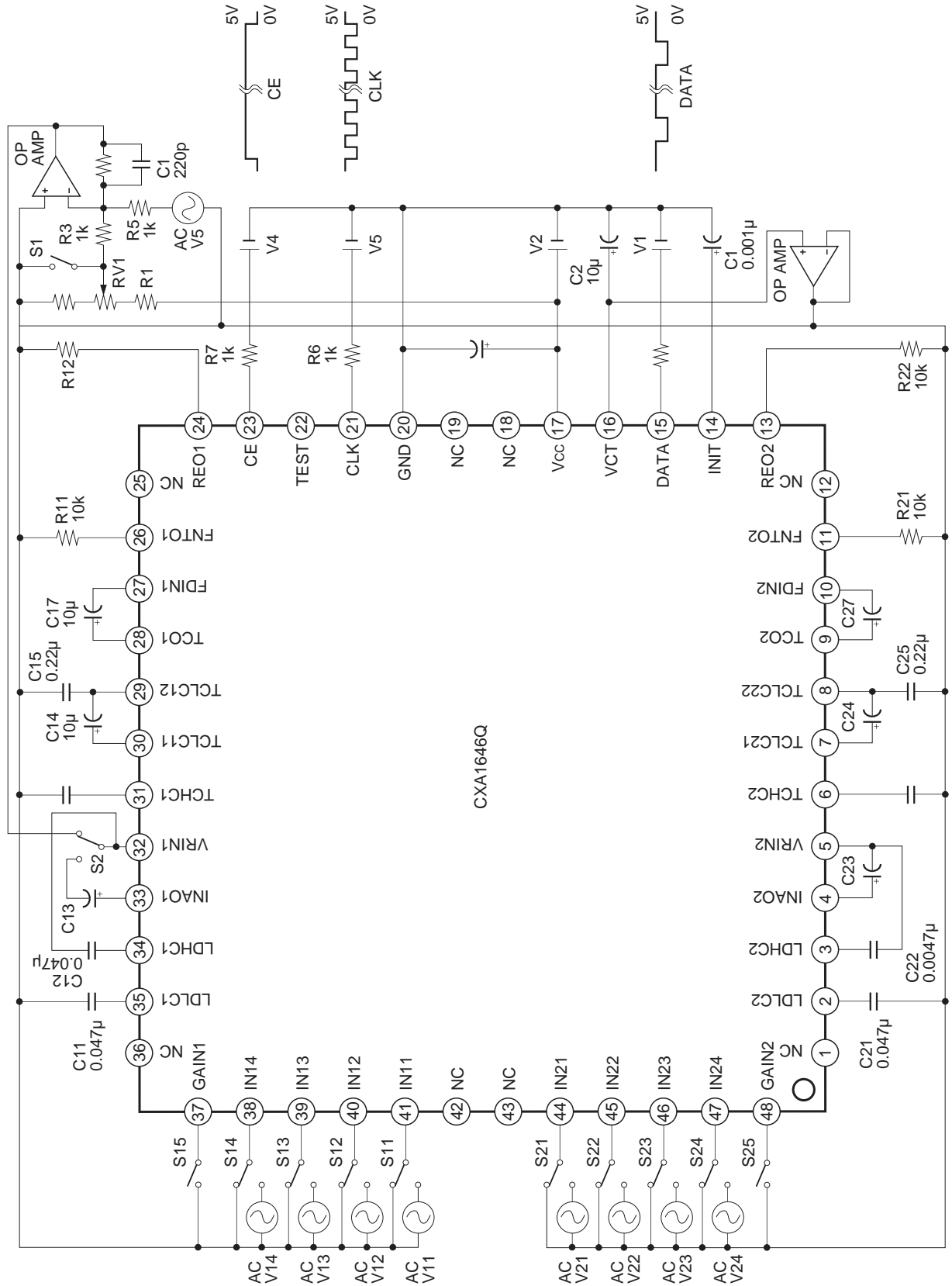


Electrical Characteristics

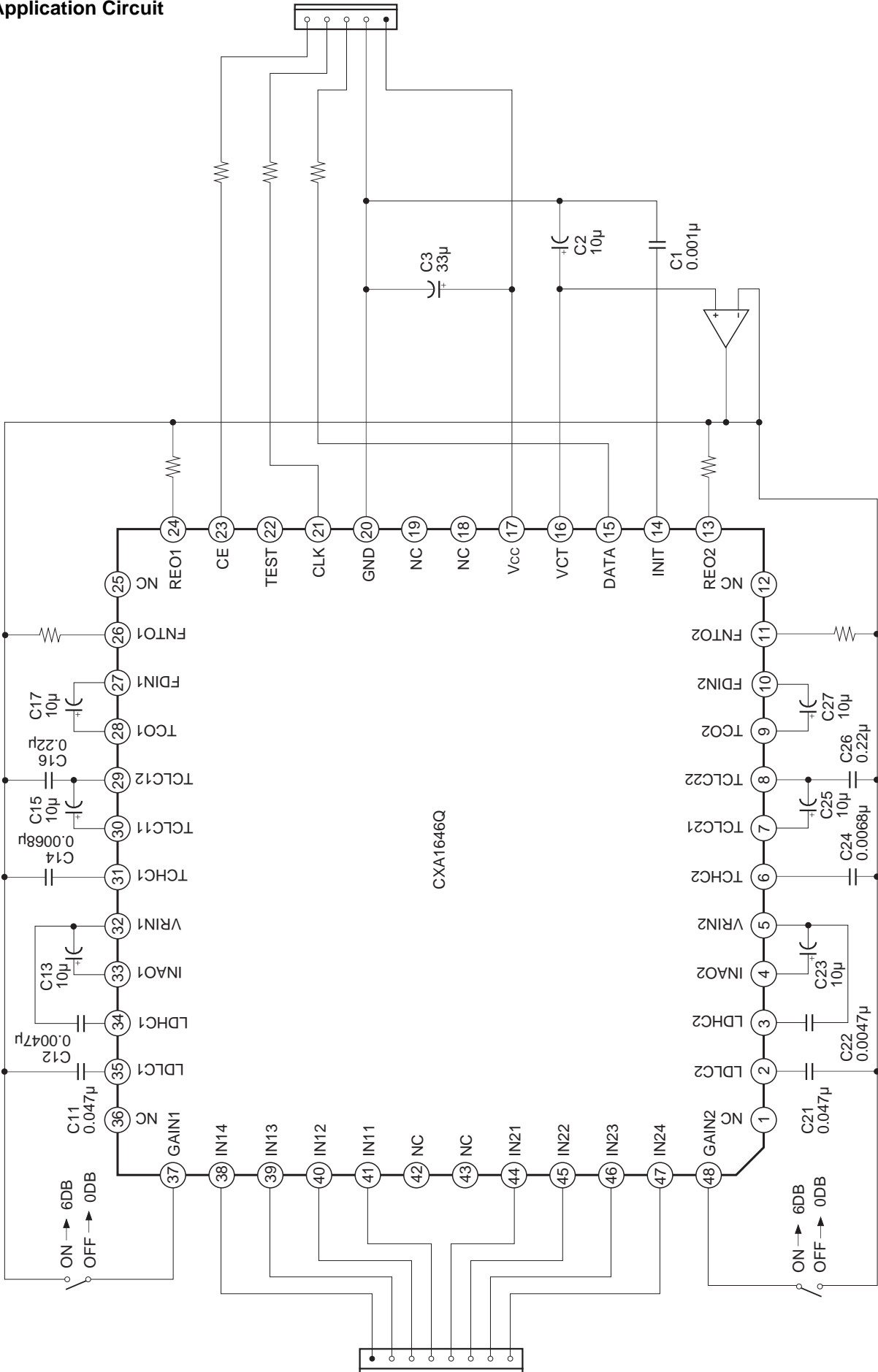
(V_{CC} = 8V, T_a = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Circuit current	I _{CC}	No signal	—	17	21	mA	
Total harmonic distortion factor	THD	1kHz, 5dBm	—	0.005	0.01	%	
Output noise voltage	V _n	Shortcircuit at input, Aweight	—	7	10	μVrms	
Maximum output voltage	V _{om}	1kHz	8	—	—	dBm	
Separation	CS	1kHz	72	90	—	dB	
Maximum attenuation factor	ATT _m		85	90	—	dB	
Loudness	LOW	G _{lb}	100Hz, VRC = -16dB	7	8	9	dB
	HIGH	G _{lh}	10kHz, VRC = -16dB	7	8	9	dB
Bass max. boost gain	G _{bb}		12	14	16	dB	
Bass max. cut gain	G _{bc}		12	14	16	dB	
Treble max. boost gain	G _{tb}		12	14	16	dB	
Treble max. cut gain	G _{tc}		12	14	16	dB	
Gain switching	G _h	GAIN = VCT	5	6	7	dB	
Input voltage	H	V _{sh}	DATA, INIT CLK, CE	3	—	6	V
	L	V _{sl}		0	—	1.5	V
Input voltage range	V _{in}	IN11 to 14 IN21 to 24 VRIN1, 2 FDIN1, 2	1	—	V _{CC} - 1	V	

Electrical Characteristic Test Circuit

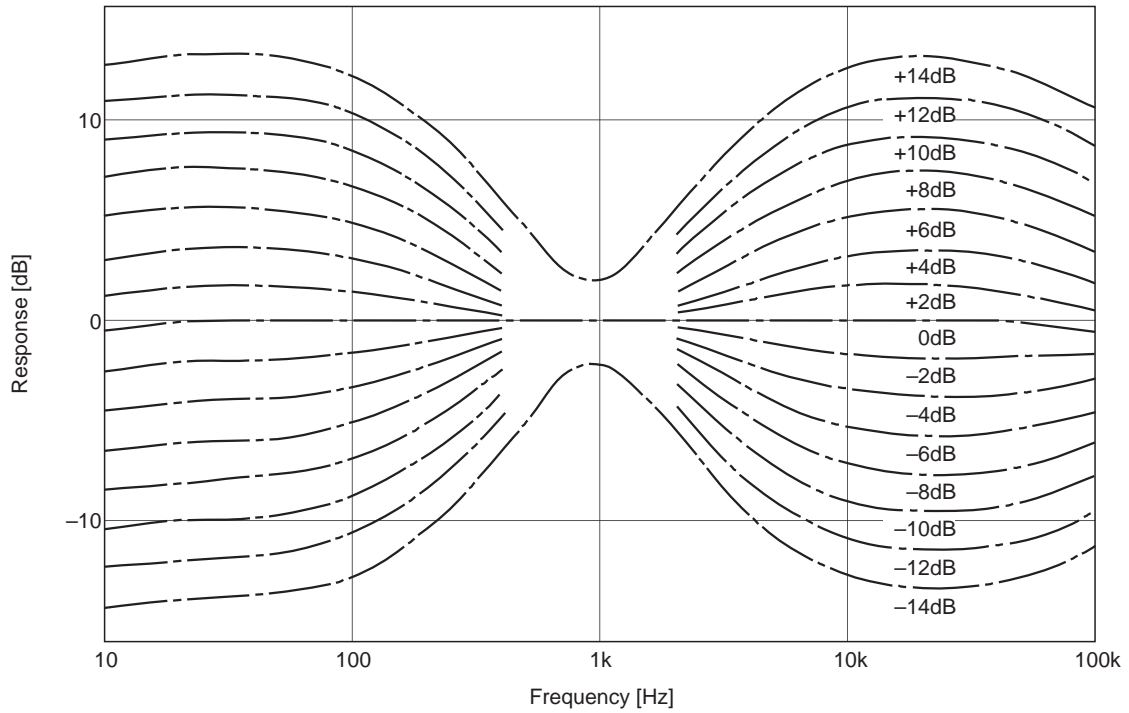


Application Circuit

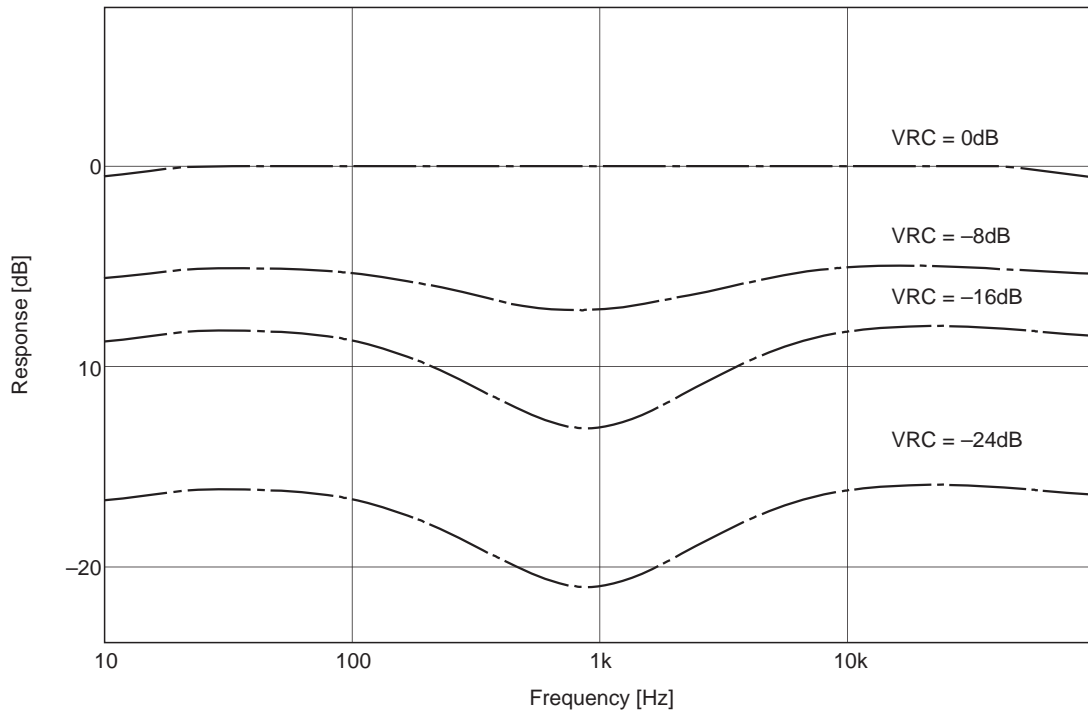


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

CXA1646Q/CXA1767Q Tone control characteristics



CXA1646Q/CXA1767Q Loud characteristics



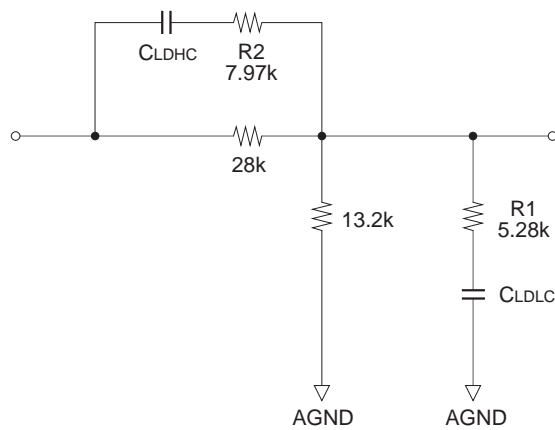
Setting Constants

• LOUD

The loudness function achieves the necessary frequency characteristics by passing through filter shown below. The resistor is built in the IC so that f_L and f_H are set by selecting $CLDLC$ and $CLDHC$.

$$1/f_L = 2\pi \cdot CLDLC \cdot R_1$$

$$1/f_H = 2\pi \cdot CLDHC \cdot R_2$$



• TONE CONTROL

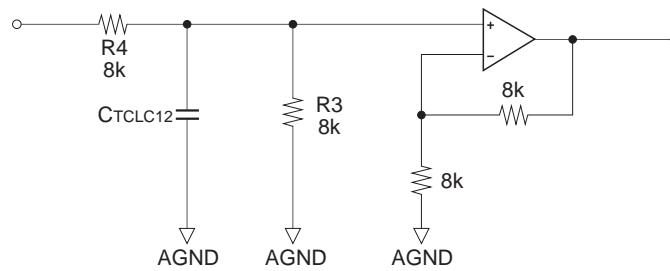
The tone control function achieves the necessary frequency characteristics by passing through LPF and HPF shown below.

The resistor is built in the IC so that f_L and f_H are set by selecting C_{TCLC12} and C_{TCHC} .

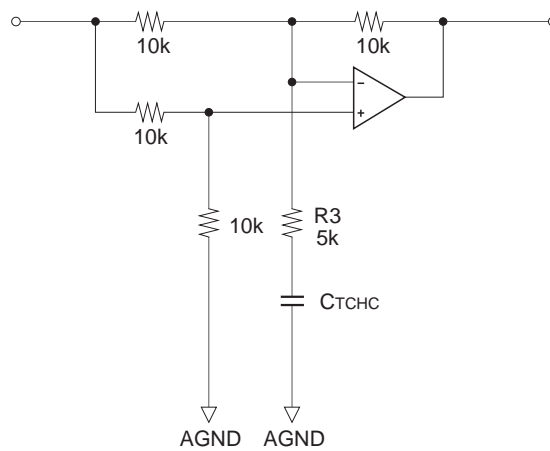
$$1/f_L = 2\pi \cdot C_{TCLC12} (R_3 // R_4)$$

$$1/f_H = 2\pi \cdot C_{TCHC} R_3$$

LPF



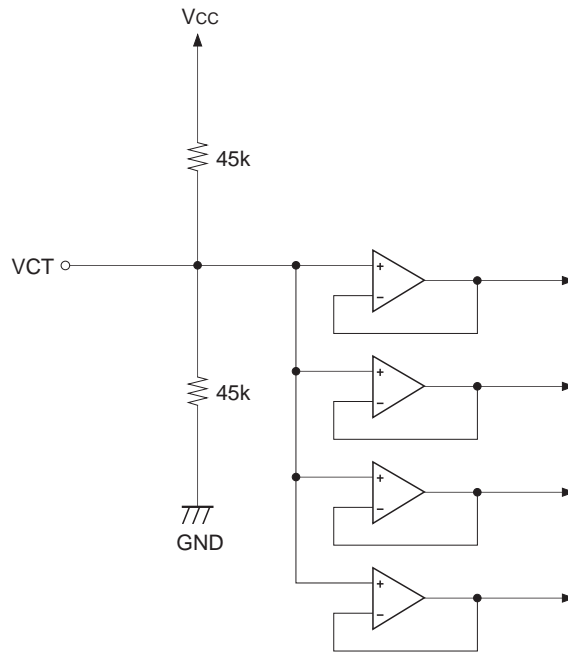
HPF



• VCT pin

The internal circuit of VCT pin has the following structure.

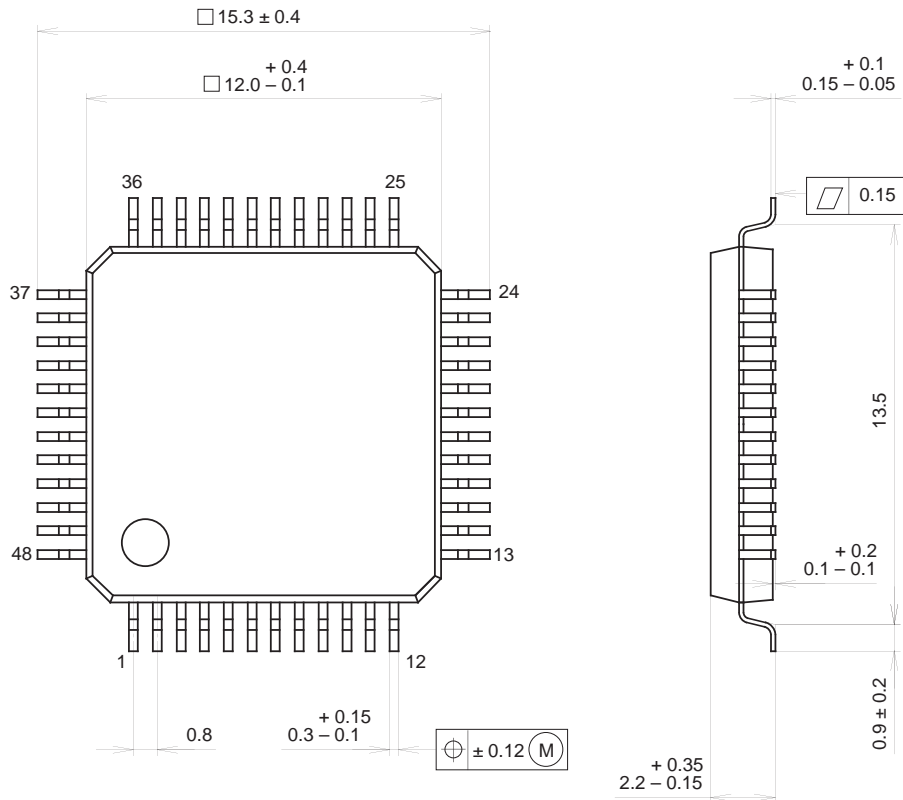
Insert a buffer when using it as a reference voltage for an external circuit.



Package Outline Unit: mm

CXA1646Q

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	—

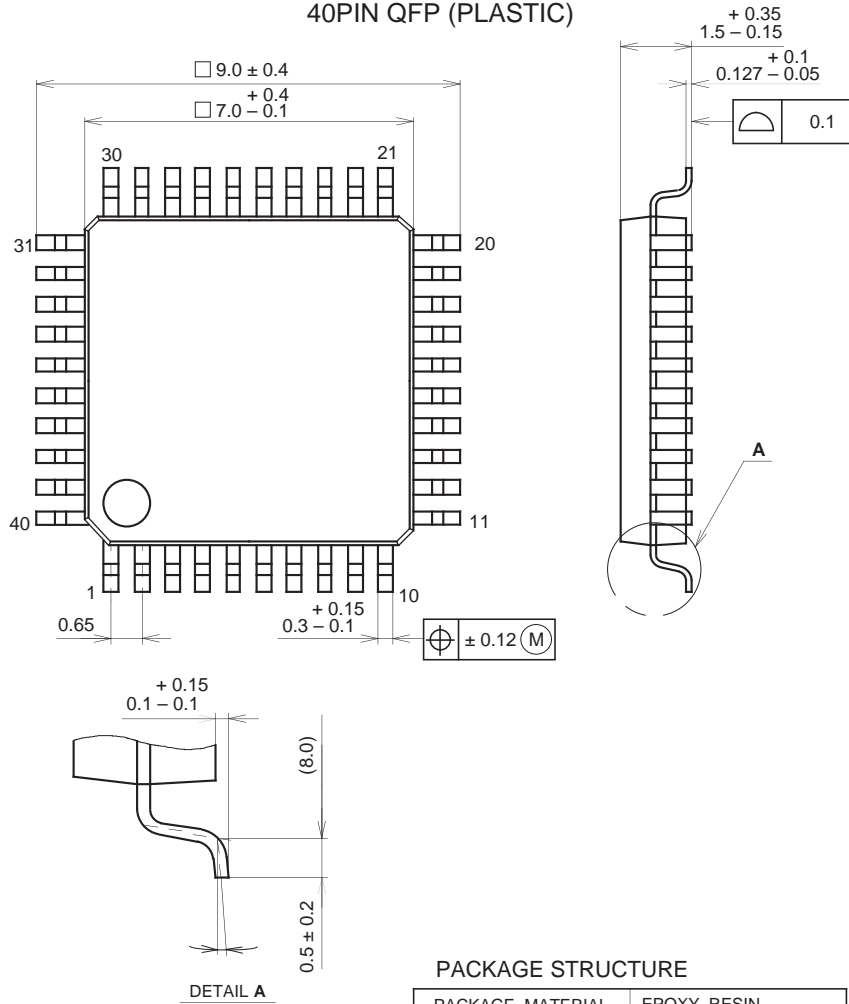
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1767Q

40PIN QFP (PLASTIC)



SONY CODE	QFP-40P-L01
EIAJ CODE	*QFP040-P-0707
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g