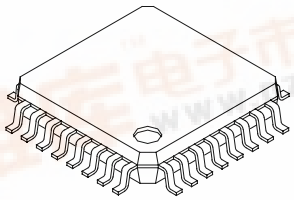
SONY

CXD1217Q

Synchronizing Signal Generator for Video Camera

32 pin QFP (Plastic)



Description

The CXD1217Q is a synchronizing signal generator for color video cameras.

Features

- Compatible with the respective systems, NTSC, PALM, PAL and SECAM
- Output is synchronized with the clock of 910f_H or 908f_H
- 25Hz offset processing by PAL system
- Color framing by the respective systems, NTSC, PALM and PAL
- Possible external synchronization by H reset, V reset and line alternate reset pins

Applications

Synchronizing signal generator for color video cameras

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

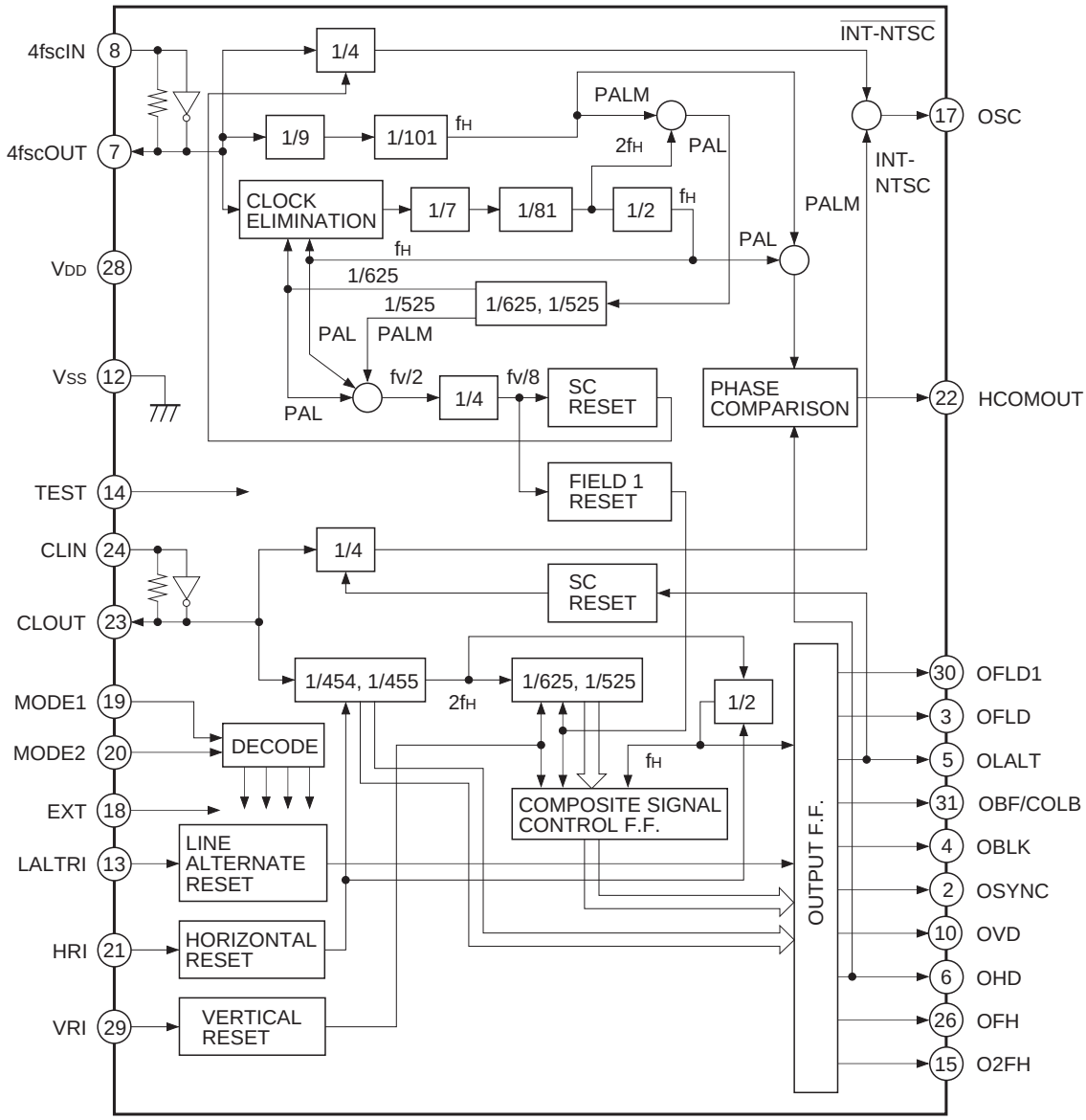
• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

E90806A79-PS

Block Diagram and Pin Configuration



Note) Pin 17 output is (a) a signal based on Pin 24 in INT mode at NTSC.
(b) each signal is based on Pin 8 in other modes.

Pin Description

Pin No.	Symbol	I/O	Description
1	NC	—	
2	OSYNC	O	Composite sync output
3	OFLD	O	Even and Odd output
4	OBLK	O	Composite blanking output
5	OLALT	O	Line alternate output
6	OHD	O	Horizontal drive output
7	4fscOUT	O	4fsc output
8	4fscIN	I	4fsc input
9	NC	—	
10	OVD	O	Vertical drive output
11	NC	—	
12	V_{SS}	—	GND pin
13	LALTRI	I	Line alternate reset input
14	TEST	I	Test input
15	O2FH	O	$2f_H$ output (Double the frequency of Pin 27)
16	NC	—	
17	OSC	O	Sub carrier output
18	EXT	I	Internal and external synchronizing modes switchover L: Internal synchronization H: External synchronization
19	MODE1	I	System selecting input 1
20	MODE2	I	System selecting input 2
21	HRI	I	Horizontal reset input
22	HCOMOUT	O	Phase comparator output
23	CLOUT	O	Clock output
24	CLIN	I	Clock input
25	NC	—	
26	OFH	O	Horizontal frequency output
27	NC	—	
28	V_{DD}	—	Power supply pin
29	VRI	I	Vertical reset signal
30	OFLD1	O	First field output
31	OBF/COLB	O	Burst flag/color blanking output
32	NC	—	

Electrical Characteristics

DC characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage 1	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	V_{SS}		0.4	V
Output voltage 2*1	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	V_{SS}		0.4	V
Output voltage 3*2	V_{OH}	I_{OH} = –4mA	V_{DD}/2			V
	V_{OL}	I_{OL} = 8mA			V_{DD}/2	V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Input current*3 (Pull-down pin)	I_{IH}	V_{IH} = V_{DD}	20	50	120	µA
Output leak current*1	I_{LZ}	At high impedance		±30		nA
Power current supply	I_{DD}	At output pin in no-load		8		mA
Feedback resistance*4	R_{FB}	V_{DD} = 5V	250k		2.5M	Ω

*1 HCOMOUT pin

*2 4fscOUT and CLOUT pins

*3 LALTRI, TEST, EXT, MODE1 and MODE2 pins

*4 4fscOUT, 4fscIN, CLOUT and CLIN pins

I/O capacitance

(V_{DD} = V_I = 0V, f_M = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}		—	—	9	pF
Output pin	C_{OUT}		—	—	11	pF

Description of Operation (See Block Diagram.)

The CXD1217 is applicable to four systems; namely, NTSC, PAL, PALM and SECAM. In order to realize them, the following relative equations of Sub-carrier (4fsclN) and Clock (CLIN) are adopted .

	Sub carrier	Clock
NTSC	4fsc = 910f_H	910f_H
PAL	4fsc = 1135f_H + 2fv	908f_H
PALM	4fsc = 909f_H	910f_H
SECAM	—	908f_H

As it is obvious from the above equations, the 4fsc and clock frequency do not coincide with each other in the PAL and PALM. Therefore matching of the clock frequency is carried out by providing PLL.

1 . MODE specified input

The CXD1217 provides four inputs to specify the respective modes.

* EXT input: Set this pin to V_{DD} side, and it becomes into external synchronizing mode. At this time, the counters in connection with the PLL loop as shown in the upper part of the block diagram become into stand still state.

* MODE1 and MODE2 inputs: These are inputs for the system selection.

MODE1	MODE2	System	
0	0	NTSC	
0	1	SECAM	
1	0	PALM	"0" → V_{SS}
1	1	PAL	"1" → V_{DD}

* TEST input: An input to be used to measure IC. This input is normally kept opened.
(Because it is dropped internally to Vss with MOS resistance.)

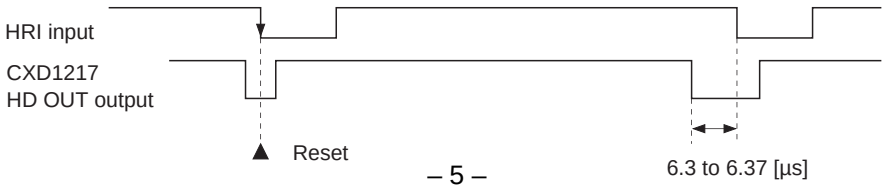
2. Reset operation

The CXD1217 has three reset inputs ; namely, HRI, VRI, LALTRI, and it works to perform reset operation when it detects falling edge. These three inputs are so designed as to take in synchronization with the IC internal clock. Therefore, it is a prerequisite that both systems should have clock frequencies that are matched as a reset operation to each other (GEN locked).

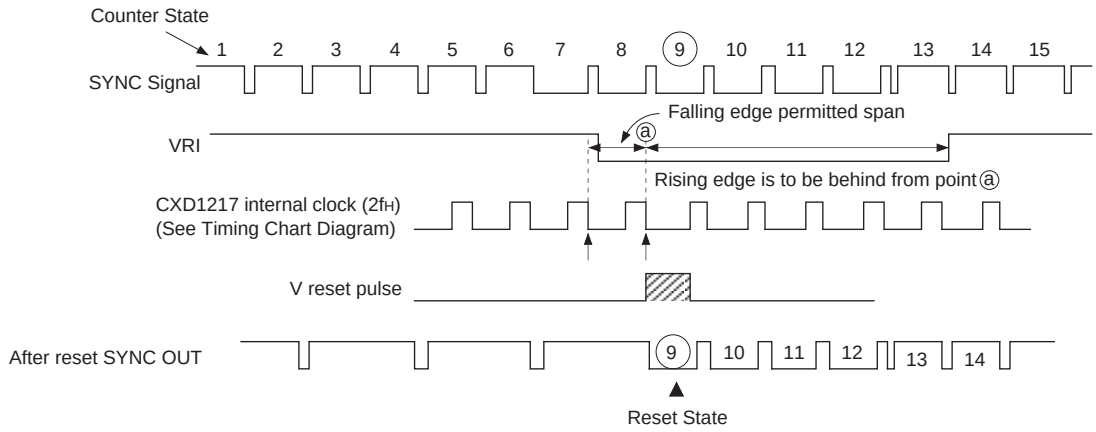
• H reset (HRI input)

When the HRI input is continuous with H synchronization, resetting is activated with the initial falling edge, and for the subsequent edges they do not have to be reset unless they are deviated more than 2-bit (140ns) against the initial edge in the internal clock. That is, if the jitter of HRI input is less than 140ns, it is absorbed. The minimum resetting pulse width is over 0.3µs.

The phase to be reset is the advanced point of 6.3 to 6.37µs (= 90 to 91-bit × 70ns) than the HRI input as shown in the diagram below.



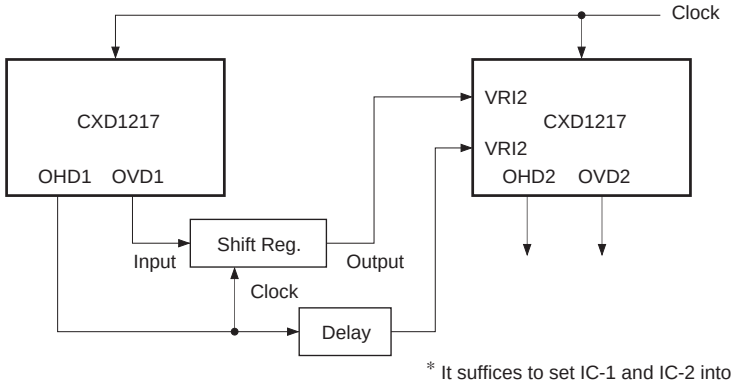
• V reset (VRI input)
When the VRI is input as shown in figure below, OSYNC can be reset at the same phase with the SYNC signal.



Since the falling edge point in the diagram above (marked with ↑) is the boundary of reset, if the falling edge of the VRI input traverses that point, it causes 1/2H deviation to the reset state.
Accordingly, if resetting is applied between two similar systems whose frequency are different, the V to which resetting is applied generates jitter of 1/2H. (When the resetting is applied continuously.)

• LALT reset (LALTRI input)
Phase relation between LALTRI pulse polarity and 2fH is the same as in the case of V resetting.

Resetting operation is basically required only in the external synchronizing mode (GEN LOCK mode). However, even in the internal synchronizing mode, it sometimes requires H and V outputs whose phases are deviated against a certain output. In that case, it suffices to use two CXD1217s and conduct the operation as follows:



* It suffices to set IC-1 and IC-2 into INT mode.

By varying the Delay and Shift Reg. of the above diagram, any phases of OHD2 and OVD2 can be provided against the respective OHD1 and OVD1.

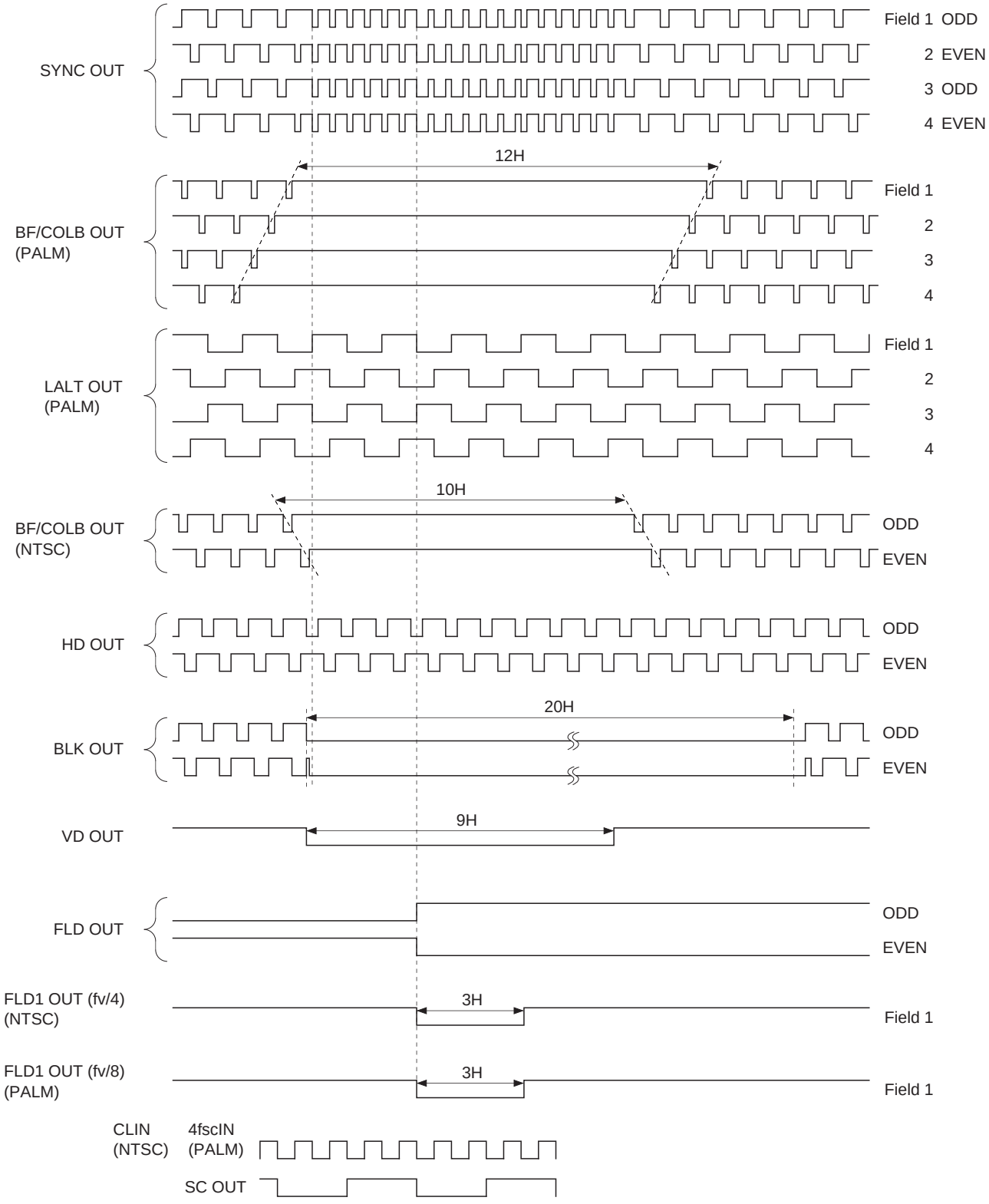
3. Color framing

In the case of internal synchronization in the individual NTSC, PAL and PALM systems, the phase relationships between SYNC of the 1st field and sub-carrier are kept stable regardless of the power supply being ON or OFF. However, as the PAL and PALM systems are comprised of PLL, the absolute values concerning the phase according to variation of the ambient temperature drifts.

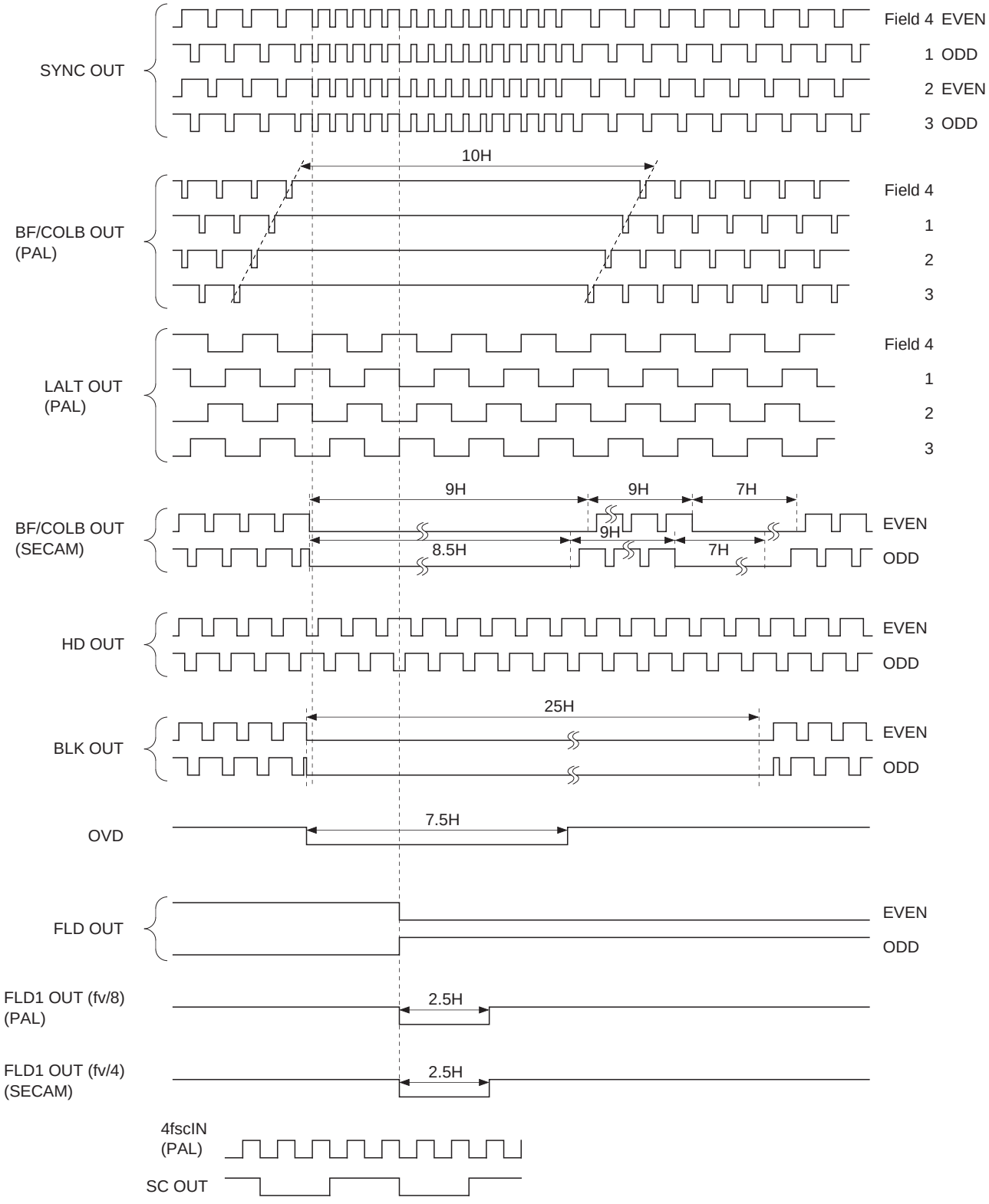
Timing Chart

Output Timing Chart Diagram

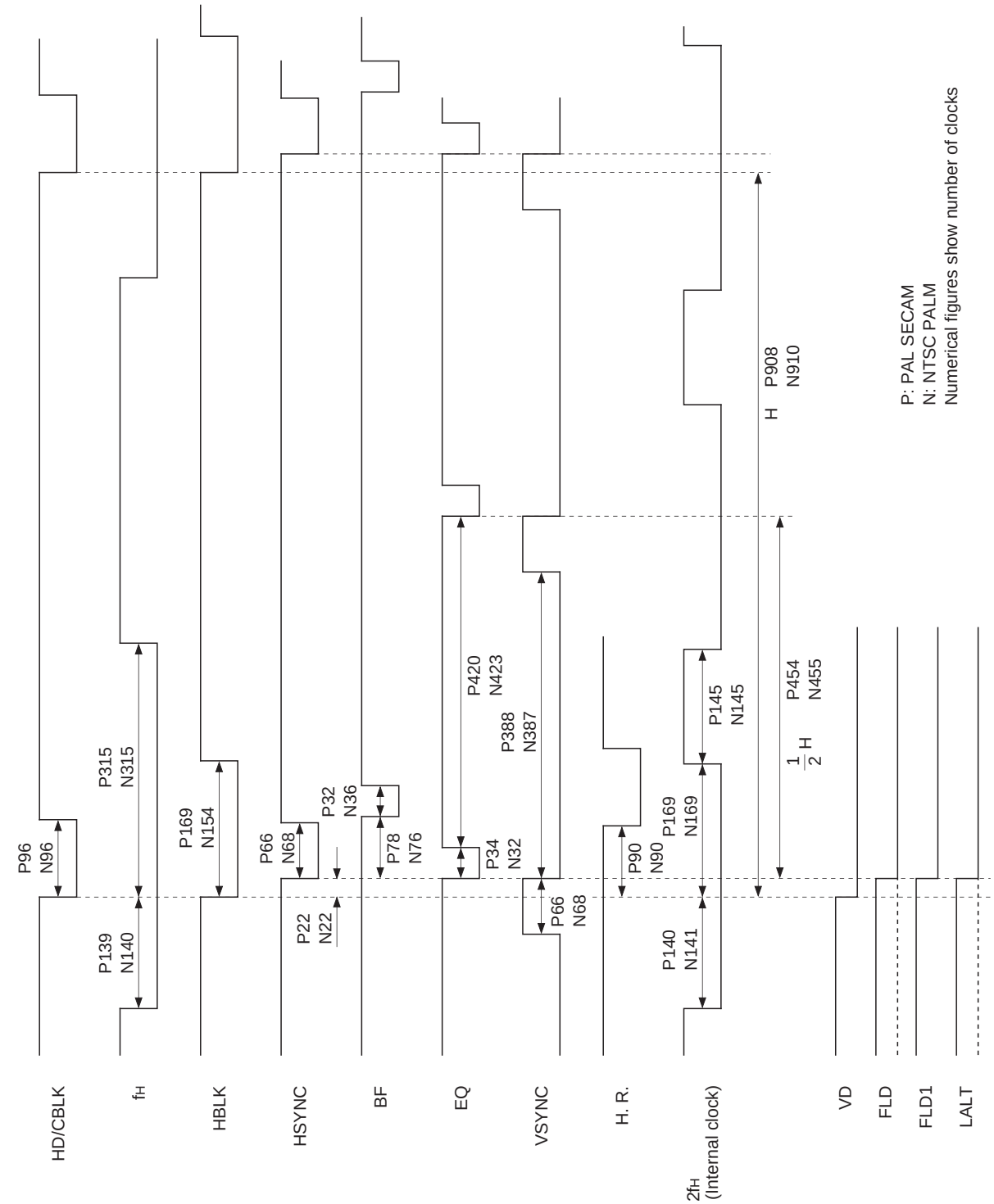
CXD1217 NTSC, PALM



CXD1217 PAL, SECAM



CXD1217 f_H

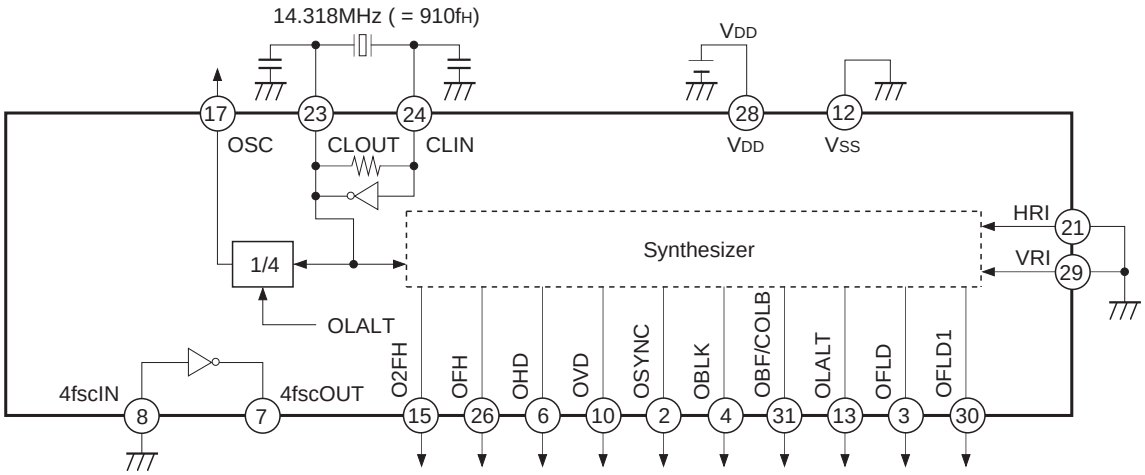

HD/CBLK
fH
HBLK
HSYNC
BF
EQ
VSYNC
H. R.
2fH (Internal clock)
VD
FLD
FLD1
LALT
P96 N96
P139 N140
P315 N315
P169 N154
P66 N68
P22 N22
P32 N36
P78 N76
P34 N32
P420 N423
P388 N387
P66 N68
P90 N90
P140 N141
P169 N169
P145 N145
1/2 H
P454 N455
H P908 N910
P: PAL SECAM
N: NTSC PALM
Numerical figures show number of clocks

Application Circuit

Basic connection in individual systems

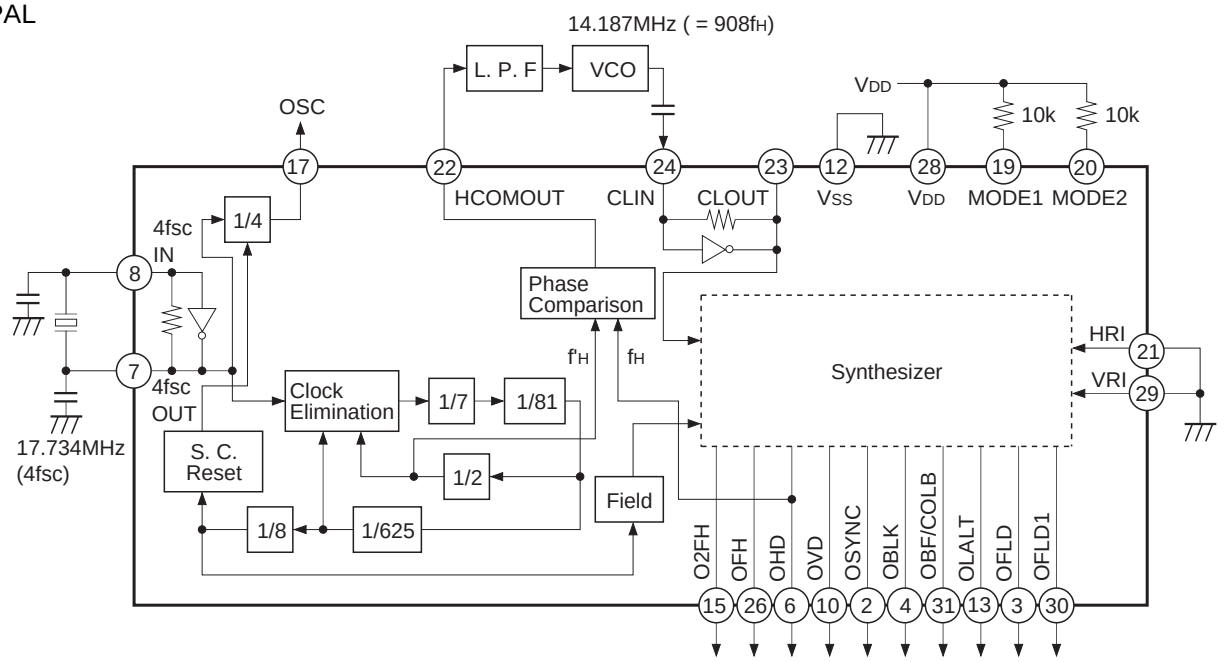
Basic connection in individual systems at internal synchronization mode (EXT input = "0") is as follows. See waveform diagram for each output.

• NTSC



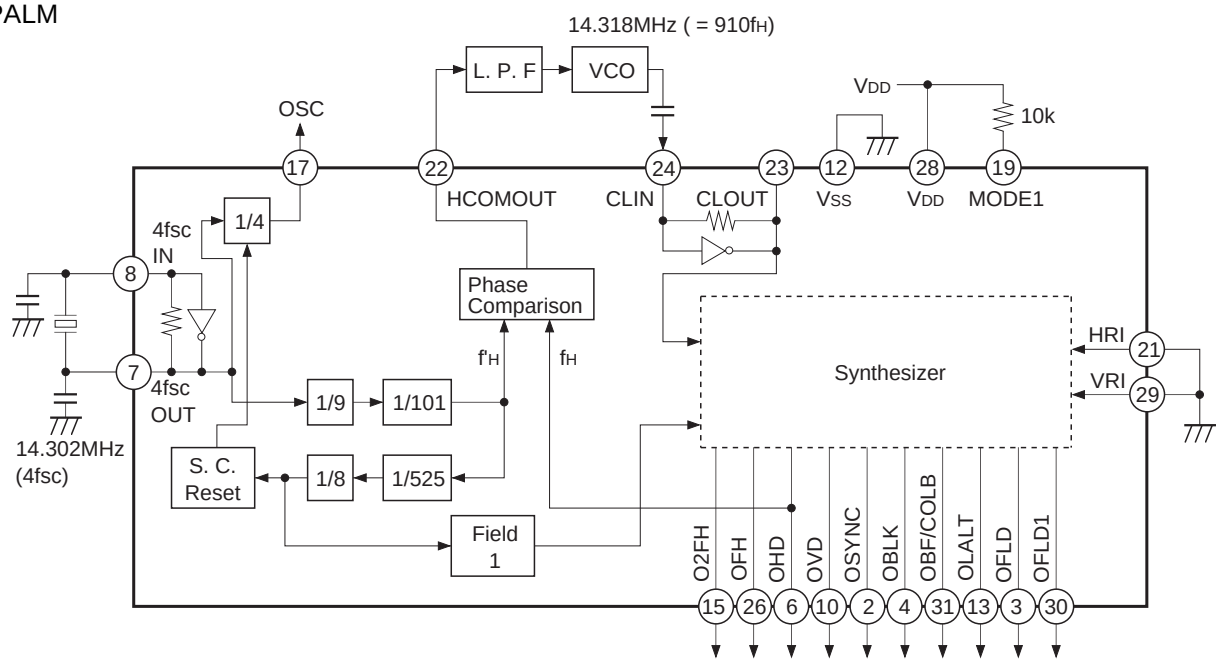
* H/2 is output for LALT OUT even in NTSC mode.
* MODE1, MODE2, EXT, TEST and LALTRI pins can be kept open.
  (If noise annoys, connect to Vss by low impedance.)

• PAL



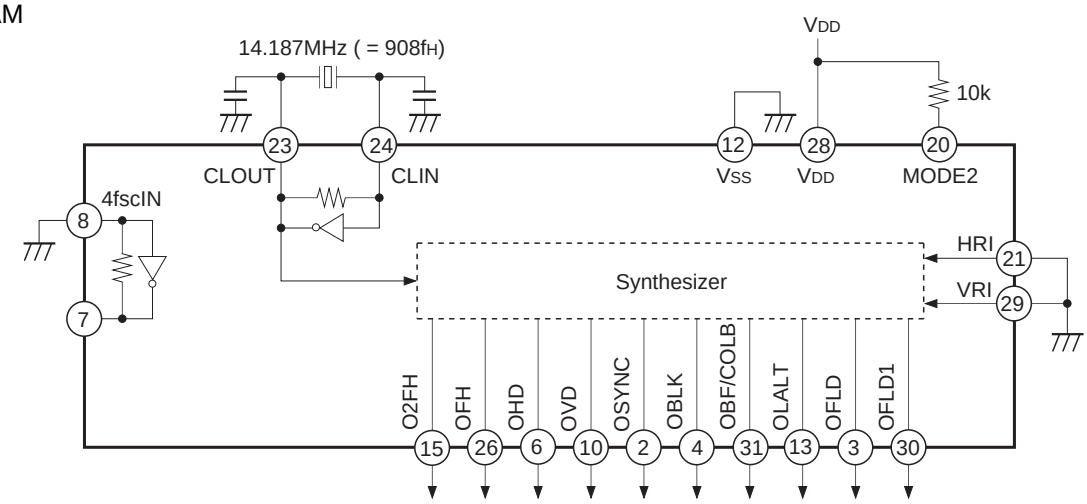
* Inverter of CLIN or CLOUT pins are usable as VCO.

• PALM



* Internal inverter is usable as VCO.

• SECAM



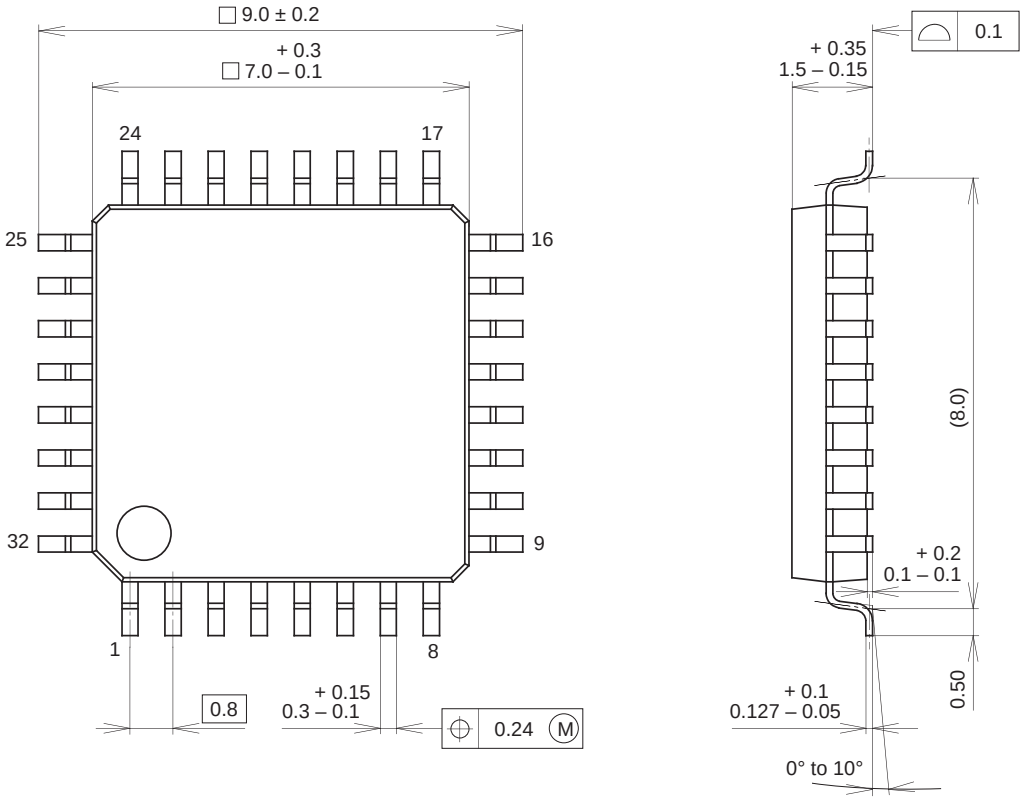
* COLB is output to BF/COLB OUT pin.

* SDR and SDB are formed in PLL using 908fH.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g