SONY

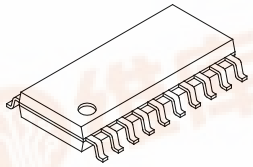
CXD1250M/N

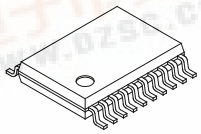
Vertical Clock Driver for CCD Image sensor

Description

CXD1250M/N is a clock driver developed for the vertical register drive of CCD Image sensor.

CXD1250M	CXD1250N
20 pin SOP (Plastic)	20 pin SSOP (Plastic)





Features

4-channel vertical clock driver and 1 channel substrate driver are built-in.

Application

CCD camera

Structure

CMOS

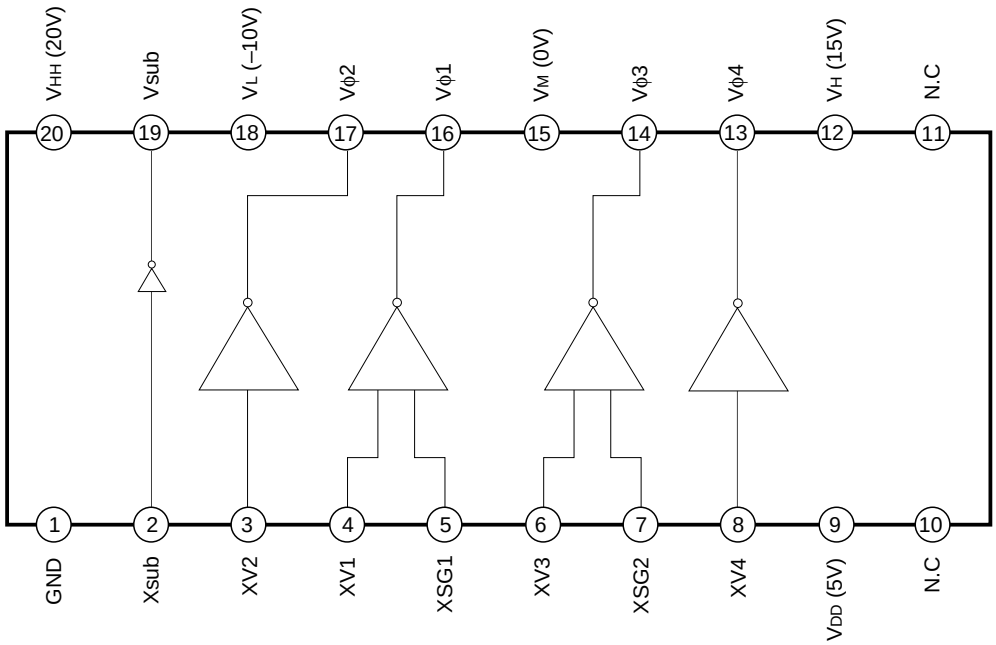
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_L – 0.3 to V_L + 35.0	V
	V_M	V_L – 0.3 to V_L + 35.0	V
	V_H	V_L – 0.3 to V_L + 35.0	V
	V_{HH}	V_L – 0.3 to V_L + 35.0	V
• Input volltage	V_I	V_L – 0.3 to V_{DD} + 0.3	V
• Output voltage	MVϕ (pins 13, 17)	V_L – 0.3 to V_M + 0.3	V
• Output voltage	HVϕ (pins 14, 16)	V_L – 0.3 to V_H + 0.3	V
• Output voltage	HHVϕ (pin 19)	V_L – 0.3 to V_{HH} + 0.3	V
• Operating temperature	Topr	–25 to +85	°C
• Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0 ± 0.5	V
	V_M	V_L + 10.0	V
	V_H	V_L + 25.0	V
	V_{HH}	V_L + 30.0	V
	V_L	–10.0	V
• Operating temperature	Topr	–20 to +75	°C

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	GND
2	Xsub	I	Output control (Vsub)
3	XV2	I	Output control (Vφ2)
4	XV1	I	Output control (Vφ1)
5	XSG1	I	Output control (Vφ1)
6	XV3	I	Output control (Vφ3)
7	XSG2	I	Output control (Vφ3)
8	XV4	I	Output control (Vφ4)
9	V_{DD}	—	Power supply (5V)
10	NC	—	
11	NC	—	
12	V_H	—	Power supply (15V)
13	Vφ4	O	Output (2 level : V_M, V_L)
14	Vφ3	O	Output (3 level : V_H, V_M, V_L)
15	V_M	—	Power supply (0V)
16	Vφ1	O	Output (3 level : V_H, V_M, V_L)
17	Vφ2	O	Output (2 level : V_M, V_L)
18	V_L	—	Power supply (–10V)
19	Vsub	O	Output (2 level : V_{HH}, V_L)
20	V_{HH}	—	Power supply (20V)

Truth Table

Input				Output		
XV1 · 3	XSG1 · 2	XV2 · 4	Xsub	Vφ1 · 3	Vφ2 · 4	Vsub
L	H	X	X	V_M	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_{HH}
X	X	X	H	X	X	V_L
L	L	X	X	V_H	X	X
H	L	X	X	Z	X	X

X : Don't care
Z : High impedance

DC Characteristics (Ta = 25°C)

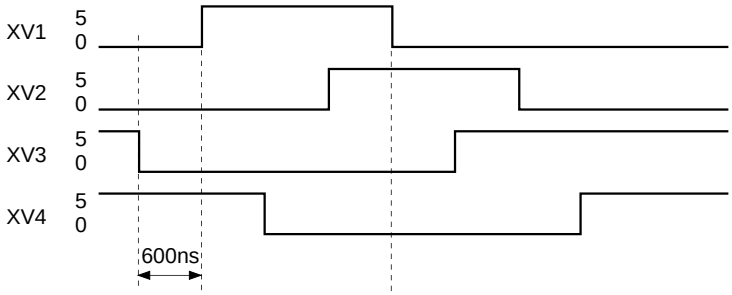
Item	Symbol	Test condition		Min.	Typ.	Max.	Unit
			Power supply				
"H" level input voltage	V_{IH}		V_{DD} = 5V V_L = –10V V_M = 0V V_H = 15V V_{HH} = 20V	3.5	—	—	V
"L" level input voltage	V_{IL}			—	—	1.5	V
"L" level output voltage	$V_{\phi L}$	$I_{\phi L}$ = 20µA		—	–10	–9.9	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M}$ = –20µA		—	0.0	0.1	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M}$ = 20µA		–0.1	0.0	—	V
"H" level output voltage	$V_{\phi H}$	$I_{\phi H}$ = –20µA		14.9	15	—	V
"HH" level output voltage	$V_{\phi HH}$	$I_{\phi HH}$ = –20µA		19.9	20	—	V
Input current	Ii			—	1.0	—	µA
Power supply current *	I_M			—	4.5	5.0	mA
Power supply current *	I_{DD}			—	0.3	0.5	mA
Power supply current *	I_H			—	0.1	0.2	mA
Power supply current *	I_{HH}			—	0.05	0.1	mA

* Suuply current at operation (See the Test Circuit)

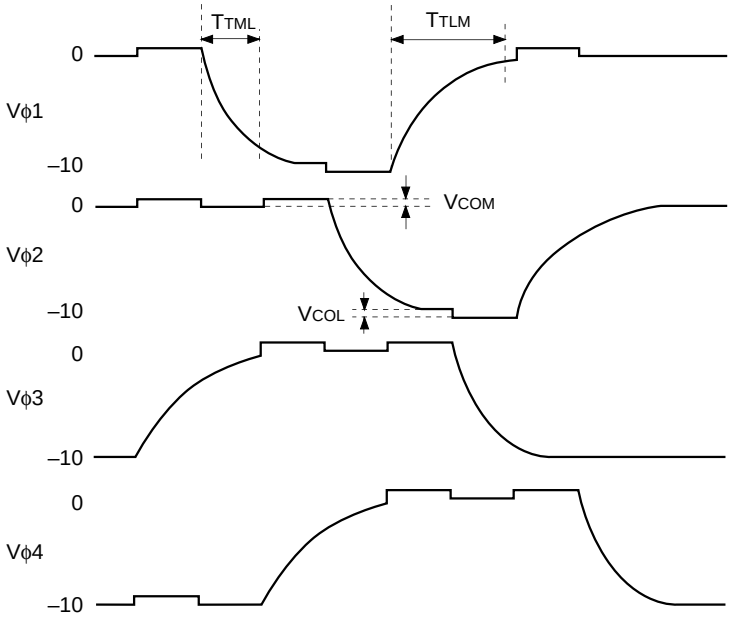
Switching Characteristics (See the Test Circuit Ta = 25°C, V_{HH} = 20V, V_H = 15V, V_M = 0V, V_L = –10V, V_{DD} = 5V)

Item	Symbol	Conditions		Max.	Min.	Unit
Output current	I_L	Vφ1 to 4 = –9.5V		–25		mA
Output current	I_{M1}	Vφ1 to 4 = –0.5V			10	mA
Output current	I_{M2}	Vφ1, 3 = 0.5V		–9		mA
Output current	I_H	Vφ1, 3 = 14.5V			12	mA
Output current	I_{SL}	Vsub = –9.5V		–12		mA
Output current	I_{SH}	Vsub = –19.5V			7	mA
Rise time $V_L \rightarrow V_M$	T_{TLM}	Vφ1 to 4 = –0.5V	After input transient	1000		ns
Fall time $V_M \rightarrow V_L$	T_{TML}	Vφ1 to 4 = –9.5V	After input transient	500		ns
Rise time $V_M \rightarrow V_H$	T_{TMH}	Vφ1, 3 = 14V	After input transient	1000		ns
Fall time $V_H \rightarrow V_M$	T_{THM}	Vφ1, 3 = 1V	After input transient	1000		ns
Rise time $V_L \rightarrow V_{HH}$	T_{TLHH}	Vsub = 17V	After input transient	200		ns
Fall time $V_{HH} \rightarrow V_L$	T_{THHL}	Vsub = –7V	After input transient	200		ns
Coupling amplitude (middle level)	V_{COM}	Vφ1 to 4		0.5		V
Coupling amplitude (low level)	V_{COL}	Vφ1 to 4		0.5		V

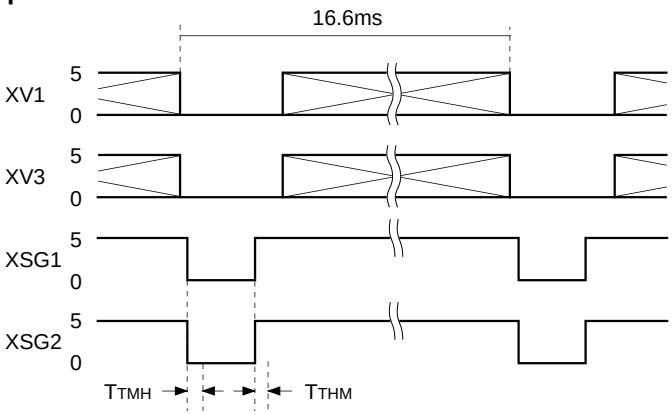
Input Waveform (Repeat Cycle 15.7kHz)



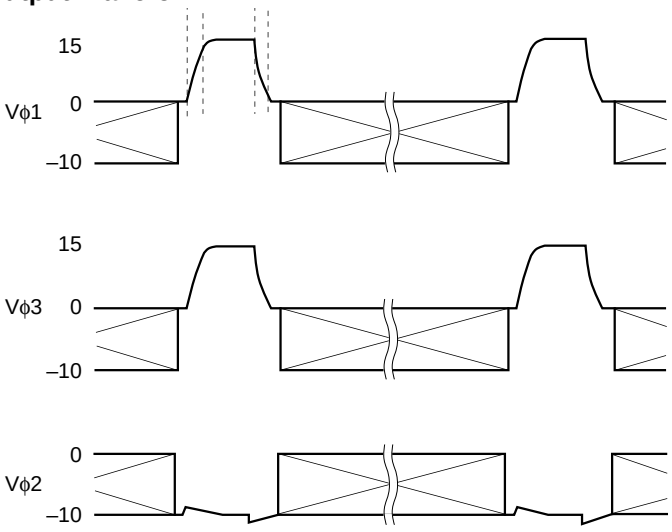
Output Waveform

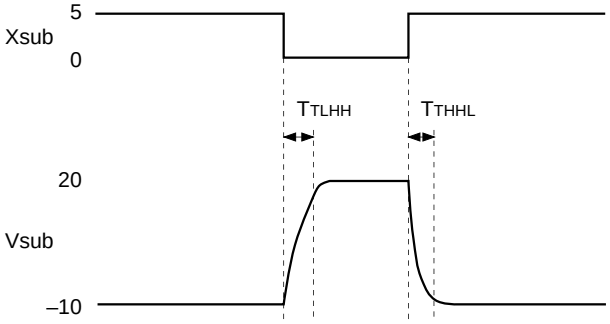


Switching Waveform
Input Waveform

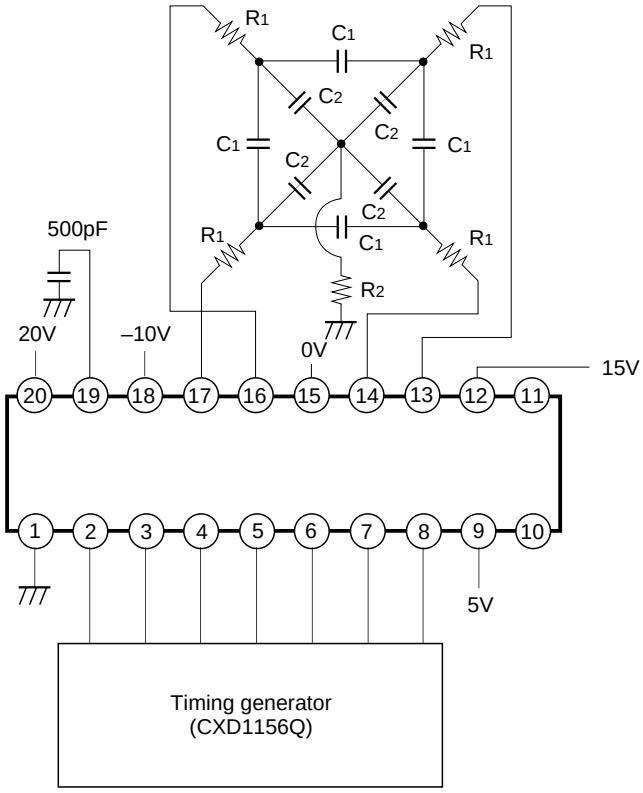


Output Waveform



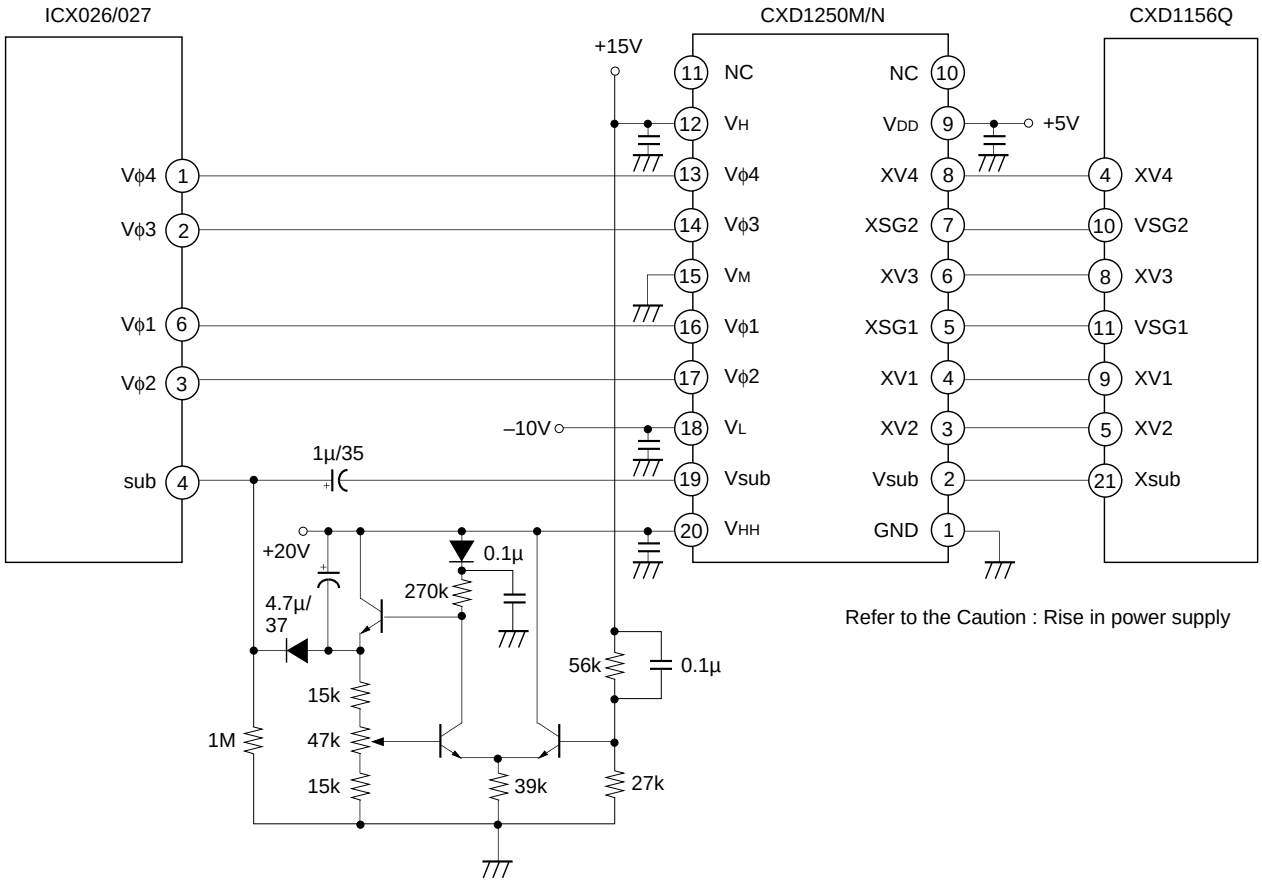


Test Circuit



R1; 27Ω
R2; 5Ω
C1; 1500pF
C2; 3300pF

Application Circuit

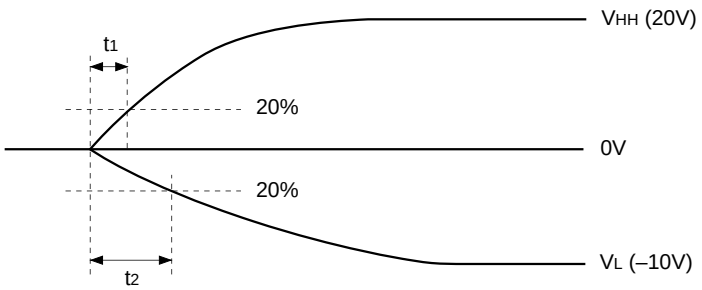


Note:
The capacitor more than 0.1μF should be connected between the ground and each pin of V_{DD}, V_H, V_{HH} and V_L .

Caution : Rise in Power Supply

When the substrate driver is in use, be careful not to let the CCD imagesensors Sub (pin 4) turn into negative voltage.

To this end, raise V_L and V_{HH} at the application circuit under the following conditions.

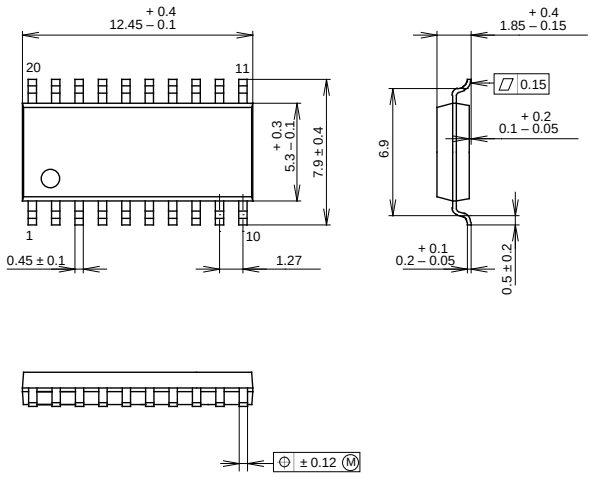


$t_2 \geq t_1 \geq 10msec$

Package Outline Unit: mm

CXD1250M

20PIN SOP (PLASTIC) 300mil



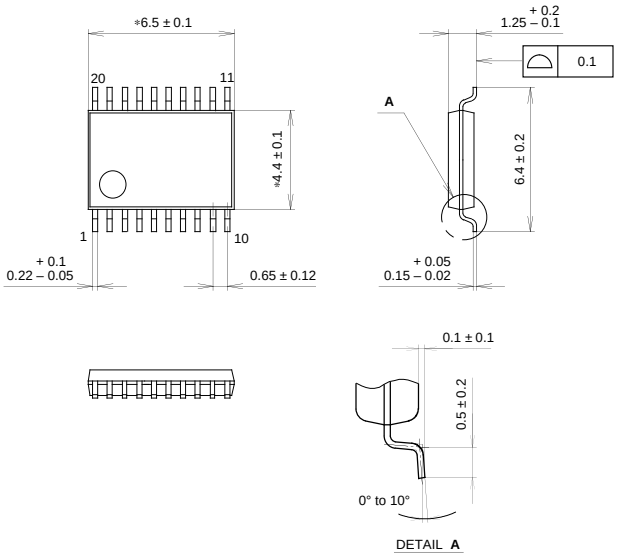
PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	*SOP020-P-0300-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

CXD1250N

20PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g