

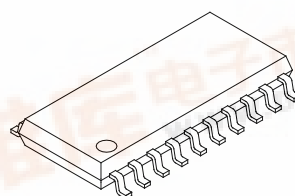
SONY**CXD1268M****CCD Vertical Clock Driver****Description**

The CXD1268M is a clock driver for CCD vertical register drive.

Features

- On-chip 4-channel driver.
(Binary driver $\times 2$, and trinary driver $\times 2$)
- Low output ON resistance provides optimal drive for large load capacity CCD.

20 pin SOP (Plastic)

**Applications**

CCD cameras

Structure

CMOS

Absolute Maximum Ratings (GND = 0V, Ta = 25°C)

Supply voltage	V _H	V _L to V _L + 25	V
Supply voltage	V _M	V _L to V _L + 17*1	V
Supply voltage	V _{DD}	GND to GND + 7	V
Supply voltage	V _L	GND - 10 to GND	V
Input voltage	V _I	-0.5 to V _{DD} + 0.5	V
Input/output clamp diode current	I _{IC} , I _{OC}	-10 to +10	mA
Maximum DC load current	I _{ODC}	-3 to +3	mA
Maximum load capacity	C _L	to 30,000	pF/pin
Allowable power dissipation	P _D	to 200	mW
Storage temperature	T _{stg}	-60 to +150	°C

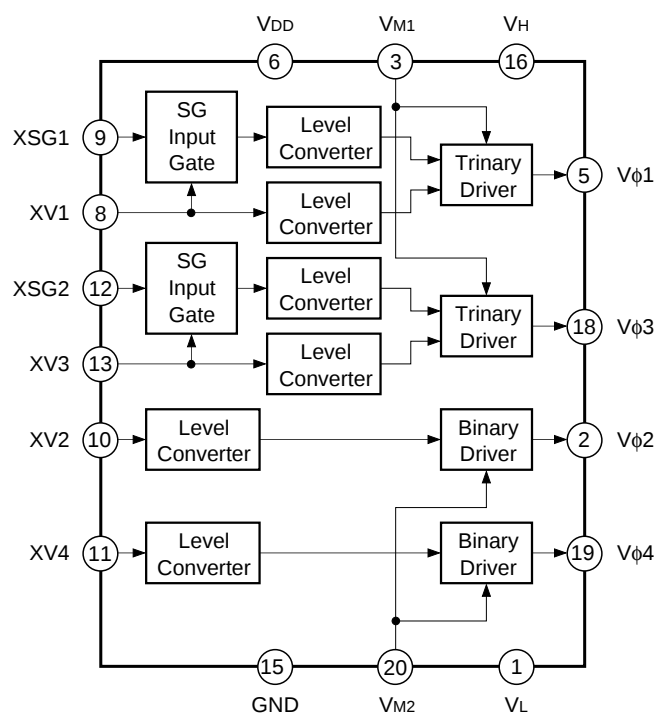
*1 Use V_M at less than V_{DD}.

Recommended Operating Conditions

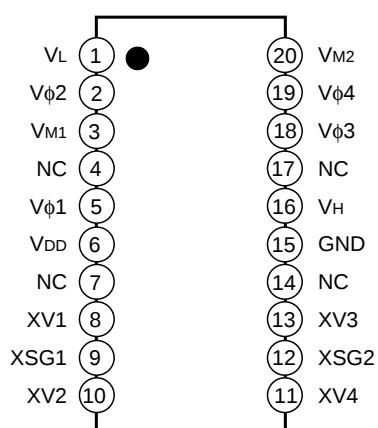
Supply voltage	V _H	V _M + 6.5 to V _M + 15.5	V
Supply voltage	V _L	V _M - 10.0 to V _M - 7.0	V
Supply voltage	V _M	0.0 to 4.0	V
Supply voltage	V _{DD}	4.75 to 5.25	V
High level input voltage	V _{IH} *2	3.5 to V _{DD}	V
Low level input voltage	V _{IL} *2	0.0 to 1.0	V
Operating temperature	T _{opr}	-10 to +60	°C

*2 V_{DD} = 5V

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	V _L	—	Low level power supply
2	V _{φ2}	O	High-voltage output (2 levels: V _{M2} , V _L)
3	V _{M1}	—	Middle level power supply for trinary
4	NC		
5	V _{φ1}	O	High-voltage output (3 levels: V _H , V _{M1} , V _L)
6	V _{DD}	—	Input section power supply
7	NC		
8	XV1	I	Output control (V _{φ1})
9	XSG1	I	Output control (V _{φ1})
10	XV2	I	Output control (V _{φ2})
11	XV4	I	Output control (V _{φ4})
12	XSG2	I	Output control (V _{φ3})
13	XV3	I	Output control (V _{φ3})
14	NC		
15	GND	—	GND
16	V _H	—	High level power supply for trinary
17	NC		
18	V _{φ3}	O	High-voltage output (3 levels: V _H , V _{M1} , V _L)
19	V _{φ4}	O	High-voltage output (2 levels: V _{M2} , V _L)
20	V _{M2}	—	Middle level power supply for binary

Truth Table

X: Don't care

Input			Output	
XV1, XV3	XSG1, XSG2	XV2, XV4	V _{φ1} , V _{φ3}	V _{φ2} , V _{φ4}
H	L	X	V _L	X
H	H	X	V _L	X
L	L	X	V _H	X
L	H	X	V _{M1}	X
X	X	L	X	V _{M2}
X	X	H	X	V _L

Electrical Characteristics

(Unless otherwise specified, $V_H = 14.5V$, $V_M = 1V$, $V_{DD} = 5V$, $GND = 0V$, $V_L = -6V$,

1. DC Characteristics

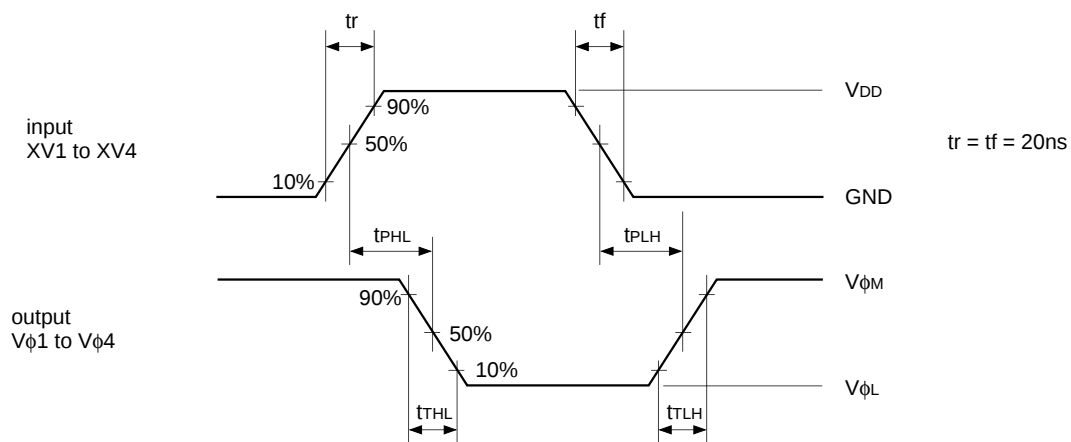
$V_{IL} = GND$, $V_{IH} = V_{DD}$, $T_a = -10$ to $+60^\circ C$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level output voltage	$V_{\phi H}$	$I_{\phi H} = -1mA$	$V_H - 0.1$		V_H	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = -1mA$	$V_M - 0.1$		V_M	V
"L" level output voltage	$V_{\phi L}$	$I_{\phi L} = 1mA$	V_L		$V_L + 0.1$	V
Input current	I_i				1.0	μA
"H" level output ON resistance	$R_{on (H)}$	$I_{\phi H} = -50mA$		18	30	Ω
"M" level output ON resistance	$R_{on (M)}$	$I_{\phi M} = -50mA$		18	30	Ω
"L" level output ON resistance	$R_{on (L)}$	$I_{\phi L} = 50mA$		18	30	Ω
Static current consumption	$I_{DD} + I_H + I_M$			10^{-4}	100	μA

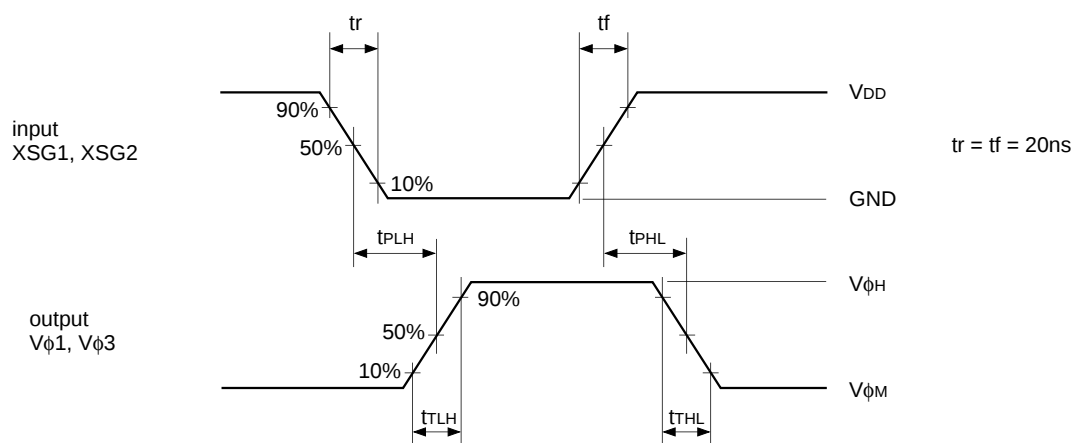
2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time $L \rightarrow M$, $M \rightarrow L$	t_{PLH} , t_{PHL}	Waveform diagram (1), no load		100	200	ns
Propagation delay time $M \rightarrow H$, $H \rightarrow M$	t_{PLH} , t_{PHL}	Waveform diagram (2), no load		200	400	ns
Rise time $L \rightarrow M$ Fall time $M \rightarrow L$	t_{TLH} , t_{THL}	Refer to waveform diagram (1), output load circuit diagram		200	300	ns
Rise time $M \rightarrow H$ Fall time $H \rightarrow M$	t_{TLH} , t_{THL}	Refer to waveform diagram (2), output load circuit diagram		200	300	ns
Operating current consumption	I_{dyn} ($I_{DD} + I_H + I_M + I_L$)	Refer to input pulse timing diagram, output load circuit diagram		6.0	10.0	mA
	I_{DD}			0.02	0.2	mA
	$I_H + I_M$			3.8	5.0	mA
	I_L		-5.0	-3.8		mA

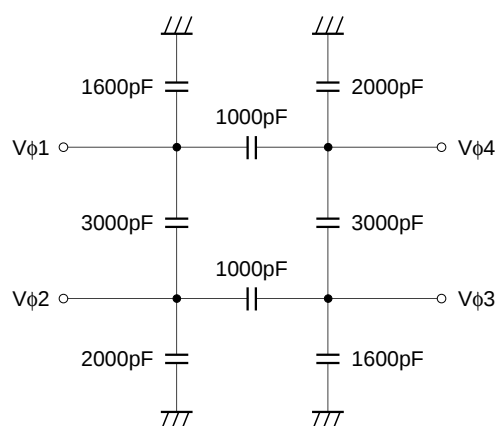
Waveform Diagram (1)



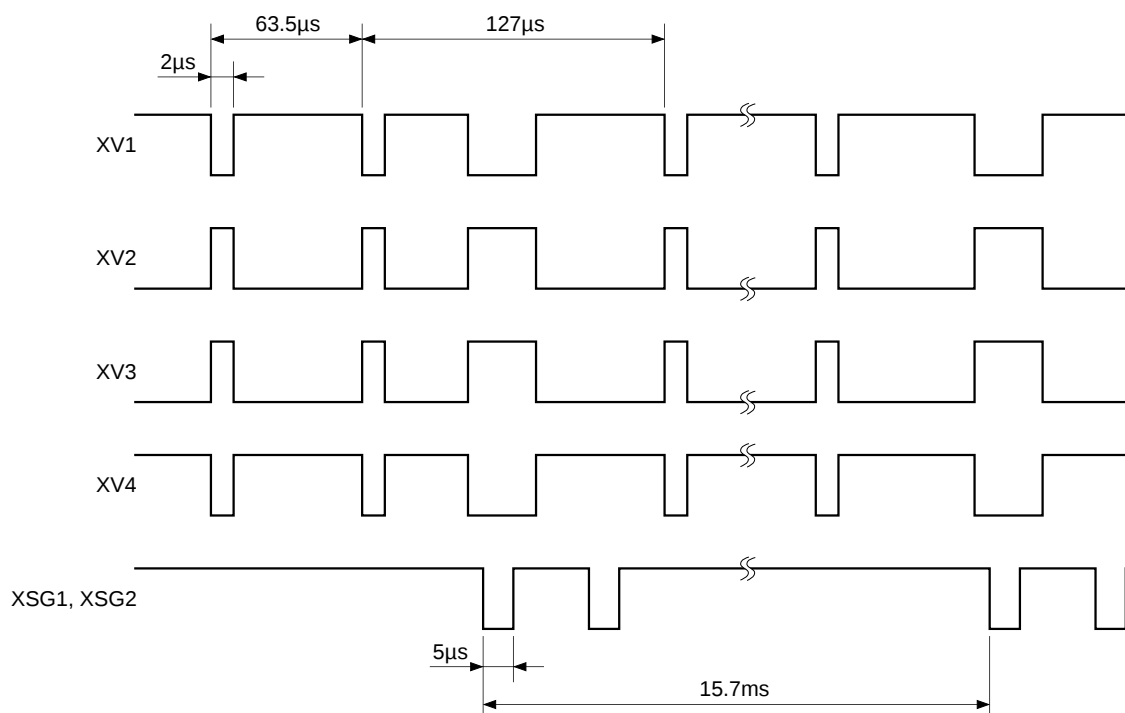
Waveform Diagram (2)



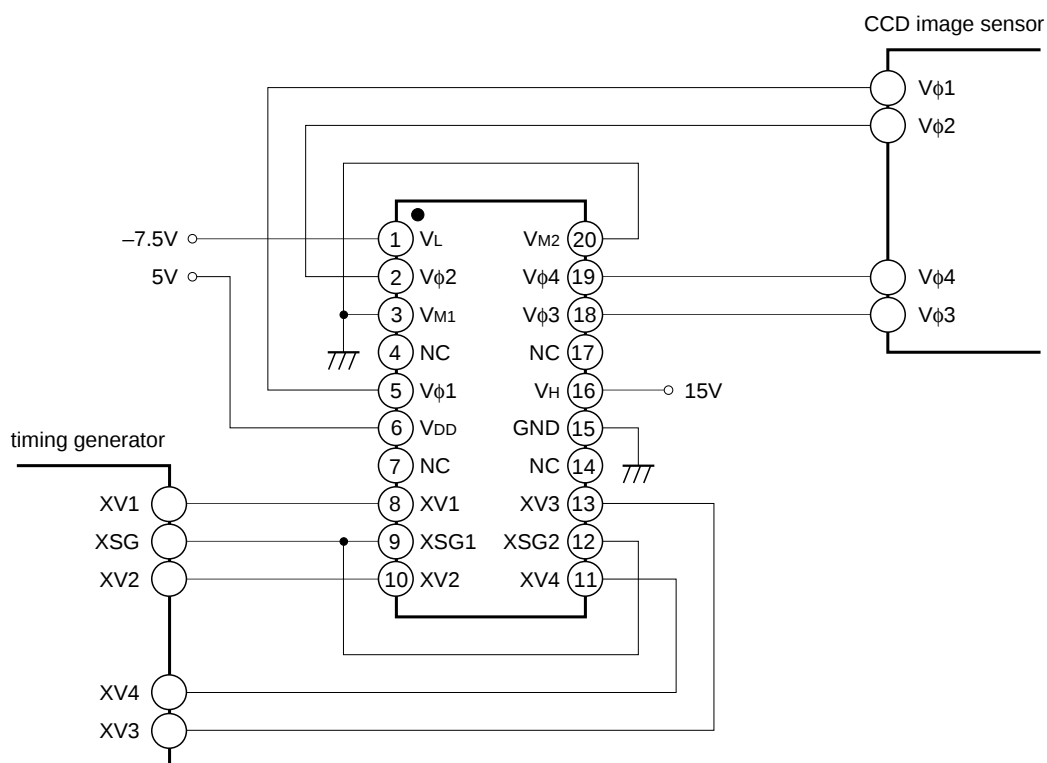
Output Load Circuit Diagram



Input Pulse Timing Diagram



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

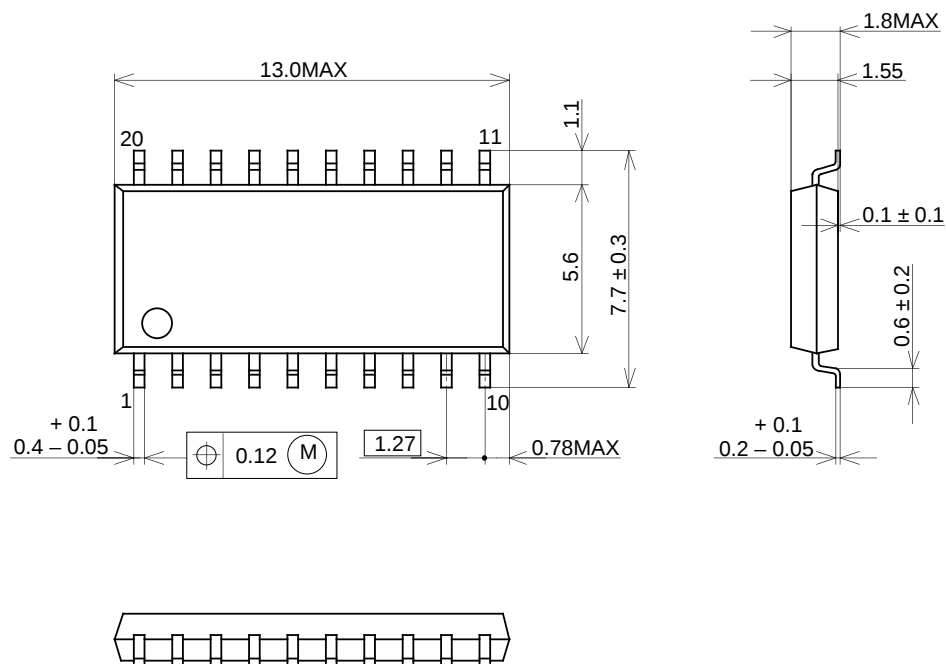
Notes on Operation

1. When applying power, be sure to apply V_H before V_{DD} and V_M .
2. XSG1 (Pin 9) and XSG2 (Pin 12) can be input separately, although they are also common input.

Package Outline

Unit: mm

20PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-20P-L071	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	SOP020-P-0300	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE	—	LEAD MATERIAL	COPPER ALLOY
		PACKAGE MASS	0.3g