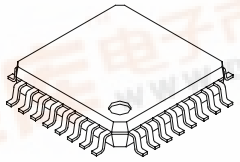
SONY

CXD2131Q

Video Aspect Ratio Identification Signal Encoder/Decoder

32 pin QFP (Plastic)



Description

The CXD2131Q is an IC that encodes and decodes video aspect ratio identification signal (conforming to EIAJ Standard CPX-1204) in the vertical blanking interval of an NTSC video signal.

Features

- The processing formerly carried out by the two chips CXA1727Q and CXD2122AQ has been consolidated into this one chip.
- Both microcomputer serial interface and I²C interface functions are built in.

Applications

Wide-screen televisions, VCRs, MUSE-NTSC converters

Structure

Silicon gate CMOS IC

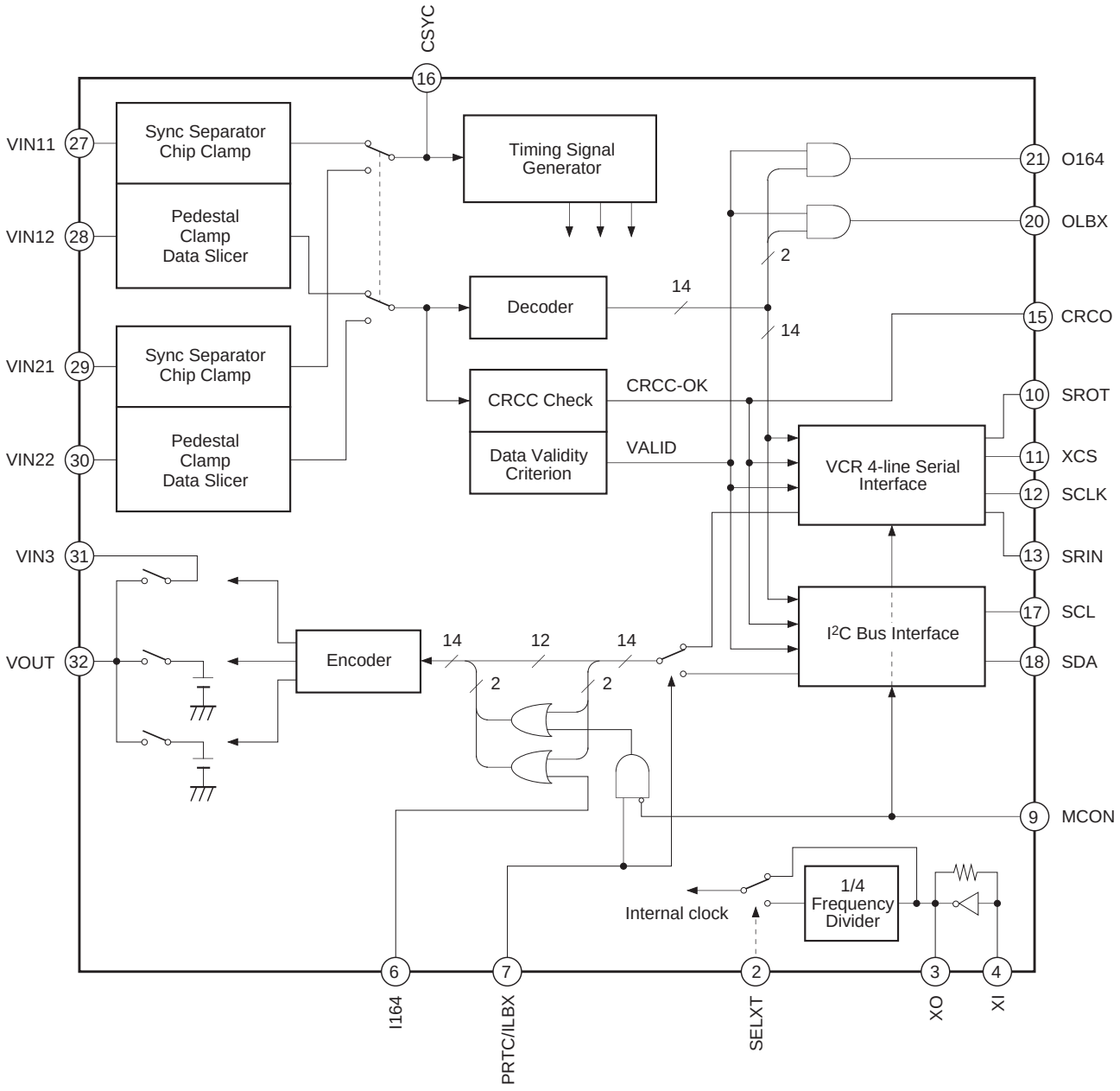
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature			
	Topr	–20 to +70	°C

Block Diagram



Pin Description

Pin No.	Symbol	I/O	I/O level	Description
1	AV_{SS}	—	ANALOG	Analog ground.
2	SELXT	I	TTL	Clock fsc/4 fsc switching; 4 fsc at 1.
3	XO	O	CMOS	Oscillator connection (fsc or 4 fsc).
4	XI	I	CMOS	Oscillator connection or clock input.
5	V_{SS}	—	—	Digital ground.
6	I164	I	TTL	Encoder input; 16:9 at 1, 4:3 at 0. Fixed to 0 when not used.
7	PRTC [ILBX]	I	TTL	Microcomputer interface switching; 0 = I^2C, 1 = serial. [Encoder input; 1 = letter-box, 0 = normal].
8	V_{DD}	—	—	Digital system power supply.
9	MCON	I	TTL	Microcomputer interface exists; 1 = yes, 0 = no.
10	SROT	I/O	TTL*1	Serial interface output to microcomputer [fixed to 0].
11	XCS [OE]	I	TTL	Select from microcomputer [encoding exists; 1 = yes].
12	SCLK [ISEL]	I	TTL	Clock from microcomputer [decoder input channel switching].
13	SRIN [LNJ1]	I	TTL	Data from microcomputer [decoder line ±1 existence].
14	XRST	I	TTL*2	Standby and reset at 0.
15	CRCO	O	CMOS	CRCC check monitor output.
16	CSYC	O	CMOS	Composite Sync monitor output.
17	SCL	I	CMOS*2	I^2C bus clock.
18	SDA	I/O	CMOS*2, 4	I^2C bus data.
19	V_{SS}	—	—	Digital ground.
20	OLBX	O	CMOS	Decoder output; 1 = letter-box, 0 = normal.
21	O164 (DTHI)	O	CMOS	Decoder output; 16:9 at 1, 4:3 at 0 (decode slicer output).
22	TST1	I	TTL*3	Test input; normally connected to Vss; when 1, Pin 21 switches to the function in parentheses ( ).
23	TST2	I	TTL*3	Test input; connect to Vss.
24	ISET1	I	ANALOG	Analog bias current setting.
25	ISET2	I	ANALOG	Analog bias current setting.
26	AV_{DD}	—	ANALOG	Analog system power supply.
27	VIN11	I	ANALOG	Sync separation input.
28	VIN12	I	ANALOG	Decoder data slicer input.
29	VIN21	I	ANALOG	Sync separation input.
30	VIN22	I	ANALOG	Decoder data slicer input.
31	VIN3	I	ANALOG	Encoder input.
32	VOUT	O	ANALOG	Encoder output.

*1 Three-state *2 Schmitt input *3 With pull-down resistor *4 Open drain

Note 1) In microcomputer-free mode when MCON = 0, Pin 7 and Pins 10 to 13 switch to the functions in parentheses [ ]. At this time connect SROT (Pin 10) to Vss.

Note 2) When TST1 = 1, Pin 21 switches to the function in parentheses ( ).

Electrical Characteristics

DC Characteristics (Logic Section)

(V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Output voltage	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	Except for Pins 3 and 18
	V_{OL}	I_{OL} = 4mA			0.4	V	
Output voltage	V_{OH}	I_{OH} = –3mA	V_{DD}/2			V	Pin 3 only
	V_{OL}	I_{OL} = 3mA			V_{DD}/2	V	
Output voltage	V_{OL}	I_{OL} = 4mA			0.4	V	Pin 18 only
Input voltage	V_{IH}		2.2			V	Except for Pins 4, 17 and 18
	V_{IL}				0.8	V	
Input voltage	V_{IH}		0.7 × V_{DD}			V	Pin 4 only
	V_{IL}				0.3 × V_{DD}	V	
Input voltage	V_{IH}		0.8 × V_{DD}			V	Pins 17 and 18 only
	V_{IL}				0.2 × V_{DD}	V	
Input leak current	I_I	V_{IN} = either V_{SS} or V_{DD}	–10		+10	µA	Except for Pins 4, 10, 22 and 23
Output leak current	I_{OZ}	V_{IN} = either V_{SS} or V_{DD}	–40		+40	µA	Pin 10 only
Current consumption	I_{DD}			15		mA	Sum of Pins 8 and 26

AC Characteristics

(V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

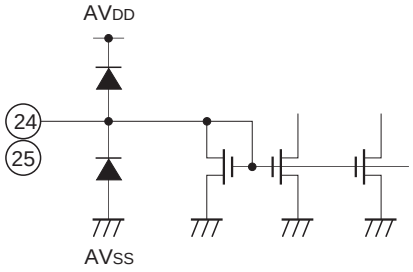
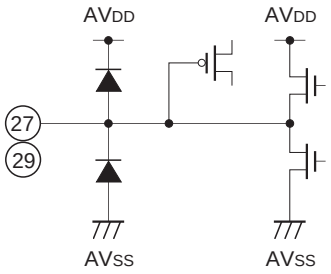
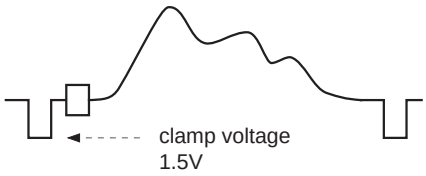
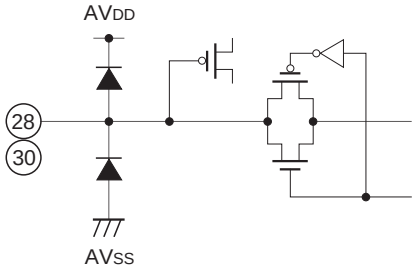
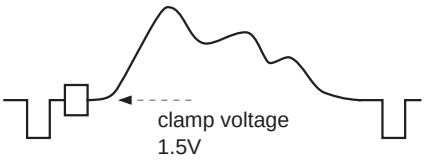
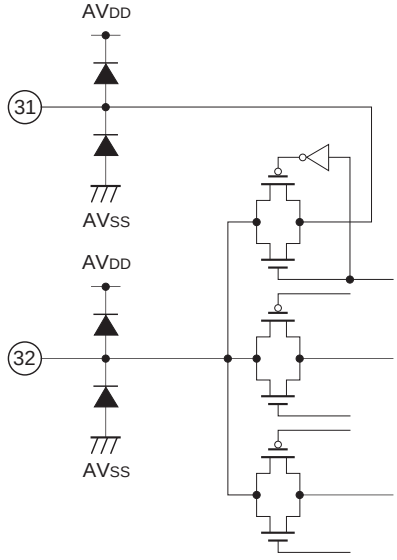
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	fxi	SELXT (Pin 2) = V_{SS}		3.58	5.0	MHz	Pin 4 input, or oscillator between Pins 3 and 4
		SELXT (Pin 2) = V_{DD}		14.3	20.0	MHz	
Serial transmission clock frequency	fsclk	MCON (Pin 9) = V_{DD} PRTC (Pin 7) = V_{DD}			10	MHz	Pin 12 Duty ratio = 50%

I/O Pin Capacitance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Input pin	C_{IN}	V_{DD} = V_I = 0V, f = 1MHz			9	pF	
Output pin	C_{OUT}	V_{DD} = V_I = 0V, f = 1MHz			11	pF	
Input/output pins	$C_{I/O}$	V_{DD} = V_I = 0V, f = 1MHz			11	pF	

Description of Pins and Electrical Characteristics

Analog Section (V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

Pin No.	Symbol	Equivalent circuit	Description
24	ISET1		Bias setting pins. Connect to AV_{DD} with 33kΩ.
25	ISET2		
27	VIN11		Chip clamp, sync separation input. 
29	VIN21		
28	VIN12		Pedestal clamp, data slicer input. 
30	VIN22		
31	VIN3		Input/output pins for encoder. ON resistance value between Pins 31 and 32: max. 350Ω.
32	VOUT		
26	AV_{DD}	Not connected to digital power supply (Pin 8) inside the IC.	Analog power supply. Connect power supply low in noise from the digital system.
1	AV_{SS}	Not connected to digital ground (Pins 5 and 19) inside the IC.	Analog ground. Connect to same potential as digital ground (Pins 5 and 19).

1. Description of video aspect ratio identification signal transfer method (aspect ratio identification)

As shown in the table below, video aspect ratio identification signal consists of 14-bit data, to which a 6-bit CRCC is appended for a total of 20 bits. On an NTSC video signal, this information is carried on lines 20 and 283 of the vertical blanking interval.

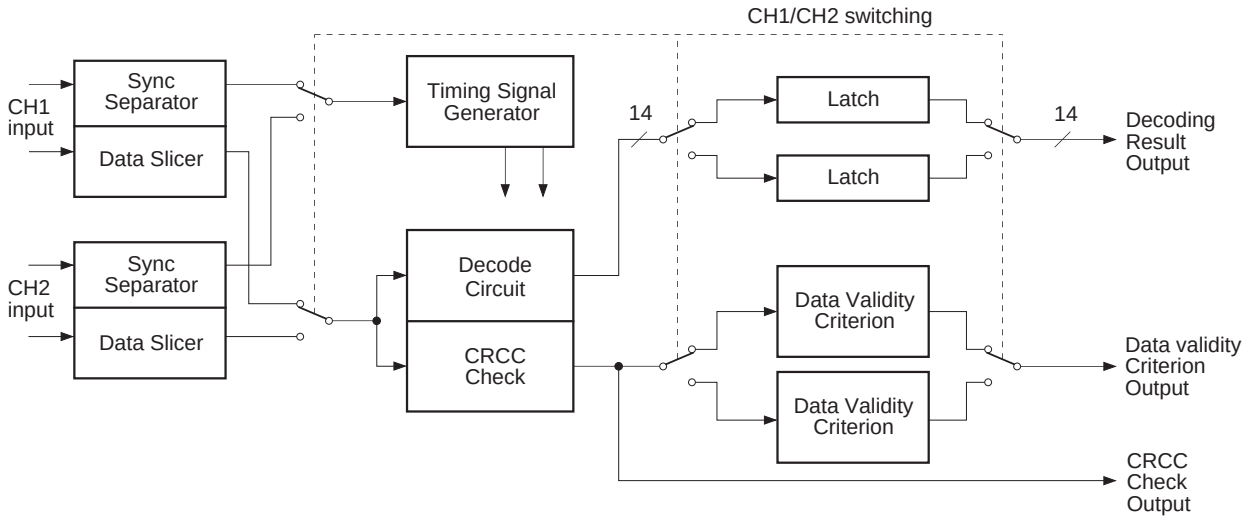
		bit-No.	Description		
				"1"	"0"
WORD0	A	1 2 3	Transfer aspect ratio Pictorial representation format Undefined	Full mode (16 : 9) Letter-box	4 : 3 Normal
	B	4 5 6	Discrimination information about the video signal and any other signal (audio signal, etc.) incident to the video and transferred simultaneously.		
WORD1		4-bit width	Word 0 dependent discrimination signal		
WORD2		4-bit width	Word 0 dependent discrimination signal, information, etc.		

(From Provisional Standard of EIAJ, CPX-1204)

2. Decoding

The CXD2131Q has a decoding function which extracts video aspect ratio identification signals from the video signal. A 1Vp-p video signal is input.

There are two video signal input systems, CH1 (Pins 27 and 28) and CH2 (Pins 29 and 30). These are switched and decoded one at a time. As shown below, the decoding circuit and CRCC check circuit are in one system, but there are two systems for the data validity criterion circuit and decoding result, for each channel. This means that even when one channel is being decoded, the decoding result for the other channel is held. ISEL performs channel switching. ISEL is set by microcomputer transmission or by pins. For CH1, ISEL = "0", and for CH2, ISEL = "1".



Further, the composite sync signal of the channel being decoded can be monitored at CSYC (Pin 16) and the CRCC check result can be monitored at CRCO (Pin 15), even during decoding.

Also, when TST1 (Pin 22) is held at high level, the data slice result for decoding can be monitored at O164 (Pin 21).

For the decoding operation, the range of the scanning lines to be decoded on the video signal can be switched by LNJ1. LNJ1 can be set by microcomputer control or by pins.

When LNJ1 is "1", only lines 20 and 283 are decoded, and when LNJ1 is "0", one line on each side of lines 20 and 283 are decoded in addition.

3. Encoding

The CXD2131Q has an encoding function which adds video aspect ratio identification signals to the video signal. A 1Vp-p video signal is encoded.
An encoded video signal is output on VOUT (Pin 32) by inputting the video signal input to the decoding function CH2 side to VIN3 (Pin 31) as well.
When this encoding function is used, decoding input must be switched to CH2.
Encoding is controlled by OE, which is set by microcomputer control or by pins. Encoding is off when OE is “0”, and the input video signal is output as it is from VOUT (Pin 32).
For example, even when CH1 is decoding, the video signal input to CH2 can be obtained as it is at VOUT if OE is set to “0”.

4. Clock

The CXD2131Q requires an fsc (= 3.579545MHz) or 4 fsc clock. When SELXT (Pin 2) is “0” the clock is fsc; when it is “1”, the clock is 4 fsc. Connect XI (Pin 4) and XO (Pin 3) when using a crystal oscillator. Input to XI for external input.

5. Settings and data input/output

There are three methods of performing the CXD2131Q settings and data input/output: direct setting by pins without using a microcomputer, the 4-line microcomputer serial interfaces, and I^2C bus interface.

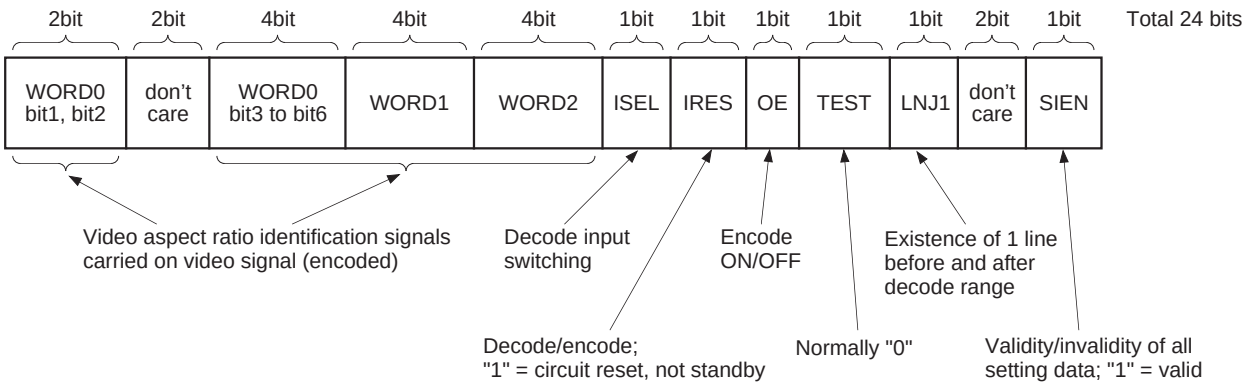
5-1. Microcomputer-free mode

Direct input/output by pins, without using a microcomputer, can be carried out by setting MCON (Pin 9) to“0”.
In this case, only the first 2 bits of the total 14 bits of video aspect ratio identification signals are input or output.
The decoding result is obtained at O164 (Pin 21) and OLBX (Pin 20). The data for encoding is input to I164 (Pin 6) and PRTC/ILBX (Pin 7).
For the various settings, decode channel switching ISEL is input to SCLK (Pin 12), decode scanning line range switching LNJ1 to SRIN (Pin 13) and encode operation existence OE to XCS (Pin 11).
Connect SROT (Pin 10), SCL (Pin 17) and SDA (Pin 18), which are unused, to Vss.

5-2. 4-line serial interface

Setting and data input/output can be carried out by microcomputer serial interface when MCON (Pin 9) is set at “1” and PRTC (Pin 7) is set at “1”.
In this case, all 14 bits of video aspect ratio identification signals are input or output.
Serial data from the microcomputer of serial transmission connects to SRIN (Pin 13), the serial clock to SCLK (Pin 12), and select to XCS (Pin 11). Serial data to the microcomputer is output at SROT (Pin 10).
Connect SCL (Pin 17) and SDA (Pin 18), which are unused, to Vss.
Serial interface bit configuration is shown in the following figures.

µCOM → CXD2131



CXD2131 → µCOM

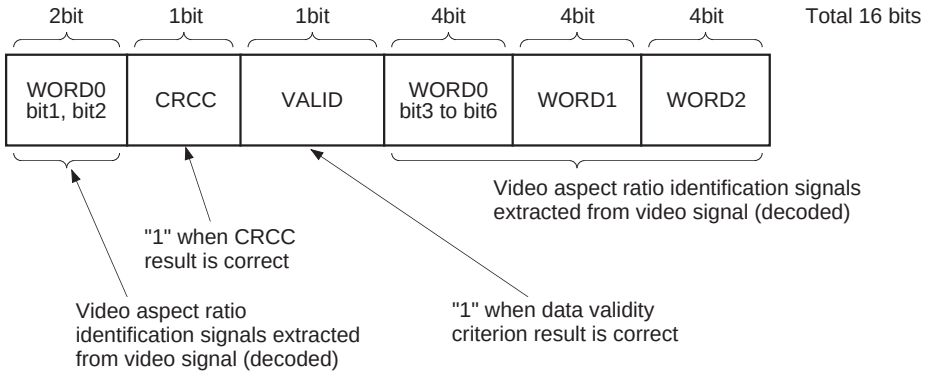
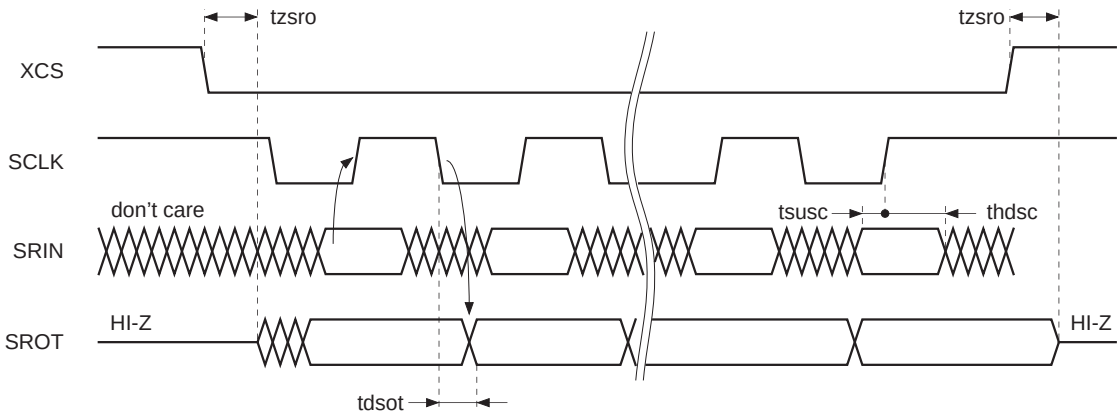


Fig. 1 (a). Bit configuration of 4-line serial interface



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Set-up to SRIN SCLK rising edge	tsusc		10			ns
Hold to SRIN SCLK rising edge	thdsc		10			ns
Delay from SROT SCLK falling edge	tdsot	Cload = 20pF			40	ns
Three-state control delay by SROT XCS	tzsro	Rload = 2kΩ			40	ns

Fig. 1 (b). 4-line serial interface timing

5-3. I²C bus interface

Setting and data input/output can be carried out by microcomputer I²C bus interface when MCON (Pin 9) is set at “1” and PRTC (Pin 7) is set at “0”.

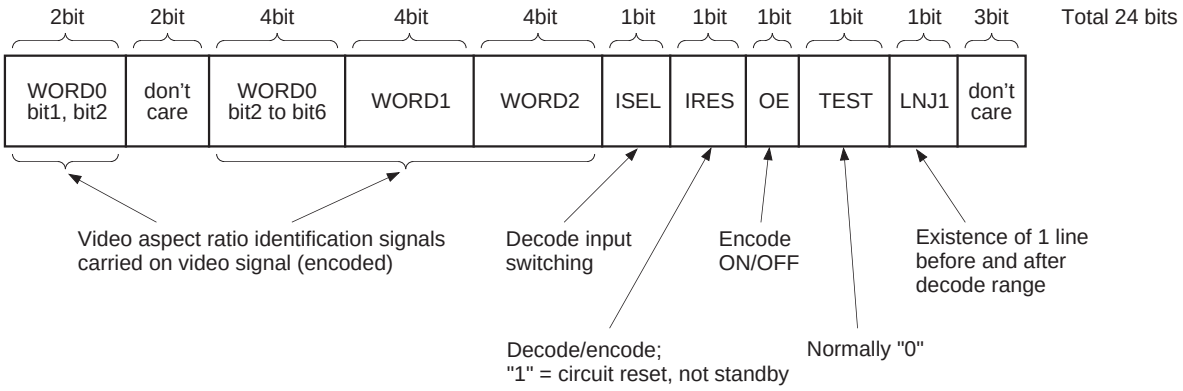
In this case, all 14 bits of video aspect ratio identification signals are input or output. This I²C bus corresponds to standard mode. I²C address is 40H.

I²C bus data connects to SDA (Pin 18) and I²C bus clock to SCL (Pin 17).

Connect SRIN (Pin 13), SCLK (Pin 12) and XCS (Pin 11), which are unused, to Vss. And leave SROT (Pin 10) open.

I²C bus interface bit configuration is shown in Fig. 2.

µCOM → CXD2131



CXD2131 → µCOM

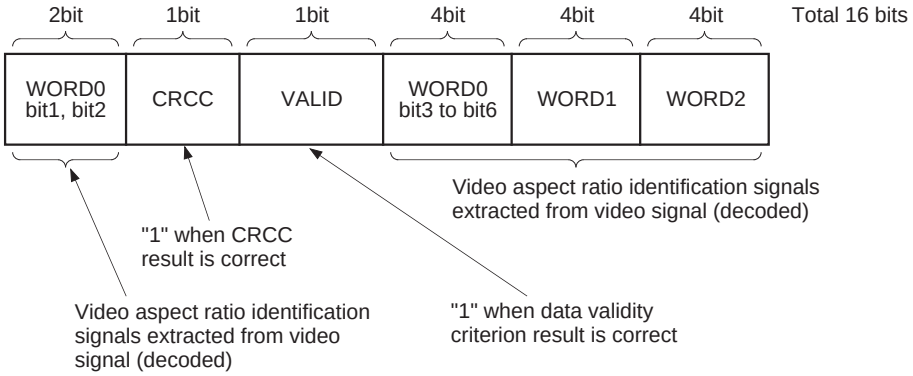


Fig. 2. Bit configuration of I²C bus interface

The CXD2131Q I²C bus interface has a subaddress function.
With the subaddress function, only the bytes after setting has started are set.
There is no subaddress function at the read side.

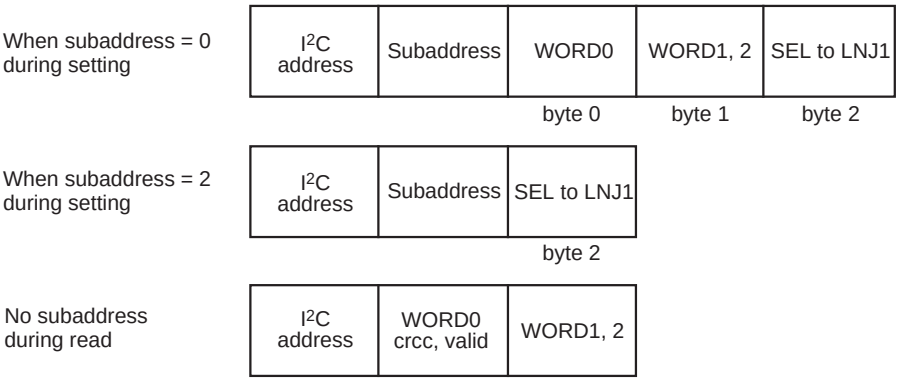
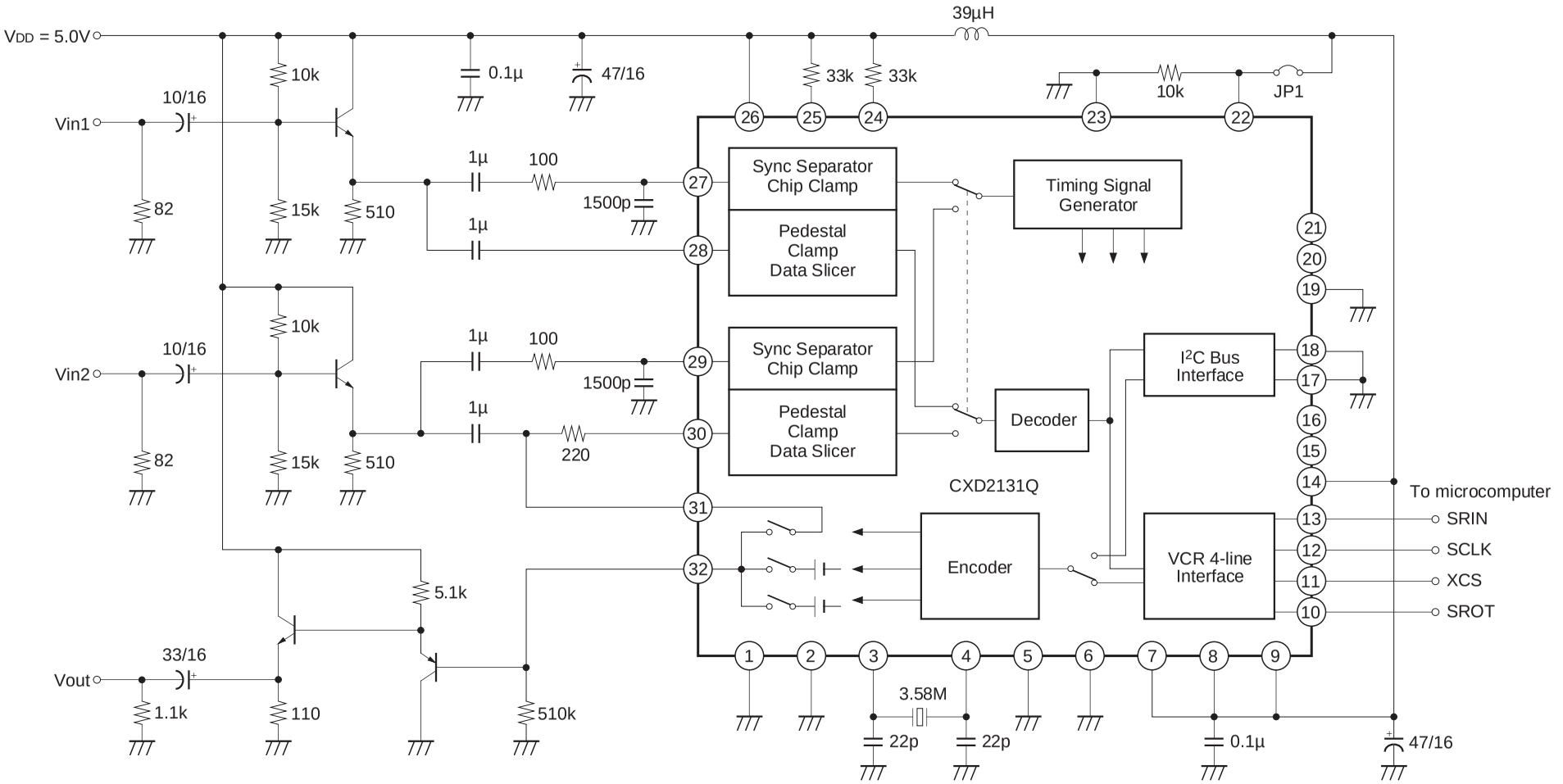


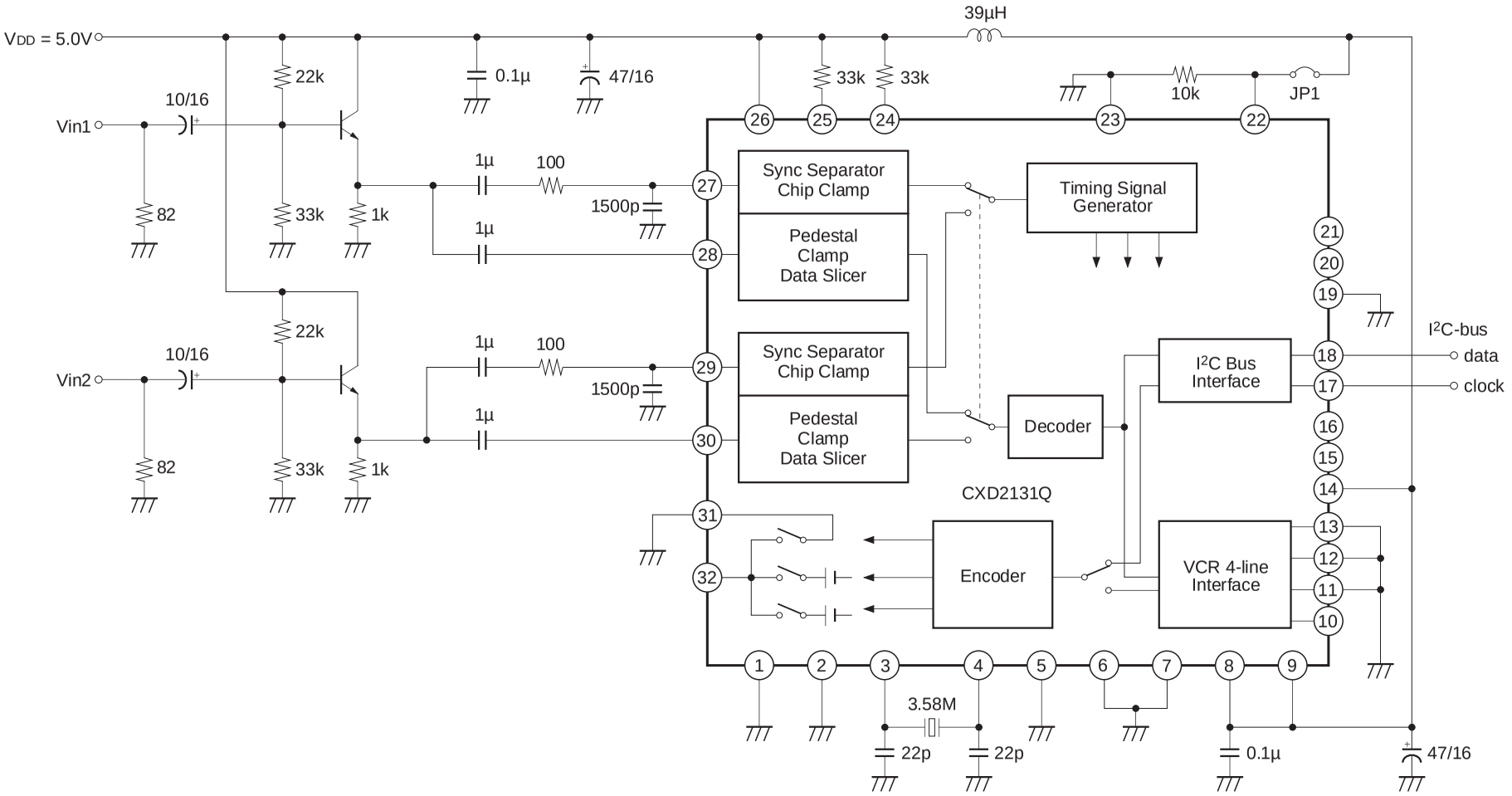
Fig. 3. Description of I²C bus and subaddress

Application Circuit (4-line microcomputer I/F for VCR, with encoder)



Note) JP1 in the figure above normally is not connected. It is only connected when monitoring slicer output from Pin 21, when checking the circuit or the like.

Application Circuit (With I²C bus, no encoder)

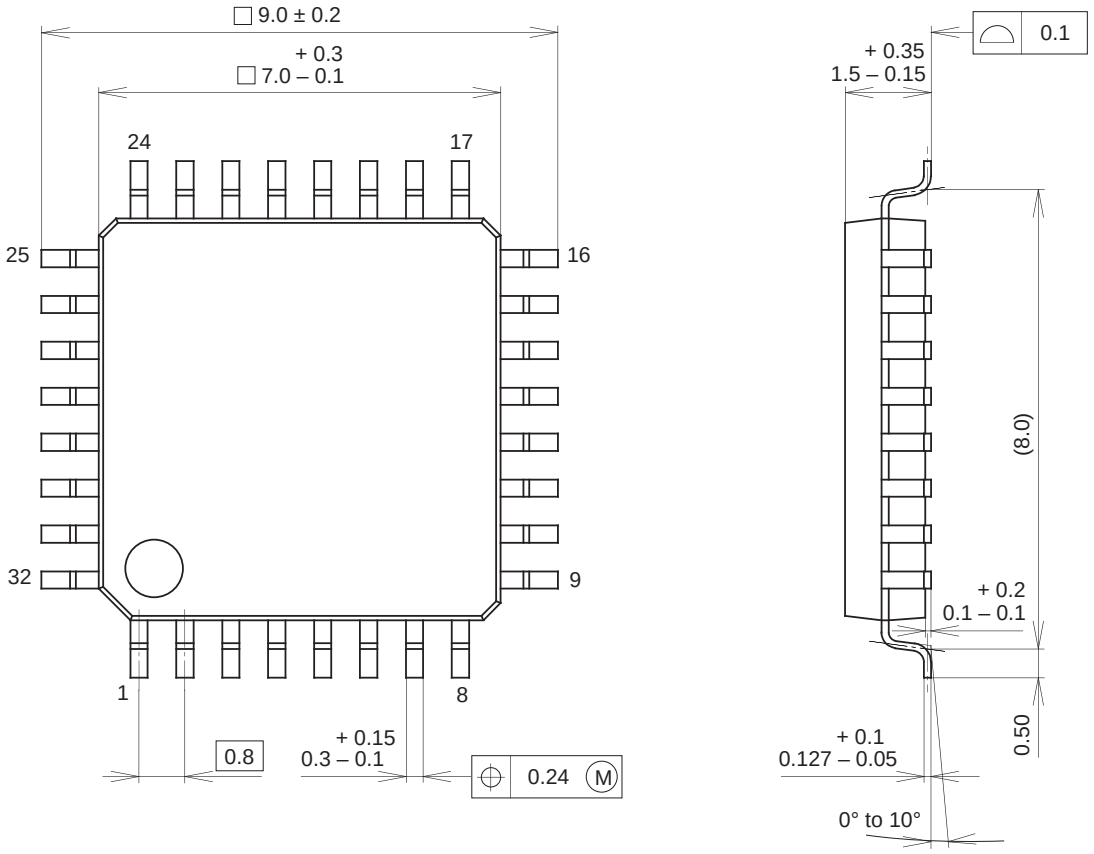


Note) JP1 in the figure above normally is not connected. It is only connected when monitoring slicer output from Pin 21, when checking the circuit or the like.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g