SONY

CXD2163R

Signal Processor LSI for Single-Chip CCD Color Camera

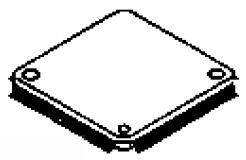
Preliminary

Description

The CXD2163R is a signal processor LSI for Ye, Cy, Mg and G single-chip CCD color cameras. In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.

This chip also has a built-in microcontroller to realize basic camera functions without a microcomputer.

100 pin LQFP (Plastic)



Features

- Single-chip CCD camera sync signal generation and luminance / chroma signal processing
- Supports NTSC/PAL modes
- Supports 360H/510H/720H/760H system CCD image sensors

- Y/C digital output pin (2 mode selection)
  - CCIR601 or 8-bit straight format
- built-in 8-bit A/D converter
  - External 9/10-bit A/D converter can be selected
- Supports external sync functions (LL, VS, VBS, etc.)
  - Sync separation circuit, phase comparator

- AE/AWB detector
- Block control functions with a built-in microcontroller
  - AE/AWB/YC/CLAMP/SG control functions
- Peripheral IC communication control functions
  - TG, EVR, EEPROM communication control

- Serial communication function (2 mode selection)
  - Microcomputer or RS232C

Applications

- Industrial CCD cameras
  (surveillance/FA/image input cameras)
- Multimedia CCD cameras
  (teleconferencing/personal computer cameras)

Applicable CCD Image Sensors

360H color CCDs
- ICX076/077AK (1/5" NTSC/PAL)

510H color CCDs
- ICX026/027CK (1/2"NTSC/PAL)
- ICX054/055AK (1/3"NTSC/PAL)
- ICX066/067AK (1/4"NTSC/PAL)

760H color CCDs
- ICX038/039BN (1/2"NTSC/PAL)
- ICX058/059AK (1/3" NTSC/PAL)
- ICX068/069AK (1/4"NTSC/PAL)

Absolute Maximum Ratings

· Supply voltage	V_{DD}	$V_{SS}-0.5$ ~	+7.0	V
· Input voltage	V_I	$V_{SS}-0.5$ ~	$V_{DD}+0.5$	V
· Output voltage	V_O	$V_{SS}-0.5$ ~	$V_{DD}+0.5$	V
· Operating temperature	Topr	−20 ~	+75	℃
· Storage temperature	Tstg	−55 ~	+150	℃

Recommended Operating Conditions

· Supply voltage	VDD	3.0~3.6	V
	AVDD	4.5~5.5	V
	AVDD3 only	3.0~3.6	V
· Operating temperature	Topr	−20~+75	℃

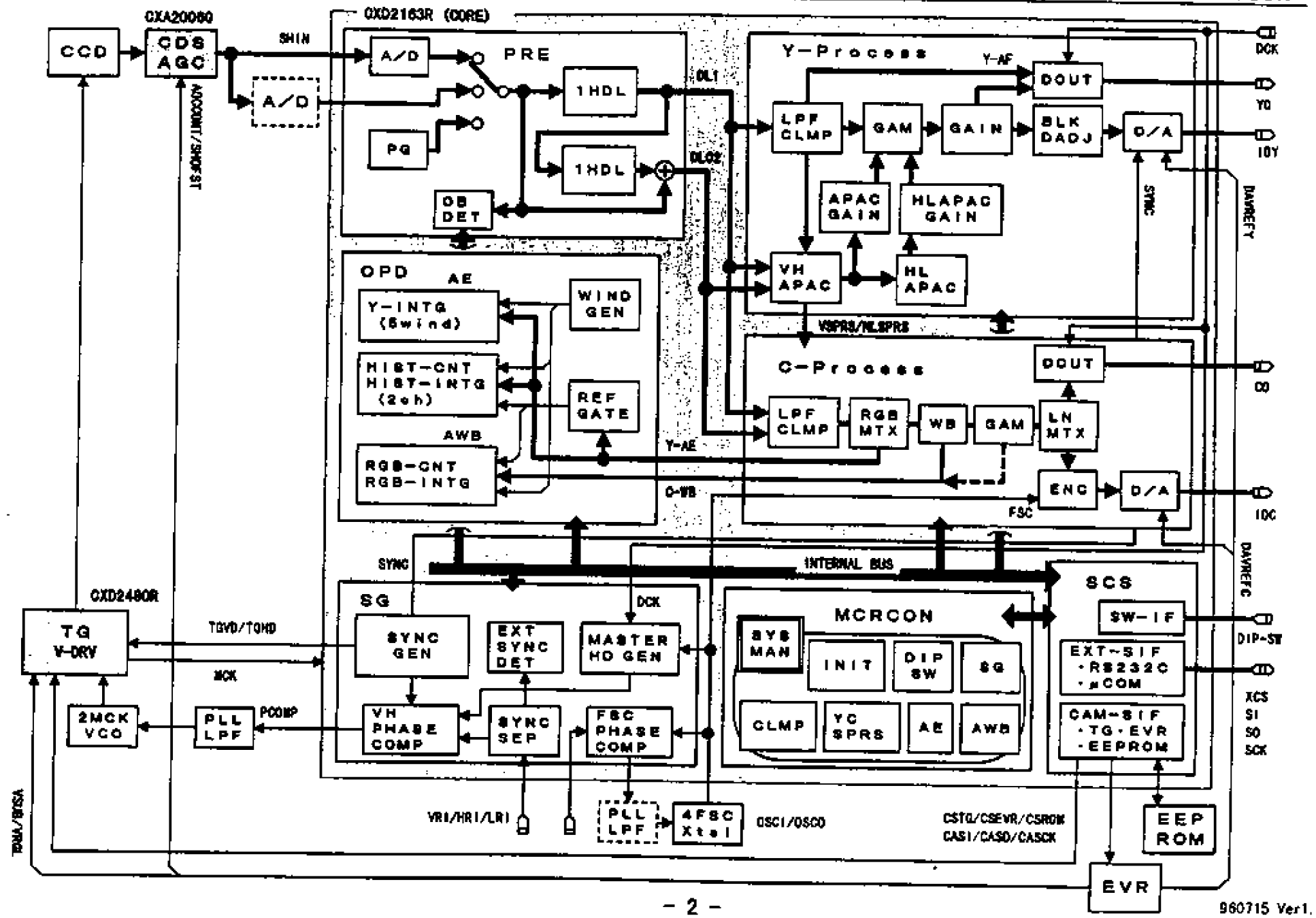
Supported Related LSIs

TG : CXD2460R
AFD : CXD2418R
AGC : CXA2006Q
ADC : CXD2311AR(10bit)
CXD2312R(9bit)

EVR: AK6420H (Asahi Kasei Micro Ltd.)
EEPROM: MB88347 (Fujitsu Ltd.)

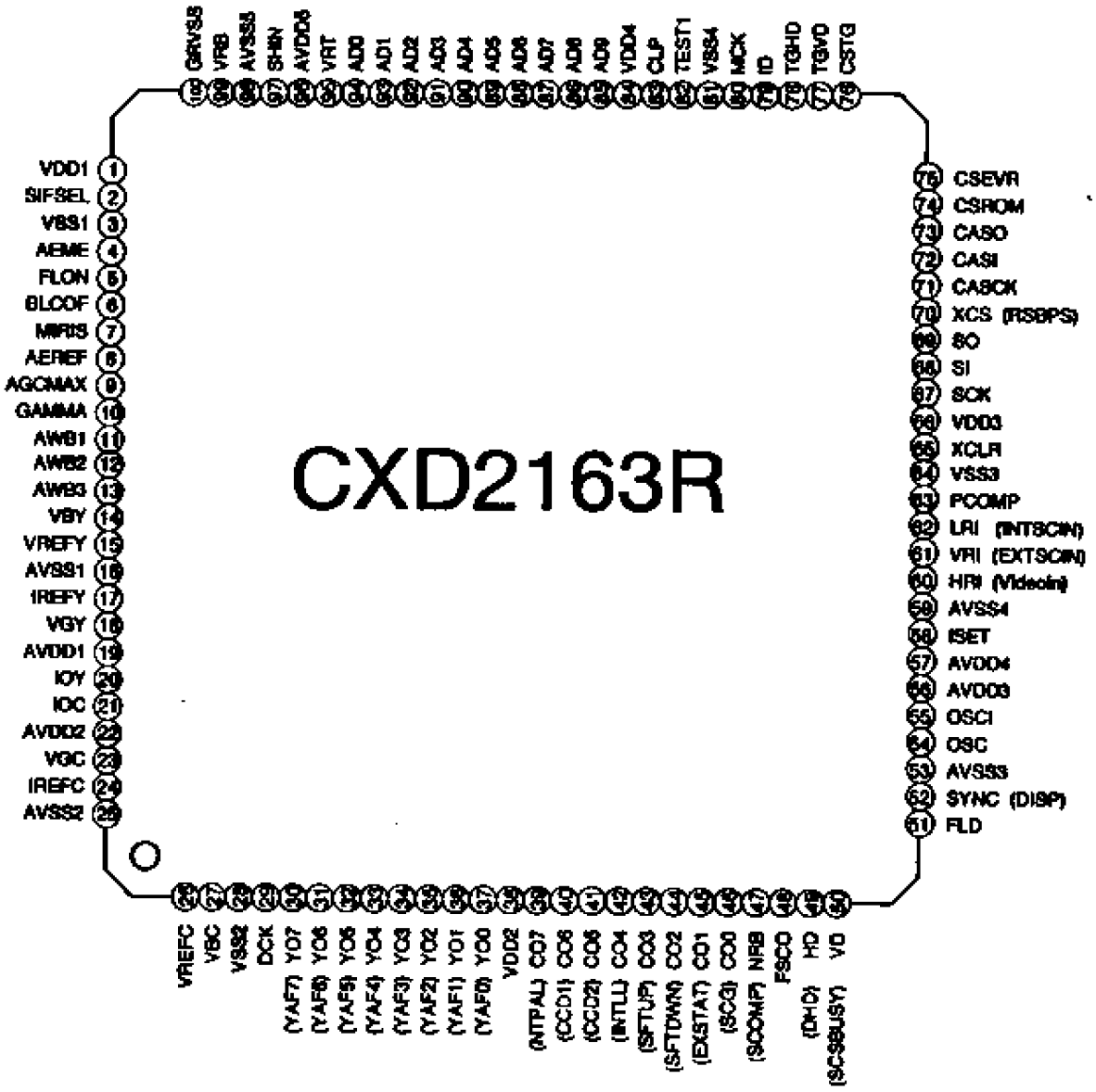
960715 Ver1.1

CXD2163 Block Diagram



960715 Ver1.1

Pin Configuration



※ Symbols in parentheses are the signal names when the LSI is switched by the serial communication settings.
All pin symbols (pin names) for the D2163 are the names next to the pin No. (outside the parentheses)

Pin Description

Pin No.	Symbol	I/O	Description			
1	VDD1	—	Digital power supply (+3.3 V)			
2	SIFSEL	I	Serial interface mode switching 0: microcomputer, 1: RS232C			
3	VSS1	—	Digital GND			
4	AEME	I	AE mode switching 0: auto, 1: manual			SW setting pin system
5	FLON	I	Flickerless mode (auto) /Shutter speed control (manual)			
6	BLCOF	I	Backlight compensation off (auto)/Shutter speed control (manual)			
7	MIRIS	I	Iris mode switching (auto) /Shutter speed control (manual)			
8	AEREF	I	AE convergence lev switching (auto) / Fixed gain mode sel.(manual)			
9	AGCMAX	I	AGC maximum gain switching (auto) / Fixed gain mode sel.(manual)			
10	GAMMA	I	Gamma correction ON/OFF			
11	AWB1	I	AWB mode switching 0: auto, 1: manual			
12	AWB2	I	ATW/push lock switching (auto)/ Fixed WB mode selection (manual)			
13	AWB3	I	Push lock signal input (auto)/ Fixed WB mode selection (manual)			
14	VBY	I (A)	Capacitor connection pin (about 0.1 uF) (for luminance signal D/A)			Luminance signal D/A
15	VREFY	I (A)	Reference voltage setting pin (for luminance signal D/A)			
16	AVSS1	—	Analog GND (for luminance signal D/A)			
17	IREFY	O (A)	Reference current setting pin (for luminance signal D/A)			
18	VGY	I (A)	Capacitor connection pin (about 0.1 uF) (for luminance signal D/A)			
19	AVDD1	—	Analog power supply (for luminance signal D/A)			
20	IOY	O (A)	Luminance signal (current) output pin			
21	IOC	O (A)	Chroma signal (current) output pin			Chroma signal D/A
22	AVDD2	—	Analog power supply (for chroma signal D/A)			
23	VGC	I (A)	Capacitor connection pin (about 0.1 uF) (for chroma signal D/A)			
24	IREFC	O (A)	Reference current setting pin (for chroma signal D/A)			
25	AVSS2	—	Analog GND (for chroma signal D/A)			
26	VREFC	I (A)	Reference voltage setting pin (for chroma signal D/A)			
27	VBC	I (A)	Capacitor connection pin (about 0.1 uF) (for chroma signal D/A)			
28	VSS2	—	Digital GND			
29	DCK	I/O	Clock I/O pin for digital output YO/CO ※1			
30	YO7	O	MSB ※2	YAF7	MSB ※2	
31	YO6	O		YAF6		
32	YO5	O	Luminance sig. digital outputs	YAF5	AF detection sig.outputs	
33	YO4	O		YAF4	(preset settings)	
34	YO3	O		YAF3		
35	YO2	O		YAF2		
36	YO1	O		YAF1		
37	YO0	O	LSB	YAF0	LSB	
38	VDD2	—	Digital power supply (+3.3 V)			

※1: The I/O direction changes according to the serial data settings and CCD type.

※2: The output sig contents change according to the serial data settings. The preset setting when cleared is YAF0 to 7 output.

Pin No.	Symbol	I/O	Description			
39	CO7	O	MSB ※3	NTPAL	TV mode switch 0: NTSC, 1: PAL ※3	Basic settings
40	CO6	O	Chroma signal digital outputs	CCD1	CCD type 0h: 360H, 1h: 510H ※3	
41	CO5	O		CCD2	Line lock mode 0: OFF, 1: ON ※3	
42	CO4	O		INTLL	Phase shifter (UP) signal input ※3	External sync system
43	CO3	O		SFTUP	Phase shifter (DOWN) signal input ※3	
44	CO2	O		SFTDWN	Ext-sync mode discrimination outp. ※3	
45	CO1	O		EXSTAT	Subcarrier gate pulse output ※3	
46	CO0	O		SCG	Color discrimination signal output ※3	
47	NRB	O		SCOMP	Subcarrier phase comparator outp ※3	
48	FSCO	O	Subcarrier output			Sync signal system
49	HD	O	H sync signal (HD)output ※4	DHD	H sync for digital output ※4	
50	VD	O	V sync signal (VD)output ※4	SCSBUSY	Serial BUSY sig. output ※4	
51	FLD	O	Field discrimination signal output			
52	SYNC	O	Composite sync sig outp ※4	DISP	OPD detection frame out ※4	
53	AVSS3	—	Analog GND (for 4fsc oscillator)			Oscillator
54	OSCO	O	4fsc oscillator output (for subcarrier generation)			
55	OSCI	I	4fsc oscillator input (for subcarrier generation)			
56	AVDD3	—	Analog power supply (+3.3 V, for 4fsc oscillator)			
57	AVDD4	—	Analog power supply (+5 V, for sync separation circuit)			Sync separator
58	ISET	I (A)	Current source input (for sync separation circuit)			
59	AVSS4	—	Analog GND (for sync separation circuit)			
60	HRI	I (A)	External sync sig. input (composite video sig. input/H reset sig. input)			
61	VRI	I	External sync signal input (external burst signal input/V reset signal input)			
62	LRI	I/O	External sync signal I/O (LALTout/LALT reset in/internal subcarrier input)			
63	PCOMP	O	Phase comparator output for HPLL/VPLL			
64	VSS3	—	Digital GND			
65	XCLR	I	Clear input pin			
66	VDD3	—	Digital power supply(+3.3 V)			
67	SCK	I	Serial ck in for microcom.communicat (fixed to 1 during RS232mode)			Ext-communication system
68	SI	I	Serial data input for microcomputer / RS232C communication			
69	SO	O	Serial data output for microcomputer / RS232C communication			
70	XCS	I	Chip select in for microcom.	RSBPS	RS232C BPS setting ※5	
71	CASCK	O	Serial clock output for camera peripheral ICs (to TG, EVR ,EEPROM)			Peripheral IC communication system
72	CASI	I	Serial data input for camera peripheral ICs (from TG, EVR ,EEPROM)			
73	CASO	O	Serial data output for camera peripheral ICs (to TG, EVR ,EEPROM)			
74	CSROM	O	Chip select output for camera peripheral ICs (to EEPROM)			
75	CSEVR	O	Chip select output for camera peripheral ICs (to EVR)			
76	CSTG	O	Chip select output for camera peripheral ICs (to TG)			

※3: The functions of these pins change according to the serial data settings.
The preset settings when cleared are basic settings / external sync system.
※4: The output contents change according to the serial data settings.
The preset settings are FSCO, HD, VD, FLD and SYNC output.
※5: Valid only during RS232C mode. RSBPS = 0: 4800 bps, 1: 9600 bps

Pin No.	Symbol	I/O	Description	
77	TGVD	O	Vertical sync signal output for TG	TG system
78	TGHD	O	Horizontal sync signal output for TG	
79	ID	I	Line color discrimination signal input	
80	MCK	I	D2163 master clock input	
81	VSS4	—	Digital GND	
82	TEST1	O	Test output (open)	
83	CLP1	O	Analog optical black clamp pulse output	
84	VDD4	—	Digital power supply (+3.3 V)	
85	AD9	I	MSB ※6	
86	AD8	I		
87	AD7	I	Digital signal data inputs from external A/D	
88	AD6	I		
89	AD5	I		
90	AD4	I		
91	AD3	I		
92	AD2	I		
93	AD1	I		
94	AD0	I	LSB	
95	VRT	I (A)	Reference top voltage input pin (for built-in A/D converter) ※6	Built-in A/D
96	AVDD5	—	Analog power supply (+5 V, for built-in A/D converter) ※6	
97	SHIN	I (A)	Analog signal input pin (for built-in A/D converter) ※6	
98	AVSS5	—	Analog GND (for built-in A/D converter) ※6	
99	VRB	I (A)	Reference bottom voltage input pin (for built-in A/D converter) ※6	
100	GRVSS	—	Analog GND for noise guard (for built-in A/D converter) ※6	

※6: AD0 to AD9 (Pins 85 to 94) or the built-in A/D (Pins 95 to 100) are selected by the serial data settings.
The preset setting when cleared is the built-in A/D.

I: Digital input
O: Digital output
I/O: Digital I/O
I (A): Analog input
O (A): Analog output

Electrical Characteristics

DC Characteristics

(Within recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}1,2,3,4,5		3.0	3.3	3.6	V
	AV_{DD}1,2	D/A out amplitude=2Vpp	4.7	5.0	5.5	V
	AV_{DD}3		3.0	3.3	5.5	V
	AV_{DD}4		4.7	5.0	5.5	V
	AV_{DD}5	A/D in amplitude = 2Vpp	4.7	5.0	5.5	V
Output voltage1	V_{OH1}*1	I_{OH} = -1.2mA	V_{DD}×0.8			V
	V_{OL1}*1	I_{OL} = 2.4mA			0.4	V
Output voltage2	V_{OH2}*2	I_{OH} = -2.4mA	V_{DD}×0.8			V
	V_{OL2}*2	I_{OL} = 4.8mA			0.4	V
Input voltage1	V_{IH1}*3		V_{DD}×0.7			V
	V_{IL}*3				V_{DD}×0.3	V
Input voltage2	V_{T+}*4,5		V_{DD}×0.8			V
	V_{T-}*4,5				V_{DD}×0.2	V
Hysteresis 1	$V_{T+}-V_{T-}$*4			0.5		V
Hysteresis 2	$V_{T+}-V_{T-}$*5			0.6		V
Input leak current1	I_{I1}*3,5	V_{IN}=V_{SS} or V_{DD}	-10		10	μA
Input leak current2	I_{I2}*4	V_{IN}=V_{SS} or V_{DD}	-40		40	μA
Input leak current3	I_{IH}*6	V_{IN}=V_{DD}	12	30	75	μA

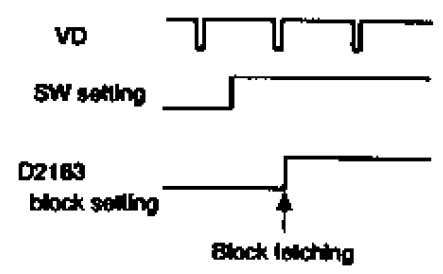
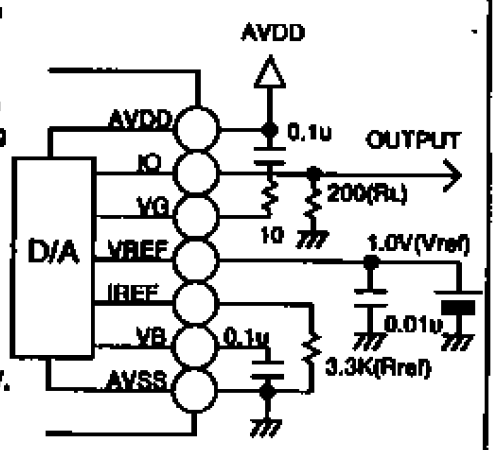
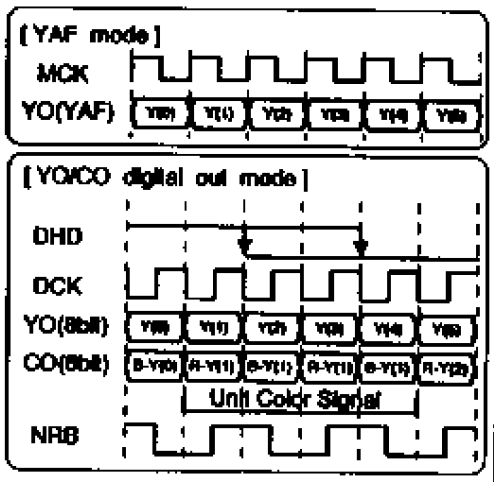
*1. All output pins other than CASCK, CASO and DCK
*2. CASCK,CASO,DCK
*3. AD9-AD0,MCK,ID,VRI,DCK,
*4. LRI,CO7-CO0,AEME,FLON,BLCOF,MIRIS,AEREF ,AGCMAX,GAMMA, AWB1-AWB3,SIFSEL
*5. XCS,SI, SCK,XCLR,CASI
*6. SIFSEL

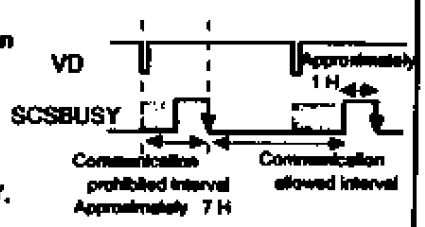
I/O Pin Capacitance

(V_{DD}=V_I=0V, f=1MHz)

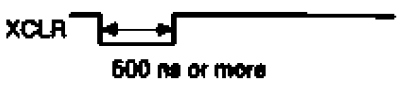
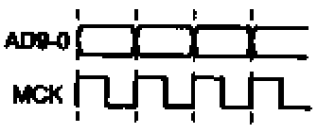
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

I/O Signals

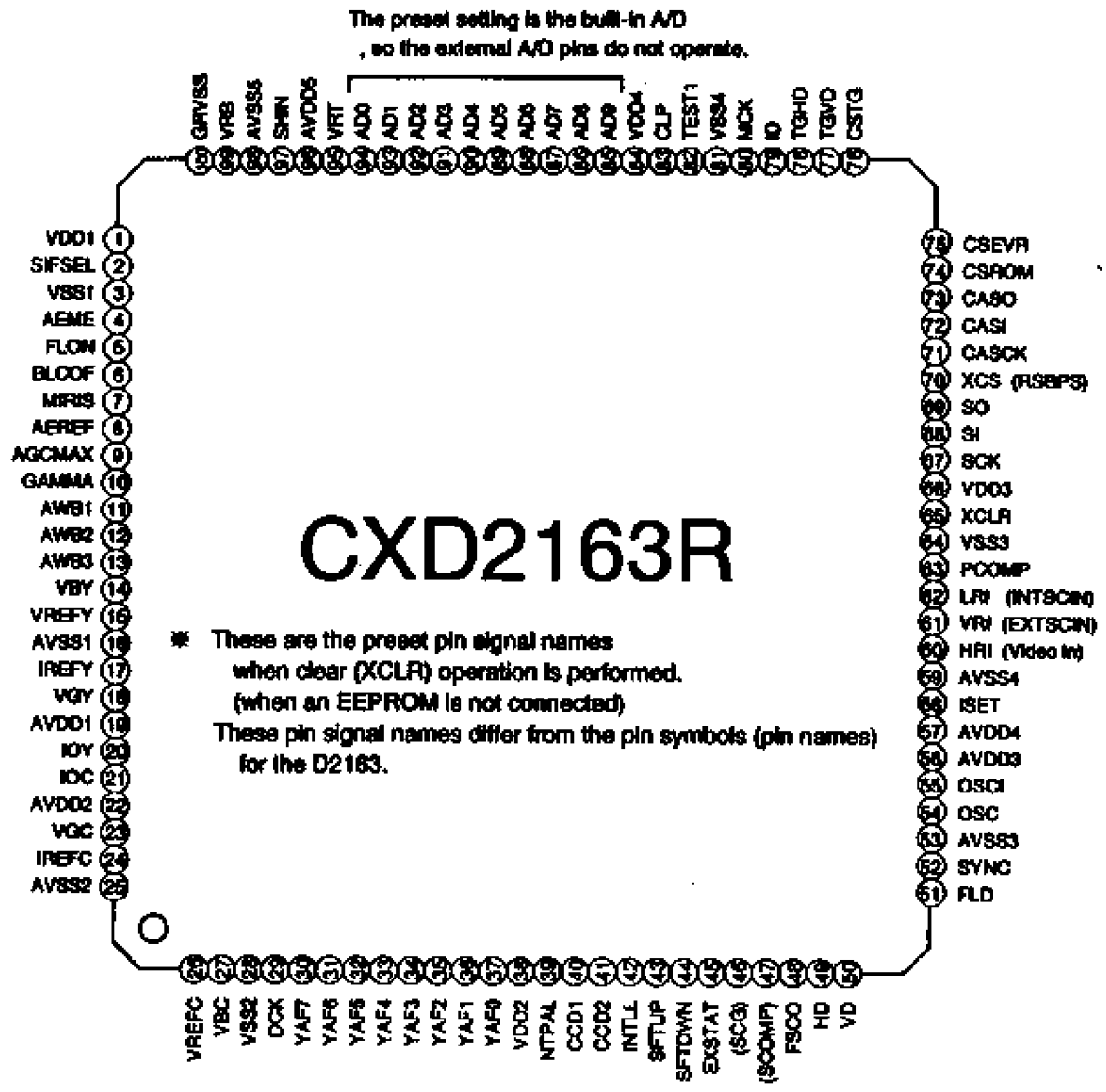
Symbol	Pin No.	Description
AEME FLON BLCOF MIRIS AEREF AGCMAX GAMMA AWB1 AWB2 AWB3	4 5 6 7 8 9 10 11 12 13	These are input pins for the SW setting. AE/AWB/gamma operation is switched by inputting high/low to these pins. The timing for loading the SW setting to each block is the V blanking following the field where the setting was input. 
VBY VREFY AVSS1 IREFY VGY AVDD1 IOY IOC AVDD2 VGC AVSS VREFC IREFC VBC	14 15 16 17 18 19 20 21 22 23 24 25 26 27	These pins form the peripheral circuit for the D/A converter that is used for luminance and chroma signal output. The voltage setting of Vref and the full-scale voltage (Vfs) of D/A can be matched by setting the ratio of RL to Rref to 1:16. The calculation is shown below: Vfs = Vref x 16 x RL/Rref * Notes - IO = Vfs/RL should be 7 mA or less. - RL should be 500 Ω or less. - When Vfs is 2 V, set the supply voltage (AVDD) to 5.0 V. Also, when 0V ≤ Vfs < 2V, operation is possible with a supply voltage (AVDD) of 3.3 V. 
YO0-7 CO0-7 NRB DCK (DHD)	30-37 39-46 47 29 (49)	YO/CO can be set to the following modes by the serial communication settings or the EEPROM setting values. CAT1 byte1 YDOUT= 0: YO=YAF mode 1: YO=Y digital out mode CAT1 byte1 UVDOUT= 0: CO= SW mode 1: CO=C digital out mode [YO = YAF mode (preset)] The Y-LPF processed luminance signal is output in sync with MCK (rise) for AF detection. The preset setting when cleared is YAF mode. [YO = Y digital out mode] The Y-LPF/gamma/aperture correction/ blanking processed luminance signal is output in sync with DCK (fall). The following output formats can be selected. CAT1 byte 1 REC601 = 0: YO = 8-bit straight binary 1: YO = REC601 [CO = SW mode (preset)] These pins are the TV mode setting/CCD type setting/external sync system I/Os. The timing for loading the setting systems is the same as for Pins 4 to 13. The preset setting when cleared is SW mode. [CO = C digital out mode] The color difference signal immediately before the chroma encoder is output in sync with DCK (fall). NRB can be used as the chroma phase reference. Output starts from the B-Y phase in sync with the fall of DHD. The starting point is defined by the frequency ratio of MCK and DCK. The following output formats can be selected. CAT1 byte 1 REC601 = 0: CO = two's complement format 1: CO = REC601 (offset binary) 

Symbol	Pin No.	Description
NRB DCK	47 29	[NRB output setting] Set (CAT1 byte 1 UVDOUT = 1) and (CAT9 byte 5 SCMPPIN = 1). [DCK I/O setting] The DCK pin is normally an input pin. However, in the following case only, MCK (13.5 MHz) is output to the DCK pin. DCK output setting: CCD type is set to 360H or 510H system ,and Set (CAT1 byte 1 SG135 = 1).
FSCO	48	This pin outputs the subcarrier frequency signal. This pin outputs the OSCI/OSCO (Pins 54 and 55) oscillation cell output, divided by 4.
HD	49	This pin is the horizontal sync signal output. It is used to align the output and phase of the D2163's built-in Y/C D/A. The output contents are switched by (CAT1 byte 14 HDPIN). To align the digital output pin YO/CO with the horizontal signal phase, switch this pin to DHD output. [DHD output setting] Set (CAT1 byte 1 DSYNC = 1).
VD	50	This pin is the vertical sync signal output. It is used to align the output and phase of the D2163's built-in Y/C D/A. The output contents are switched by (CAT1 byte 14 VDPIN). When using an external microcomputer, the field cycle microcomputer interrupt signal (SCSBUSY) can be output from this pin. The D2163 has a communication prohibited interval within the field which is convenient for synchronizing the start of microcomputer and D2163 communication. Communication is allowed after the fall of SCSBUSY.  [SCSBUSY output setting] Set (CAT1 byte 13 VDBUSY = 1).
FLD	51	This pin is the field discrimination signal output. The output contents are switched by (CAT1 byte 14 FLDPIN).
SYNC	52	This pin is the composite sync signal output. The output contents are switched by (CAT1 byte 14 SYNCPIN). The OPD (AE/AWB) detection frame (DISP) can be output from this pin. This pin should be used for analog iris detection circuits, etc. [DISP output setting] Set (CAT1 byte 13 SYNDISP = 1). [Frame type selection] Select the AE/AWB frame according to the (CAT10 byte 3 OPDDISP) code.
OSCI OSCO	54 55	These pins are connected to the internal oscillation cell. Connect a 4fsc crystal oscillator to these pins.
HRI (Video In)	60	This pin is the external sync signal input. It is connected internally to the sync separation circuit (built-in clamp) and can be used to input the composite video signal (1 Vp-p). When not using external sync, fix the HRI pin high. Input the composite video signal or H reset signal according to the following conditions. Composite video signal input: When VS/VBS is locked during auto identification mode or when (CAT9 byte 1 SGMODE) is set to VS/VBS mode. (Care should be taken when using LL together with VS/VBS during auto mode.) H reset signal: When (CAT9 byte 1 SGMODE) is set to VRHR mode.

Symbol	Pin No.	Description
VRI (EXTSCIN)	61	This pin is the external sync signal input. When inputting an external burst signal, extract the burst with an external circuit, set the burst to the digital amplitude value (3.3 Vpp) and then input it to the VRI pin. The continuous subcarrier signal can be used as the input external burst signal, but the phase comparison interval is only near the burst signal position (SCG (Pin 46)). When not using external sync, fix the VRI pin high. Input the external burst signal or V reset signal according to the following conditions. External burst signal: When VBS is locked during auto identification mode or when (CAT9 byte 1 SGMODE) is set to VBS mode. (Care should be taken when using LL together with VS/VBS during auto mode.) V reset signal: When LL/VS is locked during auto identification mode or when (CAT9 byte 1 SGMODE) is set to LL/VRHR mode.
LRI (INTSCIN)	62	This pin is the external sync signal I/O. When VBS is locked, the FSCO (Pin 48) subcarrier output can be delayed with an external circuit and then re- input to the LRI pin for use in the chroma encoder in order to phase shift the subcarrier signal generated by the D2163. (In this mode, the LRI pin functions as the clock input pin for the chroma encoder block.) The LRI pin is normally the LALT signal output, but under the following conditions it functions as the LALT reset signal input or internal subcarrier input. LALT reset signal input: When (CAT9 byte 1 SGMODE) is set to VRHR mode. Internal subcarrier input: When (CAT9 byte 5 FSCPCMP = 1) is set with VBS locked during auto identification mode; or when (CAT9 byte 5 FSCPCMP = 1) is set with (CAT9 byte 1 SGMODE) is set to VBS mode.
PCOMP	63	This pin is the charge pump type phase comparator output for HPLL/VPLL. HPLL or VPLL phase comparison is selected according to the external sync mode of the SG block. The PCOMP output status can be classified into the following three states according to the SG mode. SG mode (including auto identification mode) No PCOMP output: INT, VRHR PCOMP-V phase comparison output: LL PCOMP-H phase comparison output: VS, VBS
EXSTAT (CO1)	45	This pin is the external sync mode discrimination output. It is normally low, but goes high only when the external sync mode of the SG block is LL mode (including auto identification). This pin is convenient for switching the characteristics of the external PLL-LPF when using the PCOMP pin for both HPLL and VPLL. To use EXSTAT, set (CAT1 byte 1 UVDOUT = 0).
SCG (CO0)	46	This pin is the subcarrier gate pulse output. When the external sync mode of the SG block is VBS mode, this pin detects the externally input burst signal interval and outputs a high pulse only during the burst interval. The subcarrier phase comparator performs phase comparison only during this gate pulse interval. To use SCG, set (CAT1 byte 1 UVDOUT = 0) and (CAT9 byte 5 FSCPCMP = 1).
SCOMP (NRB)	47	This pin is the subcarrier phase comparator output. It outputs the results of comparing the external burst input (VRI (Pin 61)) and the internal burst input (LRI (Pin 62)). The comparison interval is the SCG (Pin 46) pulse interval. To use SCOMP, set (CAT1 byte 1 UVDOUT = 0) and (CAT9 byte 5 FSCPCMP = 1).

Symbol	Pin No.	Description
XCLR	65	This is the clear signal input pin. This clear operation initializes the entire chip and starts EEPROM loading operation. Input a low pulse. (This pin is active low.) 
SIFSEL SCK SI SO XCS (RSBPS)	2 67 68 69 70	These pins are the microcomputer/RS232C serial communication I/Os. [When using microcomputer communication] Set the SIFSEL pin low. SI/SO data is transferred in sync with SCK only while XCS = low. [When using RS232C communication] Set the SIFSEL and SCK pins high. At this time, the XCS pin functions as the pin (RSBPS) which sets the RS232C transfer speed. RSBPS = 0: 4800 bps, 1: 9600 bps. (See the description of the serial communication method for other details.)
CASCK CASI CASO CSROM CSEVR CSTG	71 72 73 74 75 76	These pins are the serial communication I/Os for the camera peripheral ICs. The peripheral ICs with which communication is performed are the TG, EVR and EEPROM. The TG and EVR communication timing is once per field during the V blanking. EEPROM read communication is performed for four consecutive fields only during the clear operation (XCLR). EEPROM write communication is performed once per field during the V blanking during AWB (push lock mode) and SG (external sync shifter).
TGVD TGHD ID MCK	77 78 79 80	These pins are I/Os for synchronization with the TG.
CLP1	83	This pin is the clamp pulse output for DC fixing with a S/H IC.
AD0-9	85-94	These pins are digital data inputs for the external A/D. AD0 to 9 input the A/D converted data output by the CCD in straight binary format. When using an external A/D, set (CAT1 byte 2 ADSEL = 0). When using an external 9-bit A/D, connect AD0 (Pin 94) to GND. 
VRT SHIN VRB GRVSS	95 97 99 100	These pins are analog inputs for the built-in A/D. The preset setting when cleared is the built-in A/D. GRVSS (Pin 100) is used to guard the built-in A/D from internal noise. Connect these pins to GND points with as little noise as possible.

Preset pin signal names when reset operation is performed



(1) To perform pin settings other than those noted above, write the settings to the EEPROM or switch the setting using microcomputer/RS232C communication.

(2) To operate SCG and SCOMP, switch the setting using the EEPROM or microcomputer/RS232C communication so that (CAT9 byte 5 FSCPCMP = 1).

Microcomputer communication

(1) The CXD2163's microcomputer interface circuit is designed as a serial interface with a general-purpose single-chip microcomputer.

(2) The communication method is the full duplex sync method, and serial clock sync communication is performed in both directions between the CXD2163 and microcomputer. The recommended communication speed is approximately 500 K to 1 Mbps .

(3) The CXD2163 and microcomputer are connected by the following four wiring lines.
Viewed from the CXD2163:

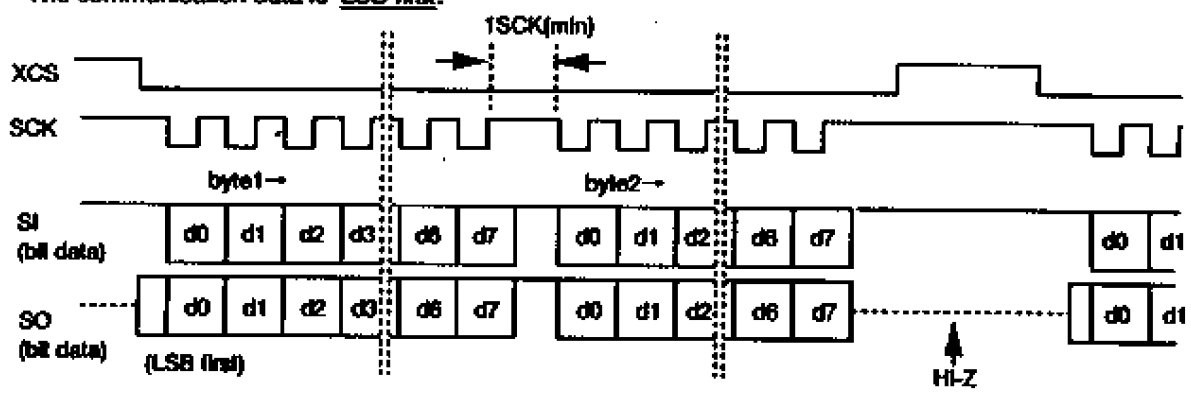
- XCS = CXD2163 chip select input
- SCK = Clock input for serial transfer
- SI = CXD2163 serial setting input (image parameters, etc.)
- SO = CXD2163 serial data output (AE/AWB integral value, etc.)

* When performing microcomputer communication, be sure to set the SIFSEL pin low.

(4) Communication timing

1. XCS is set low and the CXD2163's communication circuit is activated.
2. SI data is loaded in sync with the rise of SCK.
3. SO is output in sync with the fall of SCK.
4. Serial data is grouped in 8-bit units with the number of data set as desired.
   At least one SCK clock must be left open between 8-bit data units.
5. XCS is set high and communication ends.

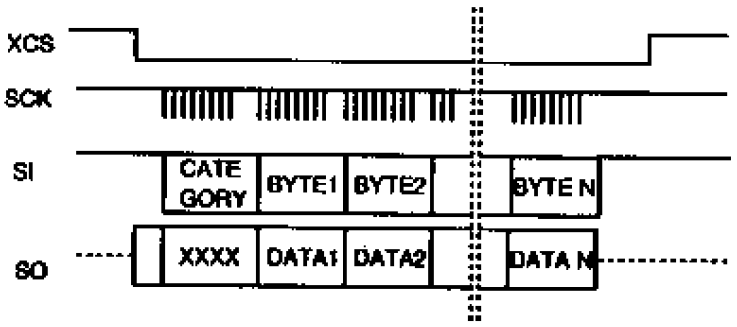
* The communication data is LSB first.



(5) Communication format

The byte string transmitted from the microcomputer while XCS is low is treated as a single category.
Categories are classified by the number sent in the first byte.
Data output is synchronized with the input, and the data output contents are determined by the category.

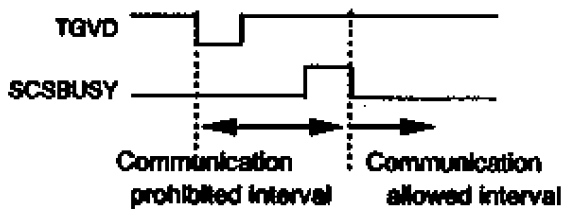
(See the Communication Parameter Table for the byte data and data output contents.
Note that the data output until the category is determined is "Don't care".)



(6) Serial communication prohibited interval The CXD2163 has an internal microcontroller and performs communication at regular intervals using an internal bus. As a result, the microcontroller occupies the internal bus and communications cannot be accepted from the external microcomputer during the following interval.

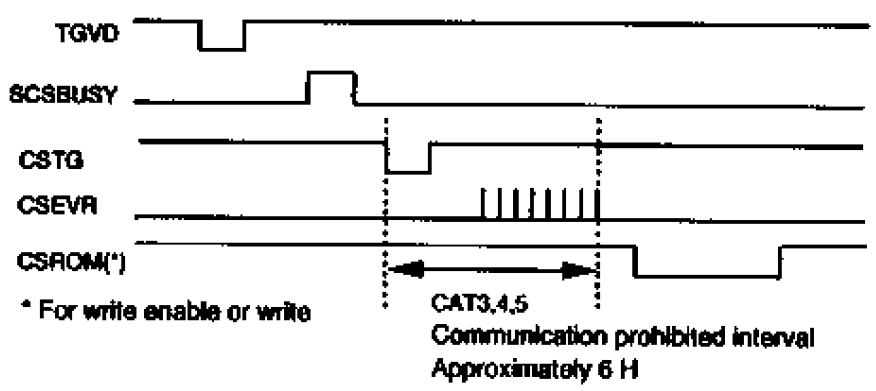
· Approximately 7 H from the fall of TGVD to the fall of SCSBUSY

* SCSBUSY uses the VD pin. CAT1 byte 13 bit 6 VDBUSY must be set to 1 in order to output this signal.



(7) Precautions when transferring data to peripheral ICs Rather than performing serial communication directly between the microcomputer and peripheral ICs (TG, EVR, EEPROM), serial communication can be performed with peripheral ICs via the CXD2163. Care must be taken for the following points when performing communication using this method.

· Communication between peripheral ICs and the CXD2163 is performed at the beginning of the field sequence. Therefore, category communication which includes data to be sent to the TG and EVR (categories 3, 4 and 5) should be performed outside of this interval.
· If communication falls within this interval, the correct data may not be sent to peripheral ICs.
· The communication timing with each IC can be checked by measuring CSTG and CSEVR. This interval is a maximum of approximately 6 H (for the 510H) . (See separate items for the EEPROM.)



(8) Communication (wiring) check
The CXD2163 is designed so that when the clear pin is set low, the serial input is latched once and then output in that condition from the serial output in order to check the communication line wiring. This method allows the signal lines from the microcomputer to the CXD2163R to be checked logically.

RS232C communication

(1) The CXD2163's RS232C interface circuit is designed for communication with the serial port of a personal computer. The CXD2163 has a built-in I/O buffer (input 16 bytes, output 32 bytes).

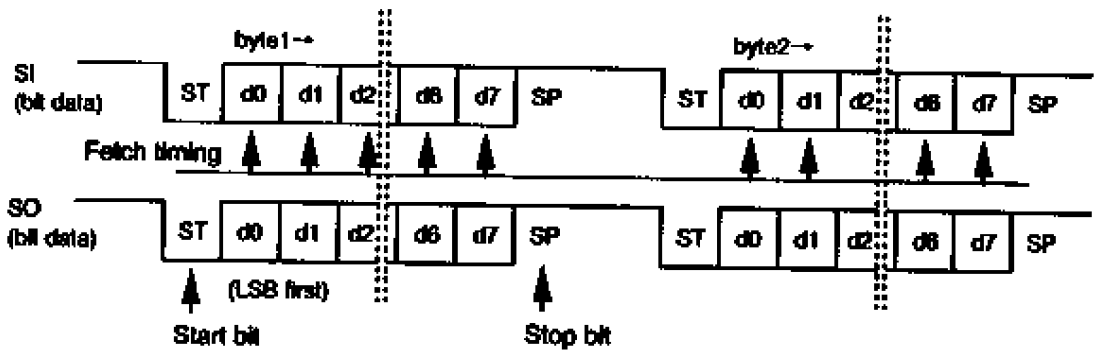
(2) The communication method is the full duplex start-stop sync method, and serial clock start-stop sync communication is performed in both directions between the CXD2163 and personal computer.
The communication speed can be switched to 9600 bps or 4800 bps.
The communication settings are an 8-bit data length, no parity, one start bit, one stop bit and no flow control.

(3) The CXD2163 and personal computer are connected by the following two wiring lines.
Viewed from the CXD2163:
- SI = CXD2163 serial setting input (image parameters, etc.)
- SO = CXD2163 serial data output (AE/AWB integral value, etc.)

* When performing RS232C communication, be sure to set the SIFSEL and SCK pins high.
* The communication speed is 9600 bps when XCS = high, and 4800 bps when XCS = low.

(4) Communication timing
1. The CXD2163 fetches 8 bits of data at the timing determined by the communication speed after the fall of SI.
2. SO is output in sync with the SI data. 3. Serial data is grouped in 8-bit units with the number of data set as desired.

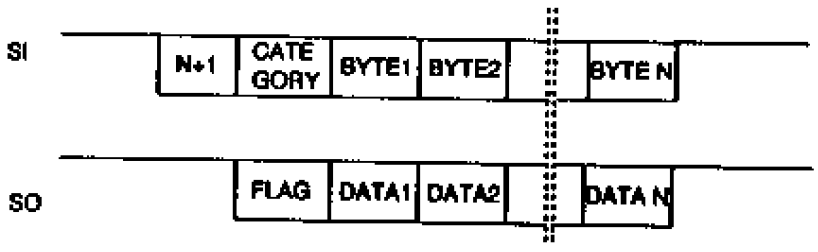
* The communication data is LSB first.



(5) Communication format

The CXD2163 sends the number of bytes in the data string to be sent in the first byte in order to divide the data string (category). The data from the second byte onward has the same format as during microcomputer communication.

Also, the serial output is output in sync with the input like with microcomputer communication. However, note that the CXD2163's internal status flag is output in the first "don't care" byte (the second input byte) during microcomputer communication. When d7 of this byte is 1, data is still remaining in the internal buffer and new communications are ignored.

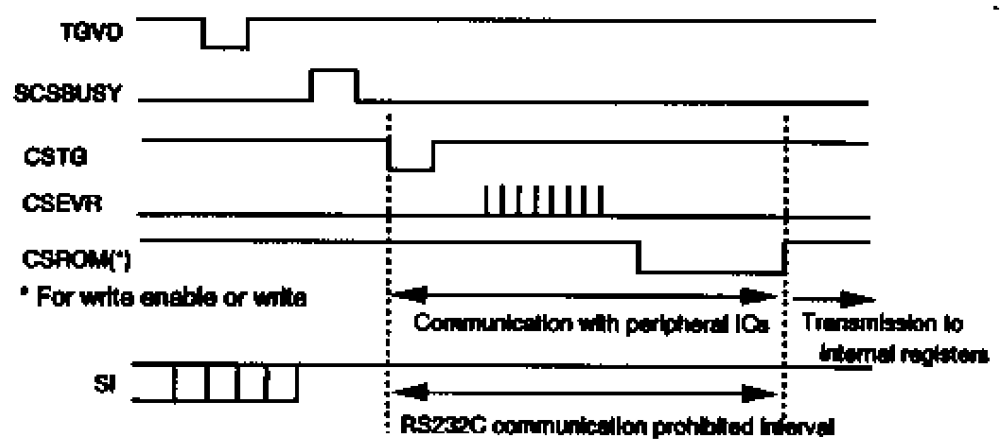


(6) Precautions for serial communication As mentioned in (5), during the CXD2163's RS232C communication mode the communication contents are first accumulated in the internal buffer and then data is sent to the internal registers after communication ends. Accordingly, the next communication is ignored until the data is read from the buffer.

Reading is normally performed immediately after communication ends and finishes in approximately 20 us. There are normally no problems with this operation, but care must be taken for the following two cases.

· When RS232C communication ends during the period from the fall of TGVD to the end of communication peripheral ICs

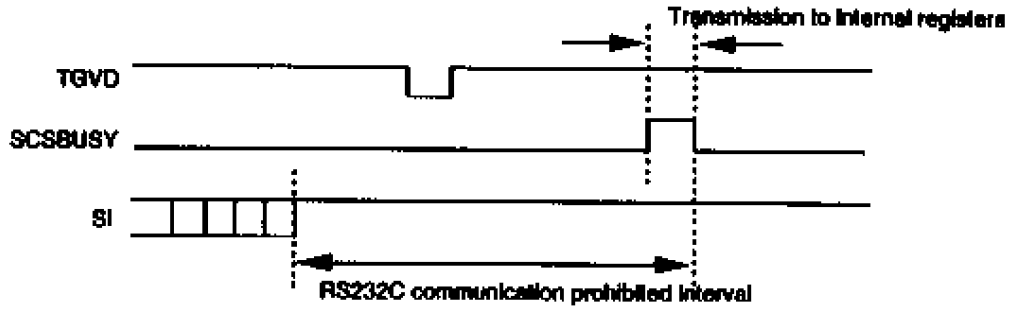
--> In this case, data is transmitted to the internal registers after data transmission with peripheral ICs. Therefore, the next communication must be performed after this transmission is completed.



· When category 8 communication is performed

* Category 8 communication data is transmitted to the internal registers one time per field while SCSBUSY is high. Accordingly, after performing category 8 communication, communication cannot be performed again until SCSBUSY changes from high to low.

* The communication prohibited interval can be checked by the internal status flag. Also, there should be a gap of at least one field between category communications.



(7) Internal status flag acquisition and clearing the internal reception buffer

· Internal status flag acquisition

It is possible to acquire only the internal status flag without sending category data. In this case, transmit 1 in the first byte and 0 in the second byte.

· Clearing the internal reception buffer

When communication stops part way due to some problem
(when the number of bytes to be transmitted sent in the first byte and the number of actually transmitted bytes differ)
The CXD2163's serial circuit status may switch to communication-busy mode.
--> In these cases, transmit 19 bytes of 0 to clear the internal reception buffer and then transmit the correct data again.

(8) Serial output limitations

The size of the internal transmission buffer is 32 bytes, so some serial outputs listed in the Communication Parameter Table may not pass through the buffer.

Category 5, 6 and 10 data are input to the buffer, but other data is read directly from the internal registers. Therefore, when communication falls within the microcomputer communication prohibited interval, accurate serial output values may not be obtained. In order to accurately read data other than category 5, 6 and 10 data, the data must be acquired by microcomputer communication.

(9) Communication check

The CXD2163 is designed so that when the clear pin is set low, the serial input is latched once and then output in that condition from the serial output in order to check the communication line wiring. This method allows the signal lines from the RS232C pins to the CXD2163 to be checked logically.

(10) Noise problems

The CXD2163 operates by detecting the falling edge of the serial input. Therefore, normal operation cannot be guaranteed when noise in excess of the logic level is present in the serial input.

Serial Data Table of CXD2163R

Classification of Serial Data

Category	I/O	Contents Byte0	Contents Byte1~
CAT1 : FIX	In	01h	Initially fixed parameters
	Out	—	—
CAT2 : FIELD	In	02h	Y/C control parameters in field cycle
	Out	—	—
CAT3 : CLAMP	In	03h	Clamp control parameters
	Out	—	OB integral data output
CAT4 : DCREF	In	04h	DC setting (EVR -related) parameters
	Out	—	—
CAT5 : AE	In	05h	AE control parameters
	Out	—	AE integral data output
CAT6 : AWB	In	06h	AWB control parameters
	Out	—	AWB integral data output
CAT7 : FIXOPD	In	07h	Initially fixed parameters for OPD
	Out	—	—
CAT8 : MCRCON	In	08h	Control parameters for Micro-controller
	Out	—	—
CAT9 : SG	In	09h	Control parameters for SG
	Out	—	SG status output
CAT10: EXTCON	In	0Ah	External control parameters (from micom/PC)
	Out	—	Y/C Sampling data output

* "Block" and "Address" located at the upper right of the Serial Communication Data Table are as follows.

Block = This indicates the block which reflects that parameter.
(the destination block for that parameter transmission)

Address = EEPROM write/read address

Communication category concepts

(1) CXD2163 category classifications are " divided by control subject " to make the byte position for each parameter easy to remember.

(2) There are three major category concepts as follows.

1: Parameters set initially during power on and set infrequently thereafter
→ CAT1 (FIX), CAT4 (DCREF), CAT7 (FIXOPD)

2: Field cycle parameters and camera signal processing system parameters which are controlled frequently as necessary
→ CAT2 (FIELD), CAT3 (CLAMP), CAT5 (AE), CAT6 (AWB), CAT9 (SG)

3: Special function setting/mode setting/control characteristic and other non- camera signal processing system parameters such as external settings from the microcomputer or personal computer and SW pin settings, etc.
→ CAT8 (MCRCON), CAT10 (EXTCON)

(3) Category numbers are assigned to maintain relevancy with preceding and following numbers. Category numbers 1 to 4 are basic camera signal processing categories which emphasize Y/C signal processing.

* CAT1 (FIX) → CAT2 (FIELD) → CAT3 (CLAMP) → CAT4 (DCREF)

Category numbers 3 to 7 are categories which emphasize Y/C feedback control. In particular, these categories contain many AE-related parameters, and related parameters are arranged in preceding and following categories.

* CAT3 (CLAMP) → CAT4 (DCREF) → CAT5 (AE) → CAT6 (AWB) → CAT7 (FIXOPD)

Category numbers 8 to 10 are categories which emphasize control functions other than the Y/C signal processing system.

* CAT8 (MCRCON) → CAT9 (SG) → CAT10 (EXTCON)

(4) Remembering the above concepts will make it easy to find communication parameters.

Points for caution when making communication settings

(Microcontroller overwrite function)

(1) The CXD2163 has a built-in microcontroller to realize camera functions without a microcomputer. The microcontroller controls the following categories with a field cycle.
CAT2 (FIELD), CAT3 (CLAMP), CAT5 (AE), CAT6 (AWB)

(2) The microcontroller sets the above categories for each field. Therefore, when setting the above categories externally using a microcomputer or personal computer, settings should be made using the following method.

(3) Even if external settings are made for categories controlled by the microcontroller, the microcontroller overwrites these settings thereby invalidating the external communication. Therefore, the microcontroller control functions must be set to OFF for each category so that overwrite is not performed. (When setting some items in a category externally, all controls for that category must be set externally.)

(CAT8 byte1,2= MCRAE, MCRAWB, MCREXT,
MCRSPRS, MCRSG, MCRDIP, MCRCLP, MCRGAM)

(4) Therefore, when performing communication settings externally, set the microcontroller control functions to OFF as outlined below.

1: When setting all microcontroller functions to OFF (external microcomputer control)
→ MCREXT = 1
2: When setting HUE/GAIN and other CAT2 (FIELD) controls
→ MCRSPRS = 1
3: When setting feedback controls such as CAT5 (AE), CAT6 (AWB) and CAT3 (CLAMP) to OFF
→ MCRAE/MCRAWB/MCRCLP = 1
4: When not using the SW pins (Pins 4 to 13) of the CXD2163
(when using the CAT8 byte 3 and 4 SW communication settings)
→ MCRGAM/MCRDIP = 1

Initial operation when cleared

(1) When a clear pulse is input to the CXD2163's clear pin (Pin 65)
The internal registers of the CXD2163 are initialized according to the following procedures.
(Particular care should be taken for the TV mode and CCD type.)

(2) When there is no EEPROM
→ When the CXD2163 performs clear operation, first EEPROM read operation is performed.
If there is no EEPROM, the first byte input from the EEPROM pin is not SS1 code so EEPROM read operation is not performed.
→ Next, the NTPAL, CCD1 and CCD2 pins (Pins 39 to 41) are input and the internal registers are initialized according to the settings of these pins.

(3) When an EEPROM is present
→ When the CXD2163 performs clear operation, first EEPROM read operation is performed.
In this case, the first byte input from the EEPROM pin is SS1 code, so the CXD2163 is divided into three fields, EEPROM read is performed and the internal registers are initialized.
→ In this case, the NTPAL, CCD1 and CCD2 pins (Pins 39 to 41) are not input so the settings of these pins are not reflected.

Category 1 : FIX [Initially fixed parameters]

		Serial Input					
Byte	bit	Name	Description	#1	Block	address	
0	0	CAT1	Category select code 01h : FIX				
	1						
	2						
	3						
	4						
	5						
	6						
	7						
1	0	NTPAL	TV system mode 0: NTSC 1: PAL	0	Common	01h	
	1	CCD1	CCD mode 0h: 360H 1h: 510H	1h	Common		
	2	CCD2	2h: 720H 3h: 760H				
	3	YDOUT	Data select for Y digital output 0: YAF out 1: Digital out	0	Y		
	4	UVDOUT	Data select for C digital output 0: TEST 1: Digital out	0	Common		
	5	REC601	Format select for digital output 0: linear 1: REC601	0	Common		
	6	DSYNC	Sync signal (HDpin) phase select 0: for Analog 1: for Digital	0	SG		
	7	SG135	PLL reference selection 0: 4fsc ref. 1: 13.5MHz ref.	0	SG		
2	0	ADSEL	A/D selection 0: Ext-A/D 1: Int-A/D	1	PRE	02h	
	1	ADINV	A/D clock polarity selection 0: Forward 1: Reversed	0	PRE		
	2	ADDLY	10ns delay for A/D output 0: 0 delay 1: 10ns delay	0	PRE		
	3	DL1CK	1 CK delay for A/D output 0: 0 delay 1: 1 CK delay	0	PRE		
	4	(low)	"0" fixed	0h			
	5						
	6						
	7	NEGPOS	Negative/positive inversion 0: Positive 1 : Negative	0	Y/C		
3	0	SETUP	Setup level setting 0 IRE (0h)~8.5 IRE (Fh) / (4bit step)	Dh	Y	03h	
	1						
	2						
	3						
	4	WCLIP	White clip level setting (Y-D/A max= 255dec) 0h: 142d 1h: 160d 2h: 178d 3h :187d 4h: 196d 5h: 205d 6h: 214d 7h :255d	8h	Y		
	5						
	6						
	7	SUP601	Setup for digital output(REC601 mode) 0:setup off 1:setup on	0	Y		
4	0	SYNLV	Sync amplitude adjust (for line adjustment) 2x(0h) ~ 2x(7h) 2LSB step	6h	Y	04h	
	1						
	2						
	3	SYNLVPM	Sync amplitude adjust direction 0: Decrease 1: Increase	1	Y		
	4	YDLY	Delay adjust for Y signal (1~16 step) 1(0h)~16(Fh) MCK step	4h	Y		
	5						
	6						
	7						
5	0	VHAPSL	Aperture slice level setting Max(Fh) ~Min(0h)=off	4h	Y	05h	
	1						
	2						
	3						
	4	VAPSL	V-aperture slice level setting Max(7h) ~Min(0h)=off	4h	Y		
	5						
	6						
	7	VAPLIM	V-aperture limiter switch 0: off 1: on	0	Y		
6	0	HLAPSL	High light aperture slice level adjustment	4h	Y	06h	
	1						
	2						
	3						
	4	HLAPPC	High light aperture threshold level adjustment	3h	Y		
	5						
	6	HLAPDS	High light aperture detect point selection 0:det before γ 1: det γ	0	Y		
	7	dummy					

#1: Initial setting value with Power-on

Category 1 : FIX [Initially fixed parameters]

		Serial Input				
Byte	bit	Name	Description	#1	Block	Address
7	0	HLAPPG	LSB MSB High light aperture signal positive gain adjustment	3h	Y	07h
	1					
	2	HLAPMG	LSB MSB High light aperture signal negative gain adjustment	2h	Y	
	3					
	4	dummy				
	5					
	6					
	7					
8	0	RMATY	LSB R signal color separation matrix coefficient R = Cr + <RMATY> x Yr + <RMATC> x Cb ×0.5(7Fh)~×0.0(00h)~×−0.5(80h) MSB (Data format -2's)	32h	C	08h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	RMATC	LSB R signal color separation matrix coefficient R = Cr + <RMATY> x Yr + <RMATC> x Cb ×0.5(7Fh)~×0.0(00h)~×−0.5(80h) MSB (Data format -2's)	F8h	C	09h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	BMATY	LSB B signal color separation matrix coefficient B = Cb + <BMATY >x Yb + <BMATC> x Cr ×0.5(7Fh)~×0.0(00h)~×−0.5(80h) MSB (Data format -2's)	32h	C	0Ah
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	BMATC	LSB B signal color separation matrix coefficient B = Cb + <BMATY> x Yb + <BMATC> x Cr ×0.5(7Fh)~×0.0(00h)~×−0.5(80h) MSB (Data format -2's)	D3h	C	0Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
12	0	BSTLV	LSB Burst level adjustment Burst level = <BSTLVL>X2 (LSB) NTSC: 12h PAL: 0Dh MSB	0Dh	C	0Ch
	1					
	2					
	3					
	4					
	5	CPHSEL	LSB Chroma identification signal reference phase selection MSB 0h: 0delay 1h: 1delay 2h: 2delay 3h: 3delay (1delay=1MCK)	1h	SG	
	6					
	7	LIDSEL	Line identification signal reference phase selection 1:ID sig inv.	0	C	
13	0	MODSW	Chroma encoder modulation switch 0: ON 1: OFF	0	C	0Dh
	1	(low)	"0" fixed	0		
	2	ENCSW	Encoder clock switch 0: ON 1: OFF	0	C	
	3	SYNCSW	Sync switch for Y D/A converter 0: ON 1: OFF	0	Y	
	4	(low)	"0" fixed	0		
	5	SYNDISP	SYNC pin output selection 0: Sync 1: Diap (OPD wind)	0	SG	
	6	VDBUSY	VD pin output selection 0: VD 1:SCSBUSY	0	SG	
	7	(low)	"0" fixed	0		

#1: Initial setting value with Power-on

Category 1 : FIX [Initially fixed parameters]

	Serial Input					
Byte	bit	Name	Description	#1	Block	Address
14	0 1	SYNPIN	LSB Sync pin output selection MSB 0h: SYNC 1h:CBLK 2h: BF 3h: SCG	0h	SG	0Eh
	2 3	FLDPIN	LSB FLD pin output selection MSB 0h: SYNC 1h:CBLK 2h: BF 3h: SCG	0h	SG	
	4 5	VDPIN	LSB VD pin output selection MSB 0h: SYNC 1h:CBLK 2h: BF 3h: SCG	0h	SG	
	6 7	HDPIN	LSB HD pin output selection MSB 0h: SYNC 1h:CBLK 2h: BF 3h: SCG	0h	SG	

#1: Initial setting value with Power-on

Category 2 : FIELD [Field communication parameters]

		Serial Input				
Byte	bit	Name	Description	#1	Block	Address
0	0 1 2 3 4 5 6 7	CAT2	LSB Category select code 02h : FIELD MSB			
1	0 1 2 3 4 5 6 7	YGAIN	Adjustment of luminance signal gain ×2(FFh)~×0 (00h)	86h	Y	0Fh
2	0 1	HAPGL	LSB H-aperture (low band) gain adjustment 0h: x0 1h: x0.5 2h: x1 3h: x2 MSB	3h	Y	10h
	2 3	HAPGH	LSB H-aperture (high band) gain adjustment 0h: x0 1h: x1 2h: x2 3h: x4 MSB	2h	Y	
	4 5 6 7	VAPG	LSB V-aperture gain adjustment ×1 (Fh)~×0(0h) MSB	Fh	Y	
3	0 1 2 3	VHAPG	LSB V-aperture gain adjustment ×1 (Fh)~×0(0h) MSB	8h	Y	11h
	4 5	HLAPG	LSB High light aperture gain adjustment MSB	2h	Y	
	6 7	dummy				
4	0 1	CSVLV	LSB Chroma suppress (V-aperture) level selection MSB	0h	C	12h
	2 3	CSVTH	LSB Chroma suppress (V-aperture) threshold level selection MSB	1h	Y	
	4 5	CSHLV	LSB Chroma suppress (high light) level selection MSB	0h	C	
	6 7	CSHTH	LSB Chroma suppress (high light) threshold level selection MSB	2h	Y	
5	0 1 2	YGAM	LSB Y gamma level adjustment High γ (Fh)~Low γ (0h) MSB	4h	Y	13h
	3	YSGAMLV	Y gamma : low level signal compress level selection	0	Y	
	4 5 6	YKNE	LSB Y knee level adjustment MSB	0h	Y	
	7	YSGAMSW	Y gamma : low level signal compress function switch 1: ON	0		
6	0 1 2	CGAM	LSB Chroma gamma level adjustment High γ (Fh)~Low γ (0h) MSB	4h	C	14h
	3	CKNCLIPO	Chroma knee clip level 0 selection	1h	C	
	4 6 8	CKNE	LSB Chroma knee level adjustment MSB	7h	C	
	7	CKNCLIP1	Chroma knee clip level 1 selection	1	C	

#1: Initial setting value with Power-on

Category 2 : FIELD [Field communication parameters]

		Serial Input				
Byte	bit	Name	Description	#1	Block	Address
7	0	RBQUAD	LSB Quadrant selection for independent adjustment of linear matrix 0: OFF 1st quadrant (bit 0) 2nd quadrant (bit 1) 1: ON 3rd quadrant (bit 2) 4th quadrant (bit 3) MSB	Fh	C	
	1					
	2					
	3					
	4	CONGAIN	Control gain selection for linear matrix adjustment 1: gain set	1	C	
	5	CONHUE	Control hue selection for linear matrix adjustment 1: hue set	1	C	
	6	dummy				
	7					
8	0	RYGAIN	LSB Linear matrix coefficient R-Y GAIN X-1(80h)~X0(00h)~X1(7Fh) MSB (Data format -2's)	19h	C	4Fh 51h 53h 55h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	BYGAIN	LSB Linear matrix coefficient B-Y GAIN X-1(80h)~X0(00h)~X1(7Fh) MSB (Data format -2's)	0Dh	C	50h 52h 54h 56h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	RYHUE	LSB Linear matrix coefficient R-Y HUE X-1(80h)~X0(00h)~X1(7Fh) MSB (Data format -2's)	D0h	C	57h 59h 5Bh 5Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	BYHUE	LSB Linear matrix coefficient B-Y HUE X-1(80h)~X0(00h)~X1(7Fh) MSB (Data format -2's)	F8h	C	58h 5Ah 5Ch 5Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 3 : CLAMP [Clamp control parameters]

		Serial Input					Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0-7	CAT3	Category select code 03h : CLAMP				0-7	—	Unfixed data output	
1	0-7	BLACK1L	Black level adjustment for digital clamp(S1) LSB 8bit ->Integral part= 7bit ->decimal part= 2bit (total 9bit= int7. dec2 bit) (Data format –BIN)	00h	Y/C	15h	0-7	OB1L	OB integral level output for digital clamp (S1) LSB 8bit ->Integral part= 7bit ->decimal part= 5bit (total 12bit= int7. dec5 bit) (Data format –BIN)	PRE
2	0-7	BLACK2L	Black level adjustment for digital clamp(S2) LSB 8bit ->Integral part= 7bit ->decimal part= 2bit (total 9bit= int7. dec2 bit) (Data format –BIN)	00h	Y/C	16h	0-3	OB1M	OB integral level output for digital clamp (S1) MSB 8bit (Data format –BIN)	PRE
							4-7	OB2M	OB integral level output for digital clamp (S2) MSB 8bit (Data format –BIN)	PRE
3	0	BLACK1M	BLACK1 MSB 1bit	0	Y/C	17h	0-7	OB2L	OB integral level output for digital clamp (S2) LSB 8bit ->Integral part= 7bit ->decimal part= 5bit (total 12bit= int7. dec5 bit) (Data format –BIN)	PRE
	1	BLACK2M	BLACK2 MSB 1bit	0	Y/C					
	2-7	dummy								
4	0-7	SHOFST	Offset voltage adjustment for S/H IC (FFh)~(00h) (Data format –BIN)	3Dh	EVR ch7	18h	0-7	—	Unfixed data output	
5	0-7	EVRUSR	EVR voltage adjustment for USR setting (FFh)~(00h) (Data format –BIN)	69h	EVR ch8	19h	0-7	—	Unfixed data output	
6	0-7	(low)	"0" fixed	00h		1Ah	0-7	—	Unfixed data output	

#1: Initial setting value with Power-on

Category 3 : CLAMP [Clamp control parameters]

	Serial Input						Serial Output		
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description
7	0 1 2 3 4 5 6 7	(low)	"0" fixed	0		18h	0 1 2 3 4 5 6 7	—	Unfixed data output

#1: Initial setting value with Power-on

Category 4 : DCREF [DC setting parameters]

		Serial Input				
Byte	bit	Name	Description	#1	Block	Address
0	0 1 2 3 4 5 6 7	CAT4	MSB LSB Category select code 04h : DCREF			
1	0 1 2 3 4 5 6 7	DAVRFY	MSB LSB Reference voltage adjustment for Y-D/A converter	70h	EVR ch3	1Ch
2	0 1 2 3 4 5 6 7	DAVRFC	MSB LSB Reference voltage adjustment for C-D/A converter	68h	EVR ch4	1Dh
3	0 1 2 3 4 5 6 7	VSUB	MSB LSB VSUB adjustment for CCD	80h	EVR ch5	1Eh
4	0 1 2 3 4 5 6 7	VRGL	MSB LSB VRGL adjustment for CCD	80h	EVR ch6	1Fh

#1: Initial setting value with Power-on

Category 5 : AE [AE control parameters / AE integral output]

Byte	bit	Serial Input Name	Description	#1	Block	Address	bit	Serial Output Name	Description	Block
0	0–7	CAT5	Category select code 05h : AE				0–7	—	Unfixed data output	
1	0–7	AGCCNT	Voltage control data for AGC-amp GAIN	1Eh	EVR ch2	20h	0–7	INTEG0L	WIND0 Y integral data output LSB 8bit (Data format =BIN)	OPD
2	0–7	IRISV	Voltage control data for mechanical IRIS	FFh	EVR ch1	21h	0–7	INTEG0M	WIND0 Y integral data output MSB 8bit (Data format =BIN)	OPD
3	0	TGSHTM	Shutter speed data (MSB)	0	TG		0–7	INTEG1L	WIND1 Y integral data output LSB 8bit (Data format =BIN)	OPD
	1	TGSHTHL	Shutter speed mode 0:high 1:low	0	TG					
	2	TGSHTON	Shutter SW 0:OFF 1:ON	0	TG					
	3	(low)	"0" fixed	0	TG	—				
	4	TGNTPAL	TV mode for TG 0: NTSC 1:PAL	0	TG					
	5	TGCCD1	CCD mode for TG	1h	TG					
	6	TGCCD2	0h: 380H 1h:510H 2h: 720H 3h: 760H							
	7	(high)	"1" fixed	1	TG					
4	0–7	TGSHTL	Shutter speed data (LSB)	00h	TG	—	0–7	INTEG1M	WIND1 Y integral data output MSB 8bit (Data format =BIN)	OPD
5	0	HREF1HL	Polarity switch of HIST comp1	0	OPD	—	0–7	INTEG2L	WIND2 Y integral data output LSB 8bit (Data format =BIN)	OPD
	1	HREF2HL	Polarity switch of HIST comp2	0	OPD	—				
	2–7	dummy	0: REF <= YAE 1: REF >= YAE			—				
6	0–7	HREF1	Reference level setting for HIST comp1	00h	OPD	—	0–7	INTEG2M	WIND2 Y integral data output MSB 8bit (Data format =BIN)	OPD

#1: Initial setting value with Power-on

Category 5 : AE (AE control parameters / AE integral output]

	Serial Input						Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
7	0 1 2 3 4 5 6 7	HREF2	Reference level setting for HIST comp2	00h	OPD	——	0 1 2 3 4 5 6 7	INTG3L	WIND3 Y integaral data output LSB 8bit (Data format =BIN)	OPD
8	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTG3M	WIND3 Y integaral data output MSB 8bit (Data format =BIN)	OPD
9	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTG4L	WIND4 Y integaral data output LSB 8bit (Data format =BIN)	OPD
10	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTG4M	WIND4 Y integaral data output MSB 8bit (Data format =BIN)	OPD
11	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTGH1L	HIST1 Integral data output LSB 8bit (Data format =BIN)	OPD
12	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTGH1M	HIST1 Integral data output MSB 8bit (Data format =BIN)	OPD
13	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTGH2L	HIST2 Integral data output LSB 8bit (Data format =BIN)	OPD

#1: Initial setting value with Power-on

Serial Communication Data(11)

Category 5 : AE [AE control parameters / AE integral output]

	Serial Input						Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
14	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTGH2M	LSB HIST2 Integral data output MSB 8bit MSB (Data format =BIN)	OPD
15	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	HSTCNT1L	LSB HIST1 count data output LSB 8bit MSB (Data format =BIN)	OPD
16	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	HSTCNT1M	LSB HIST1 count data output MSB 8bit MSB (Data format =BIN)	OPD
17	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	HSTCNT2L	LSB HIST1 count data output LSB 8bit MSB (Data format =BIN)	OPD
18	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	HSTCNT2M	LSB HIST1 count data output MSB 8bit MSB (Data format =BIN)	OPD

#1: Initial setting value with Power-on

Category 6 : AWB [AWB control parameters / AWB integral output]

	Serial Input						Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0 1 2 3 4 5 6 7	CAT6	Category select code 06h : AWB				0 1 2 3 4 5 6 7	—	Unfixed data output	
1	0 1 2 3 4 5 6 7	WBR	WB-amp gain adjustment (RED channel)	3Ah	C	22h	0 1 2 3 4 5 6 7	AWBCNTL	WB integral counter data output LSB 8bit	OPD
2	0 1 2 3 4 5 6 7	WBG	WB-amp gain adjustment (GREEN channel)	26h	C	23h	0 1 2 3 4 5 6 7	AWBCNTM	WB integral counter data output MSB 8bit	OPD
3	0 1 2 3 4 5 6 7	WBB	WB-amp gain adjustment (BLUE channel)	48h	C	24h	0 1 2 3 4 5 6 7	INTGRL	WB integral data output (R-G Intg or R Intg) LSB 8bit	OPD
4	0 1 2 3 4 5 6 7	WBYREFH	Y threshord level setting for WB Intg. Top reference	D0h	OPD	D0h	0 1 2 3 4 5 6 7	INTGR	WB integral data output (R-G Intg or R Intg) 2nd 8bit	OPD
5	0 1 2 3 4 5 6 7	WBYREFL	Y threshord level setting for WB Intg. Bottom reference	04h	OPD	04h	0 1 2 3 4 5 6 7	INTGRM	WB integral data output (R-G Intg or R Intg) MSB 8bit	OPD
6	0 1 2 3 4 5 6 7	dummy					0 1 2 3 4 5 6 7	INTGGL	WB integral data output (G Intg) LSB 8bit	OPD

#1: Initial setting value with Power-on

Category 6 : AWB [AWB control parameters / AWB integral output]

Serial Input							Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
7	0-7	dummy					0-7	INTGG	WB integral data output (G intg) 2nd 8bit	OPD
8	0-7	dummy					0-7	INTGGM	WB integral data output (G intg) MSB 8bit	OPD
9	0-7	dummy					0-7	INTGBL	WB integral data output (B-G intg or B intg) LSB 8bit	OPD
10	0-7	dummy					0-7	INTGB	WB integral data output (B-G intg or B intg) 2nd 8bit	OPD
11	0-7	dummy					0-7	INTGBM	WB integral data output (B-G intg or B intg) MSB 8bit	OPD

#1: Initial setting value with Power-on

Category 7 : FIXOPD [Initially fixed parameters for OPD]

Byte	bit	Name	Description	#1	Block	Address
0	0 to 7	CAT7	Category select code 07h : OPDFIX			
1	0	AWBWSEL	AWB detect window selection 0: all wind 1: without wind0	0	OPD	25h
	1	AWBGAM	AWB detect signal selection 0: before γ 1: after γ	0	C	
	2	AWBBFSEL	AWB detect signal sel. 0: before WBamp 1: after WBamp	0	OPD	
	3	AWBDPSEL	AWB integral mode selection 0: R-G/B-G intg 1: RGB intg	0	OPD	
	4	AEMAXMIN	AE peak / bottom output sel. 0: HIST2 out 1: pe/bo out	0	OPD	
	5 to 7	dummy				
2	0 to 7	CNTOFST	Horizontal count start offset of AE / AWB detect window (COUNTER OFFSET) <CNTOFST> X 4MCK 360H 510H 720H 760H NT 1Ch 15h 1Ch 1Bh PAL 1Fh 18h 1Eh 1Dh	15h	OPD	26h
3	0 to 7	CNTWID	Horizontal unit width data of AE / AWB detect window (COUNTER WIDTH) <CNTWID> X 4MCK 360H 510H 720H 760H NT 0Bh 08h 08h 0Ch PAL 0Bh 09h 08h 0Ch	08h	OPD	27h
4	0 to 3	W4STAH	Horizontal start data of WIND4 (WIND4 START H) <W4STAH> X 4MCK	5h	OPD	28h
	4 to 7	W4WIDH	Horizontal width data of WIND4 (WIND4 WIDTH H) <W4WIDH> X 4MCK	5h	OPD	
5	0 to 3	W4STAV	Vertical start data of WIND4 (WIND4 START V) <W4STAV> X 4MCK	4h	OPD	29h
	4 to 7	W4WIDV	Vertical width data of WIND4 (WIND4 WIDTH V) <W4WIDV> X 4MCK	7h	OPD	

#1: Initial setting value with Power-on

Category 8 : MCRCON [Micro-controller parameters]

Serial Input						
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT8	LSB Category select code 08h : MCRCON MSB			
1	0	AWBCO	LSB AWB co.process mode selection 000:copro non act 001:AWB monitor 010:AWB average 011:adjust out MSB	0	MCR	
	1					
	2					
	3	MCRAWB	Micro-controller AWB on/off	0	MCR	
	4	AECO	LSB AE co.process mode selection 000:copro non act 001:AE monitor 010:AE average 011: — MSB	0	MCR	
	5					
	6					
	7	MCRAE	Micro-controller AE 0:on 1:off	0	MCR	
2	0	MCREXT	0: Micro-controller 1: External micom (Micro-controller OFF)	0	MCR	
	1	MCRSPRS	Micro-controller FIELD control switch 0:ON 1:OFF	0	MCR	
	2	MCRSG	Micro-controller SG control switch 0:ON 1:OFF	0	MCR	
	3	MCRDIP	Micro-controller DIP switch scan 0:ON 1:OFF	0	MCR	
	4	MCRCLP	Micro-controller CLAMP control switch 0:ON 1:OFF	0	MCR	
	5	(low)	Micro-controller GAMMA-ON/OFF control switch 0:ON 1:OFF	0	MCR	
	6	MCRGAM		0	MCR	
	7	dummy				
3	0	ENTPAL	TV system mode 0: NTSC 1: PAL (MCRDIP=1)	0	MCR	
	1	ECCD1	LSB CCD mode 0h: 360H 1h: 510H (MCRDIP=1)	1	MCR	
	2	ECCD2	MSB 2h: 720H 3h: 760H			
	3	INTLL	Line lock switch 0:OFF 1:ON (MCRDIP=1)	1	MCR	
	4	(low)	"0" fixed	0		
	5			0		
	6	GAMMA	Gamma switch 0:ON 1:OFF (MCRGAM=0)and(MCRDIP=1)	0	MCR	
	7	AEME	AE mode 0: auto 1: manual (MCRDIP=1)	0	MCR	
4	0	FLON	Flickerless mode switch 0:OFF 1:ON (MCRDIP=1)	0	MCR	
	1	BLCOF	Back light compensation switch 0:ON 1:OFF (MCRDIP=1)	0	MCR	
	2	MIRIS	IRIS mode selection 0: E-IRIS 1: Mecha-IRIS (MCRDIP=1)	0	MCR	
	3	AEREF	AE convergence level sel. 0:preset 1:eeprom (MCRDIP=1)	0	MCR	
	4	AGCMAX	AGC max gain sel. 0:low(eeprom) 1:high(eeprom) (MCRDIP=1)	0	MCR	
	5	AWB1	AWB mode 0: auto 1: manual (MCRDIP=1)	0	MCR	
	6	AWB2	AWB mode (MCRDIP=1)	0	MCR	
	7	AWB3	AWB mode (MCRDIP=1)	0	MCR	
5	0	E2WR	EEPROM WRITE 1byte 0:OFF 1:WRITE	0	SCS	
	1	E2WEN	EEPROM WRITE enable 0:OFF 1:SEND	0	SCS	
	2	dummy				
	3	E2RSW	EEPROM READ mode hold switch 0: OFF 1: mode hold	0	SCS	
	4	E2RAL1	EEPROM READ - 1 0:OFF 1:READ	0	SCS	
	5	E2RAL2	EEPROM READ - 2 0:OFF 1:READ	0	SCS	
	6	E2RAL3	EEPROM READ - 3 0:OFF 1:READ	0	SCS	
	7	E2RAL4	EEPROM READ - 4 0:OFF 1:READ	0	SCS	
6	0	E2CODE	LSB EEPROM read/write code MSB	00h	EEP ROM	
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 8 : MCRCON [Micro-controller parameters]

Serial Input						
Byte	bit	Name	Description	#1	Block	Address
7	0 1 2 3 4 5 6 7	E2ADRS	EEPROM address	00h	EEP ROM	
8	0 1 2 3 4 5 6 7	E2DATA	EEPROM data	00h	EEP ROM	
9	0 1 2 3 4 5 6 7	SPCODE	Micro-controller (AE/AWB) custom code (SPECIFIC CODE)	00h	MCR	
10	0 1 2 3 4 5 6 7	SPCDAT	Micro-controller(AE/AWB) custom data (SPECIFIC DATA)	00h	MCR	
11	0 1 2 3 4 5 6 7	EAGC	External AGC control data	00h	MCR	
12	0 1 2 3 4 5 6 7	dummy				
13	0 1 2 3 4 5 6 7	dummy				

#1: Initial setting value with Power-on

Category 9 : SG (SG parameters)

Serial Input							Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0–7	CAT9	Category select code 09h : SG				0–7	—	Unfixed data output	
1	0	SGMODE	SG mode 0h:INT 1h:LL 2h:VSL 3h:VBSLHP 4h:VBSLHR 5h:VHHR 7:AUTO	0h	SG	2Ah	0–7	SGSTAT	SG status output 0h:INT 1h:LL 2h:VSL 3h:VBSLHP 4h:VBSLHR 5h:VHHR 6h:SG135 7h:AUTO	SG
	1	dummy								
	2	(low)	"0" fixed							
	3	(low)	"0" fixed	0						
	4	PALSEQ	PAL field sequence on	0	SG					
2	0–7	SFTHL	In case of H-PLL : H-Phase adjustment In case of H-RESET : Counter load value setting LSB 8bit	00h	SG	2Bh	0–7	—	Unfixed data output	
3	0–7	SFTVL	In case of V-PLL : V-Phase adjustment In case of V-RESET : Counter load value setting LSB 8bit	03h	SG	2Ch	0–7	—	Unfixed data output	
4	0–1	SFTHM	SFTH MSB 2bit	0h	SG	2Dh	0–7	—	Unfixed data output	
	2–3	SFTVM	SFTV MSB 2bit	0h	SG					
	4–7	dummy								
5	0–2	SFTSFC	Shifter setting for FSC 0deg(0h)~315deg(7h)	0h	SG	2Eh	0–7	—	Unfixed data output	
	3	FSCPCMP	FSC phase comp switch		SG					
	4–5	FSCPSEL	Phase selection for FSC output	0 0h	SG					
	6	SCMPPIN	SCOMP pin selection		SG					
	7	INVPCMP	P-comp input change (rel/vari)	0	SG					

#1: Initial setting value with Power-on

Serial Communication Data(18)

Category 10 : EXTCON [External control parameters / Sampling data output]

Serial Input							Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0 1 2 3 4 5 6 7	CAT10	LSB Category select code 0Ah : EXTCON MSB				0 1 2 3 4 5 6 7	—	Unfixed data output	
1	0 1 2 3 4 5 6 7	(low)	"0" fixed	00h			0 1 2 3 4 5 6 7	AJSTY	LSB Sampling data output for Y signal adjustment MSB (Data format = BIN)	Y
2	0 1 2 3 4 5 6	ADJSTH	LSB Horizontal phase adjustment for camera adjust pulse MSB	00h	SG		0 1 2 3 4 5 6 7	AJSTRY	LSB Sampling data output for R-Y signal adjustment MSB (Data format = BIN)	C
	7	ADJSTVL	Vertical phase adj.(LSB)	0	SG					
3	0 1	ADJSTVM	Vertical phase adjustment for camera adjust (MSB)	0h	SG		0 1 2 3 4 5 6 7	AJSTBY	LSB Sampling data output for B-Y signal adjustment MSB (Data format = BIN)	C
	2	DISPMIX	Wind display 0:OFF 1:ON	0	Y					
	3	OPDADJ	OPD adjust mode switch	0	OPD					
	4 5 6 7	OPDDISP	OPD window display selection	0h	OPD					
4	0	PGON	Test pattern signal on / off	0	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	
	1	PGMIXAL	TP display on full picture	0	SG					
	2	PGLIDSEL	Signal phase sel. in line	0	SG					
	3	PGBIDSEL	Chroma ID phase sel.	0	SG					
	4	PGCOLSEL	Color bar / raster output sel.	0	SG					
	5 6 7	PGCOL	LSB Color selection MSB	0h	SG					
5	0	PGHV	TP H / V switch	0	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	
	1	PGRSTR	Raster setting	0	SG					
	2 3	PGPTSL	TP pattern selection	0	SG					
	4	PGSIDSEL	TP by Serial data indicate	0	SG					
	5	PGSIDAL	TP by serial data on full pict.	0	SG					
	6 7	PGGAIN	TP signal level selection MIN(0h)~MAX(3h)	0	SG					
6	0 1 2 3 4 5 6 7	PGDCRS2	LSB Serial data for test pattern MSB (Data format = BIN)	00h	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	

#1: Initial setting value with Power-on

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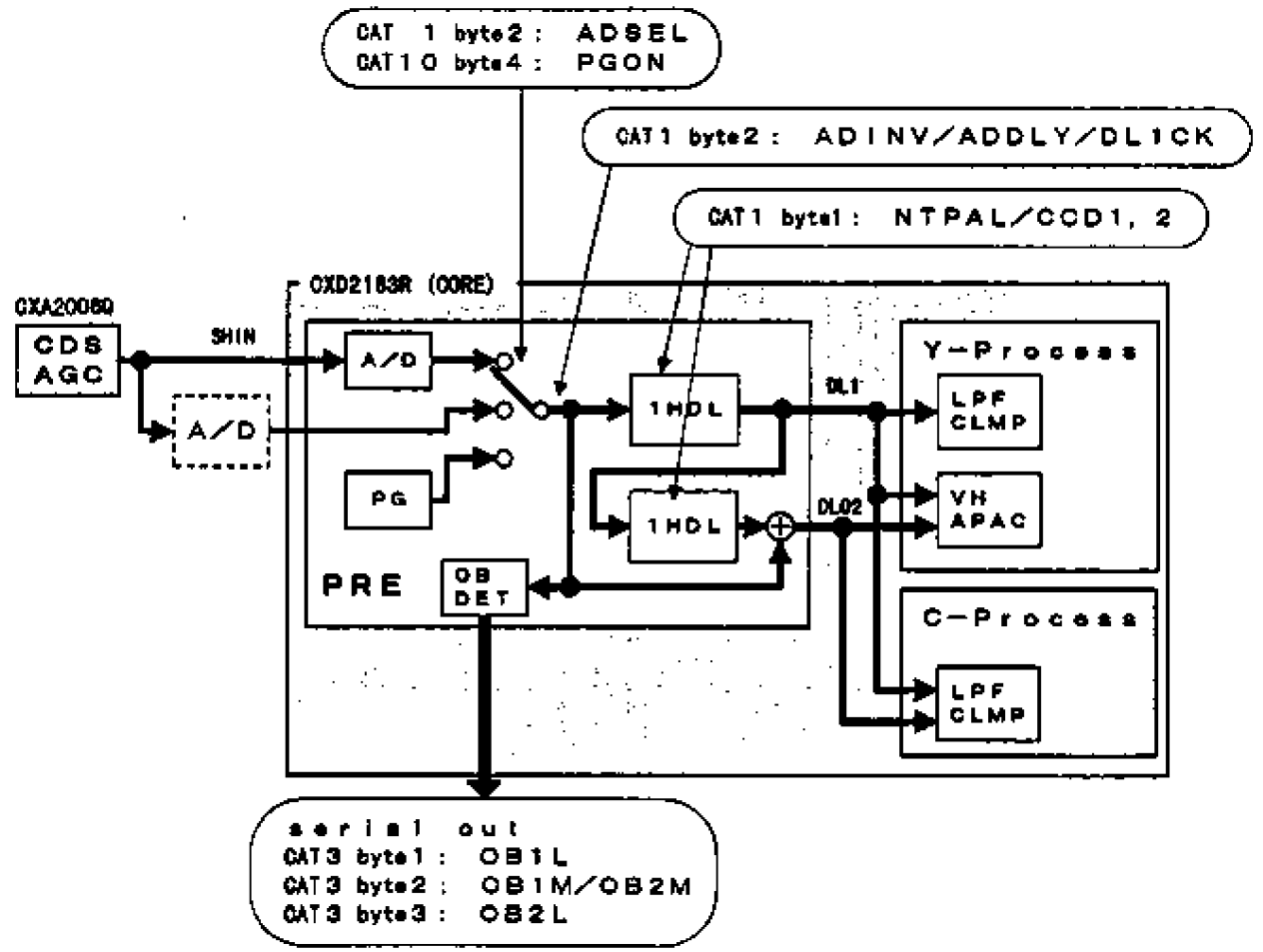
Category 10 : EXTCON [External control parameters / Sampling data output]

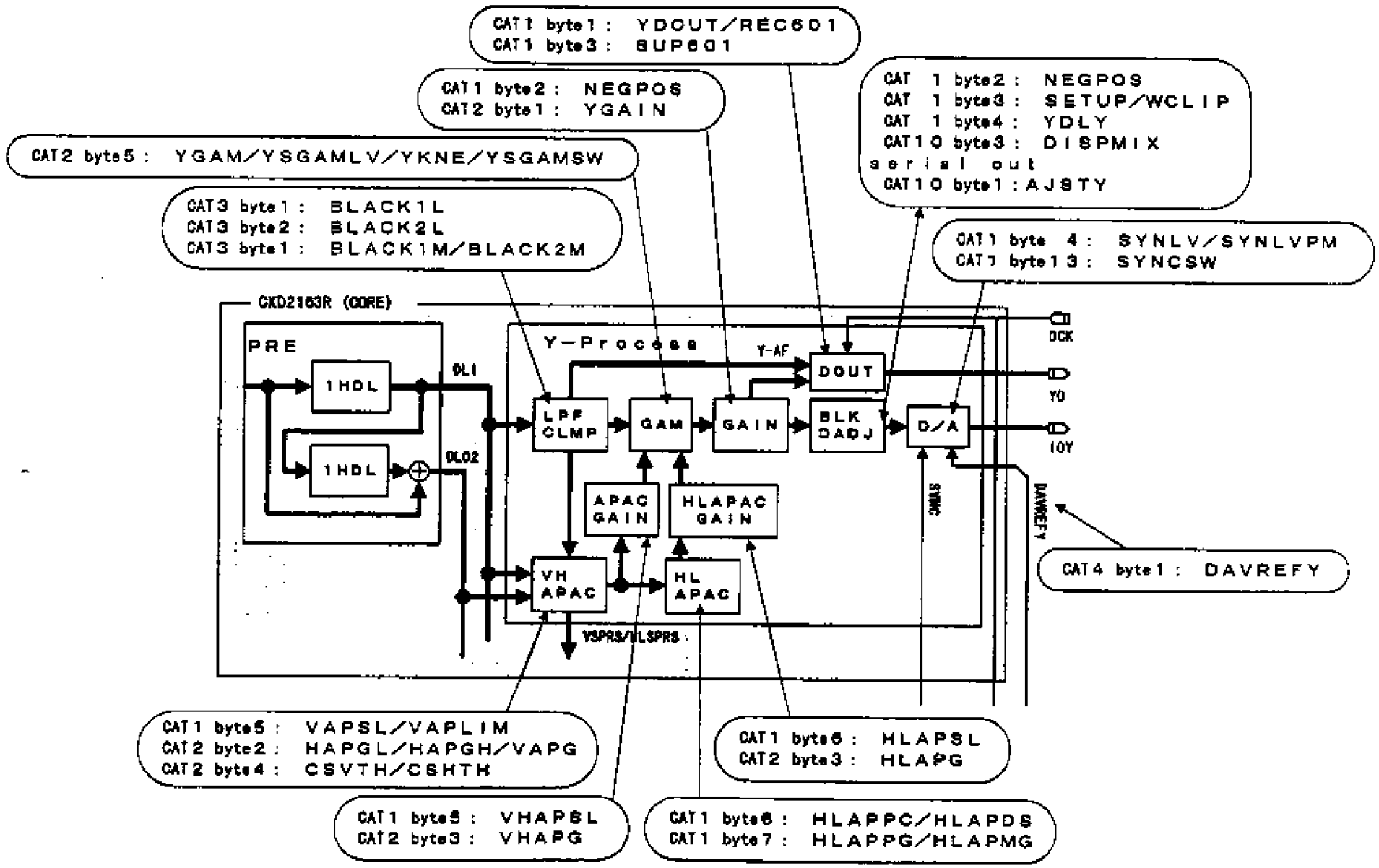
	Serial Input						Serial Output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
7	0 1 2 3 4 5 6 7	PGDCRS1	LSB Serial data for test pattern MSB	00h	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	
8	0 1 2 3 4 5 6 7	PGDCBS2	LSB Serial data for test pattern MSB	00h	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	
9	0 1 2 3 4 5 6 7	PGDCBS1	LSB Serial data for test pattern MSB	00h	SG		0 1 2 3 4 5 6 7	—	Unfixed data output	

#1: Initial setting value with Power-on

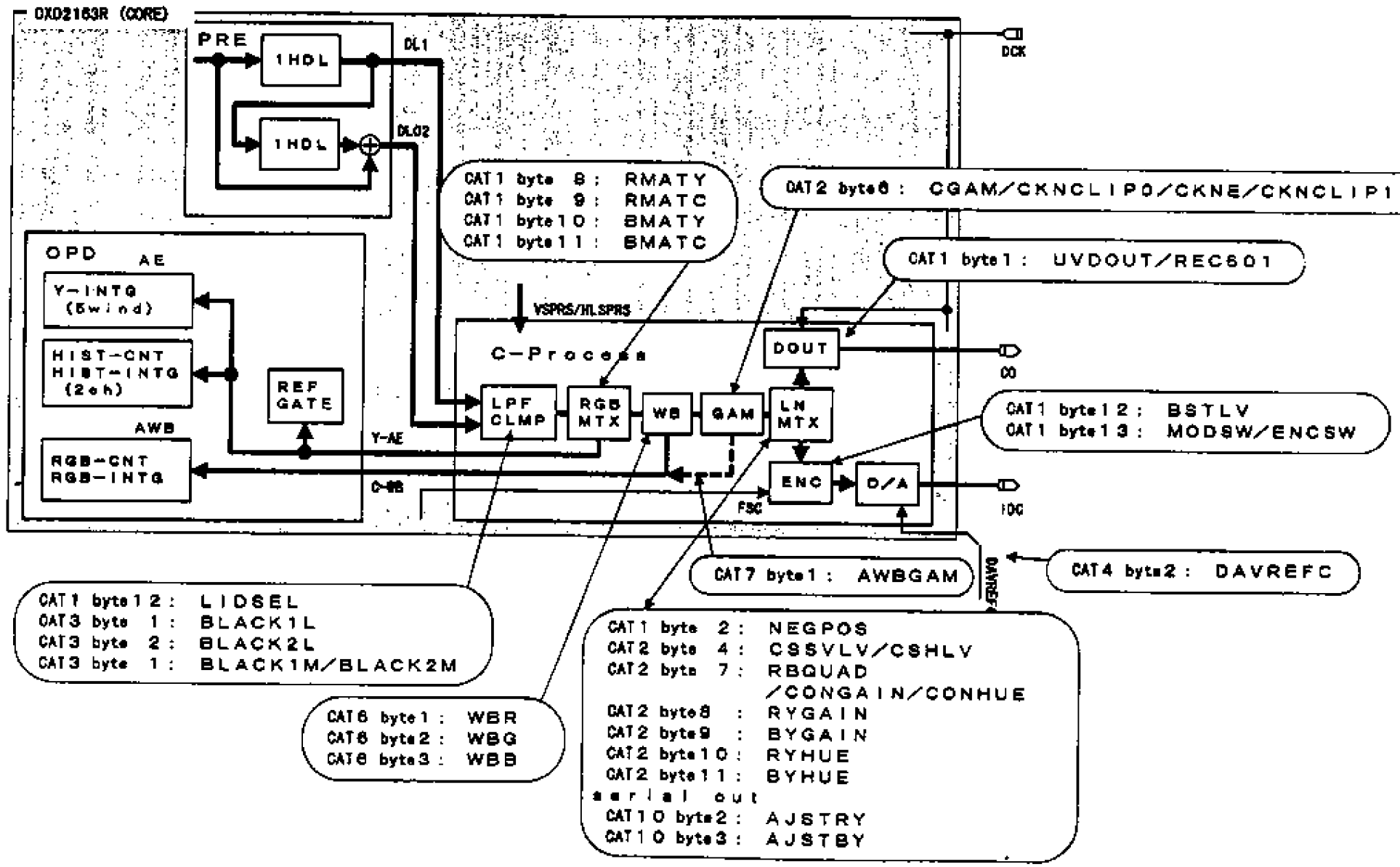
[Serial parameter position (PRE block)]



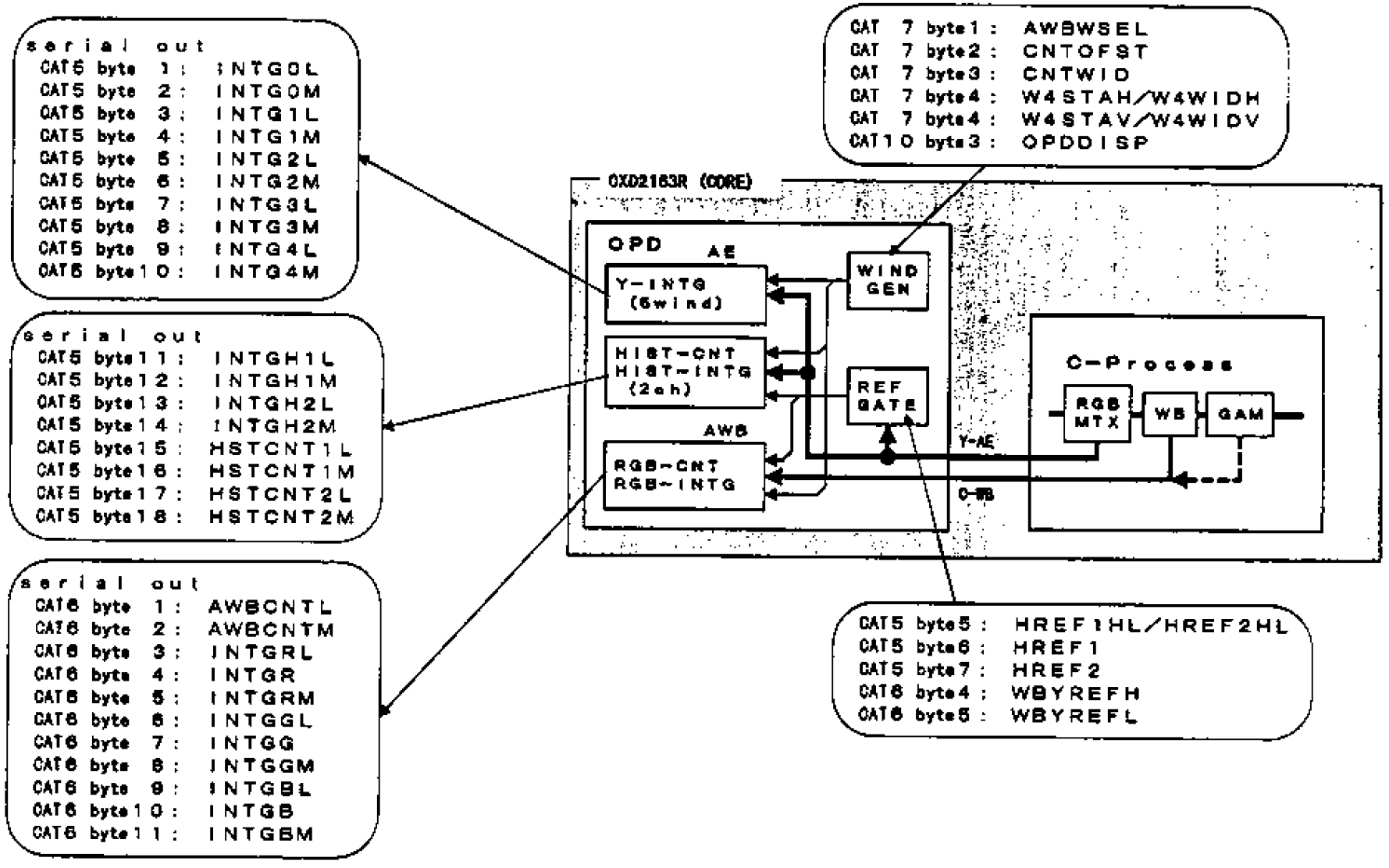
[Serial parameter position (Y－Process block)]



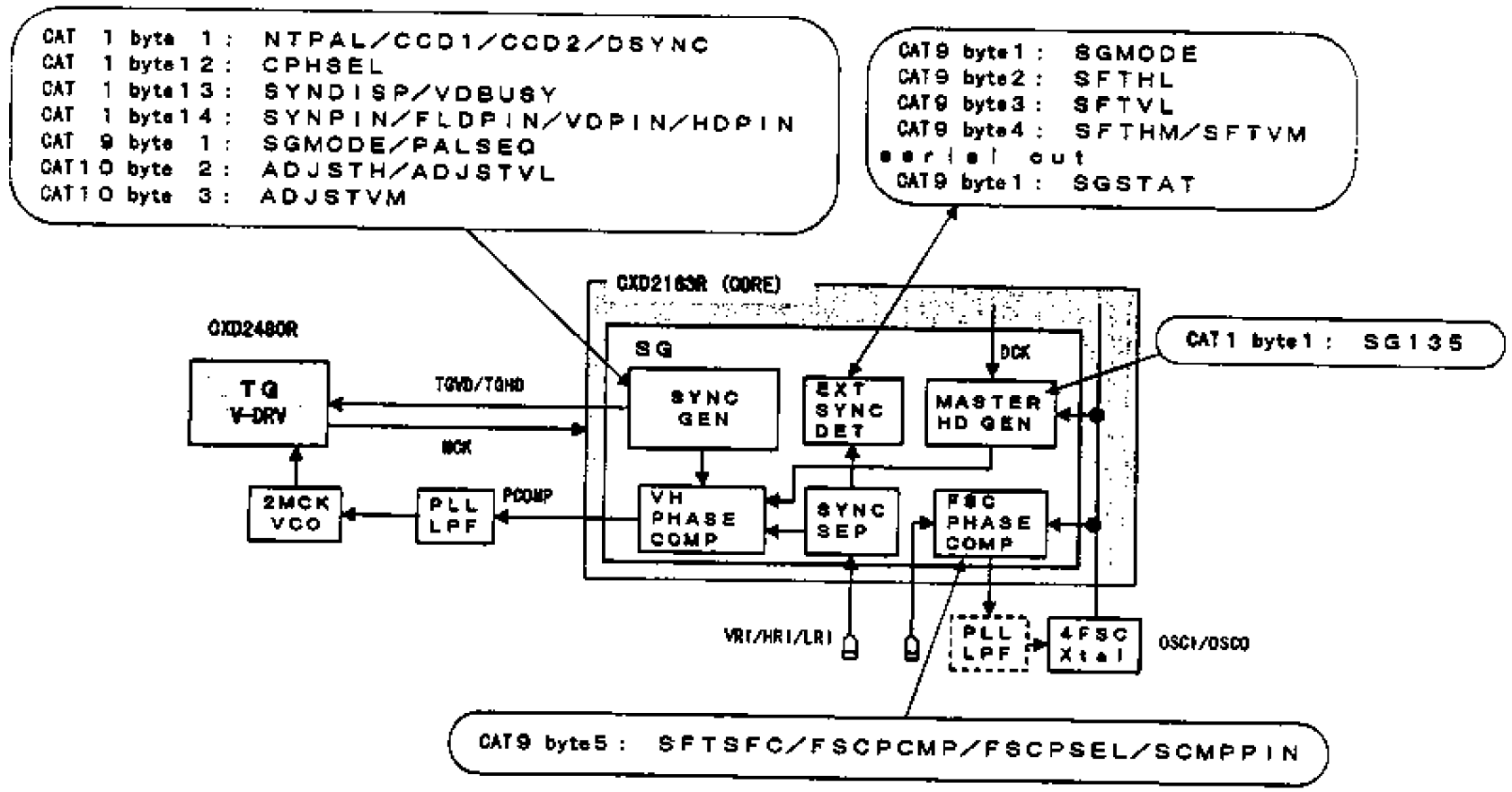
[Serial parameter position (C－Ｐｒｏｃｅｓｓ block)]



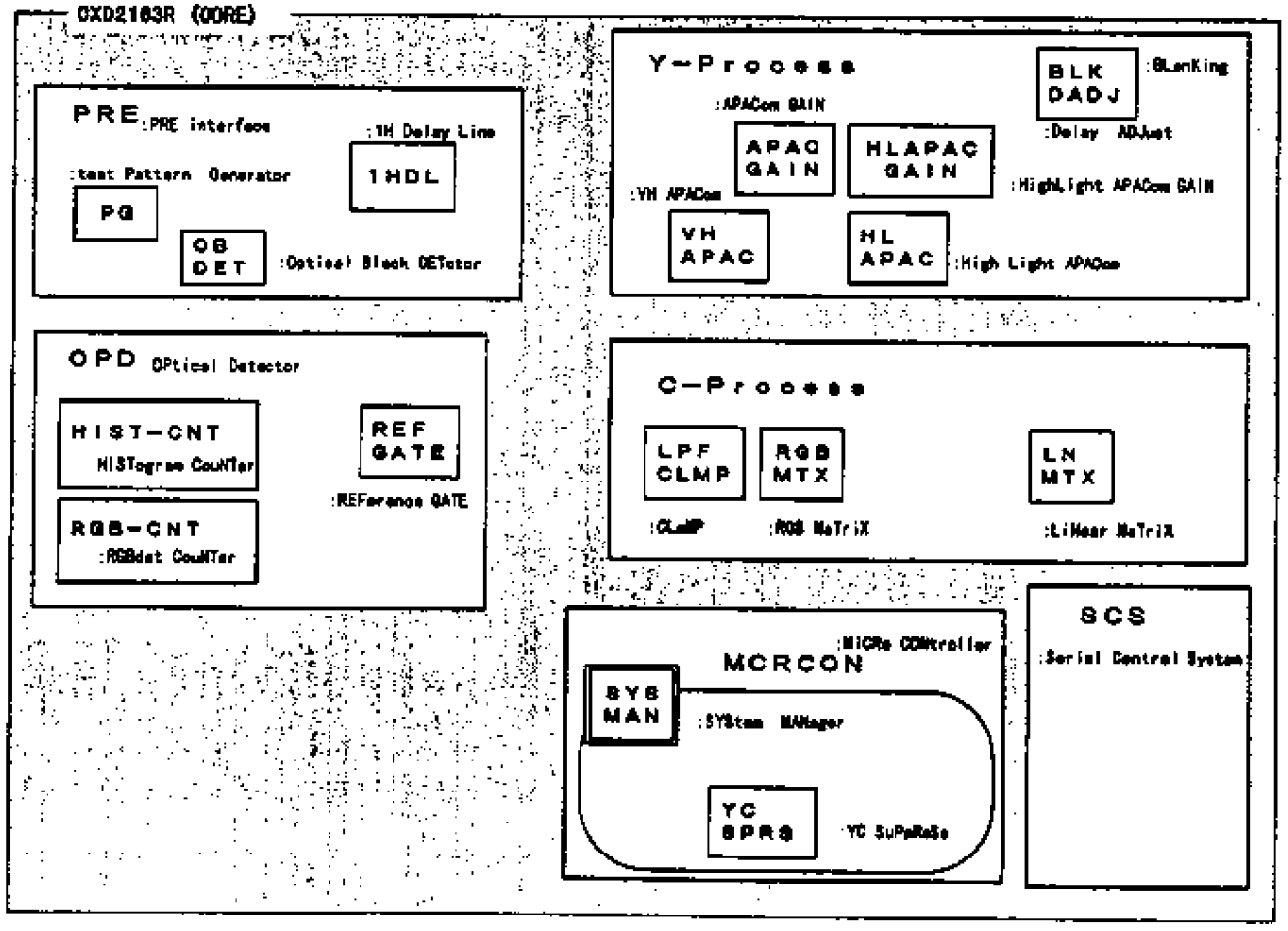
[Serial parameter position (OPD block)]



[Serial parameter position (SG block)]



[Abbreviation of CXD2163 block name]



Spec code: AE (CAT8 byte9 code= 0Xhex)

Code	bit	Name	Description	#1	Block	Address
01	0 1 2 3 4 5 6 7	AESPED	LSB AE Feedback speed MSB	08h		2fh
02	0 1 2 3 4 5 6 7	AEUSR	LSB AE USR define typical video level MSB	04h		30h
03	0 1 2 3 4 5 6 7	AGCMAXL	LSB AE AGC-amp max gain at low-mode DIP switch MSB	88h		31h
04	0 1 2 3 4 5 6 7	AGCMIN	LSB AE AGC-amp min gain MSB	11h		32h
05	0 1 2 3 4 5 6 7	SHTLIM	LSB AE shutter limmit MSB	07h		33h
06	0 1 2 3 4 5 6 7	AGCMAXH	LSB AE AGC-amp max gain at high-mode DIP switch MSB	EEh		34h

#1: Initial setting value with Power-on

Spec code: AE (CAT8 byte9 code= 0Xhex)

Code	bit	Name	Description	#1	Block	Address
07	0 1 2 3 4 5 6 7	AEBLLV	LSB AE Back Light Level MSB	10h		35h
08	0 1 2 3 4 5 6 7	HISTOFF	LSB AE HISTOGRAM function switch 0: on 1: off MSB	0h		36h
09	0 1 2 3 4 5 6 7	W0WEIT	LSB AE Wind0 weight MSB	1h		37h
0A	0 1 2 3 4 5 6 7	W1WEIT	LSB AE Wind1 weight MSB	5h		38h
0B	0 1 2 3 4 5 6 7	W2WEIT	LSB AE Wind2 weight MSB	Ah		39h
0C	0 1 2 3 4 5 6 7	W3WEIT	LSB AE Wind3 weight MSB	Ah		3Ah

#1: Initial setting value with Power-on

Spec code: AWB (CAT8 byte9 code= 1Xhex)

Code	bit	Name	Description	#1	Block	Address
11	0 1 2 3 4 5 6 7	AWBSPED	AWB Feedback speed	05h		35h
12	0 1 2 3 4 5 6 7	AWBFRAM	AWB Convergence area (Chroma vector FRAME)	00h		36h
13	0 1 2 3 4 5 6 7	WBRSFT	WB Convergence point shift (Red) at FL mode	08h		37h
14	0 1 2 3 4 5 6 7	WBBSFT	WB Convergence point shift (Blue) at FL mode	0Ch		38h
15	0 1 2 3 4 5 6 7	WBUSRR	WB Convergence point (Red) at USR define mode	4Fh		39h
16	0 1 2 3 4 5 6 7	WBUSRB	WB Convergence point (Blue) at USR define mode	8Ch		3Ah

#1: Initial setting value with Power-on

Spec code: AWB (CAT8 byte9 code= 1Xhex)

Code	bit	Name	Description	#1	Block	Address
17	0 1 2 3 4 5 6 7	AWBPRER	LSB AWB WB-amp gain (Red) at PRE white balance mode MSB	3Ah		41h
18	0 1 2 3 4 5 6 7	AWBPREB	LSB AWB WB-amp gain (Blue) at PRE white balance mode MSB	90h		42h

#1: Initial setting value with Power-on

Spec code: FIXOPD (CAT8 byte9 code= 2Xhex)

Code	bit	Name	Description	#1	Block	Address
21	0 1 2 3 4 5 6 7	SPCNTWID	H COUNTER width	06h		43h
22	0 1 2 3 4 5 6 7	SPW4STAH	Wind4 H START	05h		44h
23	0 1 2 3 4 5 6 7	SPW4WIDH	Wind4 H WIDTH	05h		45h
24	0 1 2 3 4 5 6 7	SPW4STAV	Wind4 V START	07h		46h
25	0 1 2 3 4 5 6 7	SPW4WIDV	Wind4 V WIDTH	4h		47h

#1: Initial setting value with Power-on

Spec code: Suppress (CAT8 byte9 code= 3Xhex)

Code	bit	Name	Description	#1	Block	Address
31	0 1 2 3 4 5 6 7	CSPRSSTA	Chroma suppress start point (AGC gain)	52h		48h
32	0 1 2 3 4 5 6 7	CSPRSEND	Chroma suppress end point (AGC gain)	80h		49h
33	0 1 2 3 4 5 6 7	CSPRSLV	Chroma suppress suppress level at end point	8Ah		4Ah
34	0 1 2 3 4 5 6 7	ASPRSSTA	Apacom suppress start point (AGC gain)	3Dh		4Bh
35	0 1 2 3 4 5 6 7	ASPRSEND	Apacom suppress end point (AGC gain)	80h		4Ch
36	0 1 2 3 4 5 6 7	ASPRSLV	Apacom suppress suppress level at end point	00h		4Dh

#1: Initial setting value with Power-on

Quadrant parameter of linear matrix (CAT2 byte7 ~11)

Code	bit	Name	Description	#1	Block	Address
	0		LSB	19h		4Fh
	1					
	2					
	3	RYGAIN1	R-Y Gain 1st quad			
	4					
	5					
	6					
	7		MSB			
	0		LSB	0Dh		50h
	1					
	2					
	3	BYGAIN1	B-Y Gain 1st quad			
	4					
	5					
	6					
	7		MSB			
	0		LSB	19h		51h
	1					
	2					
	3	RYGAIN2	R-Y Gain 2nd quad			
	4					
	5					
	6					
	7		MSB			
	0		LSB	0Dh		52h
	1					
	2					
	3	BYGAIN2	B-Y Gain 2nd quad			
	4					
	5					
	6					
	7		MSB			
	0		LSB	19h		53h
	1					
	2					
	3	RYGAIN3	R-Y Gain 3rd quad			
	4					
	5					
	6					
	7		MSB			
	0		LSB	0Dh		54h
	1					
	2					
	3	BYGAIN3	B-Y Gain 3rd quad			
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Quadrant parameter of linear matrix (CAT2 byte7 ~11)

Code	bit	Name	Description	#1	Block	Address
	0		LSB	19h		55h
	1					
	2					
	3					
	4	RYGAIN4	R-Y Gain 4th quad			
	5					
	6					
	7		MSB			
	0		LSB	0Dh		56h
	1					
	2					
	3					
	4	BYGAIN4	B-Y Gain 4th quad			
	5					
	6					
	7		MSB			
	0		LSB	D0h		57h
	1					
	2					
	3					
	4	RYHUE1	R-Y Hue 1st quad			
	5					
	6					
	7		MSB			
	0		LSB	F8h		58h
	1					
	2					
	3					
	4	BYHUE1	B-Y Hue 1st quad			
	5					
	6					
	7		MSB			
	0		LSB	D0h		59h
	1					
	2					
	3					
	4	RYHUE2	R-Y Hue 2nd quad			
	5					
	6					
	7		MSB			
	0		LSB	F8h		5Ah
	1					
	2					
	3					
	4	BYHUE2	B-Y Hue 2nd quad			
	5					
	6					
	7		MSB			

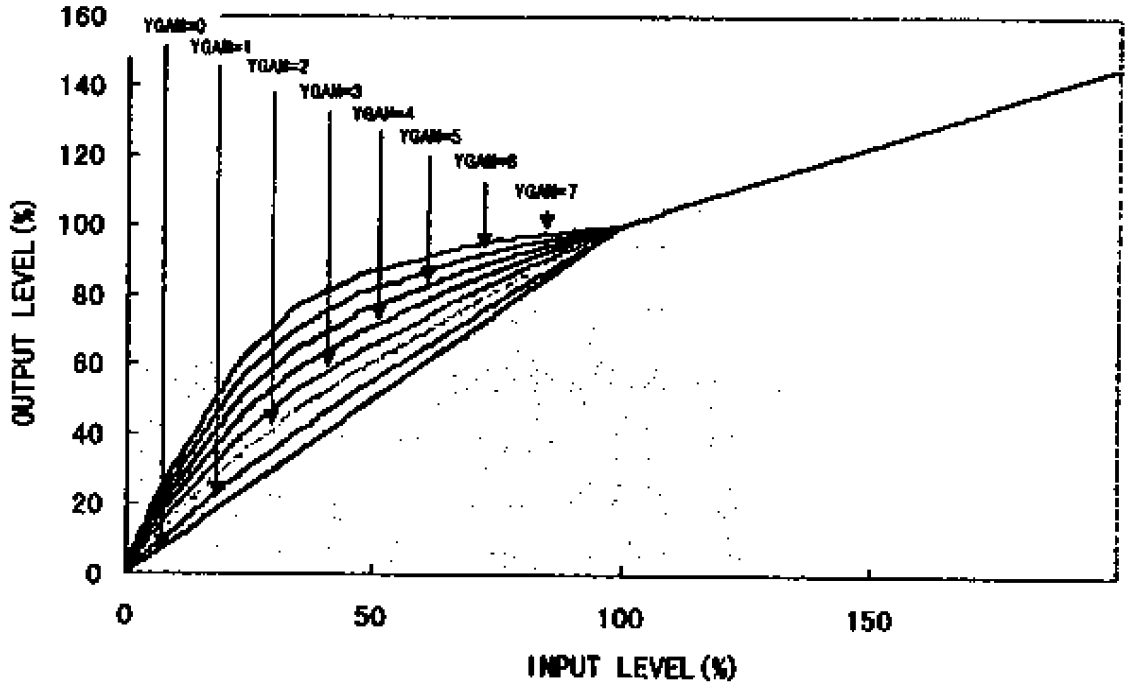
#1: Initial setting value with Power-on

Quadrant parameter of linear matrix (CAT2 byte7 ~11)

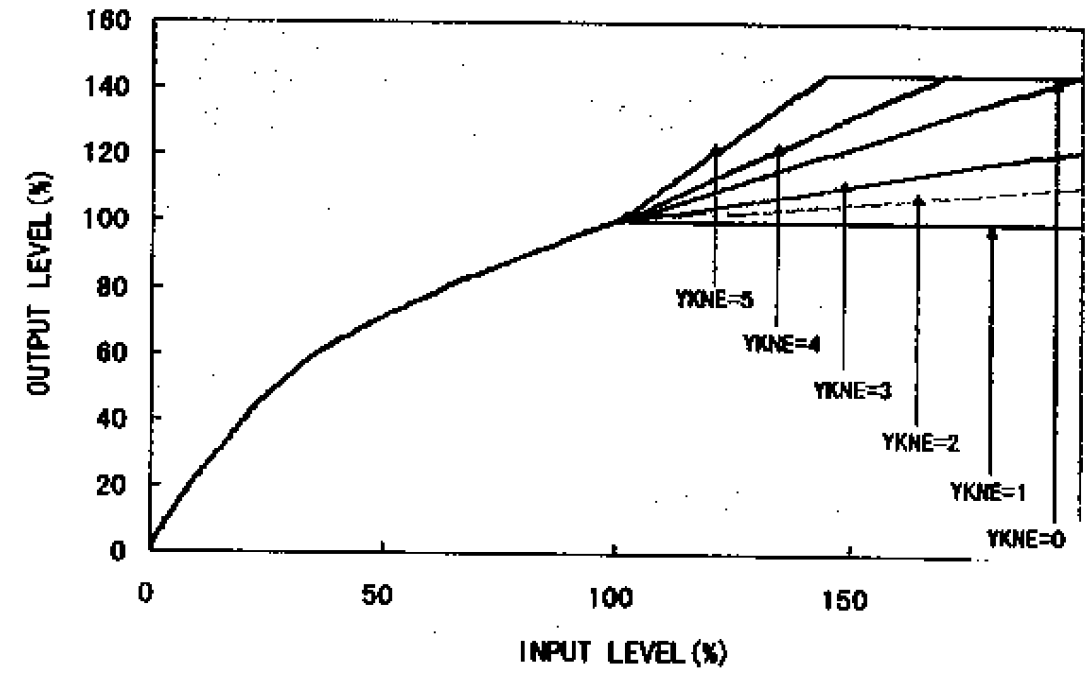
Code	bit	Name	Description	#1	Block	Address
	0	RYHUE3	R-Y Hue 3rd quad	D0h		6Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	BYHUE3	B-Y Hue 3rd quad	F8h		5Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	RYHUE4	R-Y Hue 4th quad	D0h		5Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	BYHUE4	B-Y Hue 4th quad	F8h		5Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Y-GAMMA (YKNE=0)



Y-KNEE (YGAM=4)



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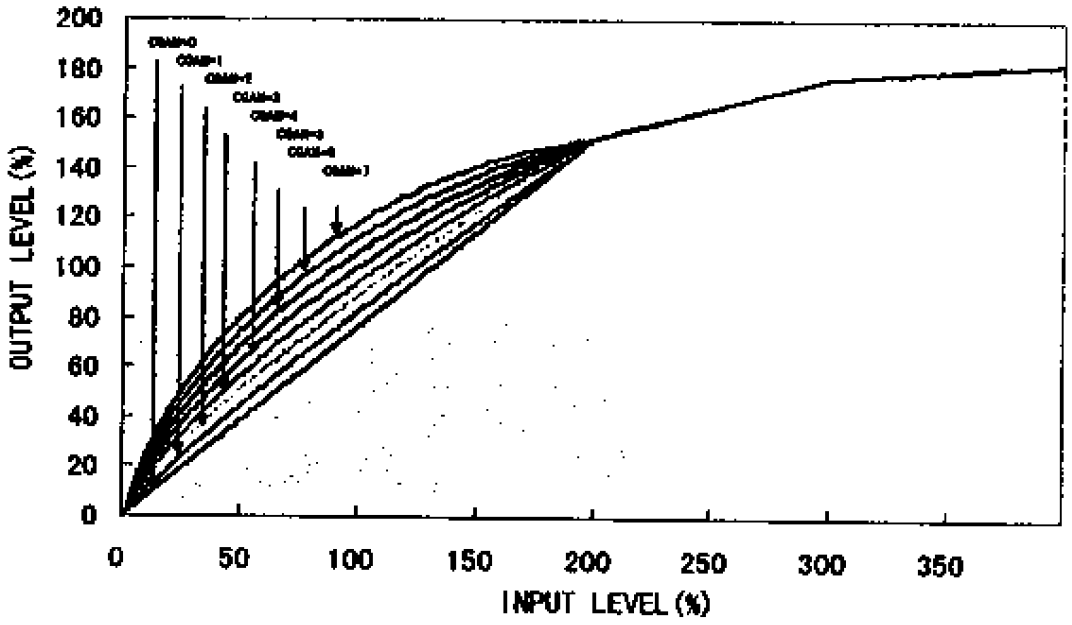
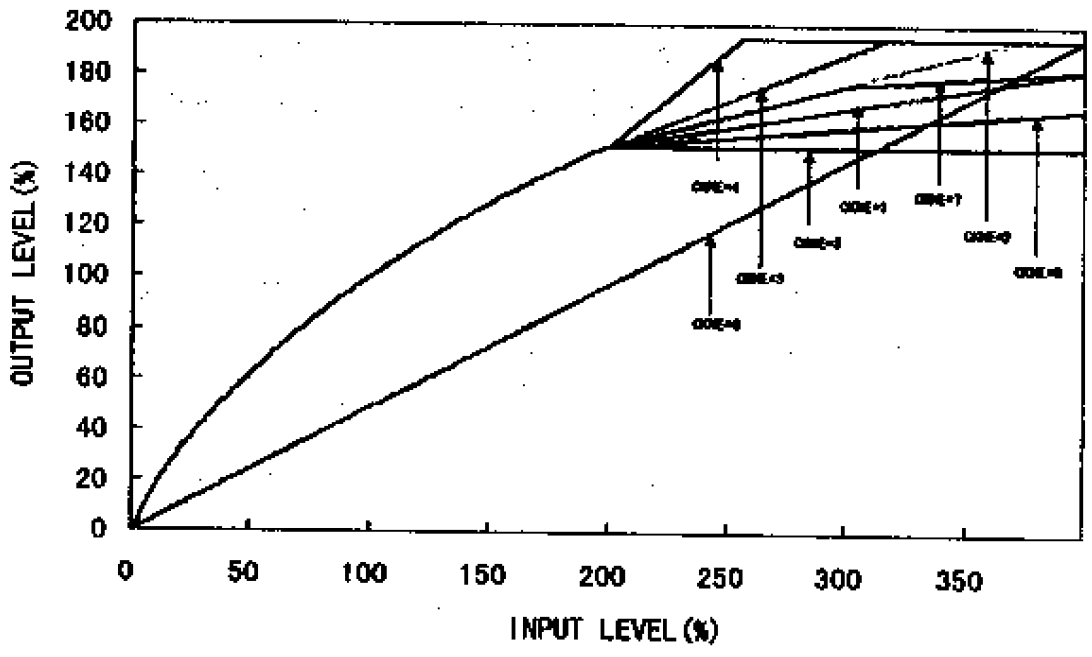
C-GAMMA (CKNE=7)

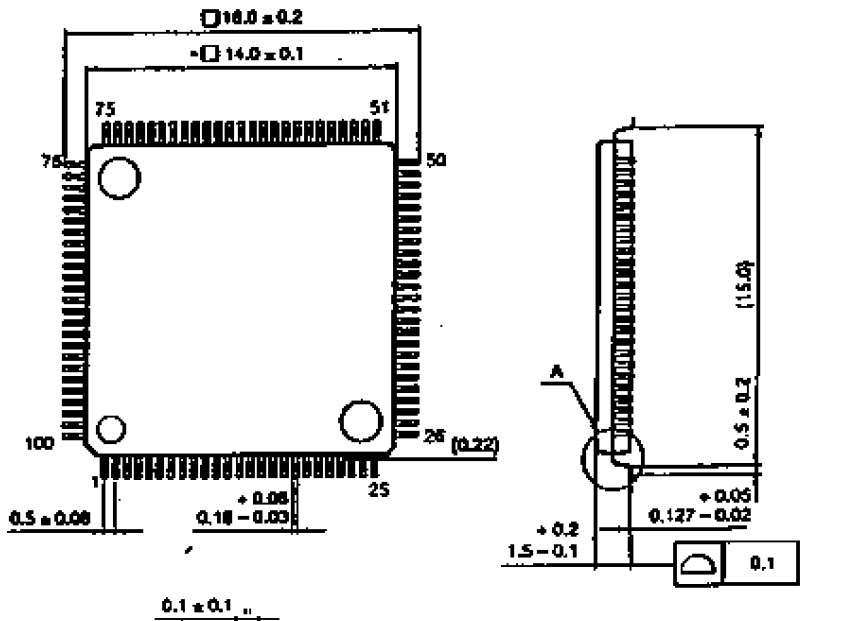


C-KNEE (CGAM=4)



Package Outline Unit: mm

100PIN LQFP (PLASTIC)



DETAIL A

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————