SONY

CXD2306Q

10-bit 80MSPS 1ch D/A Converter

Description

The CXD2306Q is a 1-ch 10-bit 80MSPS D/A converter for fine monitor and video, and is ideal for high definition TVs and high resolution displays.

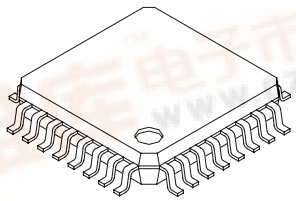
Features

- 10-bit resolution
- Maximum conversion rate 80MSPS
- Differential linearity error ±0.5 LSB
- Low power consumption 150 mW(max.)
  (When 80MSPS 200 Ω load, 2 Vp-p is output)
- Single 5 V power supply
- Built-in independent constant-voltage source
- Stand-by function

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



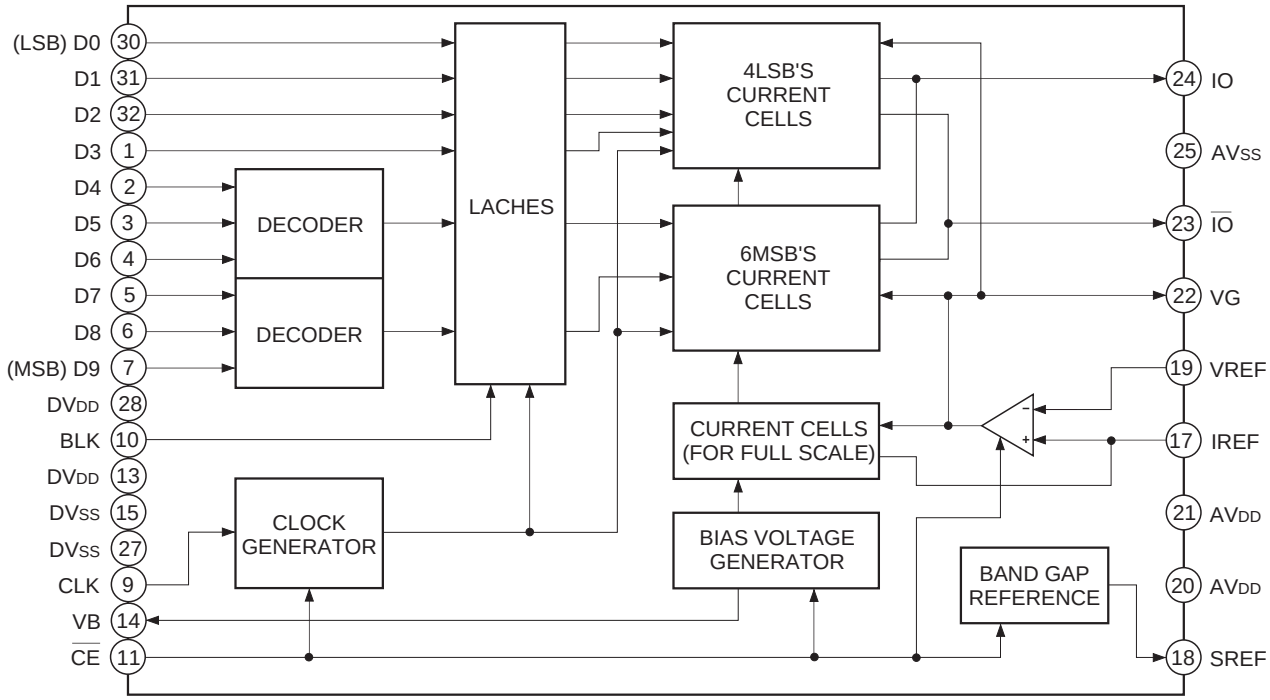
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Output voltage	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

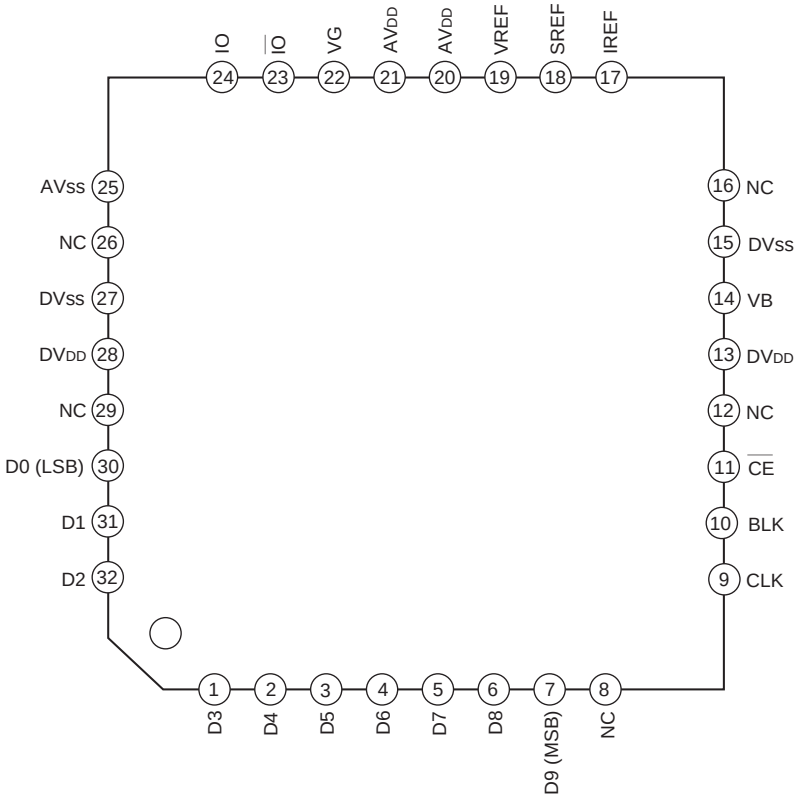
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	5.0 ± 0.25	V
	DV_{DD}, DV_{SS}	5.0 ± 0.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	t_{PW1}, t_{PW0}	5.6 (min.)	ns
• Operating temperature	topr	–20 to +85	°C

Block Diagram and Pin Configuration



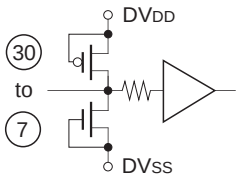
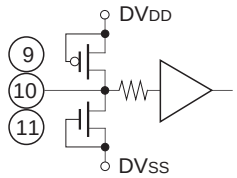
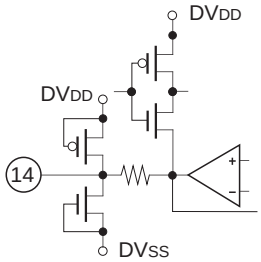
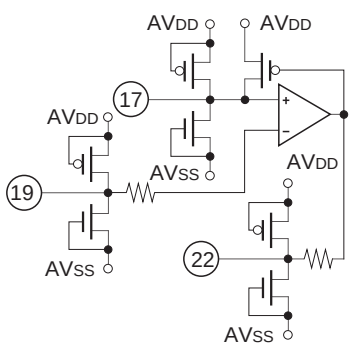
Pin Configuration

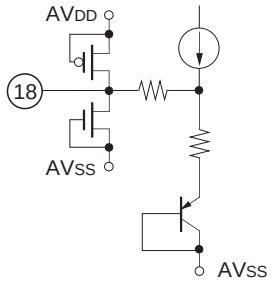
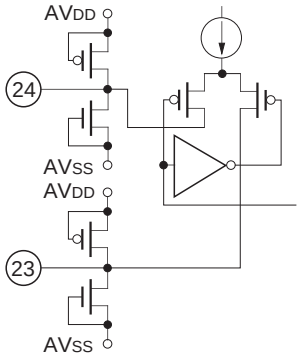


27 to 15 Digital section

17 to 25 Analog section

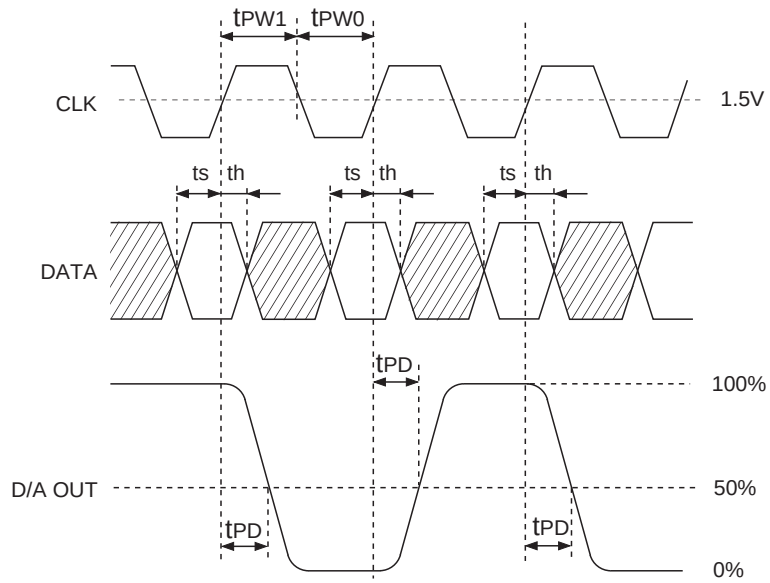
Pin Description and Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
30 to 32 1 to 7	D0 to D9	I		Digital input. 30 pin D0 (LSB) to 7 pin D9 (MSB)
8, 12,16, 26, 29	NC	—		NC pin
9	CLK	I		Clock input
10	BLK			Blanking input. This is synchronized with the clock input signal. No signal (0 V output) at high and output state at low.
11	$\overline{CE}$			Chip enable input. This is not synchronized with the clock input signal. No signal (0 V output) at high makes power consumption minimum.
13, 28	DVDD	—		Digital power supply
14	VB	O		Connect a capacitor of approximately 0.1 µF.
15, 27	DVSS	—		Digital ground
17	IREF	O		Reference current output. Connect resistance “RIR” which is 16 times output resistance “R”.
19	VREF	I		Reference voltage input. Sets output full scale value.
22	VG	O		Connect a capacitor of approximately 0.1 µF.

Pin No.	Symbol	I/O	Equivalent circuit	Description
18	SREF	O		Independent constant-voltage source output pin using band gap reference. Stable voltage independent of the fluctuation for supply voltage can be get by connecting to VREF. See Application Circuit 2 for details.
20, 21	AVDD	—		Analog power supply
23	$\overline{IO}$	O		Inverted current output. Connect to GND normally.
24	IO			Current output. Output can be retrieved by connecting resistance. The standard is 200 Ω.
25	AVSS	—		Analog ground

Description of Operation

Timing Chart



I/O Correspondence Table

(When 2.00 V output full-scale voltage)

Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1 1 1	2.0 V
: 1 0 0 0 0 0 0 0 0 0	1.0 V
: 0 0 0 0 0 0 0 0 0 0	0 V

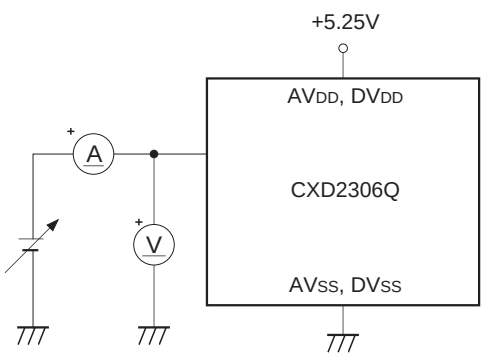
Electrical Characteristics (F_{CLK}=80 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, V_{REF}=2.0 V, R_{IR}=3.3 kΩ, Ta=25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Conversion speed	F_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +85 °C	0		80	MSPS
Integral non-linearity error	E_L	Endpoint	–2.0		2.0	LSB
Differential non-linearity error	E_D		–0.5		0.5	LSB
Precision guaranteed output voltage range	V_{OC}		1.8	1.92	2.0	V
Output full-scale voltage	V_{FS}		1.8	1.92	2.0	V
Output full-scale current	I_{FS}		9.0	9.6	10	mA
Output offset voltage	V_{OS}	When D0 to D9= "0000000000" input			1	mV
Glitch energy	GE	R_{OUT}=100 Ω, 1 Vp-p output		50		pV•s
Differential gain	DG			2.5		%
Differential phase	DP			1.3		deg
Supply current	I_{DD}	$\overline{CE}$=L			30	mA
	I_{STB}	$\overline{CE}$=H			1	
Analog input resistance	R_{IN}	VREF	1			MΩ
Input capacitance	C_I				9	pF
Output capacitance	C_O	IO		50		pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V	2.15			V
	V_{IL}	Ta=–20 to +75 °C			0.85	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V	–5		5	µA
	I_{IL}	Ta=–20 to +75 °C				
SREF output voltage	V_{SR}		1.0		1.3	V
Setup time	ts		5.0			ns
Hold time	th		1.0			ns
Propagation delay time	t_{PD}			10		ns
$\overline{CE}$ enable time ∗1	t_E	$\overline{CE}$=H→L		1	2	ms
$\overline{CE}$ disable time ∗1	t_D	$\overline{CE}$=L→H		1	2	ms

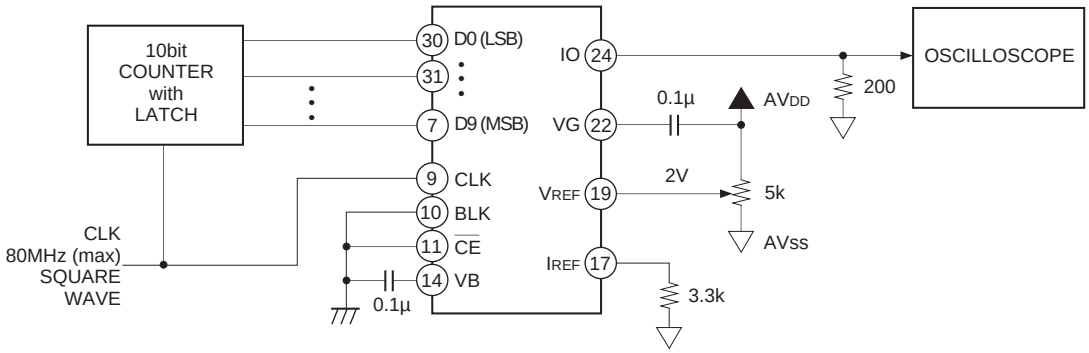
∗1 When the external capacitor for the VG pin is 0.1 µF.

Electrical Characteristics Measurement Circuit

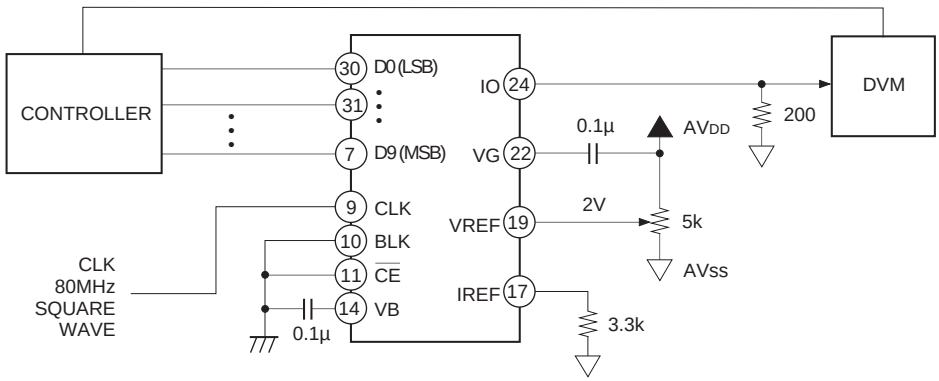
Analog Input Resistance
Digital Input Current } **Measurement Circuit**



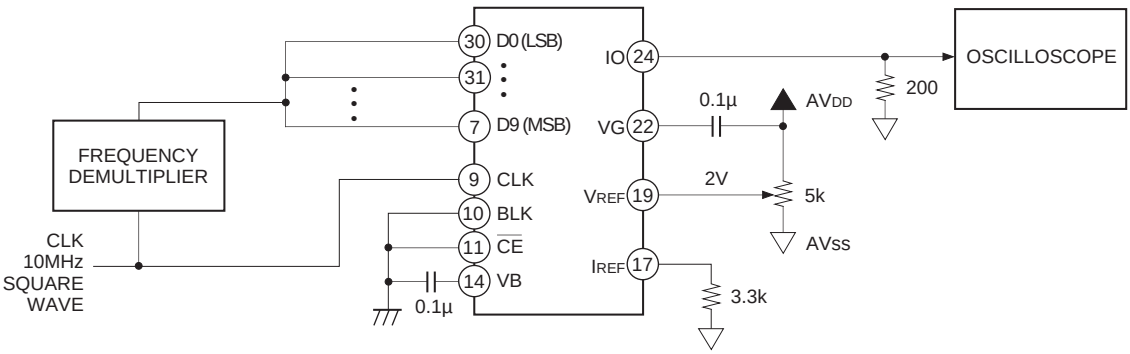
Maximum Conversion Rate Measurement Circuit



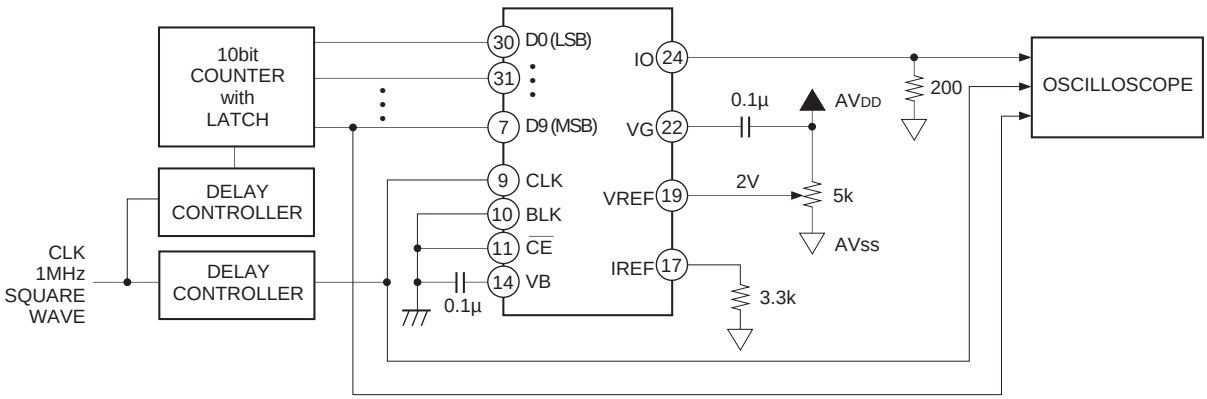
DC Characteristics Measurement Circuit



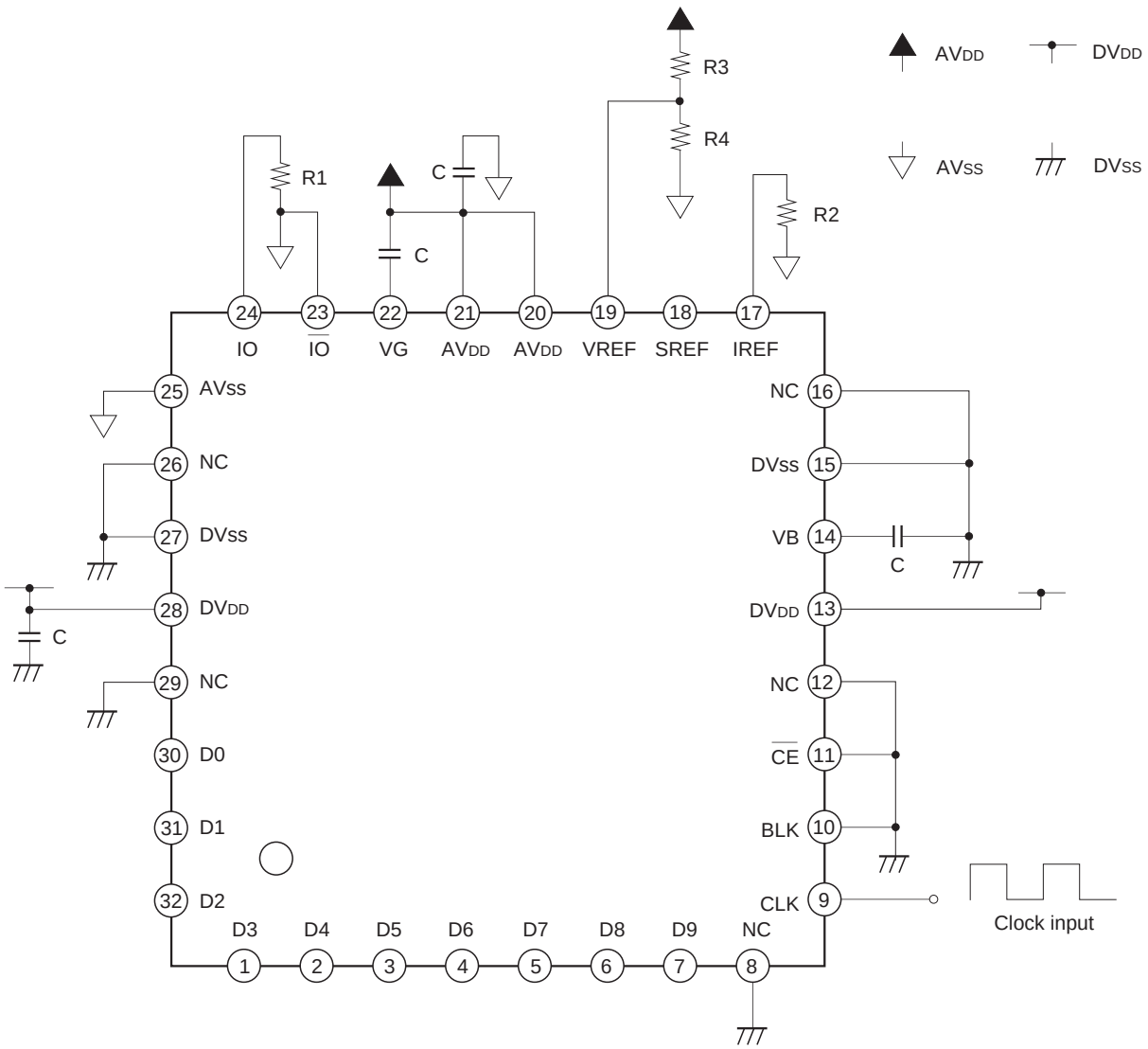
Propagation Delay Time Measurement Circuit



Setup Time / Hold Time / Glitch Energy — Measurement Circuit



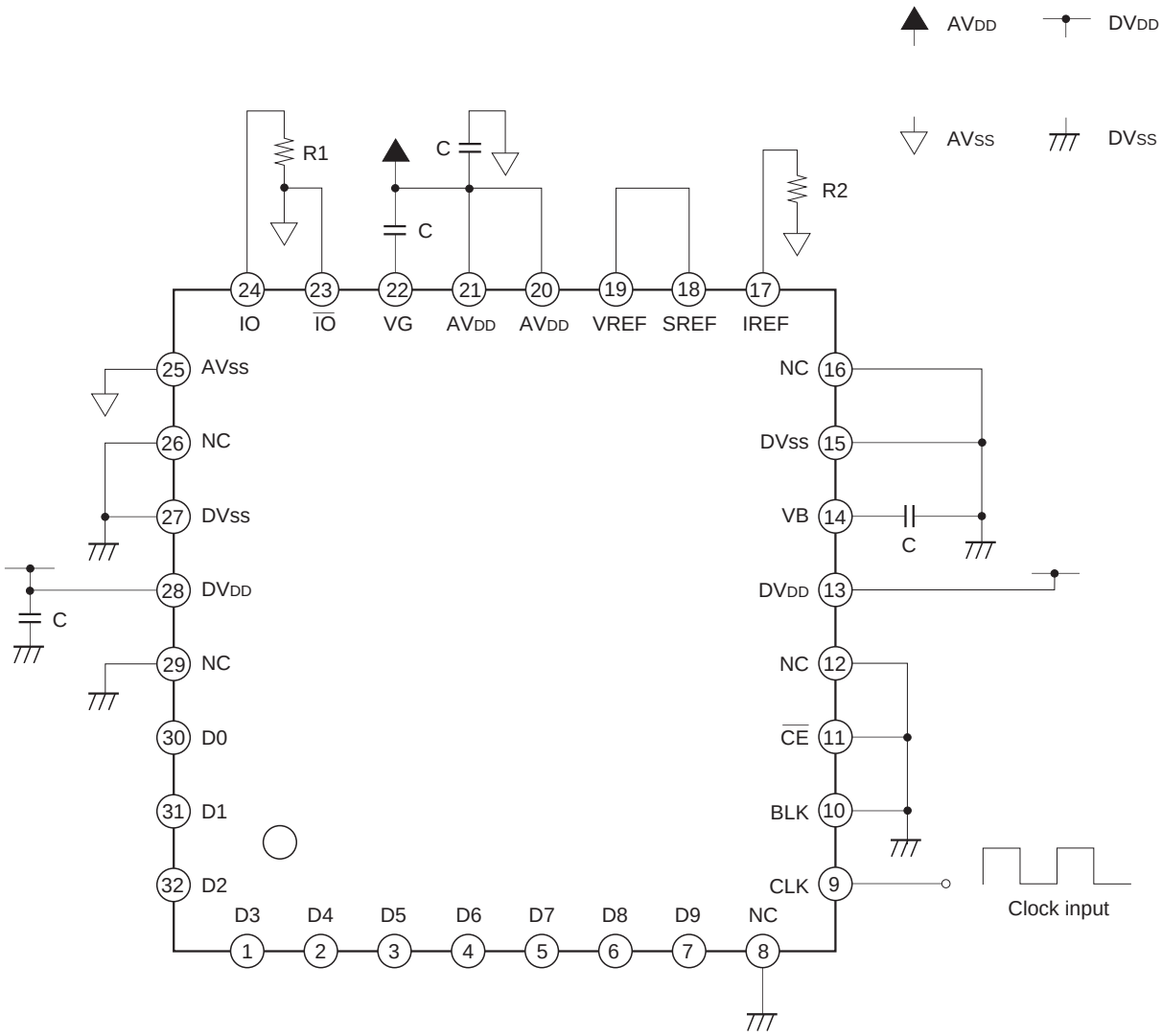
Application Circuit 1



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- Pin 18 is left open when using normally
- R1 = 200Ω
- R2 = 3.3kΩ (R_{IR})
- R3 = 3.0kΩ
- R4 = 2.0kΩ
- C = 0.1µF

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- R1 = 200Ω
- R2 = 2.0kΩ
- C = 0.1µF

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- Selecting the Output Resistance

  CXD2306Q is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin IO.

  Specifications: Output full-scale voltage V_{FS} = 1.8 to 2.0 [V]
  Output full-scale current I_{FS} = 10 or less [mA]

  Calculate the output resistance from $V_{FS} = I_{FS} \times R_{OUT}$. Connect a resistance sixteen times the output resistance to the reference current pin IREF. In some cases, as this value may not exist, a similar value can be used instead.

  Note that the V_{FS} will be the following.

  $$V_{FS} = V_{REF} \times 16\ R_{OUT}/R_{IR}$$

  V_{REF} is the voltage set at the VREF pin, R_{OUT} is the resistor to be connected to the current output pin IO and R_{IR} is the resistor to be connected to the IREF. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data settling time. Set the best values according to the purpose of use.

- Correlation between Data and Clock

  For CXD2306Q to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (ts) and hold time (th) as specified in "Electrical Characteristics".

- Power supply and ground

  Separate the analog and digital signals around the device to reduce noise effects. Bypass the power supply pin to each ground with a 0.1 µF ceramics capacitor as near as possible to the pin for both the digital and analog signals.

- Latch up

  Analog and digital power supply must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on.

- SREF

  The SREF is an independent regulated voltage source. By connecting it to the VREF, stable output amplitudes that do not depend on fluctuations in the power supply can be obtained.

  In this case, as $V_{FS} = V_{SR} \times 16R_{OUT}/R_{IR}$, set the V_{FS} according to R_{IR}. Where V_{SR} is the output voltage of SREF. Do not use this pin as the reference power supply for other IC because this pin is for the exclusive use of the CXD2306Q.

- $\overline{IO}$ pin

  The $\overline{IO}$ pin is the inverted current output pin described in the Pin Description. The sum of the currents output from the IO pin and the $\overline{IO}$ pin becomes the constant value for any input data.

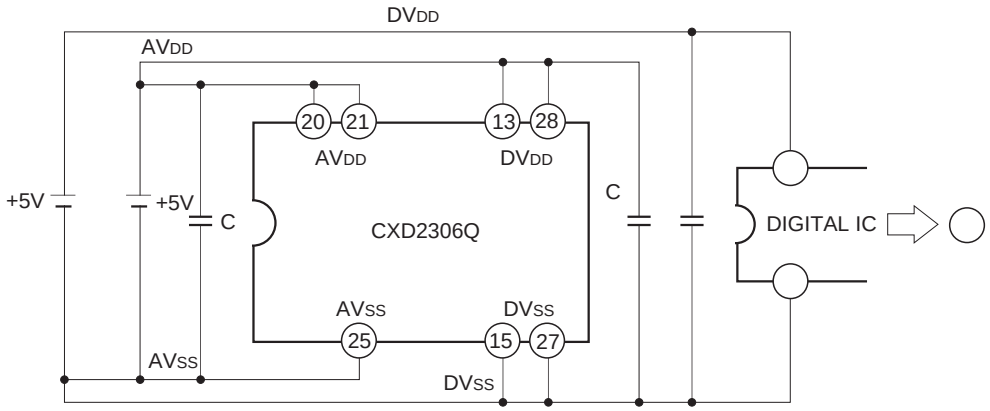
  However, the performances such as the linearity error of the $\overline{IO}$ pin output current is not guaranteed.

Latch Up Prevention

The CXD2306Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pin 20 and 21) and DV_{DD} (Pin 11 and 28), when power supply is ON.

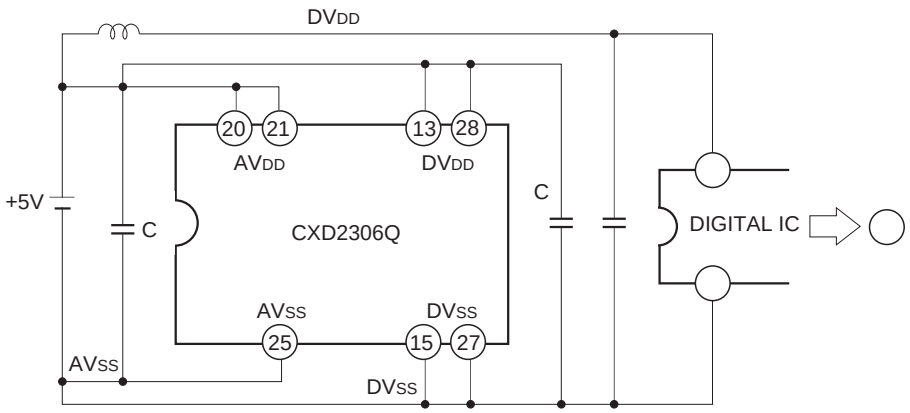
1. Correct usage

a. When analog and digital supplies are from different sources

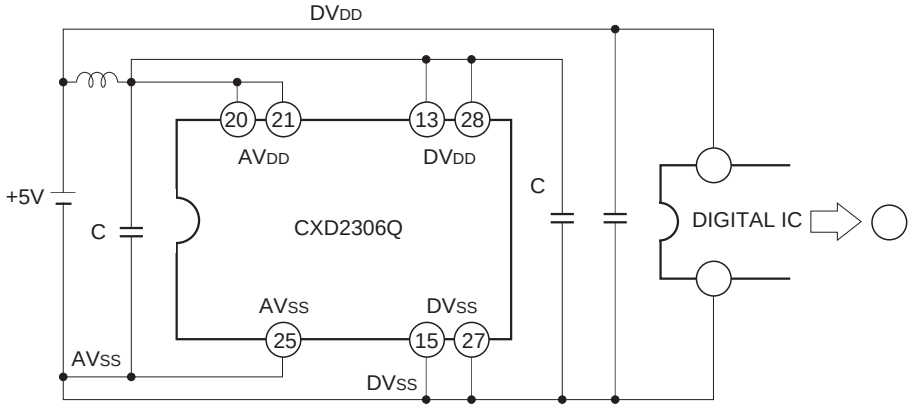


b. When analog and digital supplies are from a common source

(i)

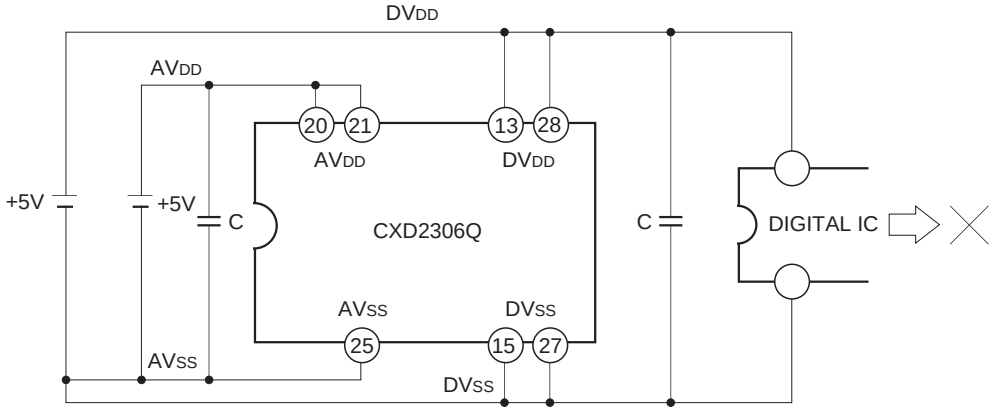


(ii)



2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources



b. When analog and digital supplies are from common source

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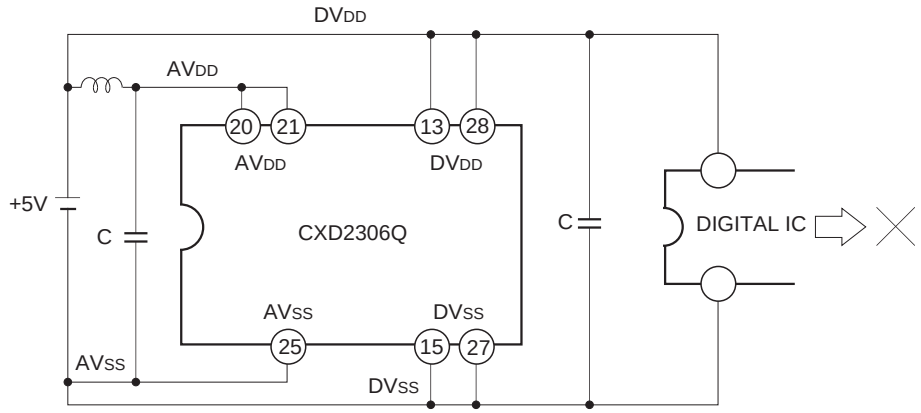
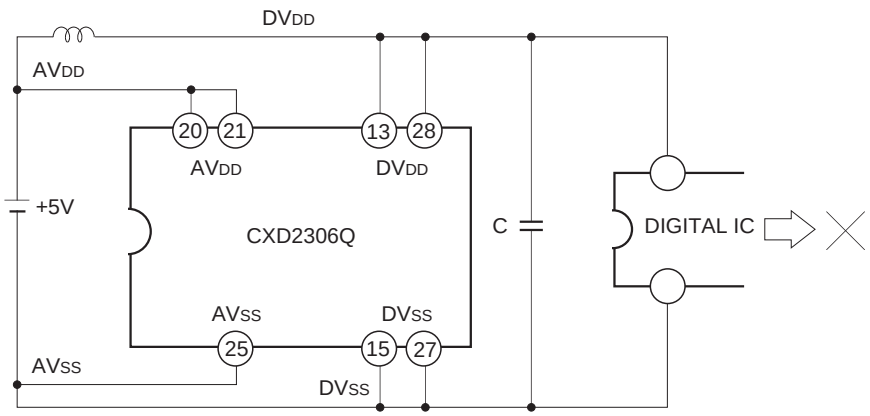


(ii)



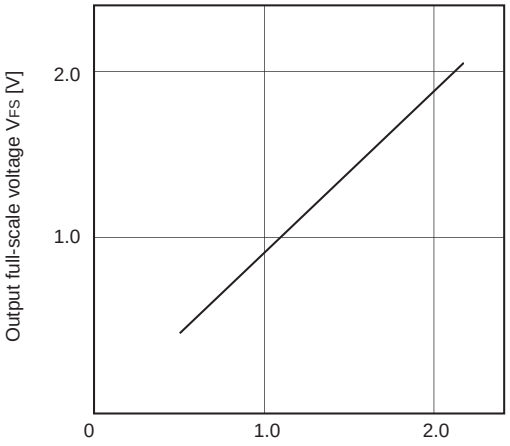


Fig. 1. Reference voltage vs. Output full-scale voltage

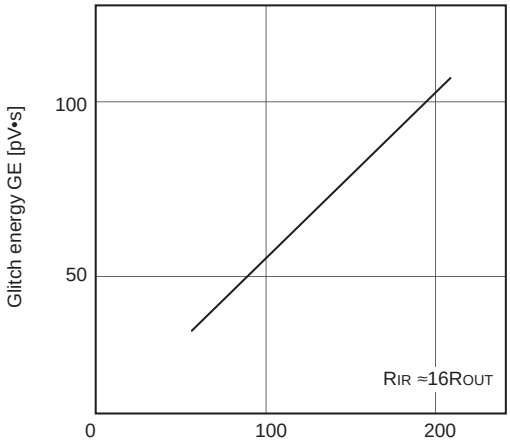


Fig. 2. Glitch energy vs. Output resistance

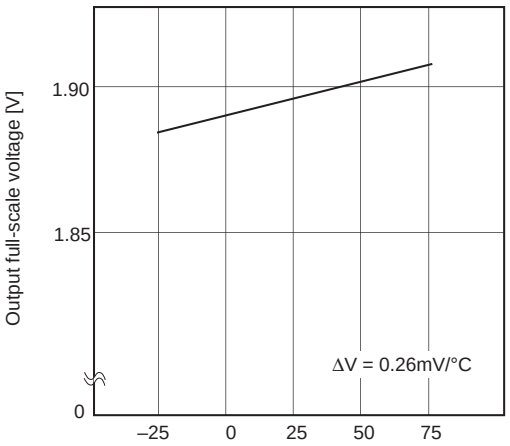


Fig. 3. Ambient temperature vs. Output full-scale voltage

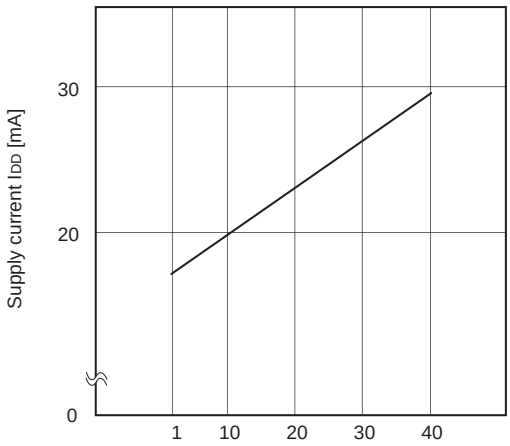


Fig. 4. Output frequency vs. Supply current

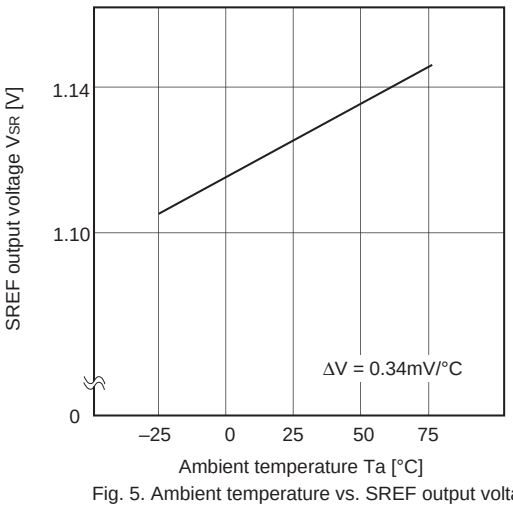
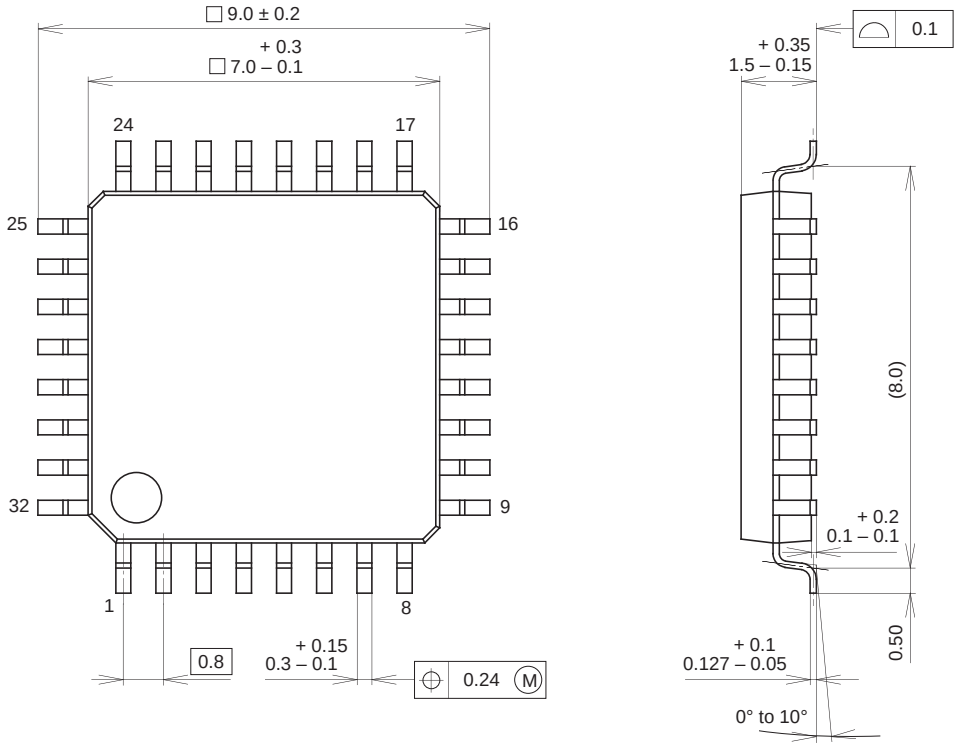


Fig. 5. Ambient temperature vs. SREF output voltage

Standard masurement conditions and description
- AVDD=DVDD=5V
- VREF=2.0V
- ROUT=200Ω
- RIR=3.3kΩ
- Ta=25°C
- Input data in Fig. 4=all 0, rectangular wave of all 1, clock freq.=80MHz.

Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g