SONY

CXD2434ATQ

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD2434ATQ is an IC developed to generate the timing pulses required by the Progressive Scan CCD image sensors as well as signal processing circuits. The CXD2434ATQ adds EFS operation when using the high-speed electronic shutter and other changes to the CXD2434TQ specifications.

Features

- External trigger function
- Electronic shutter function
- Supports non-interlaced operation
- 30 frames/s
- Built-in driver for the horizontal (H) clock
- Base oscillation 1560 f_H (24.5454 MHz)

Applications

Progressive Scan CCD cameras

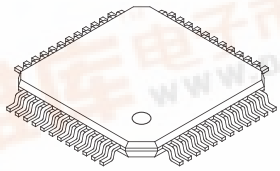
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX084AK, ICX084AL

48 pin TQFP (Plastic)



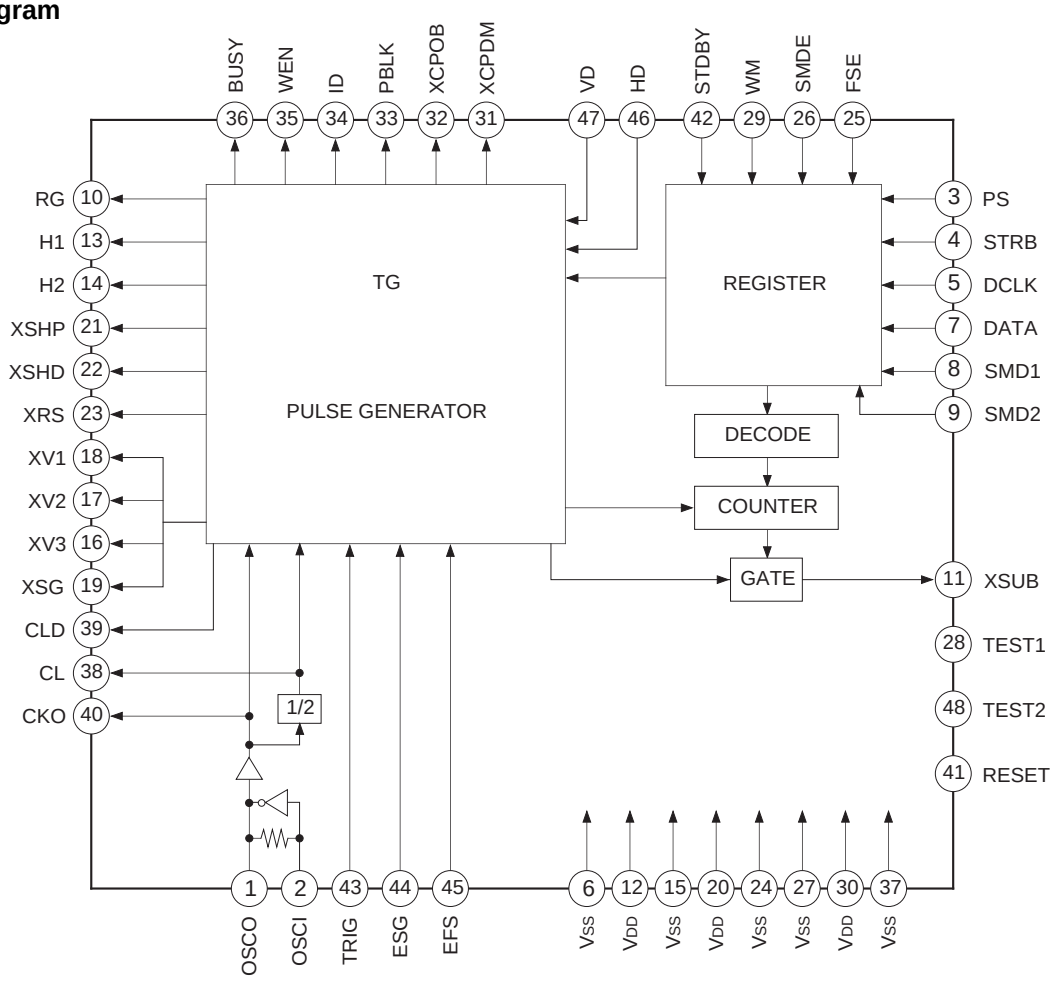
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	V_{SS} –0.5 to +7.0	V
• Input voltage	V_I	V_{SS} –0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS} –0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

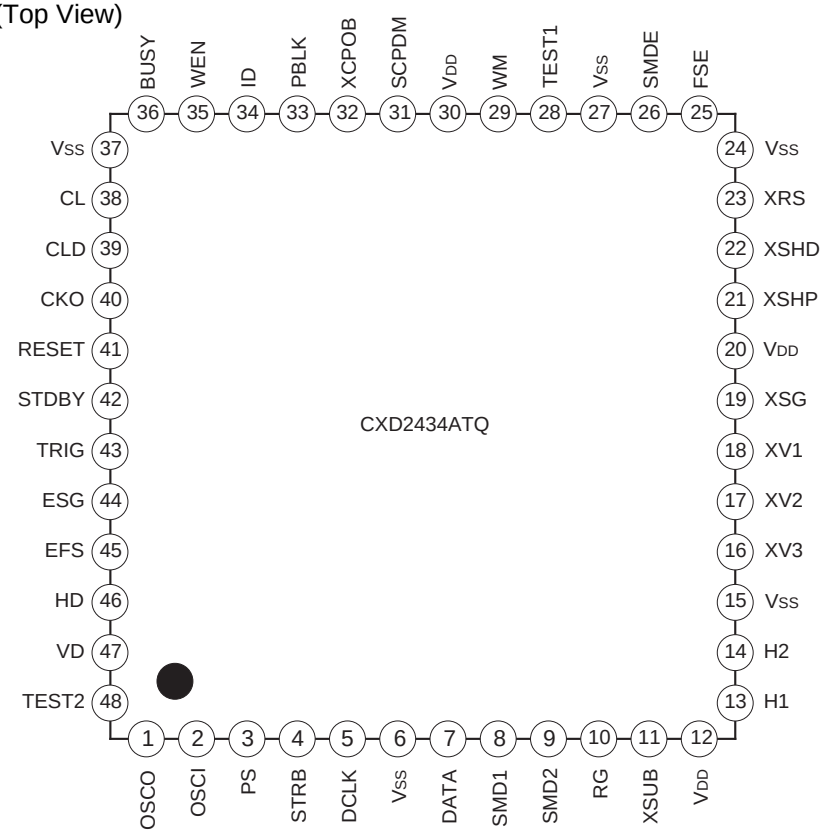
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation.
2	OSCI	I	Inverter input for oscillation.
3	PS	I	Switching for electronic shutter speed input method. (With pull-up resistor) Low: Serial input, High: Parallel input
4	STRB	I	Shutter speed setting. (With pull-up resistor)
5	DCLK	I	Shutter speed setting. (With pull-up resistor)
6	V_{SS}	—	GND
7	DATA	I	Shutter speed setting. (With pull-up resistor)
8	SMD1	I	Shutter mode setting. (With pull-up resistor)
9	SMD2	I	Shutter mode setting. (With pull-up resistor)
10	RG	O	Reset gate pulse output.
11	XSUB	O	CCD discharge pulse output.
12	V_{DD}	—	Power supply.
13	H1	O	Clock output for horizontal CCD drive.
14	H2	O	Clock output for horizontal CCD drive.
15	V_{SS}	—	GND
16	XV3	O	Clock output for vertical CCD drive.
17	XV2	O	Clock output for vertical CCD drive.
18	XV1	O	Clock output for vertical CCD drive.
19	XSG	O	Sensor charge readout pulse output.
20	V_{DD}	—	Power supply.
21	XSHP	O	Sample-and-hold pulse output.
22	XSHD	O	Sample-and-hold pulse output.
23	XRS	O	Sample-and-hold pulse output.
24	V_{SS}	—	GND
25	FSE	I	Switching for external trigger discharge operation. (With pull-up resistor) Low: No high-speed discharge, High: High-speed discharge
26	SMDE	I	Switching for readout timing. (With pull-up resistor) Low: ESG input valid, High: ESG input invalid
27	V_{SS}	—	GND
28	TEST1	I	Test. (With pull-down resistor)
29	WM	I	WEN mode setting. (With pull-down resistor) Low: Effective line, High: XSG synchronization
30	V_{DD}	—	Power supply.
31	XCPDM	O	Clamp pulse output.
32	XCPOB	O	Clamp pulse output.
33	PBLK	O	Blanking cleaning pulse output.
34	ID	O	Line identification output.
35	WEN	O	Write enable output.
36	BUSY	O	Trigger mode flag output.
37	V_{SS}	—	GND
38	CL	O	780 f_H clock output.
39	CLD	O	AD conversion pulse output.

Pin No.	Symbol	I/O	Description
40	CKO	O	1560 f_H clock output.
41	RESET	I	RESET. (With pull-up resistor) Low : Reset, High : Normal
42	STDBY	I	Standby. (With pull-up resistor) Low: Internal clock supply stopped, High: Normal
43	TRIG	I	External trigger input. (With pull-up resistor)
44	ESG	I	External readout input. (With pull-up resistor)
45	EFS	I	Vertical CCD discharge input. (With pull-up resistor)
46	HD	I	Horizontal sync signal input.
47	VD	I	Vertical sync signal input.
48	TEST2	I	Test. (With pull-up resistor)

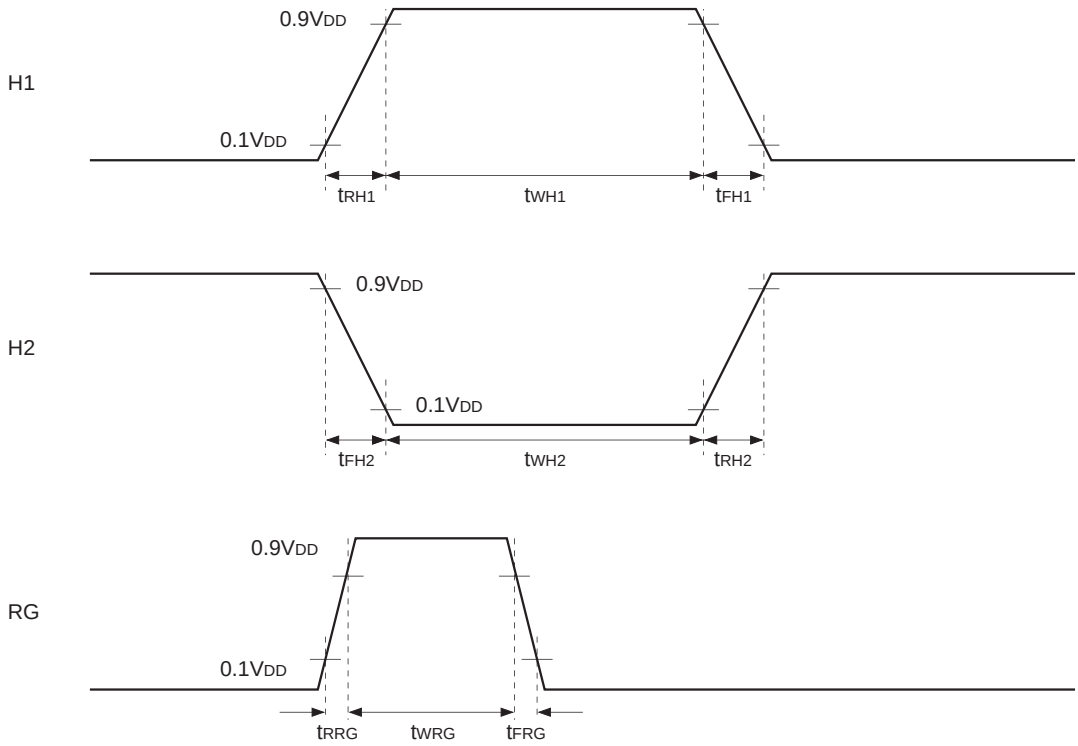
Electrical Characteristics

1. DC Characteristics V_{DD}=4.75 V to 5.25 V Topr= –20 to +75 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1	V_{IH1}		0.7 V_{DD}			V
(Input pins other than those listed below)	V_{IL1}				0.3 V_{DD}	V
Input voltage 2	V_{IH2}		0.7 V_{DD}			V
(Pin 2)	V_{IL2}				0.3 V_{DD}	V
Output voltage 1	V_{OH1}	I_{OH}=–2.5 mA	V_{DD}–0.4			V
(Output pins other than those listed below)	V_{OL1}	I_{OL}=4.5 mA			0.4	V
Output voltage 2	V_{OH2}	I_{OH}=–5.0 mA	V_{DD}–0.4			V
(Pins 21, 22, 23, 38, 39 and 40)	V_{OL2}	I_{OL}=9.0 mA			0.4	V
Output voltage 3	V_{OH3}	I_{OH}=–7.5 mA	V_{DD}–0.4			V
(Pin 10)	V_{OL3}	I_{OL}=13.5 mA			0.4	V
Output voltage 4	V_{OH4}	I_{OH}=–14.0 mA	V_{DD}–0.4			V
(Pins 13 and 14)	V_{OL4}	I_{OL}=24.0 mA			0.4	V
Output voltage 5	V_{OH5}		V_{DD}/2			V
(Pin 1)	V_{OL5}				V_{DD}/2	V
Feedback resistor	R_{FB}	V_{IN}=V_{SS} or V_{DD}		1 M		Ω
Pull-up resistor	R_{PU}	V_{IL}=0 V		50 k	100 k	Ω
Pull-down resistor	R_{PD}	V_{IH}=V_{DD}		50 k	100 k	Ω
Current consumption	I_{DD}	V_{DD}=5 V		40		mA

2. AC Characteristics

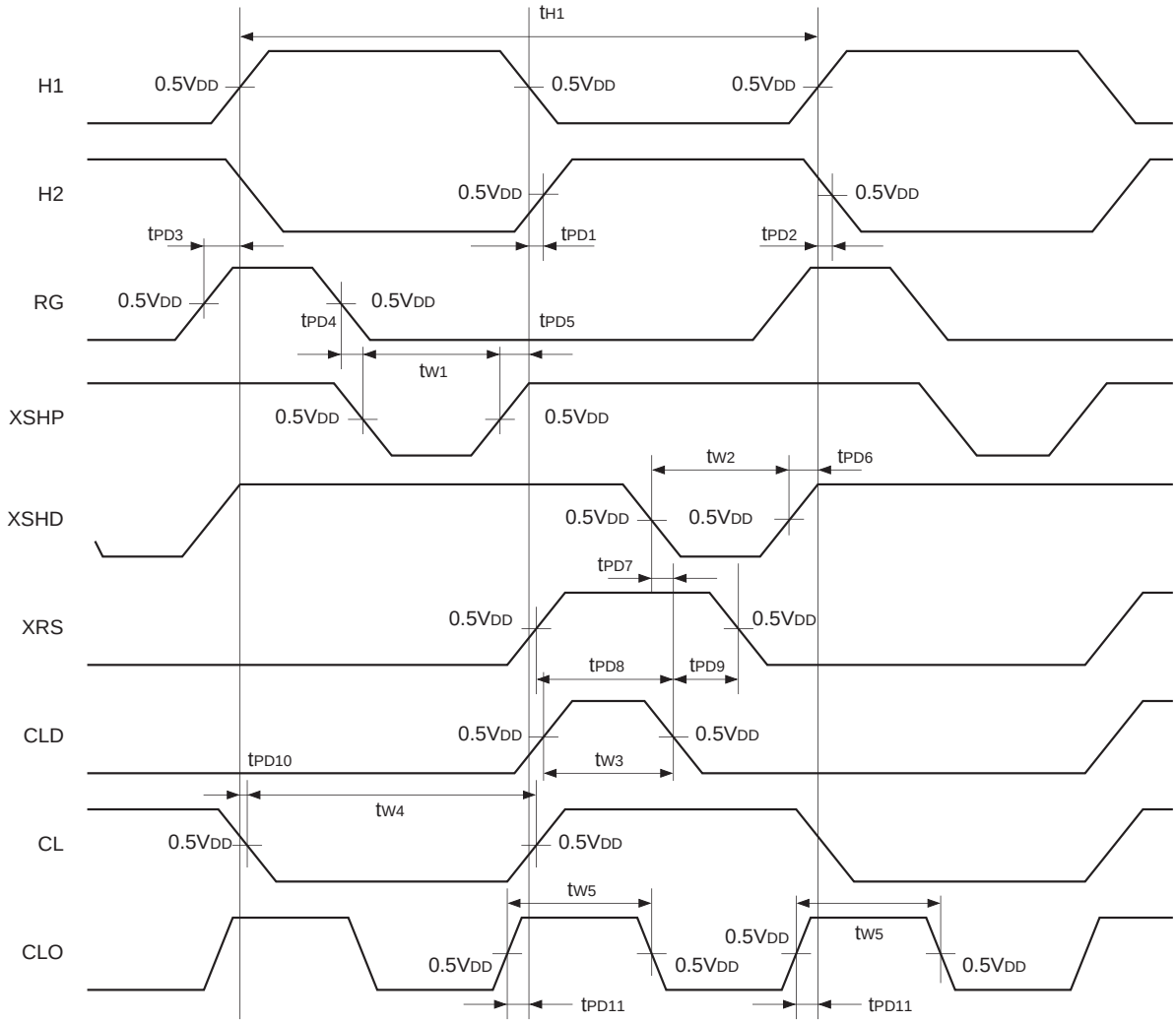
1) Waveform characteristics of H1, H2 and RG



V_{DD}=5.0 V, Topr=25 °C, load capacitance of H1 and H2=100 pF, load capacitance of RG=10 pF

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{RH1}	H1 rise time		6	15	ns
t_{FH1}	H1 fall time		5	15	ns
t_{WH1}	H1 high level time	25	35		ns
t_{RH2}	H2 rise time		6	15	ns
t_{FH2}	H2 fall time		5	15	ns
t_{WH2}	H2 low level time	25	35		ns
t_{RRG}	RG rise time		2	5	ns
t_{FRG}	RG fall time		2	5	ns
t_{WRG}	RG high level time	10	15	20	ns

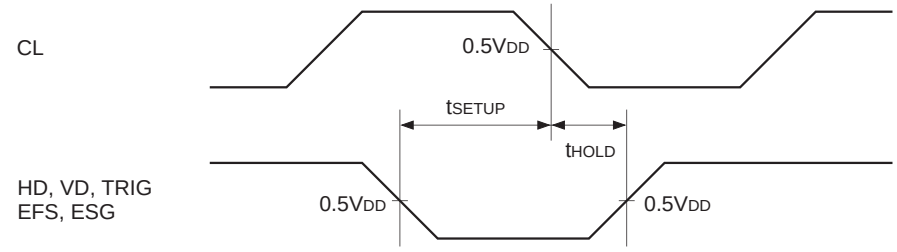
2) Phase characteristics of H1, H2, RG, XSHP, XSHD, XRS, CL, CLD and CKO



VDD=5.0 V, Topr=25 °C, load capacitance of CL and CKO=30 pF, load capacitance of CLD, XSHP, XSHD, XRS and RG=10 pF

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{H1}	H1 cycle		82		ns
t_{PD1}	H2 rising delay, activated by the falling edge of H1	–5	0	5	ns
t_{PD2}	H2 falling delay, activated by the rising edge of H1	–5	0	5	ns
t_{PD3}	H1 rising delay, activated by the rising edge of RG	–5	0	5	ns
t_{PD4}	XSHP falling delay, activated by the falling edge of RG	–2	4	10	ns
t_{PD5}	H1 falling delay, activated by the rising edge of XSHP	–7	2	7	ns
t_{PD6}	H1 rising delay, activated by the rising edge of XSHD	–5	2	7	ns
t_{PD7}	CLD falling delay, activated by the falling edge of XSHD	–5	2	7	ns
t_{PD8}	CLD falling delay, activated by the rising edge of XRS	17	22	27	ns
t_{PD9}	XRS falling delay, activated by the falling edge of CLD	0	8	15	ns
t_{PD10}	CL falling delay, activated by the rising edge of H1	–5	0	5	ns
t_{PD11}	H1 rising (falling) delay, activated by the rising edge of CKO	–5	2	7	ns
t_{W1}	XSHP pulse width	13	18	23	ns
t_{W2}	XSHD pulse width	15	20	25	ns
t_{W3}	CLD pulse width	17	22	27	ns
t_{W4}	CL pulse width	38	41	45	ns
t_{W5}	CKO pulse width	17	20	24	ns

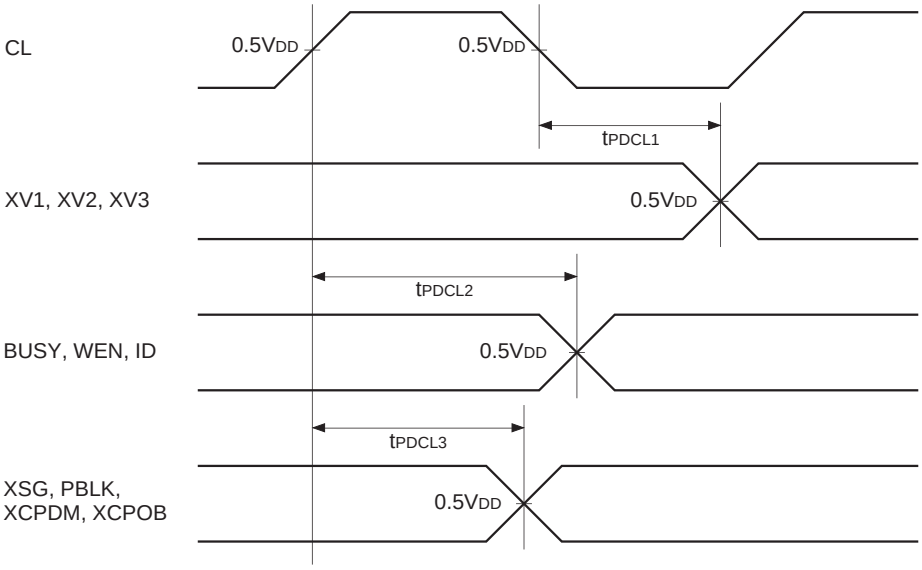
3) Phase conditions of HD, VD, TRIG, EFS and ESG



V_{DD}=5.0 V, Topr=25 °C, load capacitance of CL=30 pF

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{SETUP}	HD, VD, TRIG, EFS and ESG setup time, activated by CL	20			ns
t_{HOLD}	HD, VD, TRIG, EFS and ESG hold time, activated by CL	5			ns

4) Phase characteristics of XV1, XV2, XV3, XSG, PBLK, XCPDM, XCPOB, BUSY, WEN and ID



V_{DD}=5.0 V, Topr=25 °C, load capacitance of CL=30 pF,
load capacitance of XV1, XV2, XV3, XSG, PBLK, XCPDM, XCPOB, BUSY, WEN and ID=10 pF

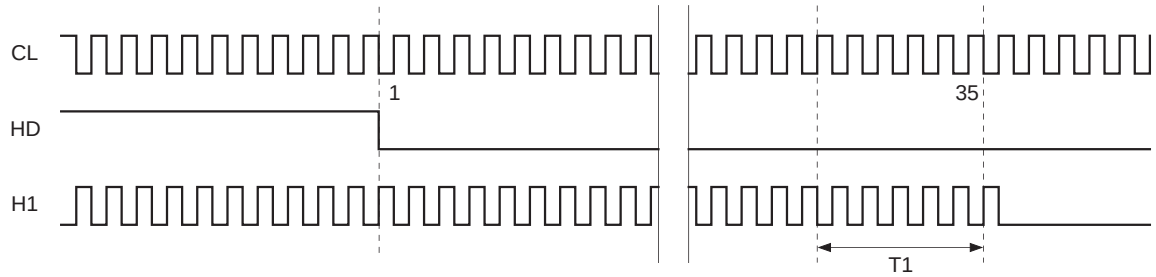
Symbol	Definition	Min.	Typ.	Max.	Unit
t_{PDCL1}	XV1, XV2 and XV3 delay, activated by the falling edge of CL	30		65	ns
t_{PDCL2}	BUSY, WEN and ID delay, activated by the rising edge of CL	40		60	ns
t_{PDCL3}	XSG, PBLK, XCPDM and XCPOB delay, activated by the rising edge of CL	40		55	ns

Description of Functions

1. Progressive Scan CCD drive pulse generation

- Combining this IC with a crystal oscillator generates a fundamental frequency of 24.5454 MHz.
- CCD drive pulse generation is synchronized with the HD and VD inputs.
  Set f_{CL} to 780 f_{HD} and fHD to 525 f_{VD}.
- The various operations are performed by the TRIG, EFS and ESG inputs. (See the following items.)

<Detection timing for VD, TRIG, EFS and ESG>



Detection timing for VD, TRIG, EFS and ESG

After HD input is detected, the status of VD, TRIG, ESG and EFS is detected during T1.
Do not change the status of VD, TRIG, ESG and EFS during T1.
When input is from a non-synchronized system, the low level period for each pulse should be set to 63.5 µs or longer to prevent misoperation.

2. Reset

The internal register values are undetermined immediately after power-on, so perform one of the following reset operations.

1. Reset by the RESET pin
   Reset is performed by setting the RESET pin low for a period of 80 ns or more. Reset can also be performed by setting the RESET pin low during power-on and then switching the RESET pin from low to high when V_{DD} rises to 4.75 V or higher. Note that when reset is performed by the RESET pin, the electronic shutter settings made by serial input are also reset.
2. Reset by turning off the electronic shutter
   Reset is performed by setting the shutter mode to electronic shutter off and inputting VD. Note that in this case the TRIG, ESG and EFS pins should all be set high.

3. Electronic shutter

<Shutter modes>

The electronic shutter has the following four shutter modes.

- Electronic shutter off : Exposure time is 1/30 s.
- High-speed electronic shutter : Exposure time is shorter than 1/30 s.
- Low-speed electronic shutter: Exposure time is longer than 1/30 s.
- Flickerless : Exposure time is 1/50 s. This is a special feature of the high-speed electronic shutter, and reduces flicker from fluorescent lights, etc. in areas with 50 Hz power supply

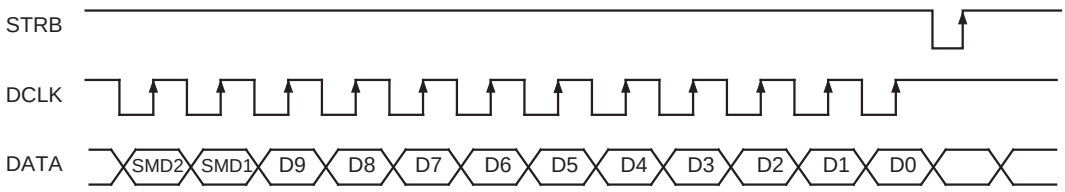
<Shutter mode and speed setting methods>

PS=Low : Serial input; set by the STRB, DCLK and DATA pins. The SMD1 and SMD2 pins are not used.

PS=High : Parallel input; set by the STRB, DCLK, DATA, SMD1 and SMD2 pins.

3-1. [Serial input]

Serial input is set by the STRB, DCLK and DATA pins. The electronic shutter mode and the meanings of the numbers indicated by D0 to 9 vary according to the SMD1 and SMD2 setting of the internal register.



SMD1	SMD2	Mode	D0 to 9
H	H	Electronic shutter off (1/30 s accumulation)	—
L	H	High-speed electronic shutter	Number of exposed lines (Note 1)
H	L	Low-speed electronic shutter	Number of exposed frames (Note 2)

Note 1) Relationship between the number of exposed lines and the exposure time

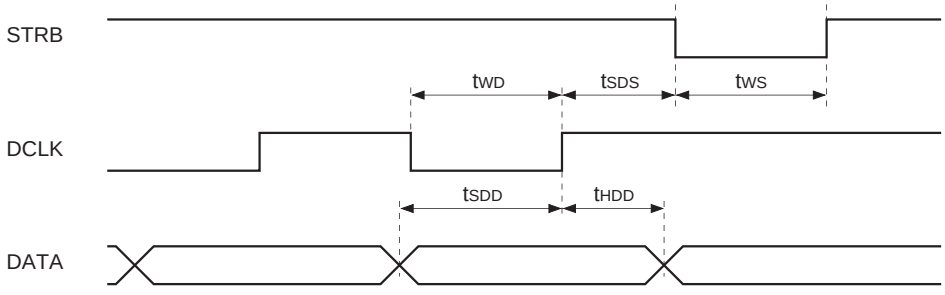
The relationship between the number of exposed lines and the exposure time is as follows.

(Exposure time)=(Number of exposed lines) × (One horizontal scan period) + (Accumulation time for the readout lines)

In this formula, one horizontal scan period equals the HD falling interval, and the accumulation time for the readout lines is the time from the rising edge of XSUB to the rising edge of XSG (456 bits). Also, (Number of exposed lines) should be set to greater than 1 but less than 524.

Note 2) The number of exposed frames should be set to greater than 1 but less than 1023. However, when the number of exposed frames is 1 and SMDE is set to high, external trigger mode does not function.

Timing Chart (Serial input)



AC characteristics for serial input

Symbol	Definition	Min.	Max.
t_{SDD}	DATA setup time, activated by the rising edge of DCLK	10 ns	—
t_{HDD}	DATA hold time, activated by the rising edge of DCLK	10 ns	—
t_{SDS}	DCLK setup time, activated by the falling edge of STRB	10 ns	—
t_{WS}	STRB pulse width	82 ns	—
t_{WD}	DCLK pulse width	82 ns	—

3-2. [Parallel input]

Mode	PS	SMD1	SMD2	STRB	DCLK	DATA	Exposure time
Electronic shutter off	H	H	H	X	X	X	1/30 s
Flickerless	H	L	L	X	X	X	1/50 s
High-speed shutter	H	L	H	H	H	H	1/60 s
	H	L	H	L	H	H	1/125 s
	H	L	H	H	L	H	1/250 s
	H	L	H	L	L	H	1/500 s
	H	L	H	H	H	L	1/1000 s
	H	L	H	L	H	L	1/2000 s
	H	L	H	H	L	L	1/4000 s
	H	L	H	L	L	L	1/10000 s
Low-speed shutter	H	H	L	H	H	H	2 FRM
	H	H	L	L	H	H	3 FRM
	H	H	L	H	L	H	4 FRM
	H	H	L	L	L	H	5 FRM
	H	H	L	H	H	L	6 FRM
	H	H	L	L	H	L	7 FRM
	H	H	L	H	L	L	8 FRM
	H	H	L	L	L	L	9 FRM

4. External trigger mode

External trigger mode starts exposure in sync with the external trigger input. No special pins are required to set this mode.

The IC prepares to shift to external trigger mode with the falling edge of the TRIG pin (Note). The timing to shift to external trigger mode varies according to the mode setting. (See the table.) The BUSY pin maintains high status during external trigger mode. Whether or not to discharge the vertical CCD charge is set by FSE.

Note) See the detection timing for VD, TRIG, EFS and ESG.

Mode settings during external trigger (Note 1)

PS	SMD1	SMD2	Description of operation
L	L	X	The IC is shifted to external trigger mode by HD, exposure is finished after the set time, and XSG is output. (Note 2) (Note 3)
H	L	H	
H	L	L	The IC is shifted to external trigger mode by HD, exposure is finished 1/50 s later, and XSG is output.
X	H	L	Do not set for external trigger.
X	H	H	Trigger input is not accepted.

Note 1) The SMD1 and SMD2 setting method varies according to the PS status. See “3. Electronic shutter”.
PS=Low : Set by serial input.
PS=High : Set by the SMD1 and SMD2 pins.

Note 2) The exposure time setting method is the same as the exposure time setting for the electronic shutter.

Note 3) When FSE=high, set the number of exposed lines from 1 to 522.

<FSE and discharge operation>

During external trigger mode, the previously exposed signal charge sometimes remains in the vertical CCD when exposure finishes. In this case, the image shot with external trigger mode is output overlapped with the previously shot image. Setting FSE to high performs discharge operation for signal charges remaining in the vertical CCD after trigger input. Discharge operation is not performed when FSE is low. This setting is only valid when SMD1 is low.

<Finishing the exposure period with ESG>

During external trigger mode, exposure can be finished in sync with the falling edge of ESG (Note). If SMDE is set to low, the XSG pulse is output regardless of the electronic shutter setting, when the falling edge of ESG is detected. ESG should be fixed to high status at all times other than during external trigger mode. Do not change SMDE while BUSY is high.

Note) See the detection timing for VD, TRIG, EFS and ESG.

<Signal after external trigger mode>

After high-speed external trigger mode is finished, the exposure time differs from that performed by the electronic shutter setting. This is because the start and finish of external trigger mode are not synchronized to VD input.

5. Discharge of the vertical CCD

During EFS is low, discharge of the vertical CCD is performed. During FSE is high in the external trigger mode, the vertical control line by line is possible. That is different from discharge operation. The falling in the effective interval of EFS is detected, discharge is not performed even if the low status is held until the next effective period. For frames using EFS, set electronic shutter off or high-speed electronic shutter. When EFS is used, WEN (WM=low) may not indicate the proper status.

<Discharge start>

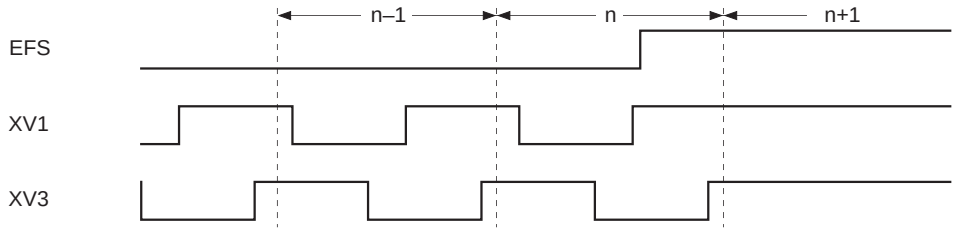
Vertical CCD discharge is started in sync with HD input after the falling edge of EFS (Note). Approximately 3420 ns (81.4 ns × 42 clock pulses) are required to transfer one line vertically.

Note) See the detection timing for VD, TRIG, EFS and ESG.

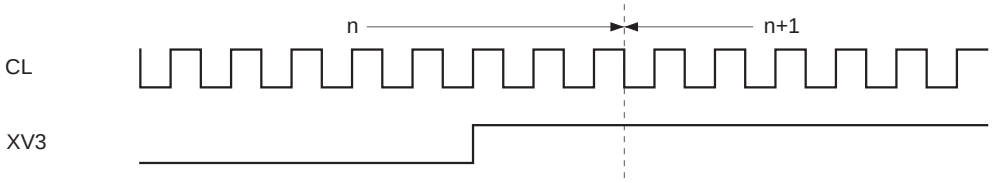
<Discharge finish>

Since the operation uses 42 clock pulses as one unit, when the rising edge of EFS is detected in interval [n], discharge operation stops from interval [n+1]. The period from the rising edge of EFS to the falling edge of VD must be longer than 2HD.

Timing Chart 1



Timing Chart 2



<Maximum number of dischargeable lines>

The number of lines transferred by discharge transfer and normal transfer during the following period should not exceed 4096 lines.

Period : The period from when the XSG pin becomes low until XSG becomes low again or the TRIG pin becomes low.

6. Internal logic stop (standby mode)

When the STDBY pin is set to low, clock supply is stopped to a part of the internal logic. However, output from the oscillation cell (OSCI and OSCO pins) as well as the CL and CKO pins does not stop. The status of each output pin when STDBY is low is shown below.

High : XSUB, XSG

Low : RG, H1, H2, XV1, XV2, XV3, XSHP, XSHD, XRS, XCPOB, XCPDM, PBLK, ID, WEN, BUSY, CLD

Not stopped : OSCO, CL, CKO

7. Mode settings

7-1. VD input-related

BUSY	SMD1	SMD2	SMDE	EFS	VD input
H	L	H	X	X	Invalid
L	H	L	X	H	Readout operation or the number of accumulated frames is counted.
	X	H			Readout operation is performed.
	X	X		L	Invalid

Note 1) When PS is high, SMD1 and SMD2 indicate the status of the SMD1 and SMD2 pins, respectively. When PS is low, these are the corresponding internal register values. See "3. Electronic shutter".

Note 2) Operation when PS=high, SMD1=low and SMD2=low conforms to that when SMD1=low and SMD2=high.

7-2. TRIG, ESG and EFS input-related

BUSY		SMDE	TRIG	ESG	EFS
H	Discharge period (Note 1)	X	Prohibited	Prohibited	Invalid
	Exposure period	H			
		L		Readout operation (Note 4)	
	Signal output period	X		Prohibited	Discharge operation (Note 6) (Note 7)
L	Before TRIG input		IC shifted to external trigger mode (Note 3)	Prohibited (Note 5)	
	After TRIG input (Note 2) (Note 3)		Prohibited		Prohibited

Note 1) Only when FSE is high.

Note 2) Valid only during low-speed shutter.

Note 3) See "4. External trigger mode".

Note 4) ESG input is valid only one time after TRIG input. Do not input ESG two times or more.

Note 5) Fix ESG to high status when BUSY is low.

Note 6) When EFS is low, readout is not activated by VD input. See "7-1. VD input-related".

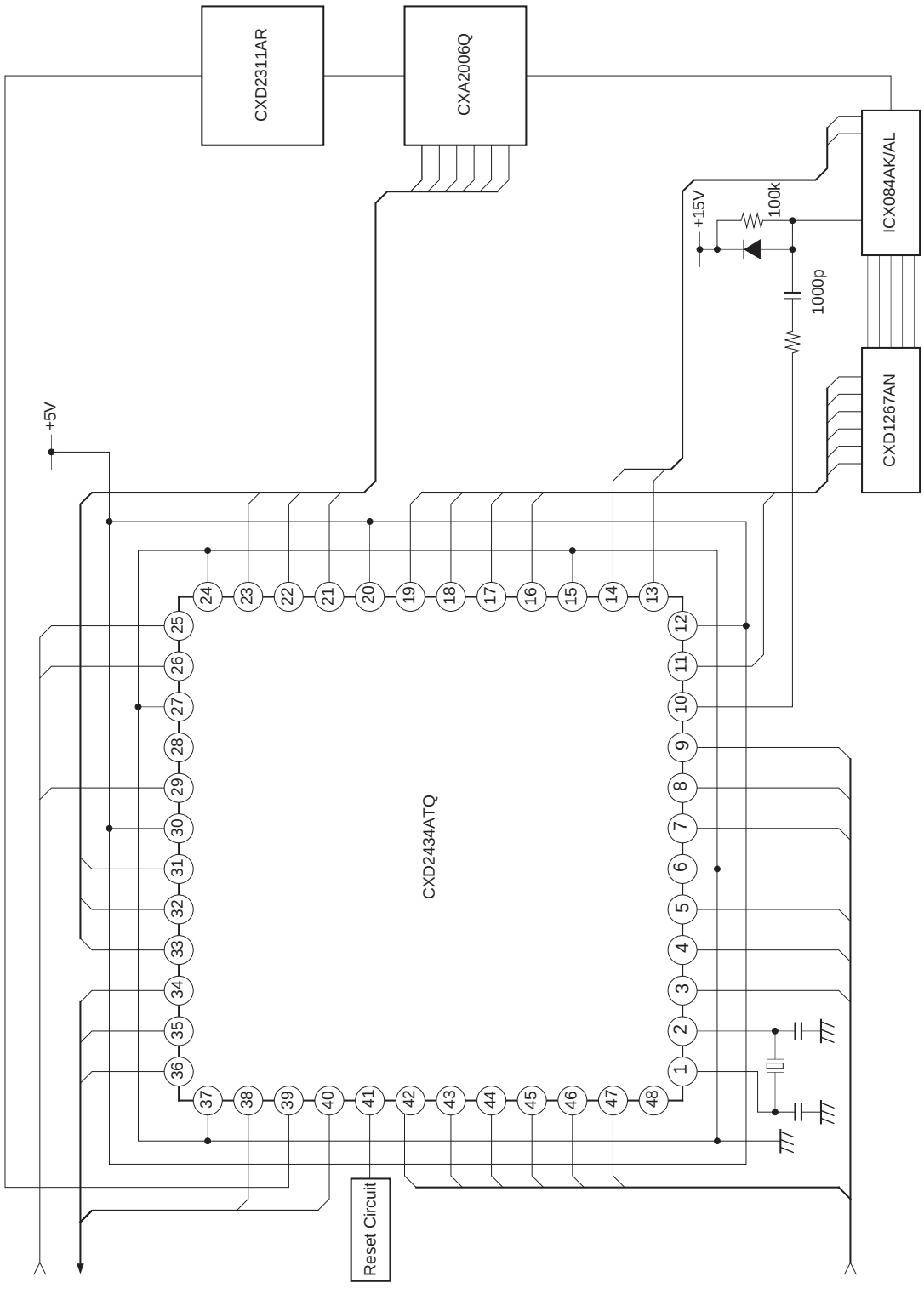
Note 7) Use in electronic shutter off state.

Note 8) In case any two pins or more among TRIG, ESG, and EFS are falled at the same time, the operation is not guaranteed.

7-3. WEN mode switching by WM

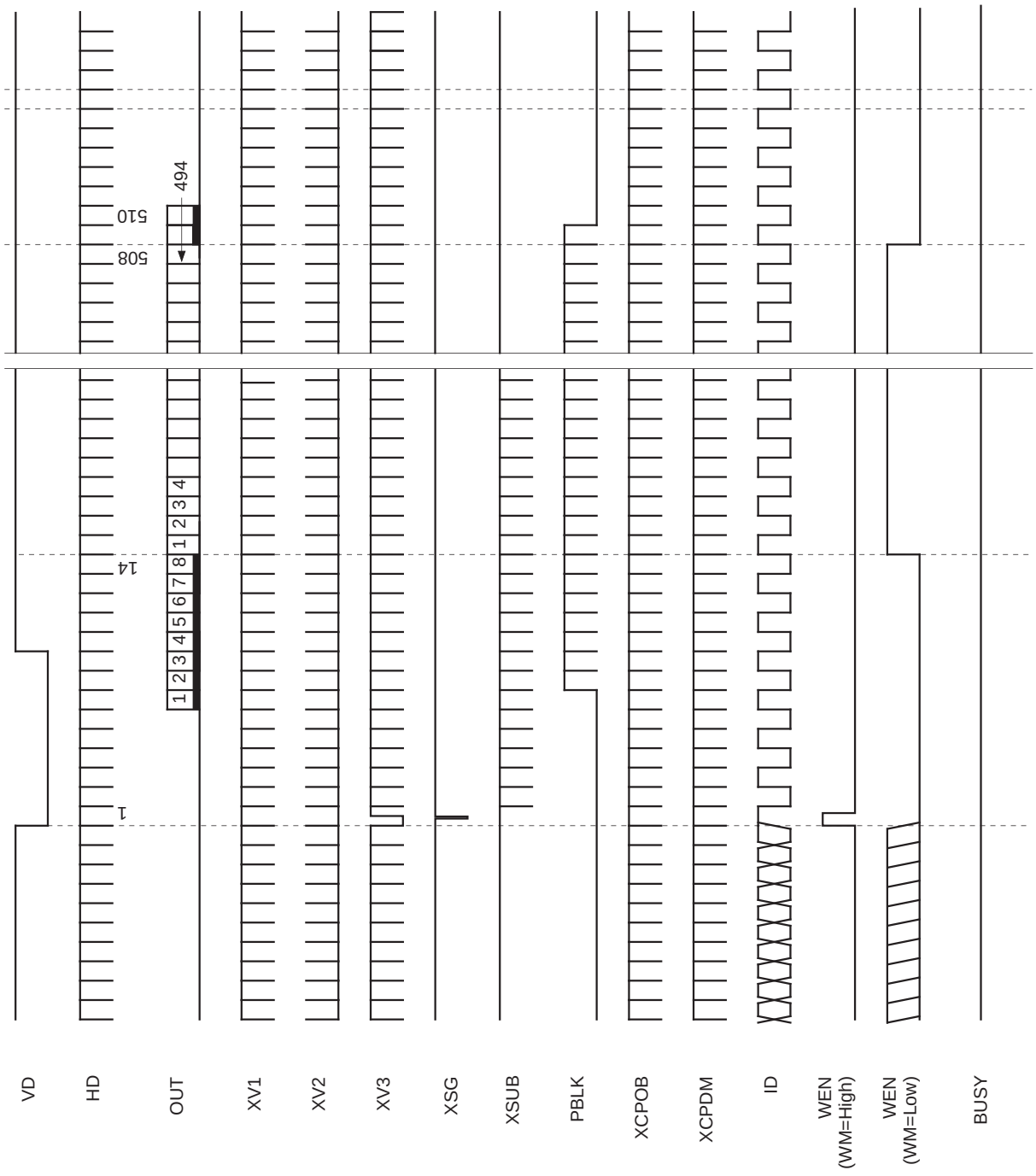
WM	Description of WEN operation
L	Lines for which the signal from the CCD is valid output high; all other lines output low.
H	Output is synchronized with XSG.

Application Circuit

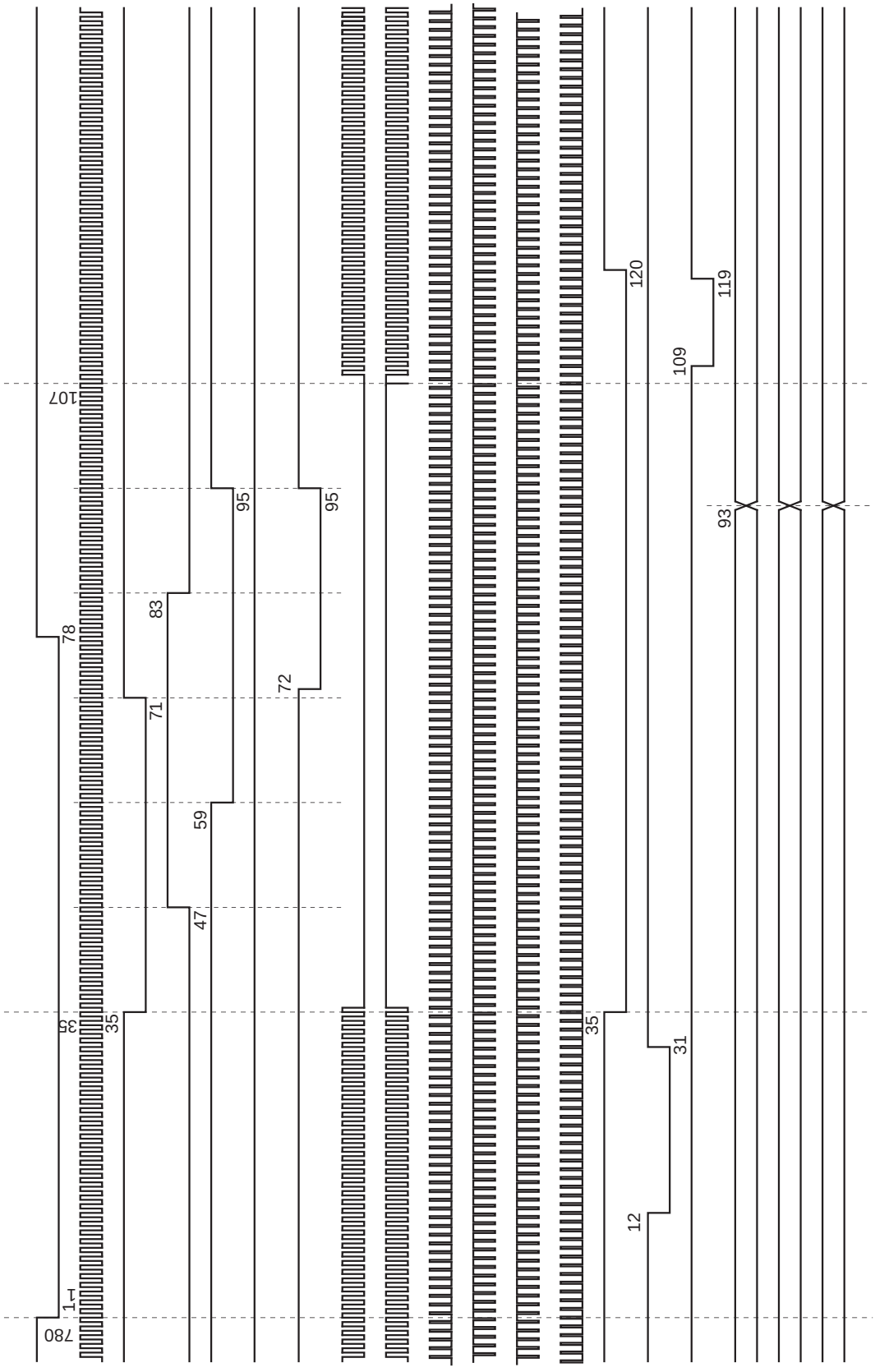


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Normal Operation (vertical synchronization)

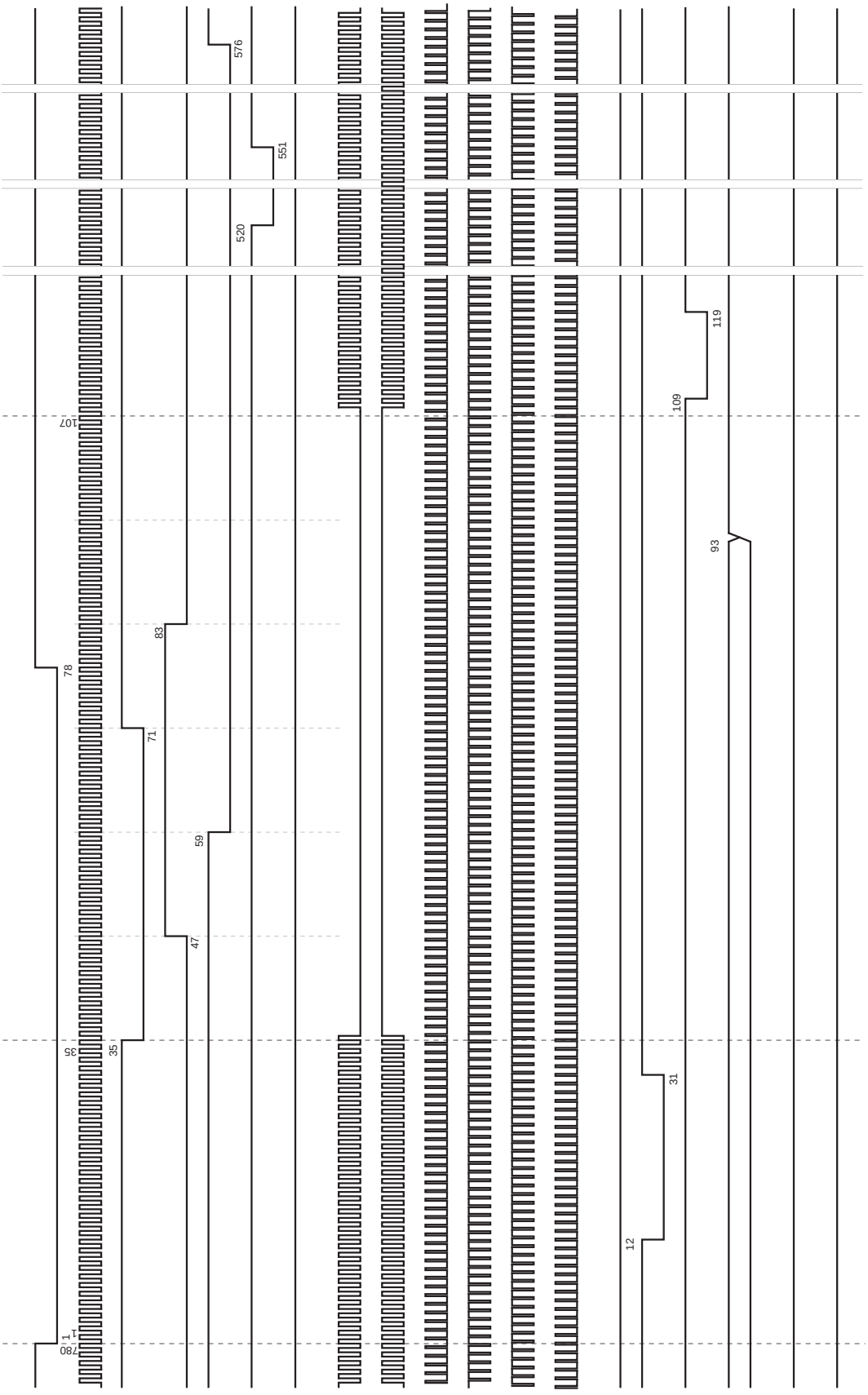


Normal Operation (horizontal synchronization)

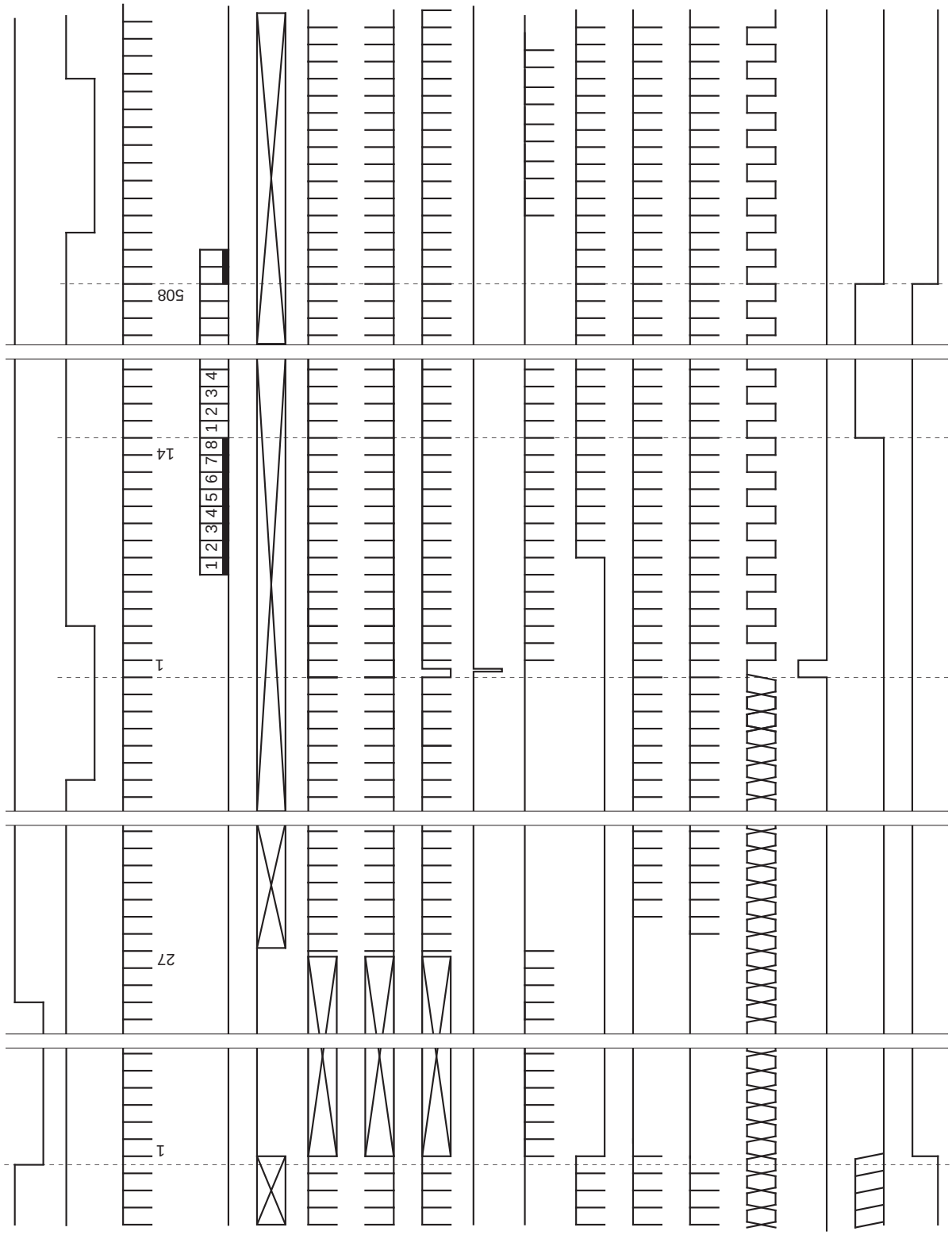


XSUB may be kept high depending on the electronic shutter setting.

Normal Operation: readout timing (horizontal synchronization)

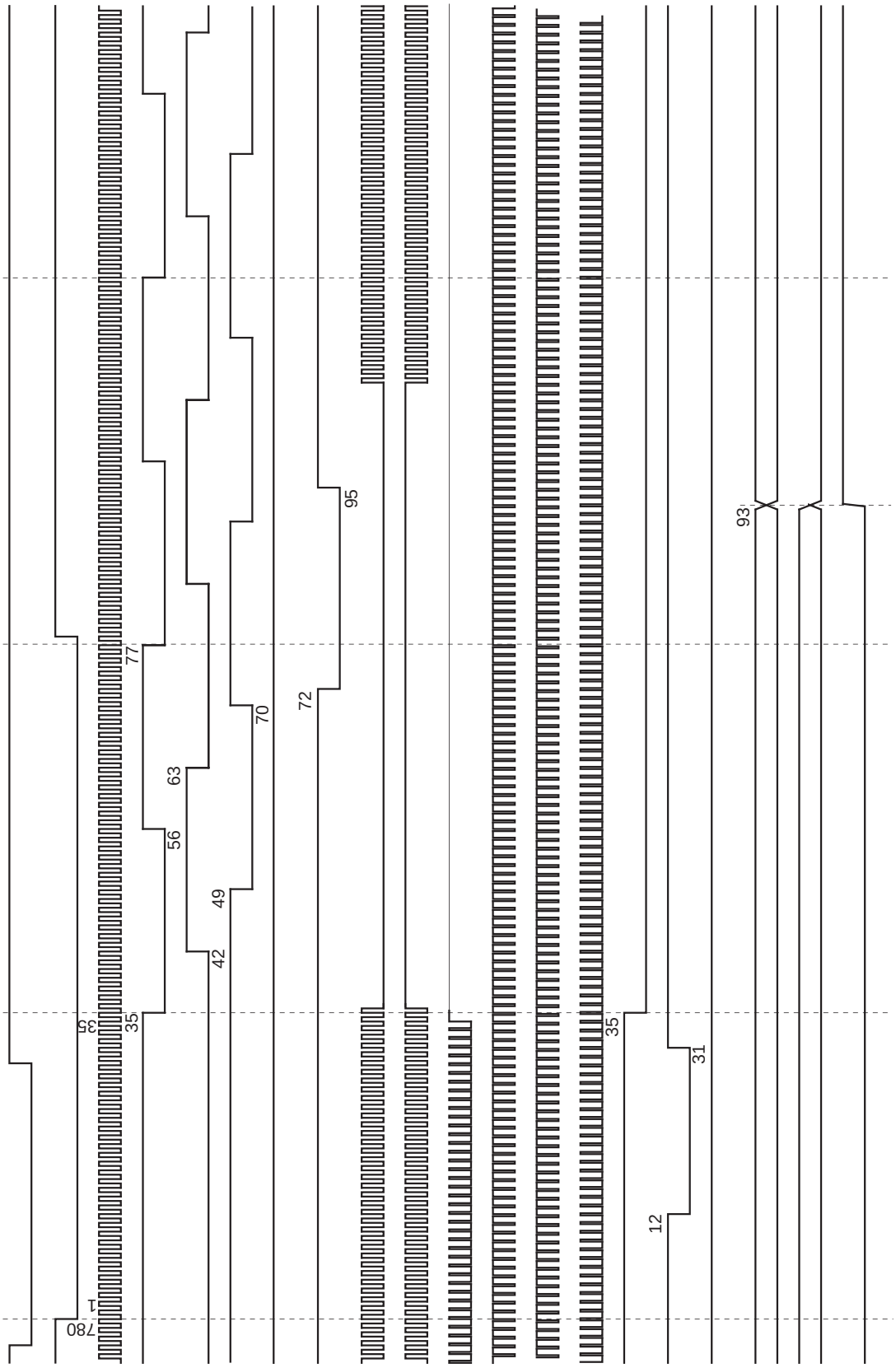


External Trigger Mode: high-speed electronic shutter, discharge (FSE=high, SMDE=high, SMD1=low, SMD2=high)

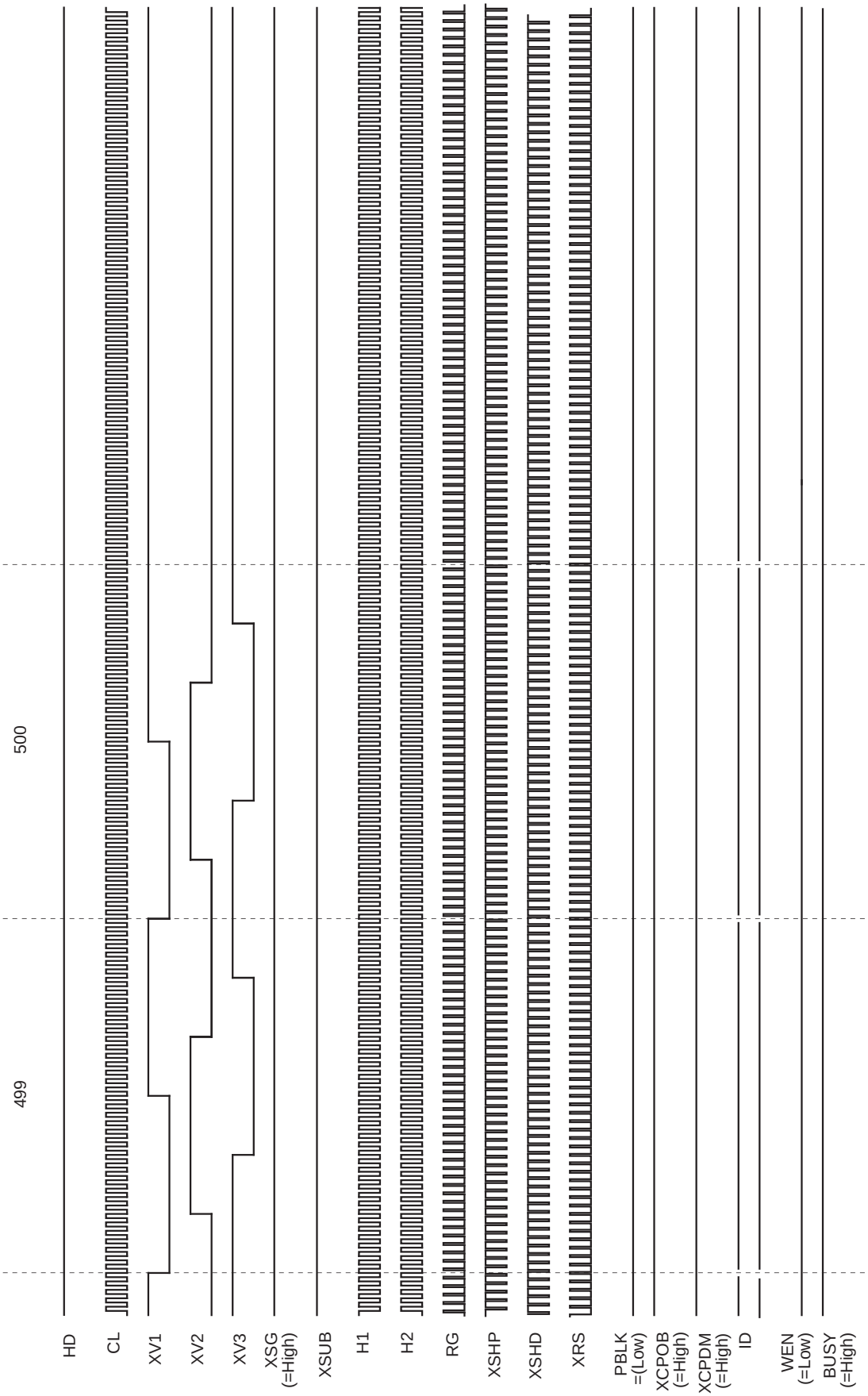


* See "3. Electronic Shutter" for the time from TRIG input to XSG.
* The fall of VD is invalid during the period while BUSY=high.

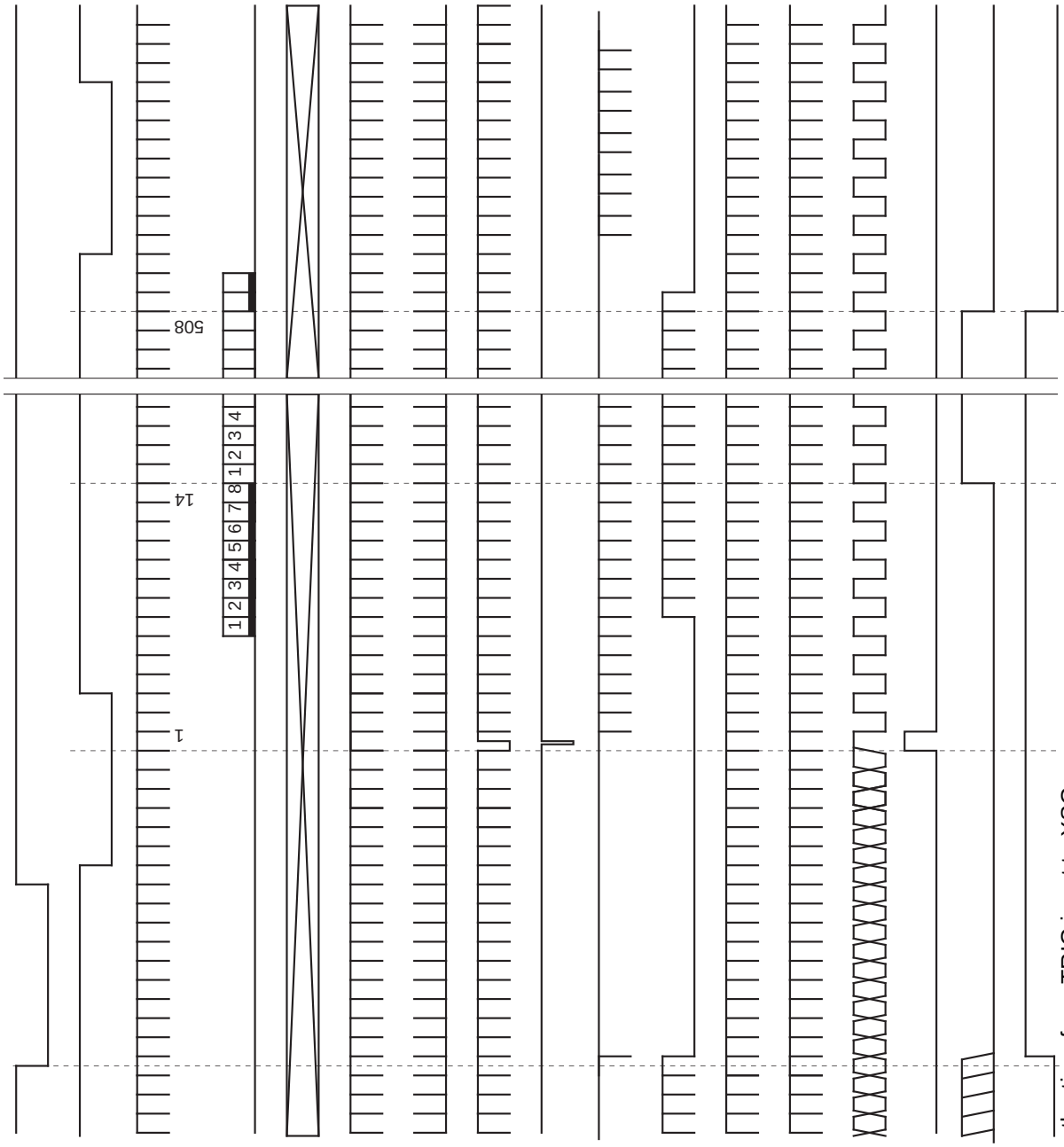
External Trigger Mode: high-speed electronic shutter, when discharge starts (FSE=high, SMD1=low, SMD2=high)



External Trigger Mode: high-speed electronic shutter, when discharge finishes (FSE=high, SMD1=low, SMD2=high)

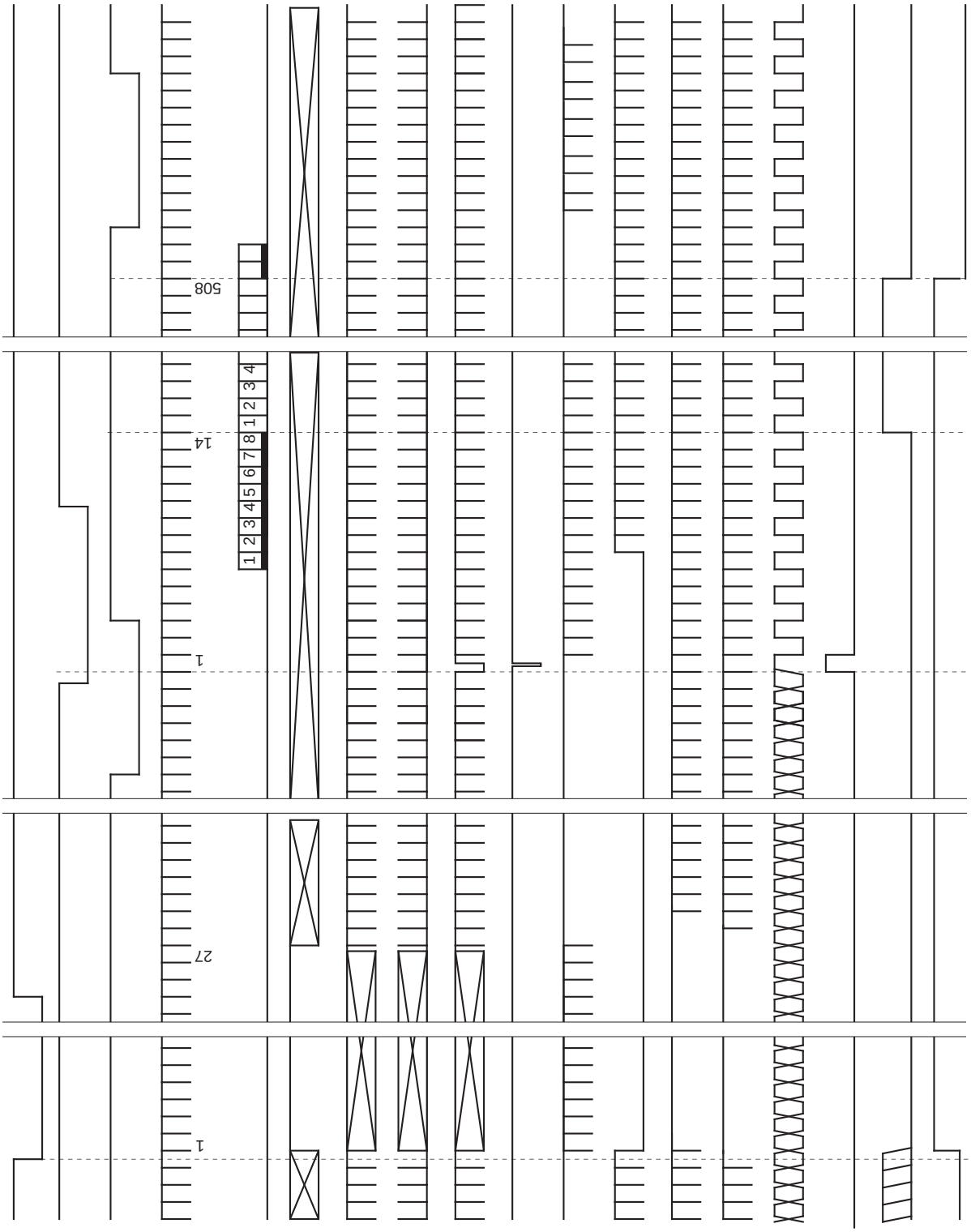


External Trigger Mode: high-speed electronic shutter, no discharge (FSE=low, SMDE=high, SMD1=low, SMD2=X)



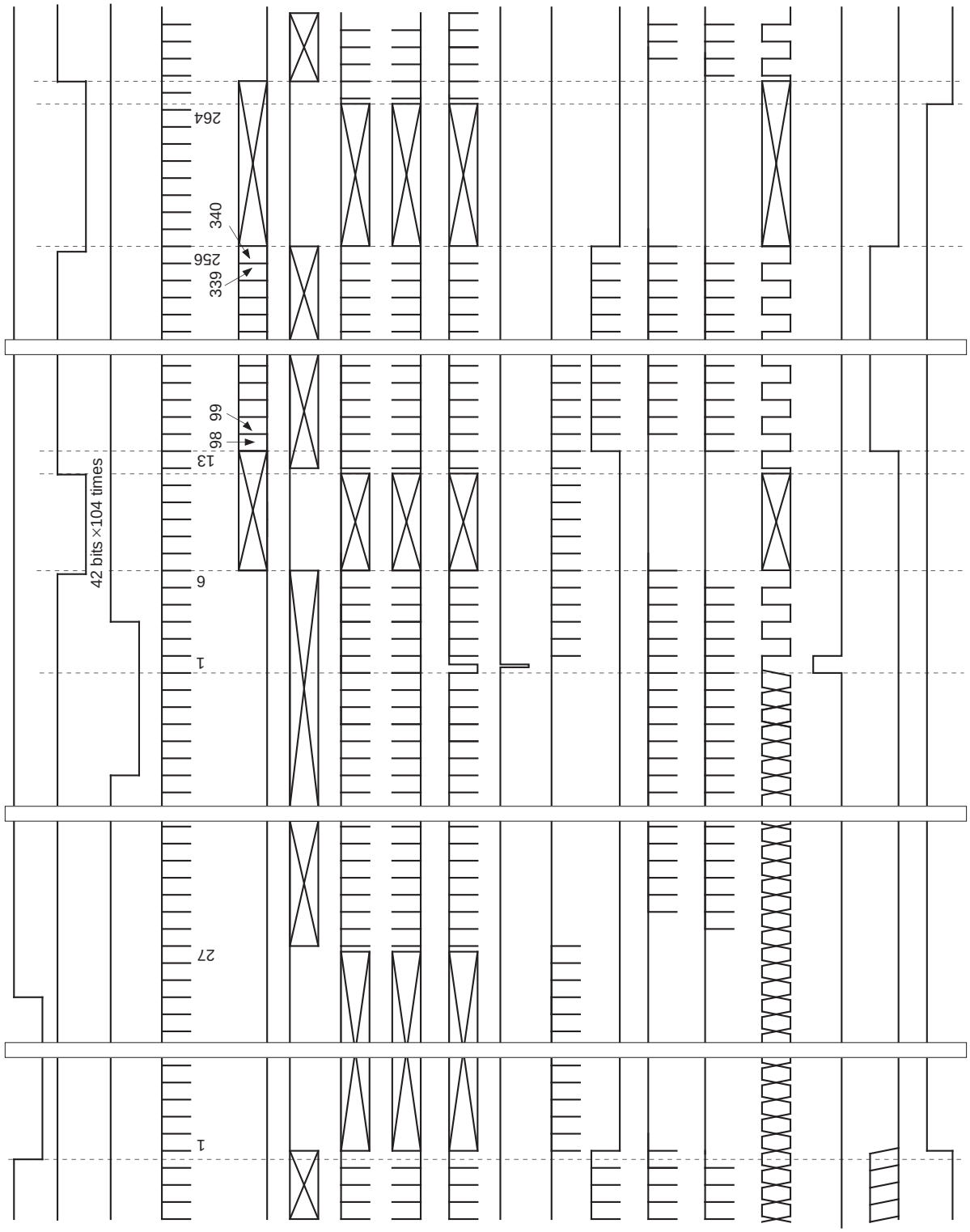
* See "3. Electronic Shutter" for the time from TRIG input to XSG.
* The fall of VD is invalid during the period while BUSY=high.

Example during ESG Input (FSE=high, SMDE=low, SMD1=low, SMD2=X)



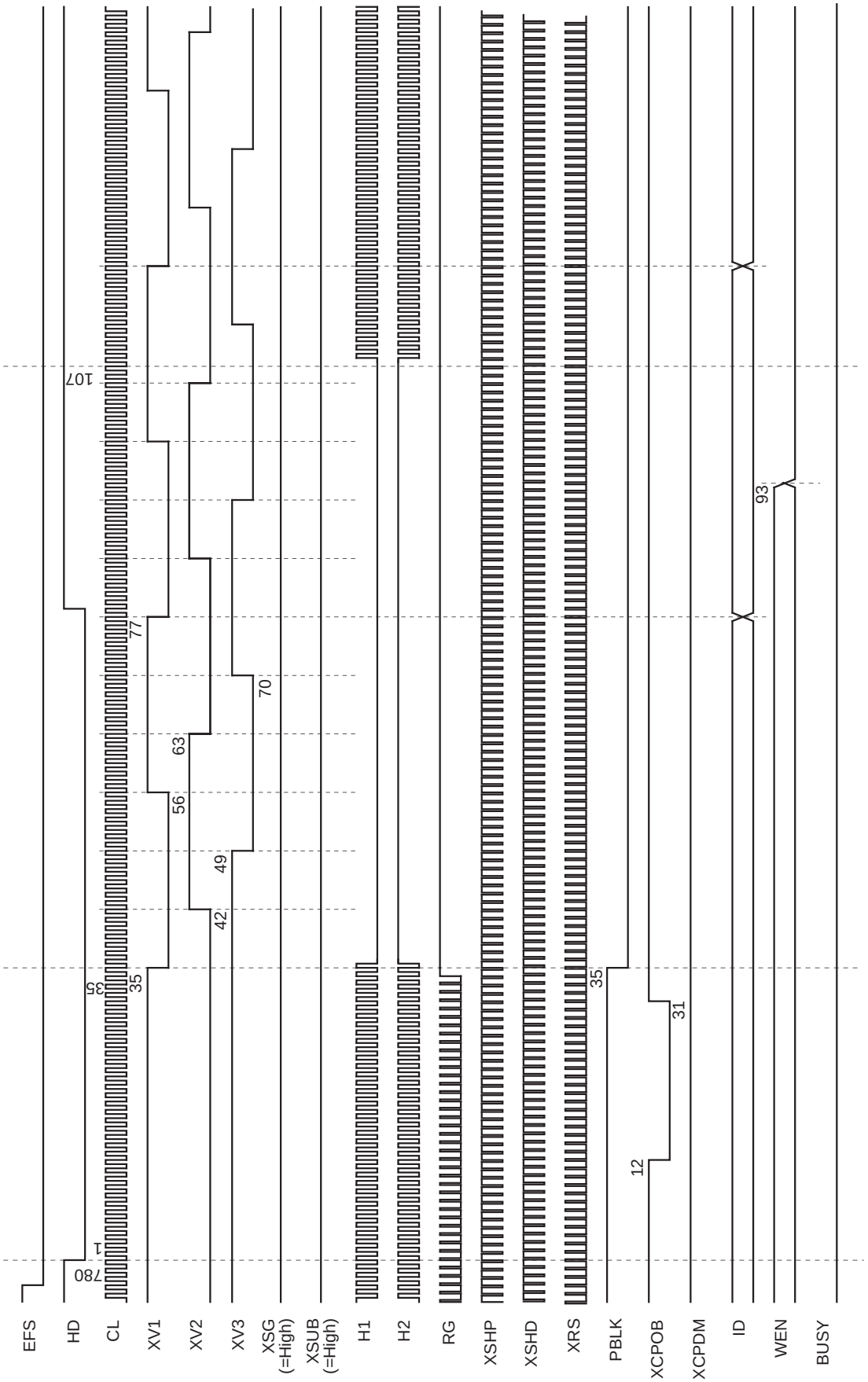
The fall of VD is invalid during the period while BUSY=high.

Example during EFS Input (trigger mode: FSE=high, SMDE=high, SMD1=low, SMD2=X)

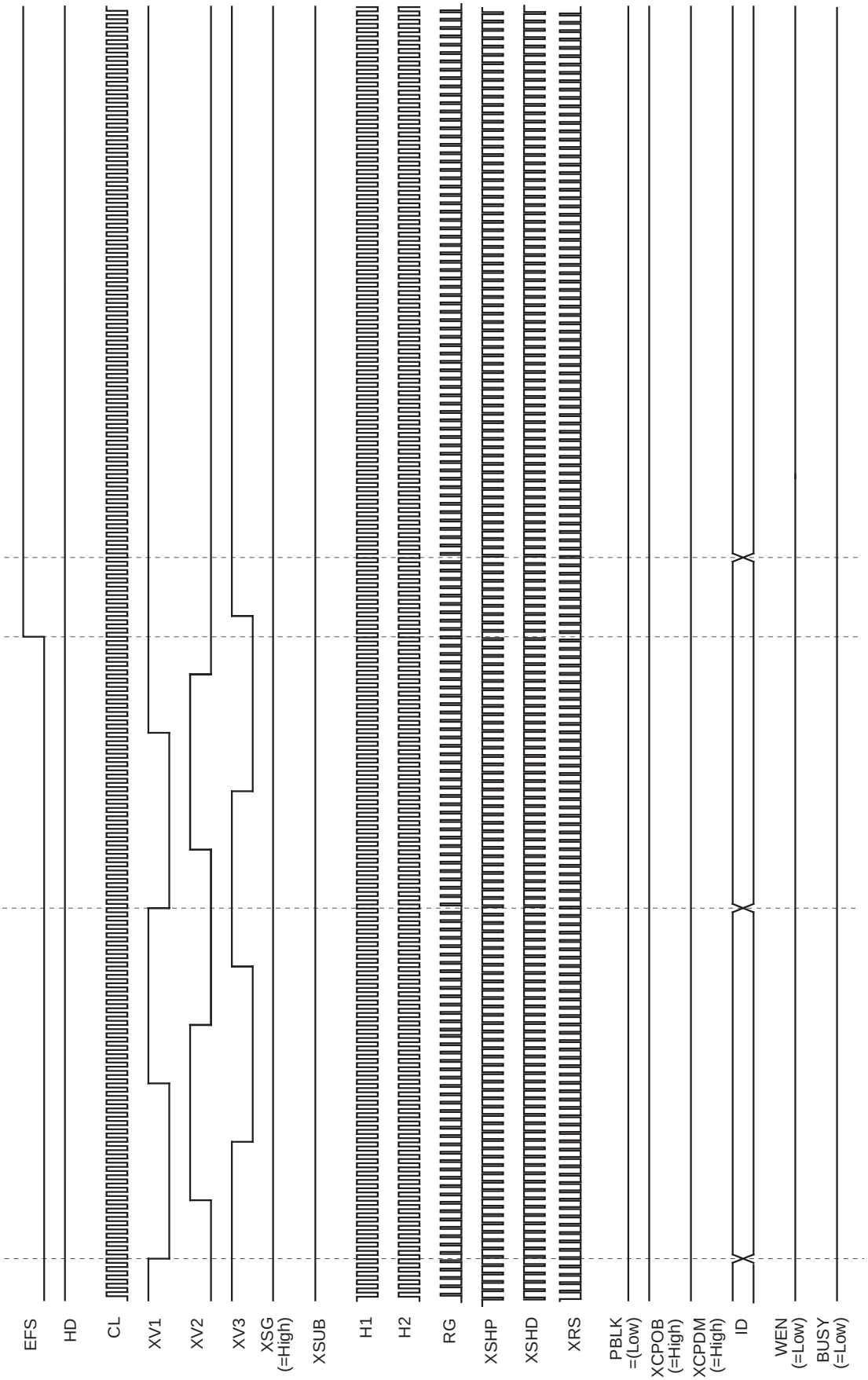


The fall of VD is invalid during the period while BUSY=high.

During EFS Input, when discharge starts

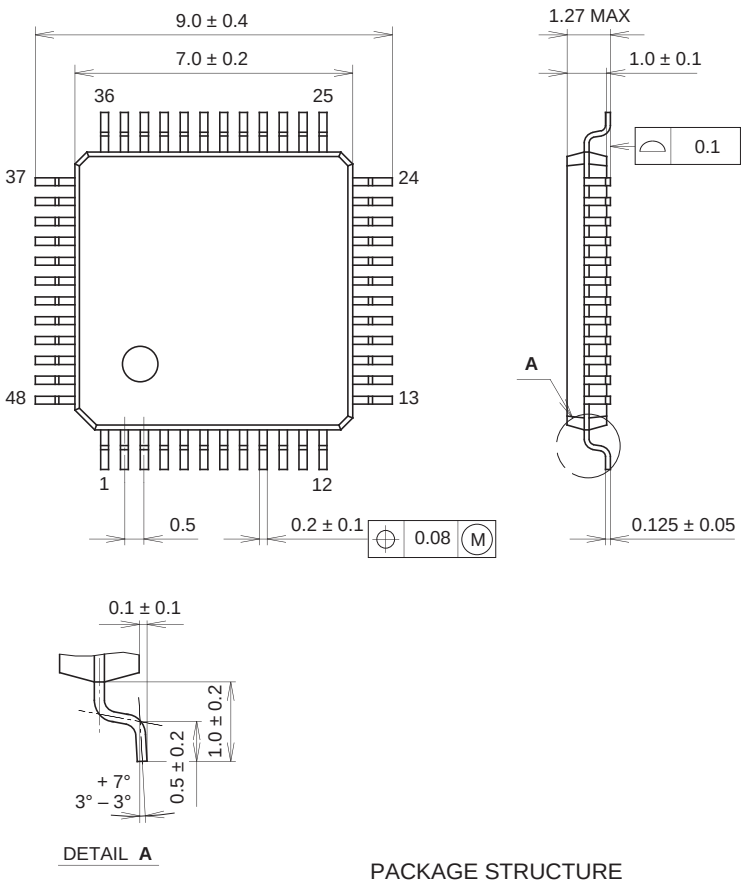


During EFS Input, when discharge finishes



Package Outline Unit : mm

48PIN TQFP (PLASTIC)



SONY CODE	TQFP-48P-L071
EIAJ CODE	TQFP048-P-0707-AN
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g