SONY

CXD2442Q

Timing Generator for LCD Panels

Description

The CXD2442Q is a timing signal generator for the SVGA LCD panel LCX016 and VGA LCD panel LCX012BL driver. This chip has a built-in serial interface circuit which supports various SVGA and VGA signals as well as double-speed NTSC and PAL signals through external control from a microcomputer, etc.

Features

- Generates the LCX016/LCX012BL drive pulse.
- Supports various SVGA and VGA signals. (LCX016/LCX012BL)

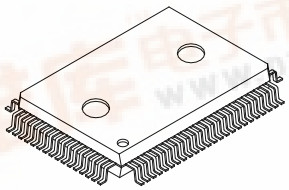
LCX016

- Aspect conversion performed at the panel side for the 832 × 624 (Macintosh17), 800 × 600 (SVGA), 640 × 480 (VGA/NTSC), 762 × 572 (PAL), 640 × 400 (PC-98), 832 × 480 (WIDE) modes.
- Line double-speed display realized with a built-in double-speed controller. (NTSC/PAL) (Line memory µPD485505: NEC)

LCX012BL

- 640 × 480 (VGA/NTSC/PAL)
- Line double-speed display realized with a built-in double-speed controller. (NTSC/PAL) (Line memory µPD485505: NEC)
- Supports double-speed PAL pulse eliminate.
- Supports SVGA pulse eliminate.
- Supports PC-98 (640 × 400) line display.
- Generates timing signal of external sample-and-hold circuit. (for RGB driver and high voltage drive sample and hold)
- Supports up/down and/or right/left inversion.
- Supports 1H inversion.
- AC drive of LCD panels during no signal

80 pin QFP (Plastic)



Applications

LCD projectors, etc.

Structure

Silicon CMOS IC

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

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"PC-98" is a registered trademark of NEC.
"VGA" is a registered trademark of IBM.
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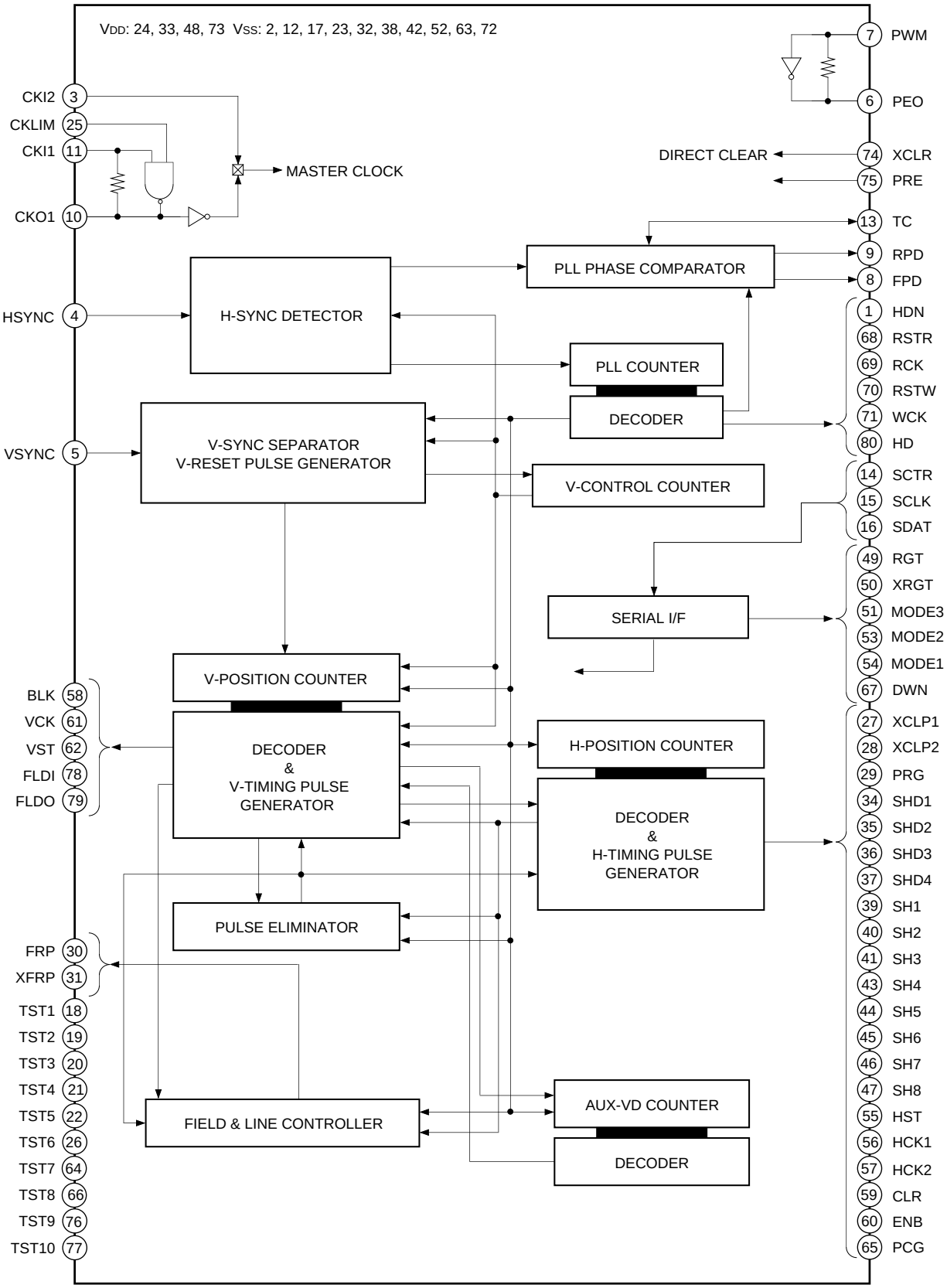
Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	HDN	O	Phase comparison pulse output	—
2	Vss	—	GND	—
3	CKI2	I	Clock input pin (SVGA, VGA)	—
4	HSYNC	I	Horizontal sync signal input pin	—
5	VSYNC	I	Vertical sync signal input pin	—
6	PEO	I/O	Loop filter integrator output pin (AV)	—
7	PWM	I	Loop filter integrator input pin (AV)	—
8	FPD	O	Phase comparator output pin (AV)	—
9	RPD	O	Phase comparator output pin (AV)	—
10	CKO1	I/O	Oscillation cell output pin (AV)	—
11	CKI1	I	Oscillation cell input pin (AV)	—
12	Vss	—	GND	—
13	TC	I/O	FPD output pulse width adjustment pin	—
14	SCTR	I	Chip select input pin (serial transfer block)	—
15	SCLK	I	Serial clock input pin (serial transfer block)	—
16	SDAT	I	Serial data input pin (serial transfer block)	—
17	Vss	—	GND	—
18	TST1	—	Test pin (Not connected.)	—
19	TST2	—	Test pin (Not connected.)	—
20	TST3	—	Test pin (Not connected.)	—
21	TST4	—	Test pin (Not connected.)	—
22	TST5	—	Test pin (Connect to GND.)	—
23	Vss	—	GND	—
24	V_{DD}	—	Power supply	—
25	CKLIM	I	CKI1 input limit pin (High: CKI1 input enabled, Low: Disabled)	H
26	TST6	—	Test pin (Not connected.)	—
27	XCLP1	O	Pedestal clamp pulse 1 output (negative polarity)	—
28	XCLP2	O	Pedestal clamp pulse 2 output (negative polarity)	—
29	PRG	O	Precharge signal pulse output (positive polarity)	—
30	FRP	O	AC drive inversion timing output	—
31	XFRP	O	AC drive inversion timing output (reverse polarity of FRP)	—
32	Vss	—	GND	—
33	V_{DD}	—	Power supply	—

Pin No.	Symbol	I/O	Description	Input pin for open status
34	SHD1	O	Sample-and-hold pulse 1 output (for driver/positive polarity)	—
35	SHD2	O	Sample-and-hold pulse 2 output (for driver/positive polarity)	—
36	SHD3	O	Sample-and-hold pulse 3 output (for driver/positive polarity)	—
37	SHD4	O	Sample-and-hold pulse 4 output (for driver/positive polarity)	—
38	Vss	—	GND	—
39	SH1	O	Sample-and-hold pulse 1 output (for high voltage drive sample and hold/positive polarity)	—
40	SH2	O	Sample-and-hold pulse 2 output (for high voltage drive sample and hold/positive polarity)	—
41	SH3	O	Sample-and-hold pulse 3 output (for high voltage drive sample and hold/positive polarity)	—
42	Vss	—	GND	—
43	SH4	O	Sample-and-hold pulse 4 output (for high voltage drive sample and hold/positive polarity)	—
44	SH5	O	Sample-and-hold pulse 5 output (for high voltage drive sample and hold/positive polarity)	—
45	SH6	O	Sample-and-hold pulse 6 output (for high voltage drive sample and hold/positive polarity)	—
46	SH7	O	Sample-and-hold pulse 7 output (for high voltage drive sample and hold/positive polarity)	—
47	SH8	O	Sample-and-hold pulse 8 output (for high voltage drive sample and hold/positive polarity)	—
48	V_{DD}	—	Power supply	—
49	RGT	O	Right/left inversion discrimination signal output (High: Right, Low: Left)	—
50	XRGT	O	Right/left inversion discrimination signal output (High: Left, Low: Right)	—
51	MODE3	O	Mode switching pin 3 output	—
52	Vss	—	GND	—
53	MODE2	O	Mode switching pin 2 output	—
54	MODE1	O	Mode switching pin 1 output	—
55	HST	O	H start pulse output	—
56	HCK1	O	H clock 1 pulse output	—
57	HCK2	O	H clock 2 pulse output	—
58	BLK	O	BLK pulse output (positive polarity)	—
59	CLR	O	CLR pulse output (positive polarity)	—
60	ENB	O	ENB pulse output (negative polarity)	—
61	VCK	O	V clock pulse output	—
62	VST	O	V start pulse output	—
63	Vss	—	GND	—
64	TST7	—	Test pin (Not connected.)	—
65	PCG	O	PCG pulse output (positive polarity)	—
66	TST8	—	Test pin (Not connected.)	—
67	DWN	O	Up/down inversion discrimination signal output (High: Down, Low: Up)	—

Pin No.	Symbol	I/O	Description	Input pin for open status
68	RSTR	O	Reset read output (for high-speed line buffer/negative polarity)	—
69	RCK	O	Read clock output (for high-speed line buffer)	—
70	RSTW	O	Reset write output (for high-speed line buffer/negative polarity)	—
71	WCK	O	Write clock output (for high-speed line buffer)	—
72	Vss	—	GND	—
73	V_{DD}	—	Power supply	—
74	XCLR	I	System clear pin (Low: All clear)	H
75	PRE	I	Preset pin (Preset to Macintosh17 mode when Low.)	H
76	TST9	—	Test pin (Not connected.)	—
77	TST10	—	Test pin (Not connected.)	—
78	FLDI	I	Field discrimination signal input	—
79	FLDO	O	Field discrimination signal output	—
80	HD	O	HD pulse output (positive polarity)	—

* H: Pull up, L: Pull down

Electrical Characteristics

1. DC characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to + 75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
Input, output voltages	V_I, Vo		Vss		V_{DD}	V	
Input voltage 1	V_{IH}	CMOS input	0.7V_{DD}			V	*1
	V_{IL}				0.3V_{DD}		
Input voltage 2	Vt+	TTL Schmitt trigger input	2.2			V	HSYNC VSYNC
	Vt–				0.8		
	Vt+ – Vt–			0.4			
Input voltage 3	Vt+	CMOS Schmitt trigger input	0.8V_{DD}			V	TC
	Vt–				0.2V_{DD}		
	Vt+ – Vt–			0.6			
Output voltage 1	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	*2
	V_{OL}	I_{OL} = 4mA			0.4		
Output voltage 2	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8			V	*3
	V_{OL}	I_{OL} = 8mA			0.4		
Output voltage 3	V_{OH}	I_{OH} = –3mA	V_{DD}/2			V	CKO1, PEO
	V_{OL}	I_{OL} = 3mA			V_{DD}/2		
Input leak current	I_I	*4	–10		10	µA	*5
	I_{IL}	*6	–40	–100	–240		*7
	I_I	*8	–40		40		*9
Output leak current	I_{OZ}	*10	–40		40	µA	*11
Current consumption	I_{DD}	*12			80	mA	At a 30pF load

*1 PRE, SCLK, SDAT, SCTR, XCLR, FLDI, CKLIM, CKI1, CKO1, CKI2, PWM, PEO

*2 MODE1, MODE2, MODE3, HD, HDN, CLR, ENB, PRG, PCG, HST, XCLP1, XCLP2, VST, BLK, FRP, XFRP, VCK, DWN, FLDO, FPD, TC, RPD, RGT, XRGT

*3 RSTR, RSTW, RCK, WCK, SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SHD1, SHD2, SHD3, SHD4, HCK1, HCK2

*4 Normal input pins (V_{IN} = V_{SS} or V_{DD})

*5 HSYNC, VSYNC, SCLK, SDAT, SCTR, CKI2

*6 Pins with pull-up resistors (V_{IN} = V_{SS})

*7 PRE, XCLR, CKLIM

*8 Bi-directional pins (input status, V_{IN} = V_{SS} or V_{DD})

*9 CKO1, PEO, TC

*10 At high impedance (V_{IN} = V_{SS} or V_{DD})

*11 RPD, FPD

*12 fclk = 60MHz, V_{DD} = 5.5V

2. AC characteristics (V_{DD} = 5.0 ± 0.5V, Vss = 0V, Topr = –20 to +75°C)

Item	Symbol	Applicable pins	Min.	Typ.	Max.	Conditions	Unit
Clock input cycle		CKI1	28.5				ns
		CKI2	16.6				
Output rise time	tr	All outputs			20	CL = 30pF	
Output fall time	tf	All outputs			20	CL = 30pF	
Cross-point time difference	Δt	HCK1, 2	–10		10	CL = 30pF	
Output rise delay time	tpr	All outputs			15	CL = 30pF	
Output fall delay time	tpf	All outputs			15	CL = 30pF	
HCK1 Duty	$t_H/(t_H + t_L)$	HCK1	48		52	CL = 30pF	%
HCK2 Duty	$t_L/(t_H + t_L)$	HCK2	48		52	CL = 30pF	

Note) SHP6, 5, 4, 3, 2, 1, 0: LLLLLLL (LSB), HDN4, 3, 2, 1, 0: LLLLL (LSB), SHD2, 1, 0: HHH (LSB), SH2, 1, 0: HLH (LSB)
The minimum value for the clock input cycle (CKI2) differs according to the mode used.

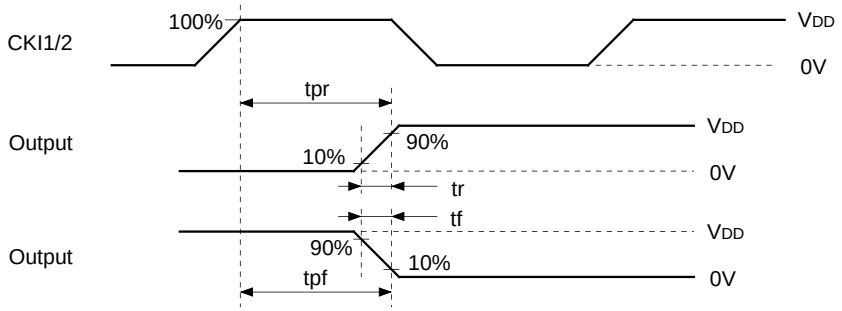
3. Serial transfer AC characteristics (V_{DD} = 5.0 ± 0.5V, Vss = 0V, Topr = –20 to +75°C)

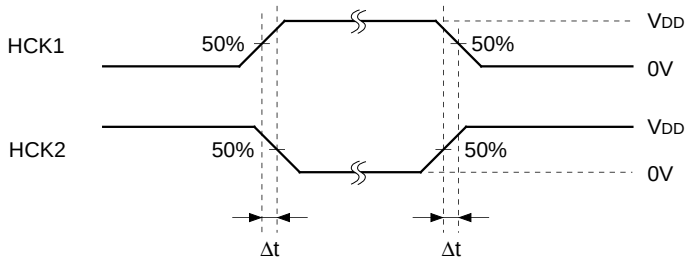
Symbol	Item	Min.	Typ.	Max.
ts0	SCTR setup time with respect to rise of SCLK	4Tns		
ts1	SDAT setup time with respect to rise of SCLK	2Tns		
th0	SCTR hold time with respect to rise of SCLK	4Tns		
th1	SDAT hold time with respect to rise of SCLK	2Tns		
tw1L	SCLK pulse width	2Tns		
tw1H	SCLK pulse width	2Tns		
tw2		5Tns		
tw3		5Tns		

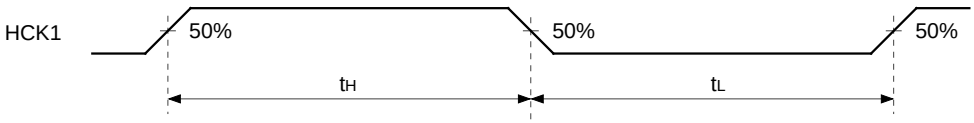
T: Master clock cycle (ns)

4. Timing definitions

AC characteristics

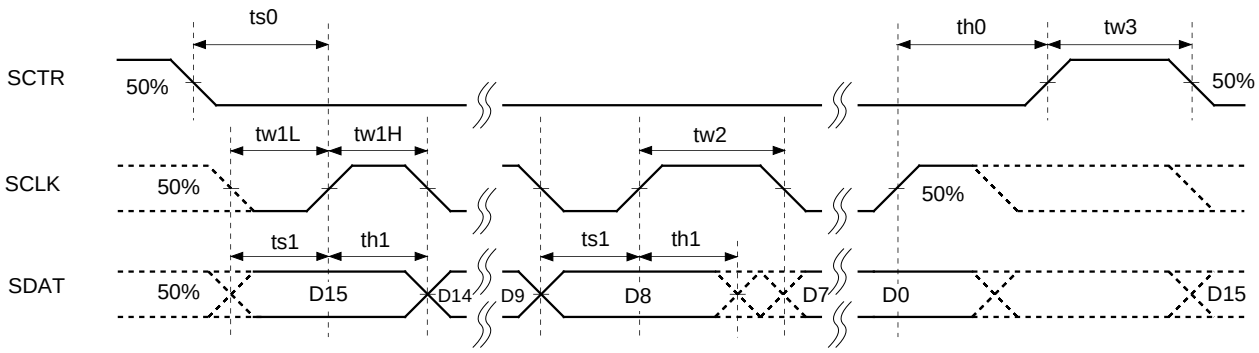






Note) HCK2 is the reverse phase of HCK1.

Serial transfer AC characteristics

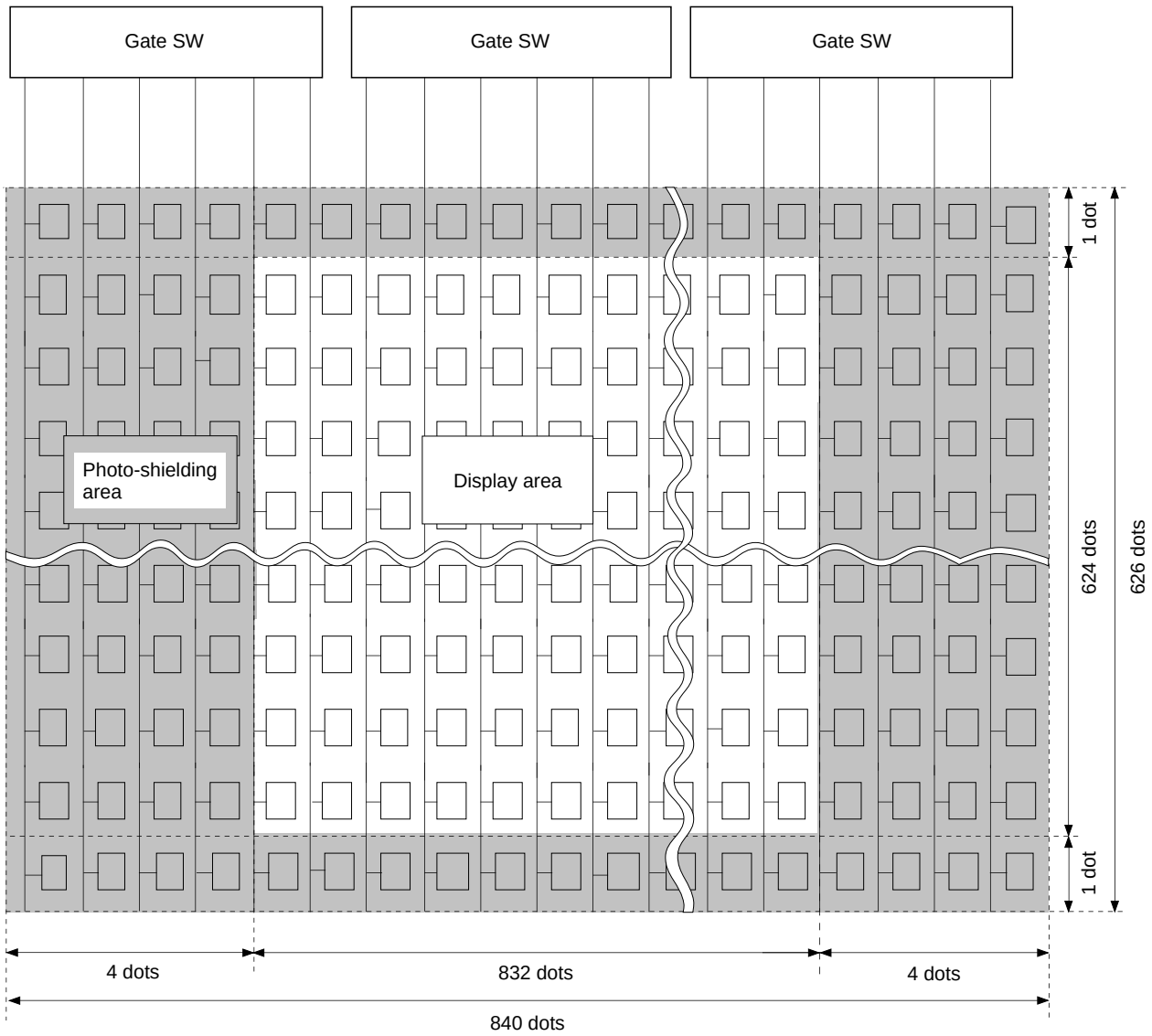


Note) See "Serial transfer timing" on P. 14 for the timing relationship between D15 to D0 and each pulse.

Dot Arrangement

The LCD panels supported by the CXD2442Q are the LCX016 and the LCX012BL. The dot arrangement is a square arrangement for both panels. The shaded region in the diagram is not displayed, however, for the LCX016, since the CXD2442Q has a built-in display area variable circuit, the number of display area dots varies according to the mode*1 to match the various signal protocols.

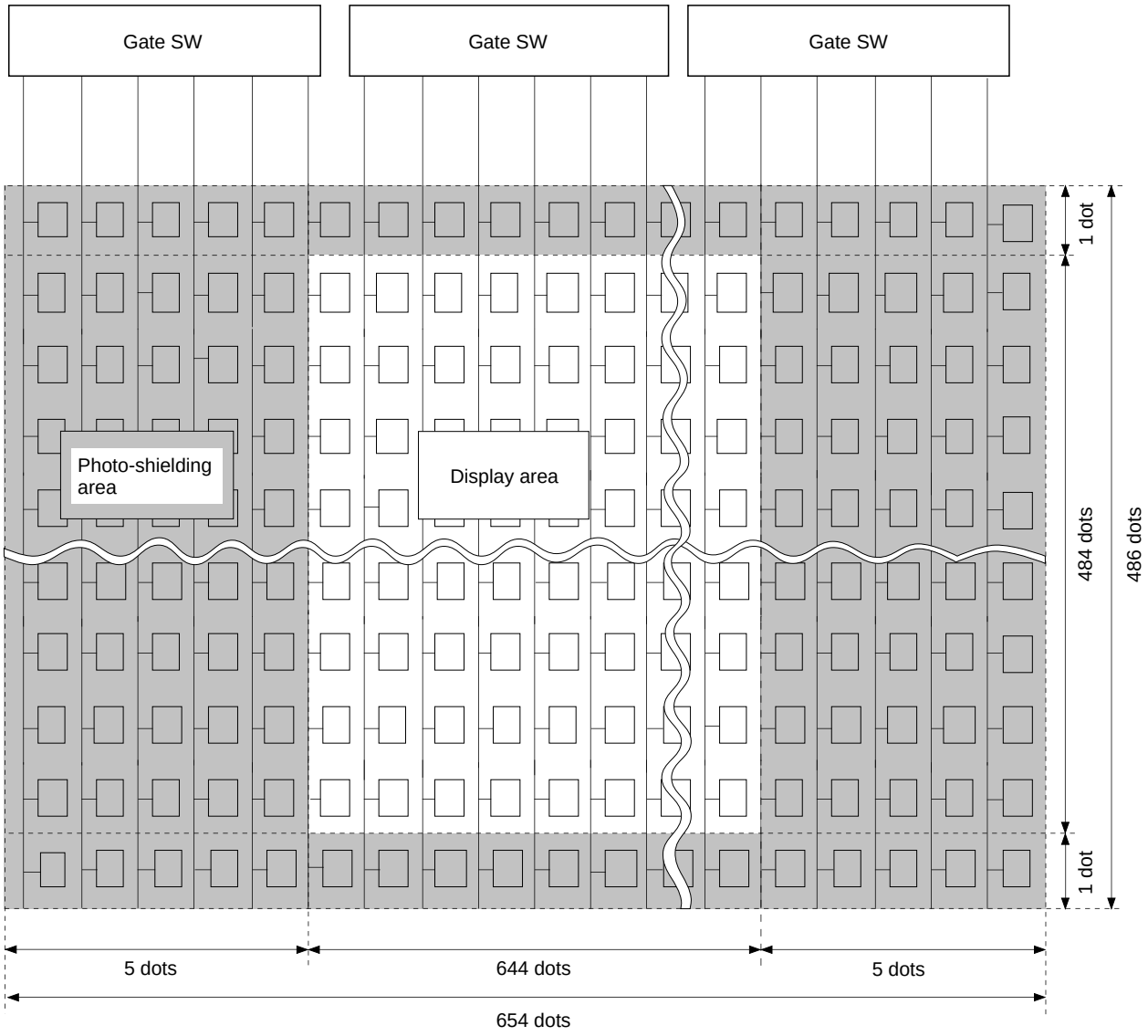
LCX016 Dot Arrangement



MODE1	MODE2	MODE3	Display mode	Number of horizontal display dots	Number of vertical display dots	Number of display dots
L	L	L	Macintosh17	832	624	519,168
L	L	H	SVGA	800	600	480,000
L	H	L	PAL	762	572	435,864
L	H	H	VGA/NTSC	640	480	307,200
H	L	L	PC-98	640	400	256,000
H	L	H	WIDE	832	480	399,360

*1 See the description of serial data specifications for details. Unit: dot

LCX012BL Dot Arrangement



Number of horizontal display dots	Number of vertical display dots	Number of display dots
644	484	311,696

Unit: dot

Input Signal Protocol

1. Horizontal sync signal

a) A standard signal (HSYNC) should be input for the following display modes.

LCX016: Macintosh17 (832 × 624), SVGA (800 × 600), VGA/NTSC (640 × 480), PC-98 (640 × 400), PAL (762 × 572), WIDE (832 × 480)

LCX012BL: VGA/NTSC/PAL (640 × 480), PC-98 (640 × 400)

However, since the CXD2442Q must be combined with a double-speed scan converter (CXD2428Q) for NTSC/PAL double-speed display when not using the built-in double-speed controller, a double-speed (see the CXD2428Q double-speed specifications), 1/2 cycle, 1/2 width horizontal sync signal (HSYNC) should be input as the standard protocol signal.

b) The input sync signal polarity is not fixed, and is set by the serial data (HPOL).

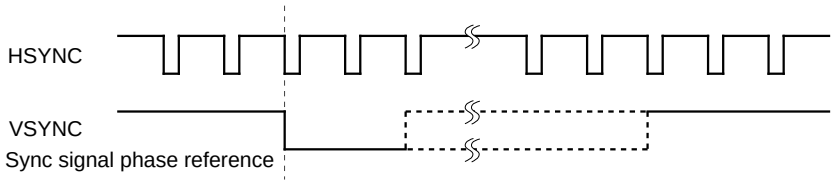
2. Vertical sync signal

a) A sync-separated, normal-speed VSYNC should be input as the vertical sync signal. However, CSYNC is also supported during NTSC/PAL display (when using the built-in double-speed controller) mode.

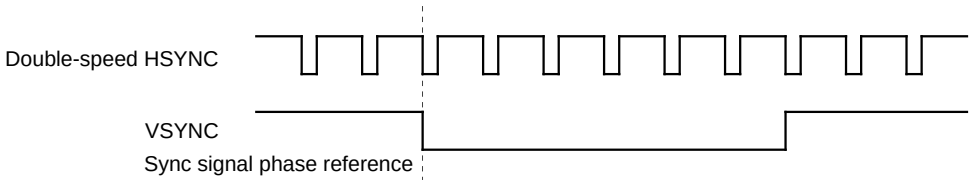
b) The input sync signal polarity is not fixed, and is set by the serial data (VPOL).

c) The phase relationship between HSYNC and VSYNC is specified as follows for the CXD2442Q.

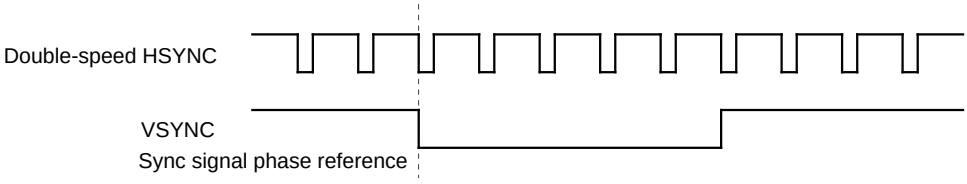
(1) Macintosh17, SVGA, VGA, PC-98, WIDE (LCX016)/VGA, PC-98 (LCX012BL)



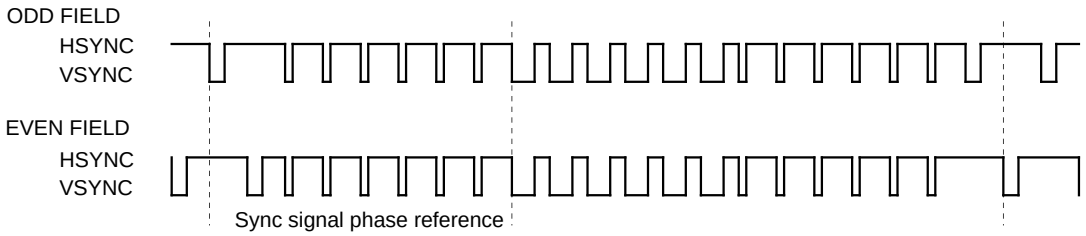
(2) Double-speed NTSC (LCX016/LCX012BL)



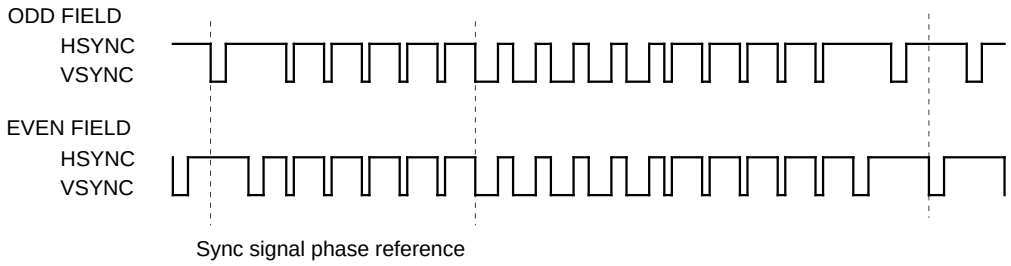
(3) Double-speed PAL (LCX016/LCX012BL)



(4) NTSC (LCX016/LCX012BL)



(5) PAL (LCX016/LCX012BL)



Notes) (2) and (3) show the timing when using a double-speed scan converter (CXD2428Q).
(4) and (5) show the timing when using the built-in double-speed controller (CXD2442Q) and a line memory (µPD485505: NEC)

Description of Operation

Sync signal input

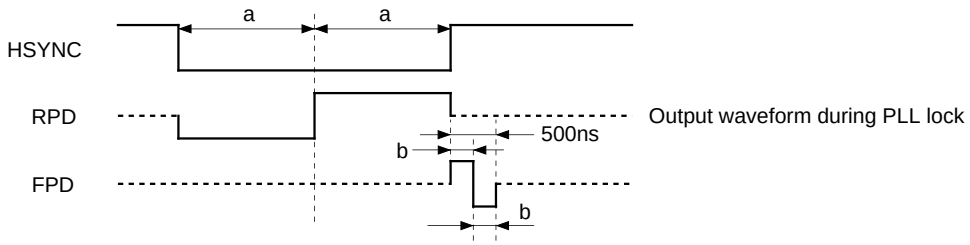
The HSYNC and VSYNC input pins support both separate SYNC and CSYNC. When using the CXD2442Q with CSYNC input, input CSYNC to both pins. (However, CSYNC input is supported only when using the built-in double-speed controller.)

Clock input

The CXD2442Q has two clock input pin systems to support two types of PLL circuits

(1) CKI1 pin

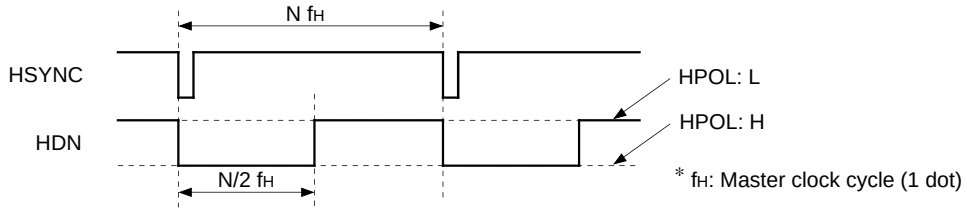
A PLL circuit is comprised by the built-in phase comparator and an external VCO circuit. CKI1 is the clock input pin when using this system, and supports the NTSC and PAL double-speed display modes (systems which use the built-in double-speed controller). The PLL clock for this system is adjusted by setting the RPD and FPD transition points so that they fall at the center of the windows as shown in the diagram below. (See the Application Circuit.)



(2) CKI2 pin

This is the clock input pin when using an external PLL IC. The 1/N frequency divider output is output from the HDN pin for the PLL IC. The HDN polarity at this time is set by the serial data HPOL.

The HDN width is calculated using the frequency division ratio N/2.



AC driving of LCD panels for no signal

The following measures have been adopted to allow AC driving of LCD panels even when there is no signal.

Horizontal direction pulse

The PLL is set to free running status. Therefore, the frequency of the horizontal direction pulse is dependent on the PLL free running frequency.

Vertical direction pulse

The number of lines is counted by an internal counter (AUX-VD COUNTER) and the vertical direction pulses (VST, FRP) are output at a specified cycle. For the CXD2442Q, no signal (free running) status is judged if there is no VSYNC input for longer than the following (free running detection) periods.

Mode	V cycle for no signal	Free running detection
NTSC	263H	468H
PAL	313H	
Other	650H	900H

Note) NTSC and PAL modes are the modes when using the built-in double-speed controller.

XCLR pin

The CXD2442Q should be forcibly reset during power on in order to initialize the serial transfer block and other internal circuits.

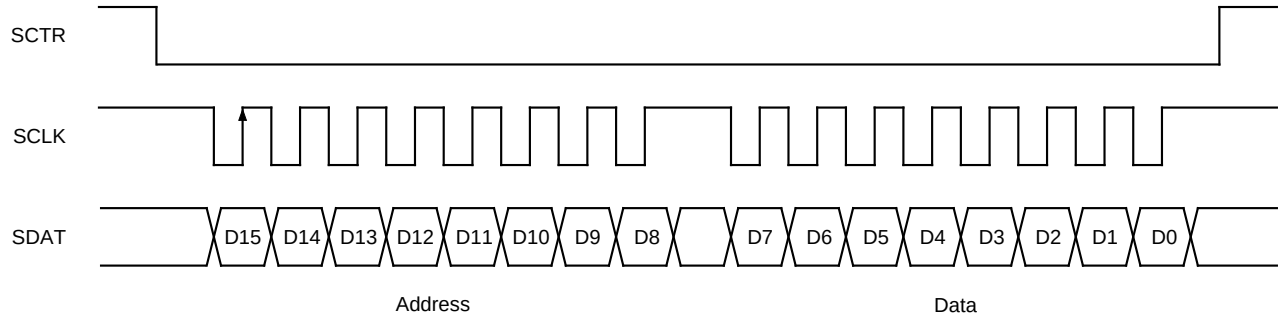
Serial transfer operation

1. Control method

The CXD2442Q operation timing is controlled by serial data.

The control data is comprised of an 8-bit address and 8-bit data, and the individual data is fetched at the rise of SCLK. This fetching operation starts from the fall of SCTR and is completed at the next rise of SCTR.

Serial Transfer Timing



2. Control data

When using the CXD2442Q, set the control data corresponding to each signal source according to the formats in the table below.

Address								Data								Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	—	—	—	—	—	PLLP10	PLLP9	PLLP8	(A) PLL frequency division ratio (1/N)
0	0	0	0	0	0	0	1	PLLP7	PLLP6	PLLP5	PLLP4	PLLP3	PLLP2	PLLP1	PLLP0	
0	0	0	0	0	0	1	0	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	(B) H-POSITION
0	0	0	0	0	0	1	1	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	(C) V-POSITION
0	0	0	0	0	1	0	0	—	—	—	HDNP4	HDNP3	HDNP2	HDNP1	HDNP0	(D) HDN-POSITION
0	0	0	0	0	1	0	1	—	SHP6	SHP5	SHP4	SHP3	SHP2	SHP1	SHP0	(E) SH-POSITION
0	0	0	0	0	1	1	0	—	—	—	—	HCKP3	HCKP2	HCKP1	HCKP0	(F) HCK-POSITION
0	0	0	0	0	1	1	1	—	—	—	—	HSTP3	HSTP2	HSTP1	HSTP0	(G) HST-POSITION
0	0	0	0	1	0	0	0	—	—	—	—	—	—	CLPP1	CLPP0	(H) CLP-POSITION
0	0	0	0	1	0	0	1	—	—	—	—	—	SHD2	SHD1	SHD0	(I) Mode settings
0	0	0	0	1	0	1	0	—	—	—	—	—	SH2	SH1	SH0	
0	0	0	0	1	0	1	1	—	—	—	MBK2	MBK1	MBK0	MBKB	MBKA	
0	0	0	0	1	1	0	0	FRP1	FRP0	VPOL	HPOL	MODE	MODE3	MODE2	MODE1	
0	0	0	0	1	1	0	1	CK	HR	DWN	RGT	HST	PCG	DSP	PC98	
—	—	—	—	1	1	1	—	—	—	—	—	—	—	—	—	—

Note) PLLP0, HP0, VP0, HDNP0, SHP0, HCKP0, HSTP0, CLPP0: LSB

Each control data is described in detail below. (A) to (I)

(A) PLLP10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These bits set the frequency division ratio (master clock) of the internal 1/N frequency divider for the PLL. The data is 11 bits and the frequency division ratio can be set up to 2045. The actual frequency division ratio should be set as follows.

Number of dots for the horizontal period – 2 = Actual number of dots set

Examples of settings for major modes are shown below.

Examples using the LCX016

1) Macintosh17 (832 × 624)

PLLP setting value = 1152 (horizontal period) – 2 → 1150 (HLLLHHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	L	L	L	H	H	H	H	H	H	L

2) SVGA (800 × 600)

PLLP setting value = 1000 (horizontal period) – 2 → 998 (LHHHHHLLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	H	H	H	L	L	H	H	L

3) VGA (640 × 480)

PLLP setting value = 896 (horizontal period) – 2 → 894 (LHHLHHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	H	H	H	H	H	L

4) PC-98 (640 × 400)

PLLP setting value = 848 (horizontal period) – 2 → 846 (LHHLHLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	L	L	H	H	H	L

5) NTSC WIDE (832 × 480)

PLLP setting value = 1014 (horizontal period) – 2 → 1012 (LHHHHHHLHLL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	H	H	H	H	L	H	L	L

6) NTSC (640 × 480)

PLLP setting value = 1560 (horizontal period) – 2 → 1558 (HHLLLLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	L	L	L	L	H	L	H	H	L

7) PAL (762 × 572)

PLLP setting value = 1880 (horizontal period) – 2 → 1878 (HHHLHLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	H	L	H	L	H	L	H	H	L

Examples using the LCX012BL

1) VGA (640 × 480)
PLLP setting value = 896 (horizontal period) – 2 → 894 (LHHLHHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	H	H	H	H	H	L

2) PC-98 (640 × 400)
PLLP setting value = 848 (horizontal period) – 2 → 846 (LHHLHLLHHHL: LSB)

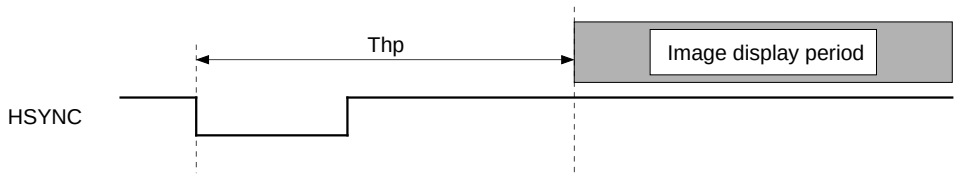
PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	L	L	H	H	H	L

3) NTSC, PAL (640 × 480)
PLLP setting value = 1560 (horizontal period) – 2 → 1558 (HHLLLLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	L	L	L	L	H	L	H	H	L

(B) HP7, 6, 5, 4, 3, 2, 1, 0

These bits set the horizontal display start position. The minimum adjustment width is 1 dot, and adjustment of up to 256 dots with 8 bits is possible using the front edge of HSYNC as the reference.



Thp: Timing from the edge of HSYNC to the start of image display

Minimum and maximum Thp setting values for each mode

LCX016

HP	7	6	5	4	3	2	1	0	832 × 624	800 × 600	762 × 572	640 × 480	640 × 400	832 × 480
Min.	H	H	H	H	H	H	H	H	185 dots	153 dots	105 dots			
Max.	L	L	L	L	L	L	L	L	440 dots	408 dots	360 dots			

LCX012BL

HP	7	6	5	4	3	2	1	0	644 × 484
Min.	H	H	H	H	H	H	H	H	110 dots
Max.	L	L	L	L	L	L	L	L	365 dots

(C) VP7, 6, 5, 4, 3, 2, 1, 0

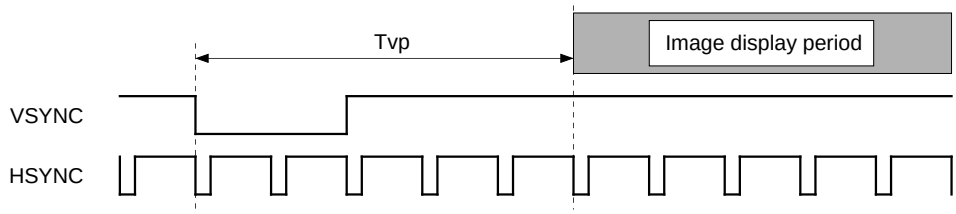
These bits set the vertical display start position. The minimum adjustment width is 1H, and adjustment of up to 256H with 8 bits is possible using the following references.

Non-interlace signal input → Front edge of VSYNC

Interlace signal input → First 1H of VSYNC

(Interlace signal input indicates NTSC or PAL double-speed display (using the built-in double-speed controller). In this case, the image is raised or lowered by two lines on the panel side with respect to a 1H adjustment.)

(1) Non-Interlace Mode



Tvp: Timing from the edge of VSYNC to the start of image display

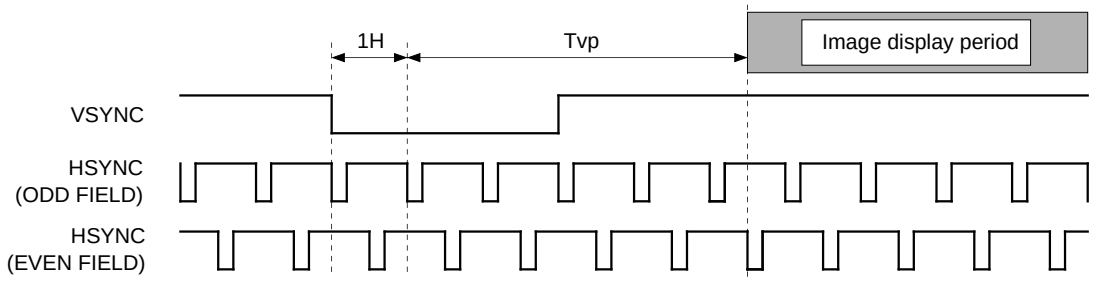
Minimum and maximum Tvp setting values

LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	Non-Interlace Mode
Min.	L	L	L	L	L	L	L	L	8H
Max.	H	H	H	H	H	H	H	H	263H

(2) Interlace Mode

(a) NTSC



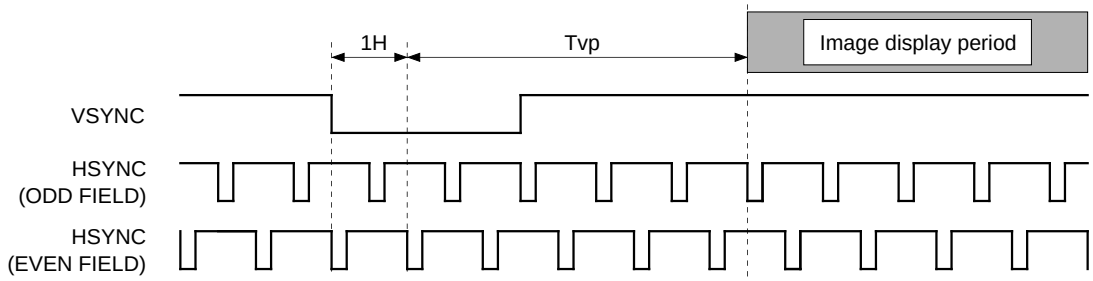
Tvp: Timing from the first 1H of the VSYNC edge to the start of image display

Minimum and maximum Tvp setting values

LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	Interlace Mode
Min.	L	L	L	L	L	L	L	L	4.5H
Max.	H	H	H	H	H	H	H	H	259.5H

(b) PAL



Tvp: Timing from the first 1H of the VSYNC edhe to the start of image display

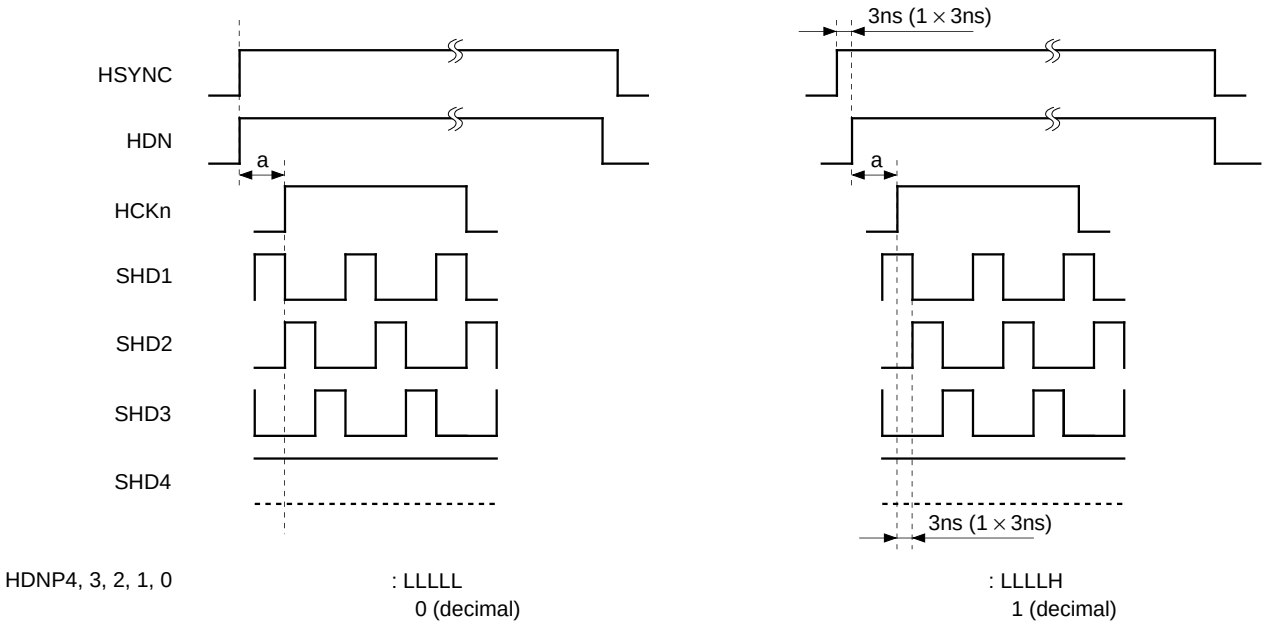
Minimum and maximum Tvp setting values

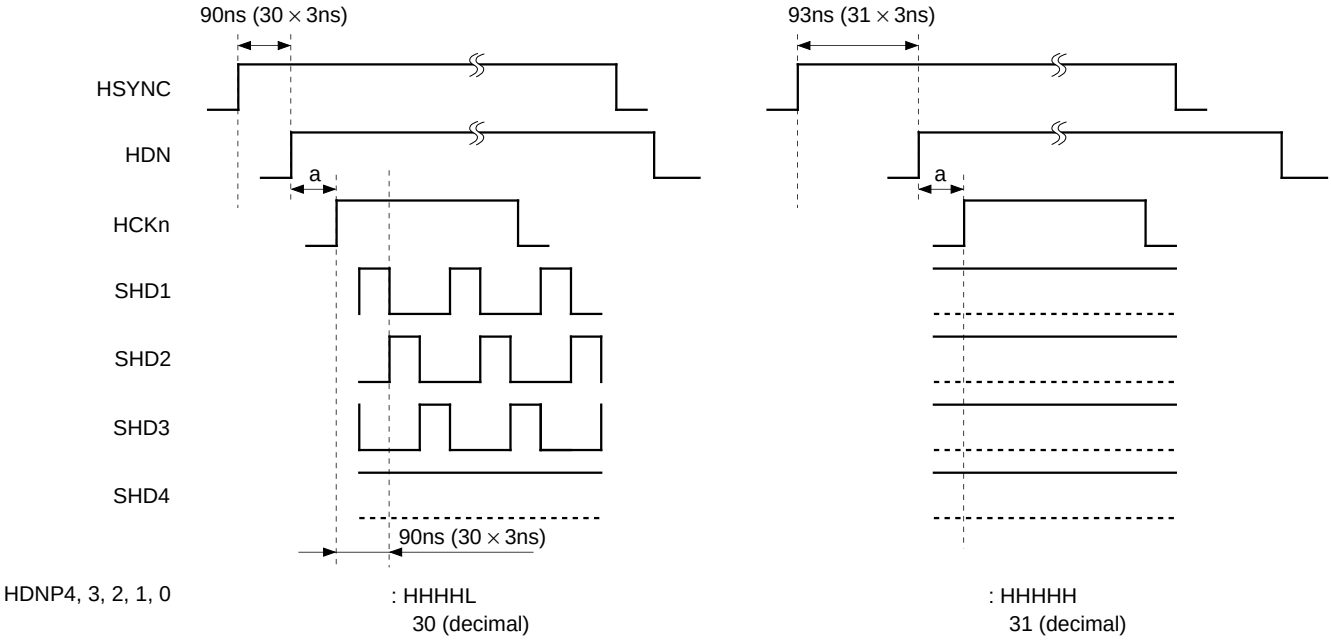
LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	Interlace Mode
Min.	L	L	L	L	L	L	L	L	4.5H
Max.	H	H	H	H	H	H	H	H	259.5H

(D) HDNP4, 3, 2, 1, 0

These bits set the timing for the phase comparison pulse HDN (for the external PLL IC). The phase relationship between the dot clock and the sync signal (HSYNC) is controlled in 3ns (Typ.) units. The control range is 32 positions with 5 bits.
Phase control for the SH pulse (SHD4, 3, 2, 1) is also performed at the same time.

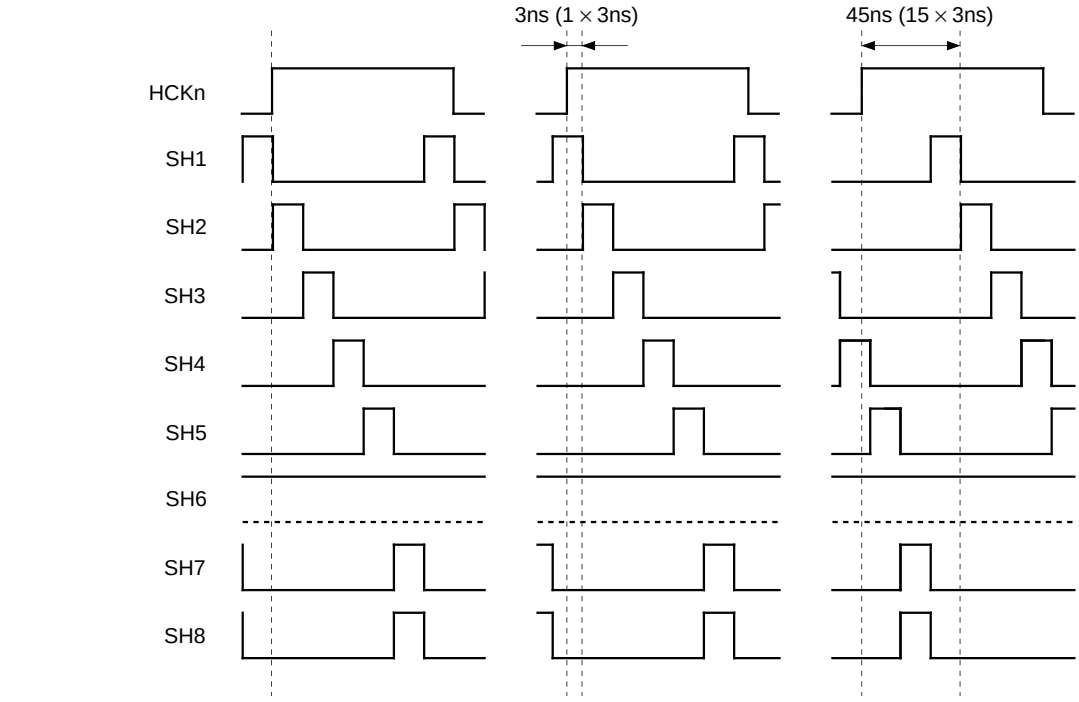


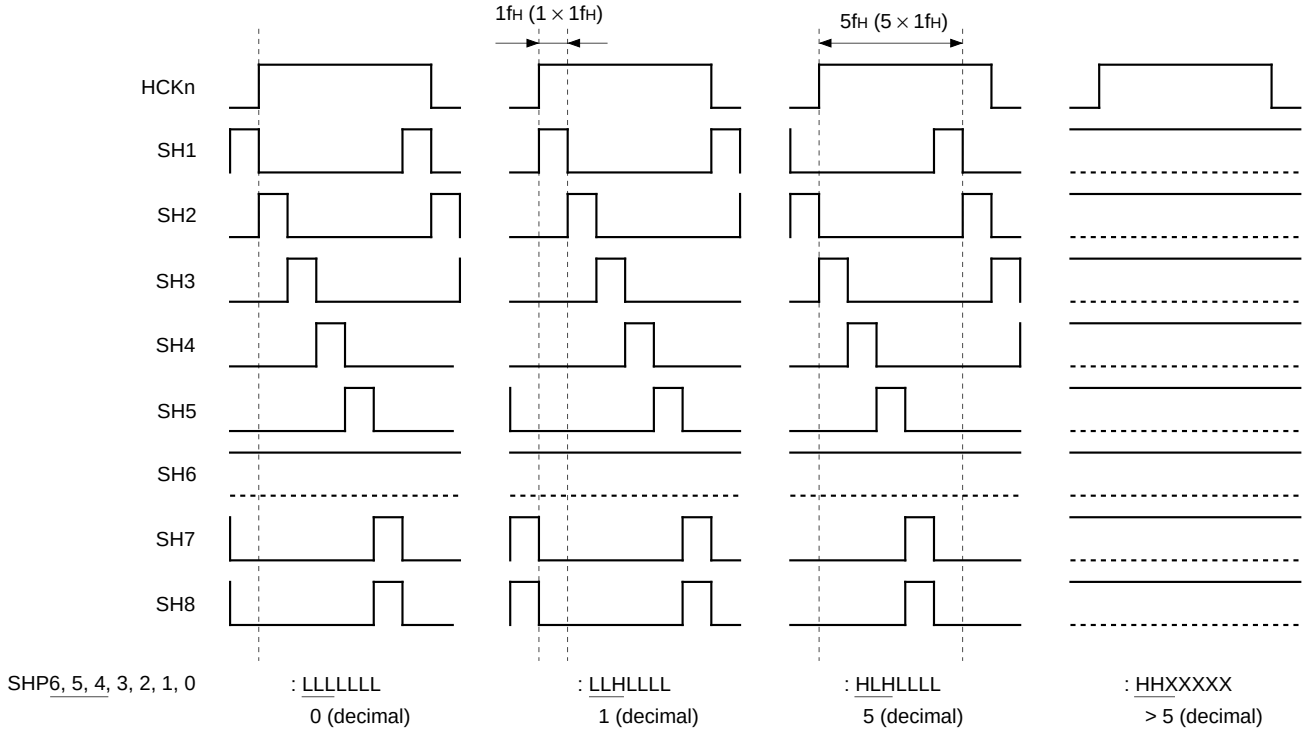


Note) The above timings assume SHD2, 1, 0: HHH and HPOL: H (serial data).
The value of a is constant regardless of the HDNP setting. n = 1, 2

(E) SHP6, 5, 4, 3, 2, 1, 0

These bits control the phase relationship between HCK1, HCK2 and SH1, 2, 3, 4, 5, 6, 7 and 8. The phase can be controlled in 1f_H units by the upper 3 bits (SHP6, 5, 4), and in 3ns (Typ.) units by the lower 4 bits (SHP3, 2, 1, 0).

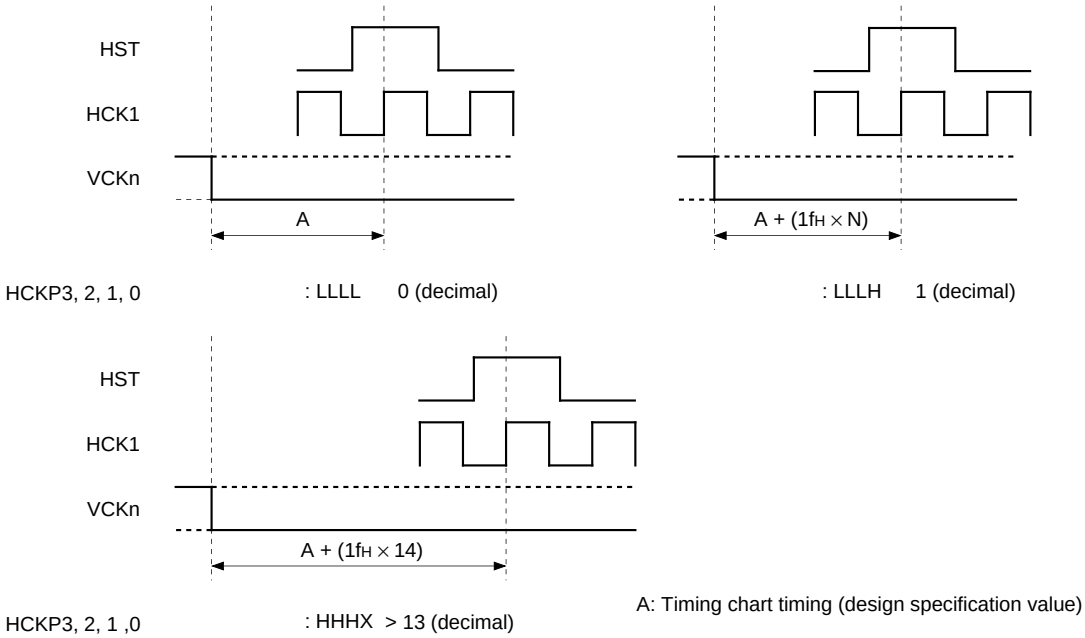




Note) The above timings assume SH2, 1, 0: HLH (serial data). n = 1, 2

(F) HCKP3, 2, 1, 0

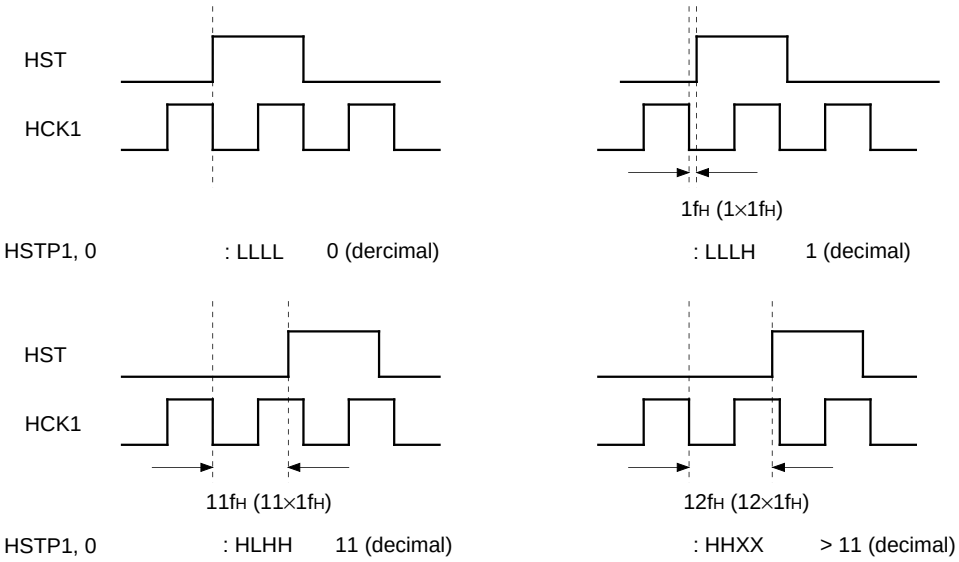
These bits control the phase relationship between the RGB signal and HCK (interlocked with HST) inside the panel, and compensate the HCK delay for the wiring load and scanner, etc. The phase can be controlled to 15 positions (1f_H increments) with 4 bits.



Note) Only HCK and HST are adjusted. The above timings assume HSTP3, 2, 1, 0: LLLH (serial data).

(G) HSTP3, 2, 1, 0

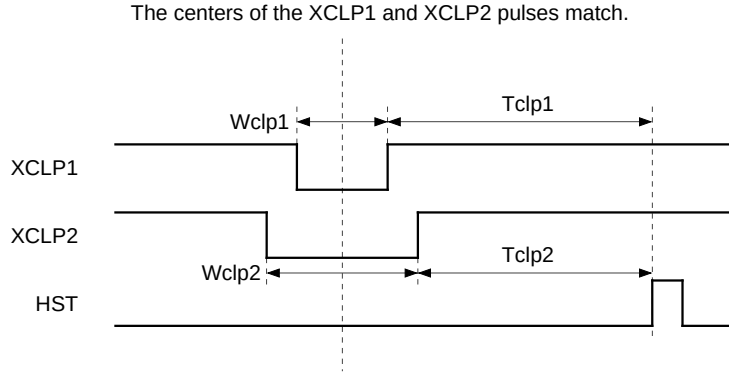
These bits control the phase relationship between HCK and HST inside the panel, and compensate the delay difference between HST and HCK for the wiring load and scanner, etc. The phase can be controlled to 12 positions (1f_H increments) with 4 bits.



Note) The above timings assume RGT: H. The HST polarity is inversed during SVGA (LCX016) mode.

(H) CLPP1, 0

These bits adjust the clamp pulse position. The timing can be set to 4 positions with 2 bits, and the adjustment width varies in accordance with each mode.



Macintosh17 (LCX016)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (HP7, 6, 5, 4, 3, 2, 1, 0)
L	L	46 dots	23 dots	69 dots	115 dots	HHHHHHHH (255) : LSB
L	H	69 dots	46 dots	69 dots	115 dots	
H	L	92 dots	69 dots	69 dots	115 dots	HHHHLLHH (243) : LSB
H	H	115 dots	92 dots	69 dots	115 dots	HHLHHHLL (220) : LSB

SVGA (LCX016)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (HP7, 6, 5, 4, 3, 2, 1, 0)
L	L	38 dots	19 dots	58 dots	96 dots	HHHHHHHH (255) : LSB
L	H	57 dots	38 dots	58 dots	96 dots	
H	L	76 dots	57 dots	58 dots	96 dots	HHHHLHHL (246) : LSB
H	H	95 dots	76 dots	58 dots	96 dots	HHHLLLHH (227) : LSB

VGA/NTSC, PAL, PC-98, WIDE (LCX016), VGA, NTSC, PAL (LCX012BL)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (HP7, 6, 5, 4, 3, 2, 1, 0)
L	L	26 dots	13 dots	38 dots	64 dots	HHHHHHHH (255) : LSB
L	H	39 dots	26 dots	38 dots	64 dots	
H	L	52 dots	39 dots	38 dots	64 dots	HHHHHLLL (248) : LSB
H	H	65 dots	52 dots	38 dots	64 dots	HHHLHLHH (235) : LSB

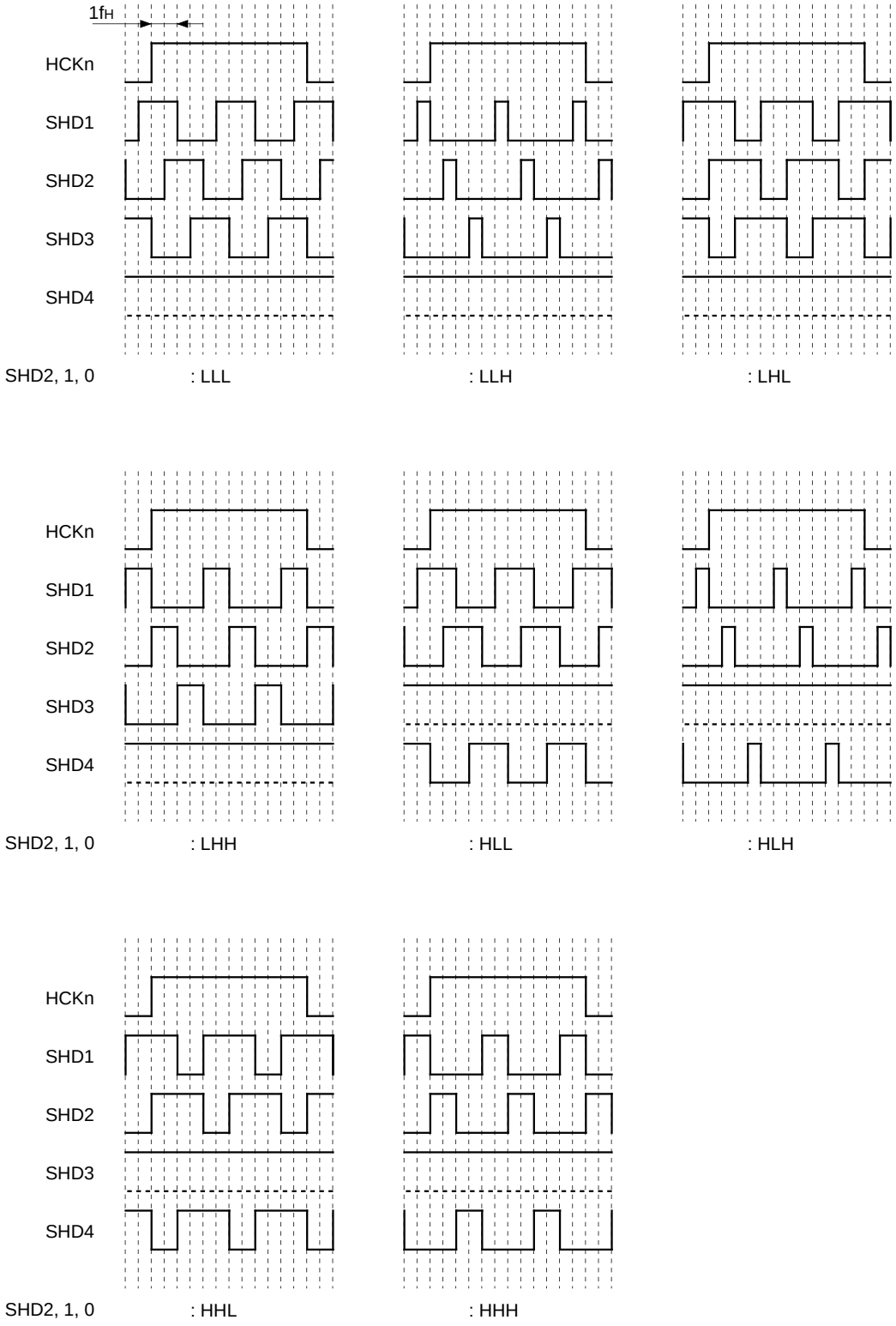
Note) When CLPP1, 0 is set to HL or HH (serial data), the XCLP pulse may not be output due to the internal logic depending on the HP serial data setting value. HP Limit is the upper limit for the serial data HP when setting each mode.

(I) Mode settings

Mode	Description	
SHD2	Resampling switching (High: Resampling, Low: No resampling)	I-1
SHD1	0.5 bit offset switching (High: No offset, Low: Offset)	
SHD0	Overlap switching (High: No overlap, Low: Overlap)	
SH2	0.5 bit offset switching (High: No offset, Low: Offset)	I-2
SH1	Overlap switching (High: Overlap, Low: No overlap)	
SH0	Overlap width switching (High: 2-dot overlap, Low: 3-dot)	
MBK2	Pulse eliminate (FRP) timing switching (High: Main, Low: Sub)	I-3
MBK1	Pulse eliminate mode switching (High: SVGA/6, 4 pulse eliminate, Low: PAL/6, 7 pulse eliminate)	
MBK0	Pulse eliminate switching (High: No pulse eliminate, Low: Pulse eliminate)	
MBKB	Pulse eliminate interval switching	
MBKA		
FRP1	FRP polarity inversion cycle switching (High: 1F, Low: 2F)	I-4
FRP0	FRP polarity inversion cycle switching (High: 1H, Low: F)	
VPOL	Input VSYNC polarity switching (High: Positive, Low: Negative)	I-5
HPOL	Input HSYNC polarity switching (High: Positive, Low: Negative)	
MODE	Mode switching (High: LCX016 mode, Low: LCX012BL mode)	I-6
MODE3	Panel display area switching signal input	I-7
MODE2		
MODE1		
CK	Input clock switching (High: CKI1, Low: CKI2)	I-8
HR	External reset switching (High: No reset, Low: Reset)	I-9
DWN	Up/down inversion discrimination signal input (High: Down, Low: Up)	I-10
RGT	Right/left inversion discrimination signal input (High: Right, Low: Left)	
HST	HST width switching (High: 12 dots wide, Low: 24 dots wide)	I-11
PCG	PCG width switching (High: Main, Low: Sub)	I-12
DSP	Double-speed mode switching (High: Normal, Low: Double-speed)	I-13
PC98	PC-98 (400-line) display switching (High: No display, Low: Display)	I-14

(I-1) SHD2, 1, 0

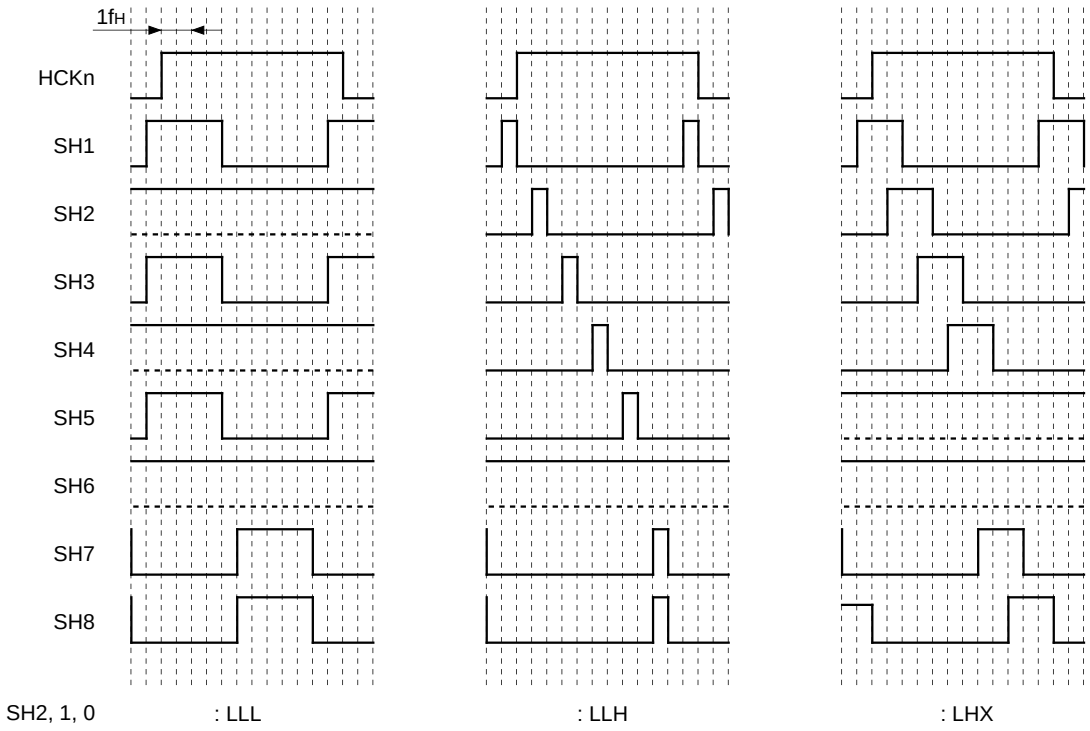
These bits set the sample-and-hold pulse (SHD) timing.
Set the timing in accordance with each display system.

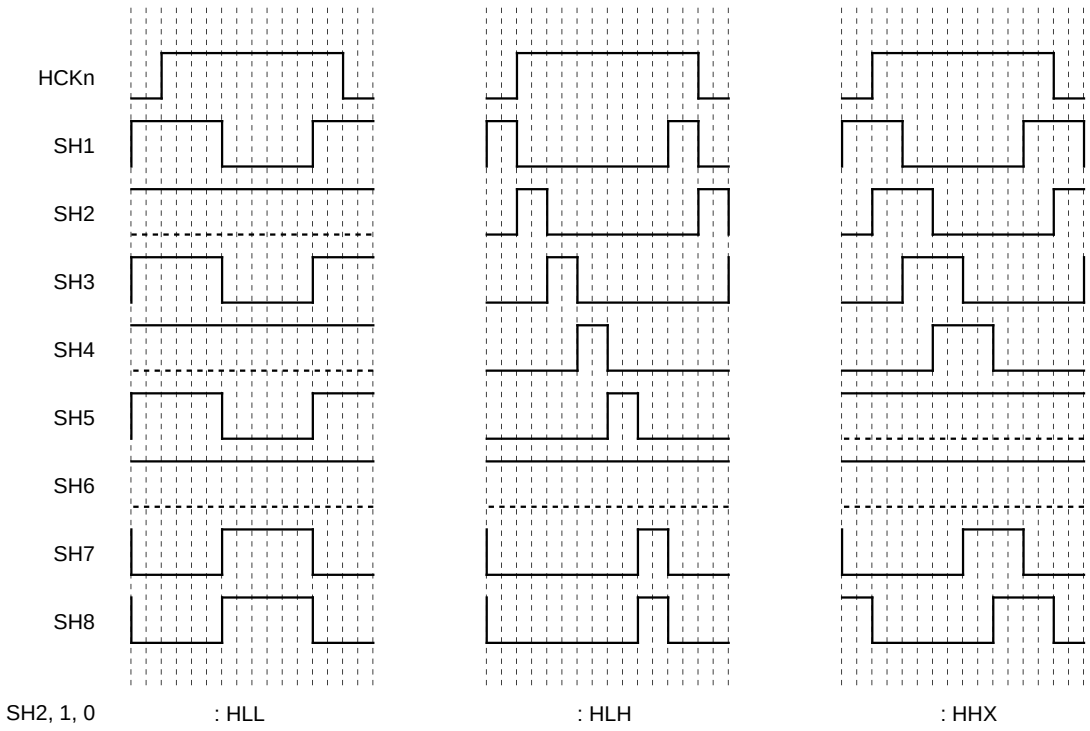


Note) The above timings assume HDN4, 3, 2, 1, 0: LLLLL (serial data). n = 1, 2

(I-2) SH2, 1, 0

These bits set the sample-and-hold pulse (SH) timing.
Set the timing in accordance with each display system.





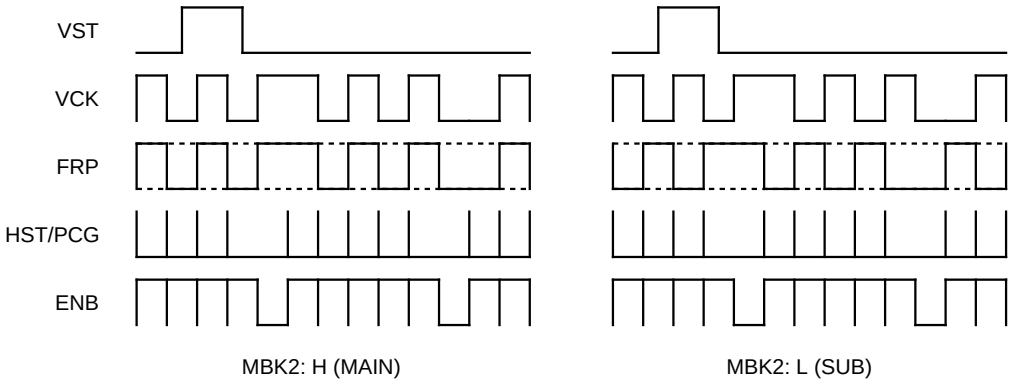
Note) The above timings assume SHP6, 5, 4, 3, 2, 1, 0: LLLLLLL (serial data). n = 1, 2

(I-3) MBK2, 1, 0, B, A

These bits set the pulse eliminate-related mode timings. These timings enable SVGA (scanning line conversion from 600 to 480 vertical lines by 6, 4 pulse eliminate) and double-speed PAL (scanning line conversion from 575 to 480 vertical lines by 6, 7 pulse eliminate) display for the LCX012BL. However, for SVGA display, the horizontal direction is supported by external signal processing.

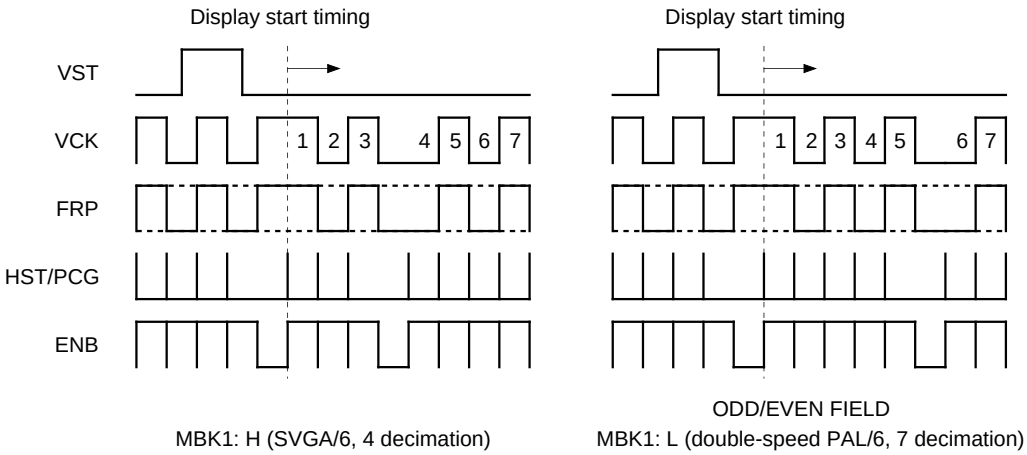
(1) MBK2

This bit sets the FRP-related pulse eliminate timing.



(2) MBK1

This bit sets the pulse eliminate mode. Select SVGA or double-speed PAL pulse eliminate mode.



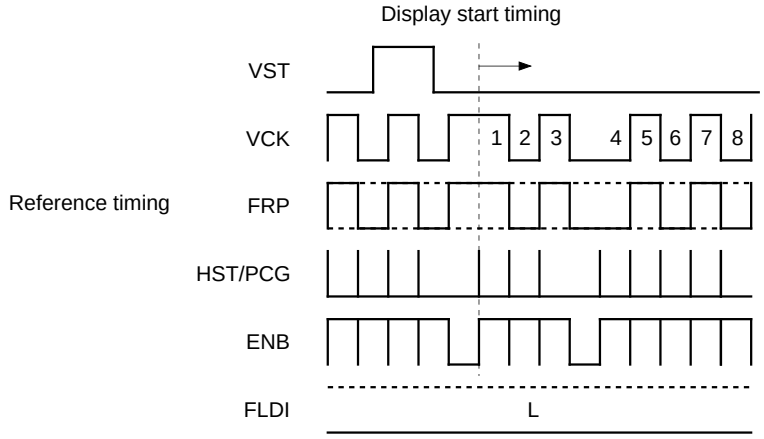
(3) MBK0

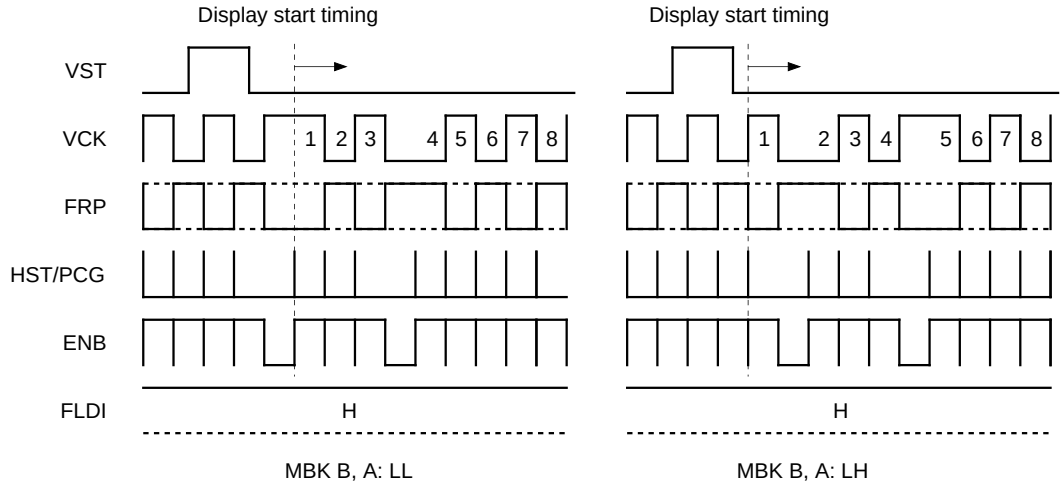
MBK0	POSITON
H	No pulse eliminate
L	Pulse eliminate

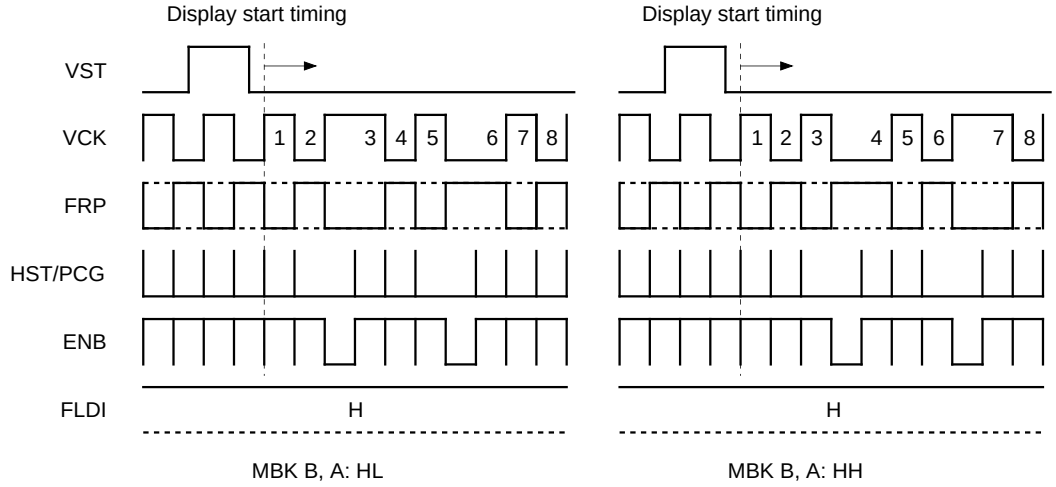
(4) MBK B, A

These bits change pulse eliminate timing for each field.

These bits determine the pulse eliminate timing for the next 1-field period using the pulse eliminate timing when the field identification pulse (FLDI) is Low as the reference. The optimal pulse eliminate position can be set by setting a pulse eliminate interval of 0 to 3H. The charts below show the pulse eliminate timing for SVGA mode, but the timing is the same for double-speed PAL pulse eliminate.



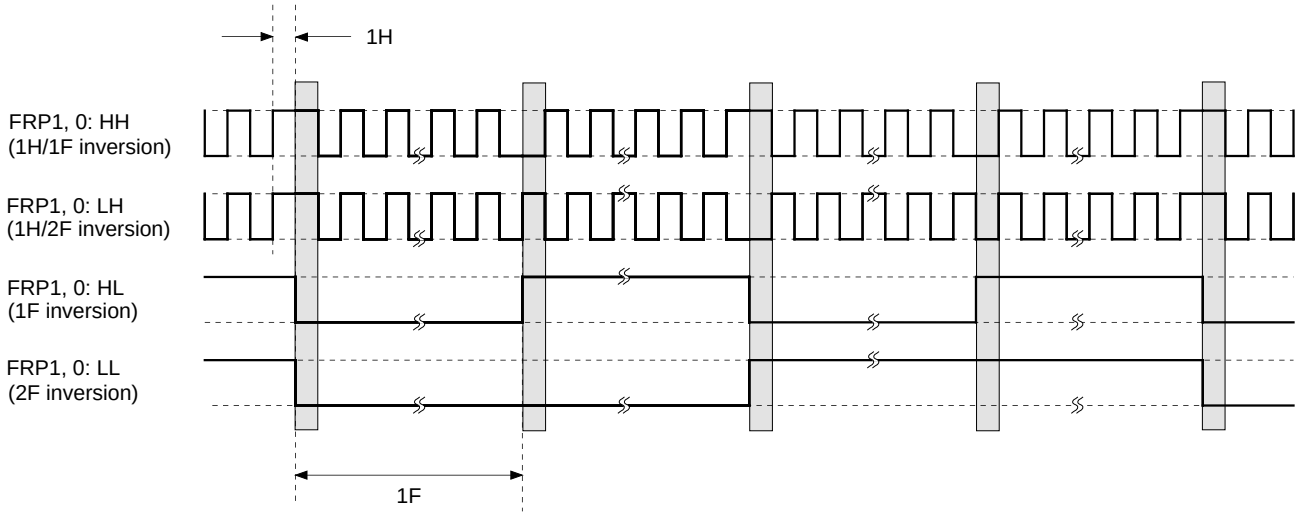




Note) MBK2: H, MBK1: H, MBK0: L

(I-4) FRP1, 0

These bits are the data for switching the LCD AC signal cycle. FRP1, 0 should normally be set to HH.



(I-5) VPOL, HPOL

These bits are the data for switching the input SYNC polarity. Sync separation processing is performed with the SYNC polarity fixed to positive by the internal logic. Therefore, the polarity must be switched when the input is positive or negative.

Accordingly, when the input SYNC is positive or negative, the VPOL and HPOL data should be set High or Low, respectively.

(I-6) MODE

This bit switches the HCK, CLR, HST and PCG timing according to the mode. Operation shifts to LCX016 mode when MODE is High, and LCX012BL mode when MODE is Low. Be sure to set this data when using the CXD2442Q in these modes.

(I-7) MODE3, 2, 1

These bits switch the panel display area. However, since the panel display area can only be switched for the LCX016, VGA/NTSC mode should be set when using the LCX012BL.

When using the LCX016

MODE	1	2	3
Macintosh17 (832 × 624)	L	L	L
SVGA (800 × 600)	L	L	H
PAL (762 × 572)	L	H	L
VGA/NTSC (640 × 480)	L	H	H
PC-98 (640 × 400)	H	L	L
WIDE (832 × 480)	H	L	H

When using the LCX012BL

MODE	1	2	3
VGA/NTSC (640 × 480)	L	H	H

* Also supports PAL display.

(I-8) CK

This bit switches the input clock. Operation shifts to CKI1 input when CK is High, and CKI2 input when CK is Low.

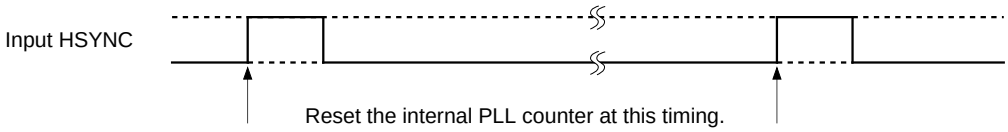
CKI1 input supports only the double-speed NTSC and PAL modes which use the built-in double-speed controller. Therefore, CKI2 input is used for other modes.

(I-9) HR

This bit controls the input HSYNC-based PLL counter reset operation. (Reset operation is allowed when HR is Low.)

Resetting the internal PLL counter at the front edge of the input HSYNC generates an output pulse synchronized to SYNC.

This function should be used with systems which do not use a PLL.



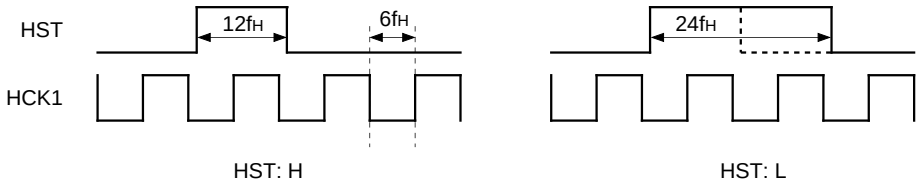
(I-10) DWN, RGT

These bits set the up/down and right/left inversion discrimination data. These settings allow display to be performed in accordance with each display system. The sample-and-hold pulse timing supports this right/left inversion function, and SH1, 2, 3 are switched with SH4, 5, 6 and SHD1 with SHD3 by switching between right scan and left scan operation, respectively.

See the Timing Charts for details.

(I-11) HST

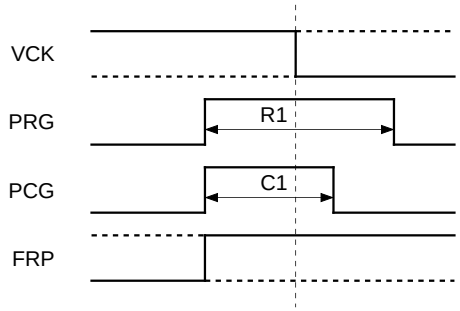
This bit adjusts the HST width.



Note) HSTP3, 2, 1, 0: LLLH

(I-12) PCG

This bit adjusts the PCG width. The PRG and FRP timings are also interlocked at this time.



Note) The VCK transition timing is constant regardless of PCG.

MODE	PCG = H		PCG = L	
	R1	C1	R1	C1
Macintosh17	97 dots	68 dots	86 dots	57 dots
SVGA	82 dots	58 dots	72 dots	48 dots
PAL	54 dots	38 dots	48 dots	32 dots
VGA/NTSC				
PC-98				
WIDE				

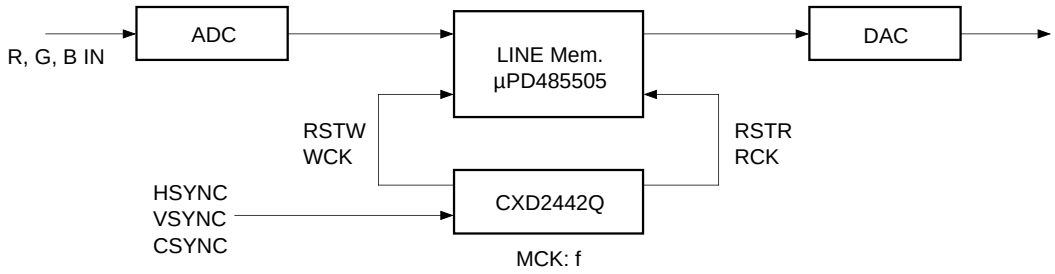
(I-13) DSP

This bit performs the double-speed NTSC and PAL display mode switching settings. Operation shifts to double-speed display mode when DSP is Low. However, DSP should be set High for other modes.

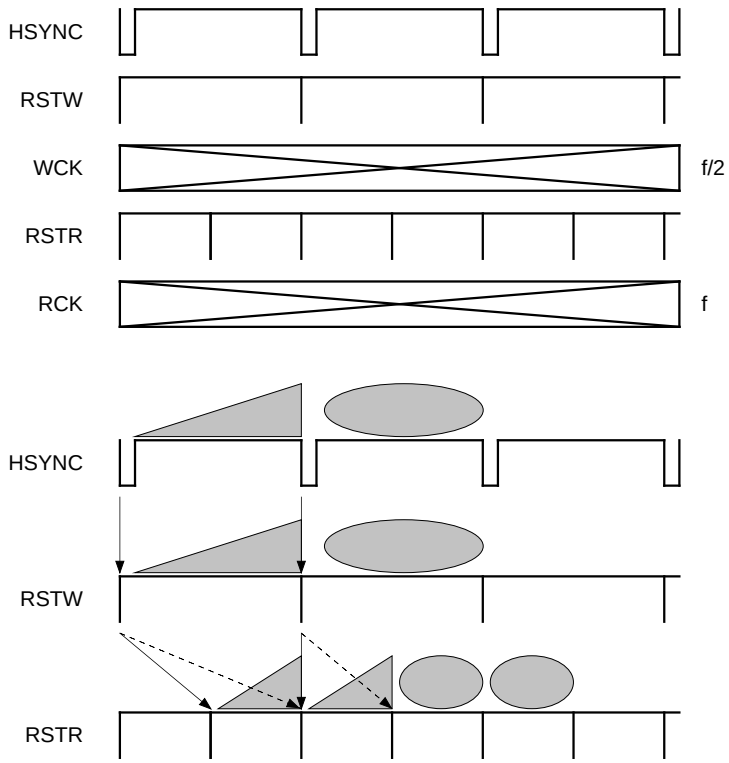
This function is only supported when the CXD2442Q's built-in double-speed controller is used. This controller is designed to use the µPD485505 (NEC/high-speed line buffer) as the system line memory IC, and generates the double-speed processing pulses RSTW (reset write), WCK (write clock), RSTR (reset read) and RCK (read clock).

Operation is as follows. Write operation is started at the RSTW timing, and this memory information is read twice at double speed at the RSTR timing which is delayed by 1/2H and 1H from the RSTW timing. Labeling the master clock frequency (MCK) as f, the write and read clock frequencies at this time are expressed as f/2 and f, respectively.

See the specifications for a detailed description of µPD485505 operation.



Double-speed display system diagram



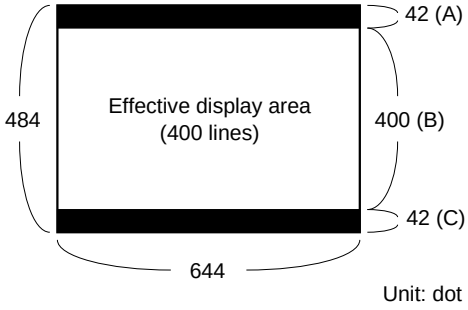
Double-speed display timing

Note) See the Timing Charts for details.

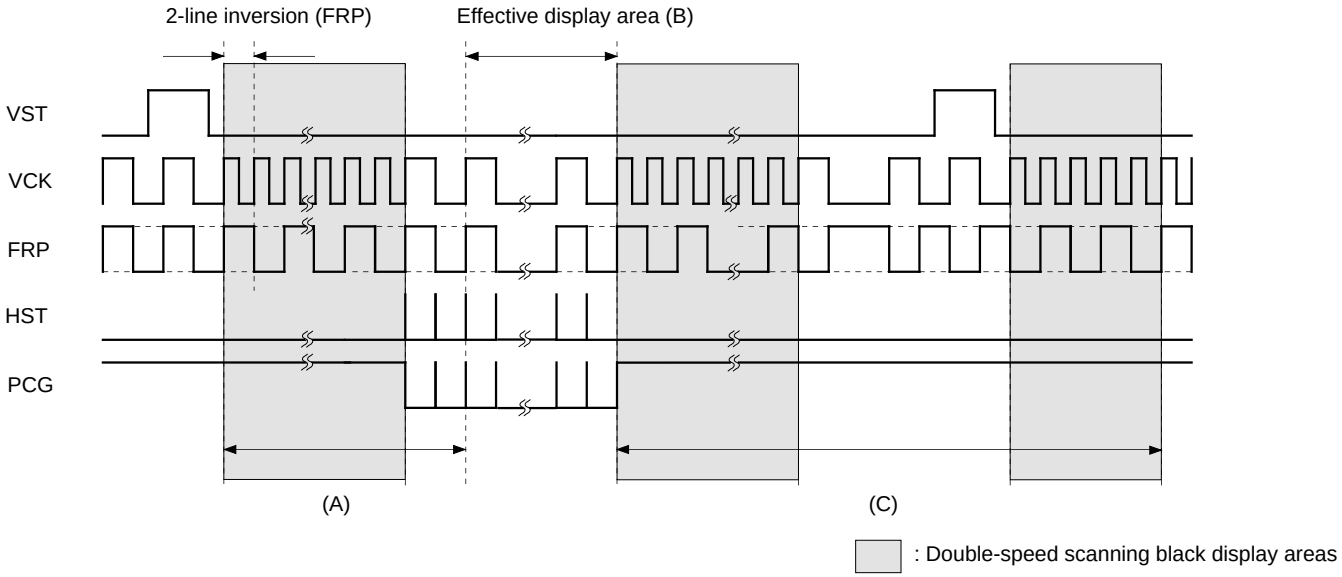
(I-14) PC-98

This bit switches the PC-98 (400-vertical line) display mode. Operation shifts to PC-98 mode when PC-98 is Low. However, since this function supports the LCX012BL, PC-98 is normally (modes other than LCX012BL/PC-98 mode) set High.

This function is used to display PC-98 (640 × 400) images in the display area of the LCX012BL (644 × 484). The upper and lower 42 lines outside of the display area are black display during this mode.
The vertical high-speed scanning and precharge black writing methods have been introduced as methods for writing these black areas. VCK is shifted to double-speed operation to realize vertical double-speed transfer and enable black display within the limited V blanking. Also, the black level during this period is determined by the PSIG (LCX012BL) level and written at the PCG (LCX012BL pin) timing.
At this time, HST is masked, limiting the video signal input.



LCX012BL panel

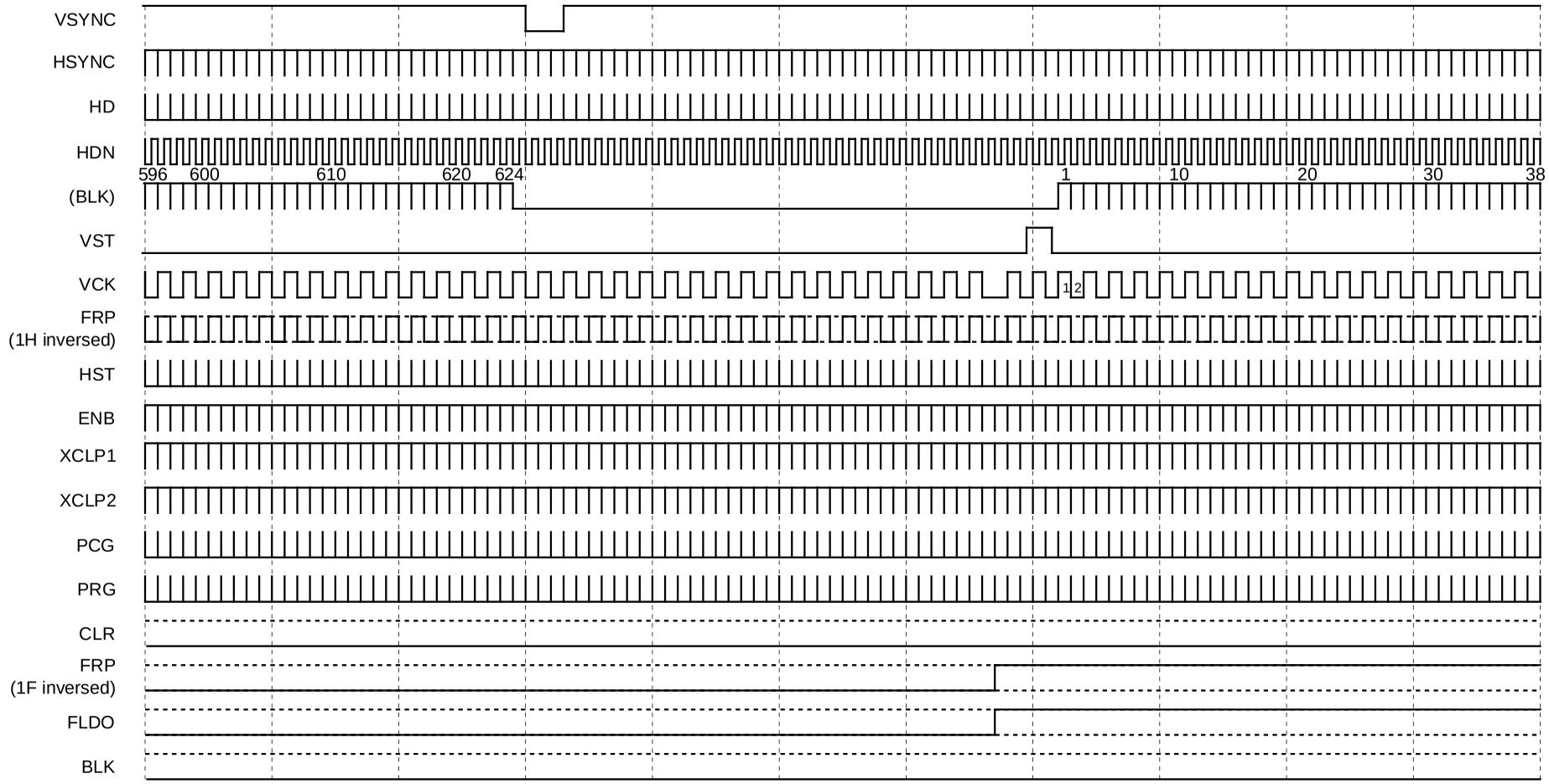


PC-98/400-line display timing

Note) FRP is inversed (panel display) every two lines during double-speed scanning.
See the Timing Charts for details.

LCX016 SVGA (Macintosh17) 832 × 624

MODE3/2/1: L/L/L MODE: H DWN: H VP: LLHLLLHH (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

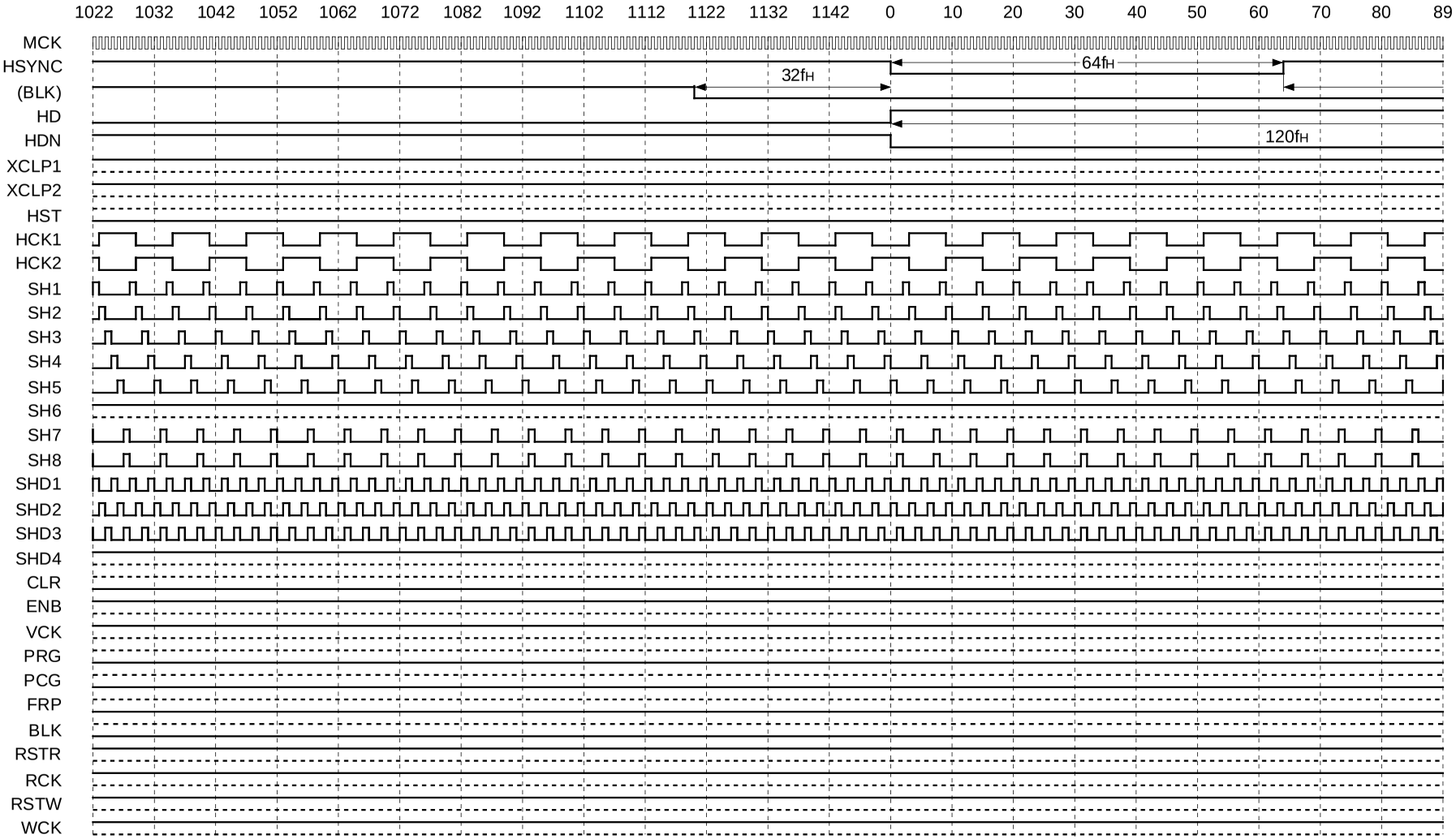


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX016 SVGA (Macintosh17) _1 832 × 624

RGT: H PLLP: HLLLHHHHHHL (LSB) HP: LHHLLHHH (LSB) HDNP: LLLLL (LSB) HP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

Loop Counter: 1152f_H
MCK f: 57.28MHz (17.46ns)

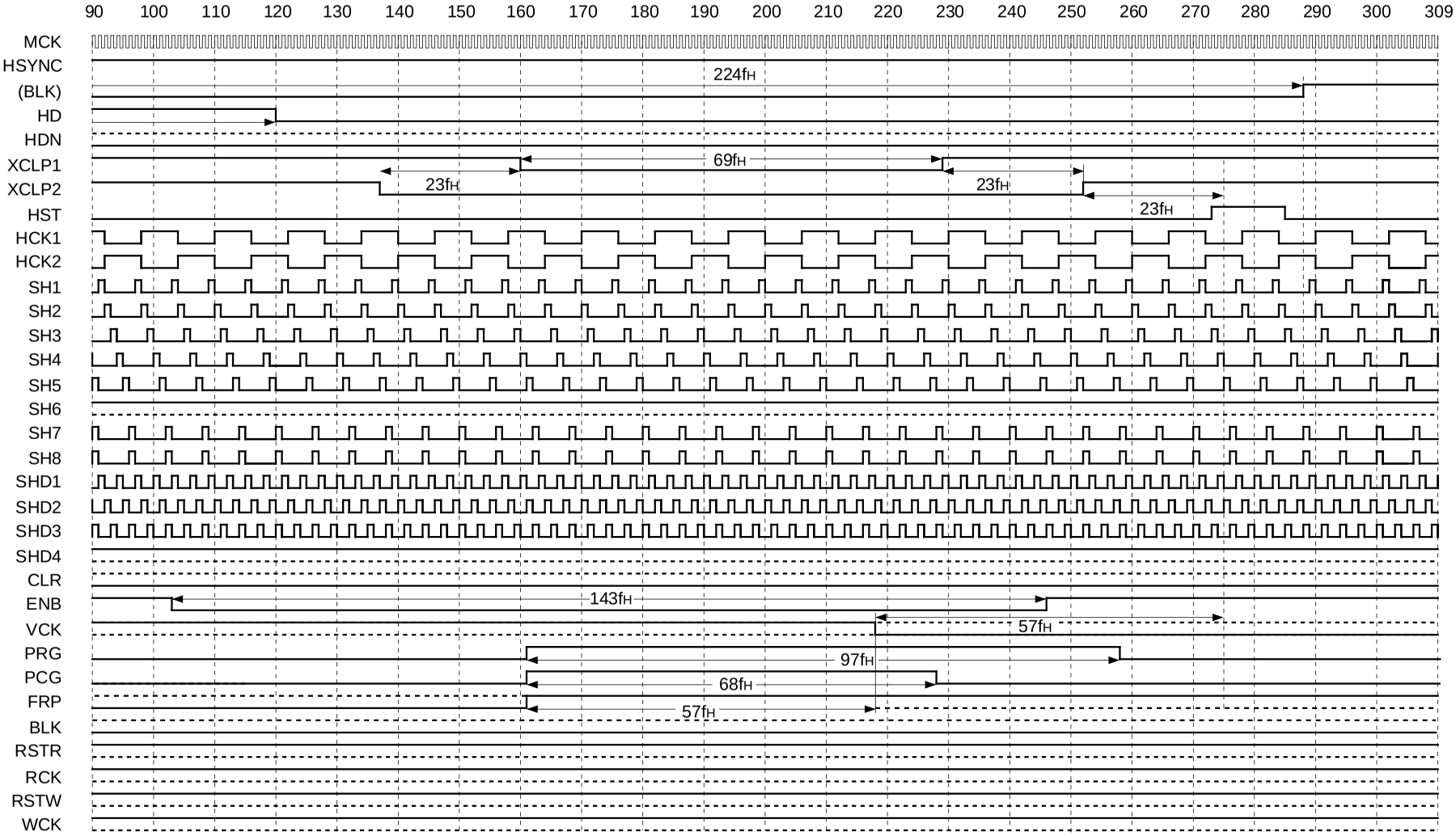


Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 SVGA (Macintosh17) _2 832 × 624

RGT: H PLLP: HLLLHHHHHHL (LSB) HP: HLLHHLLL (LSB) HDNP: LLLLL (LSB) HP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

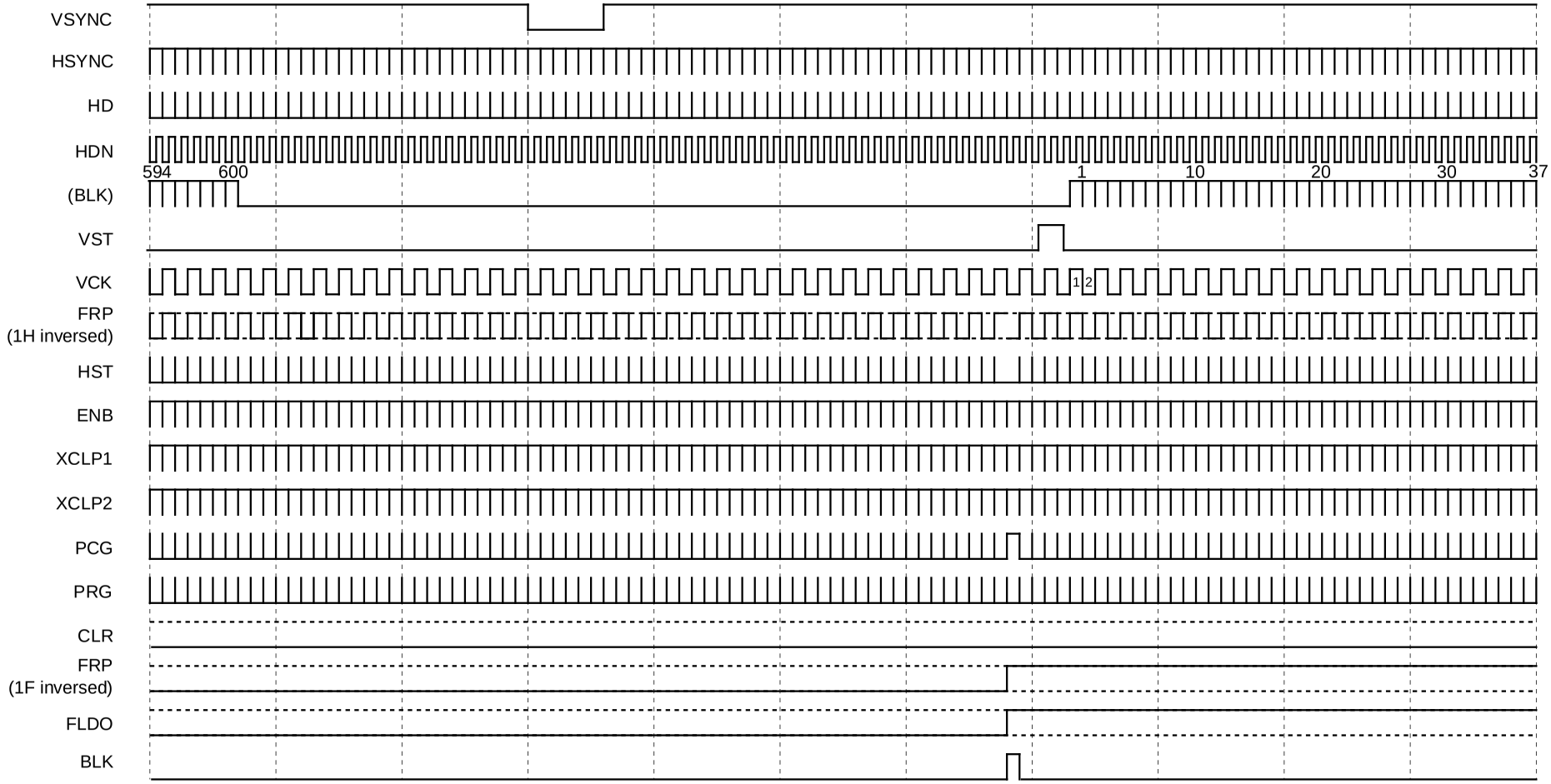
Loop Counter: 1152fH
MCK f: 57.28MHz (17.46ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 SVGA 800 × 600

MODE3/2/1: H/L/L MODE: H DWN: H VP: LLHLLHLL (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

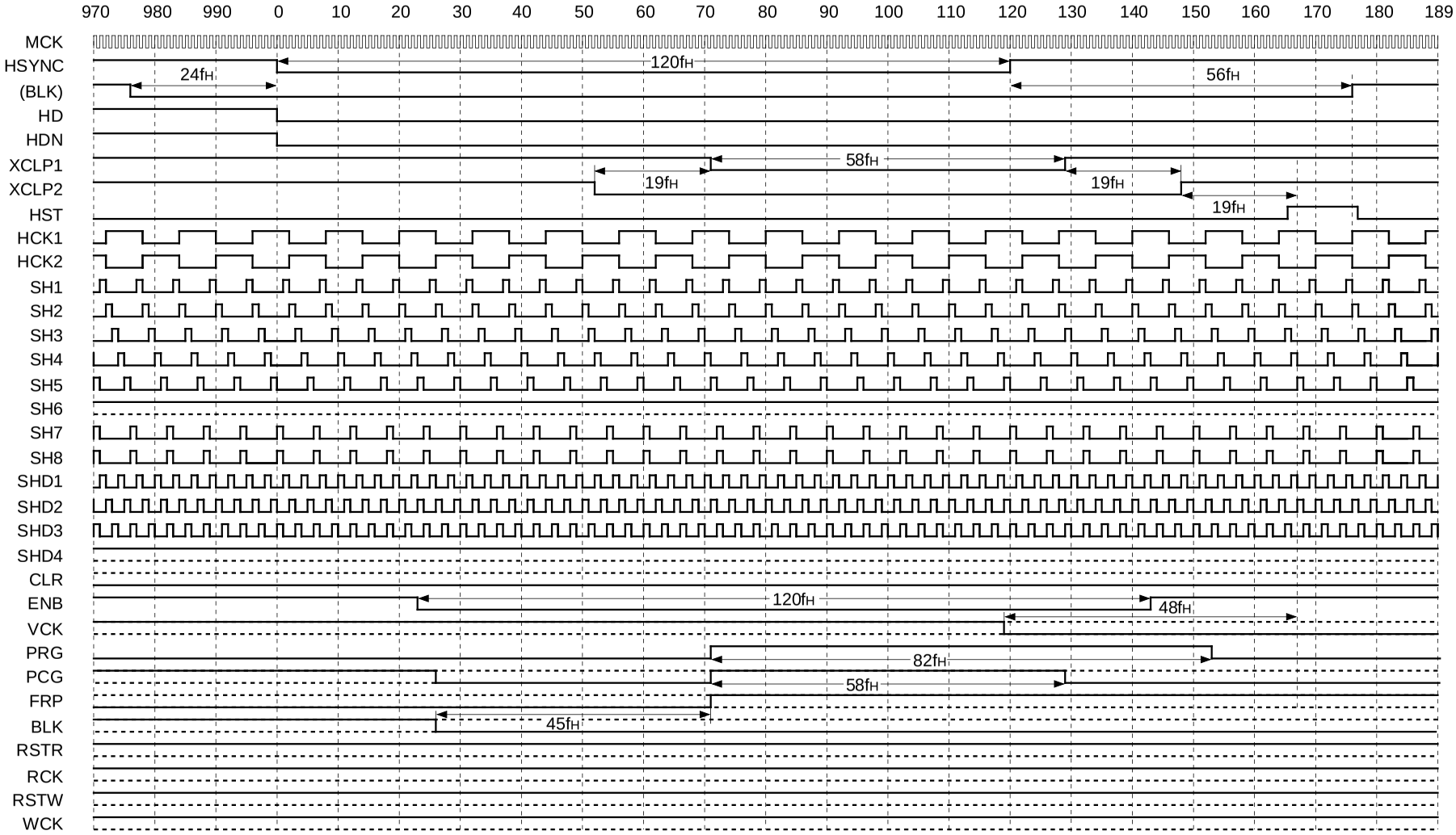


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX016 SVGA 800 × 600

RGT: H PLLP: LHHHHHLLHHL (LSB) HP: HHHLHLLL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

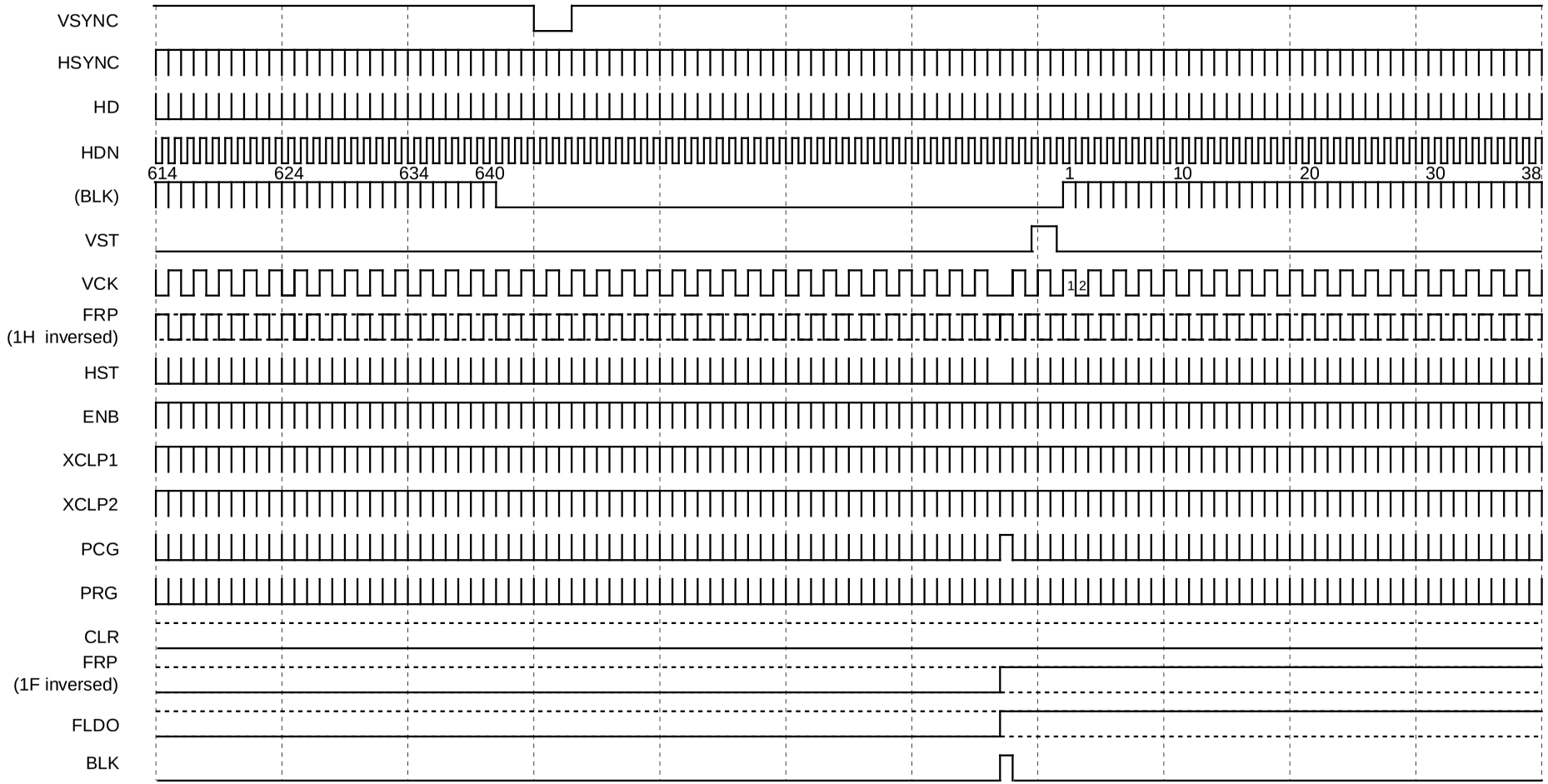
Loop Counter: 1000fH
MCK f: 48.00MHz (20.83ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 VGA 640 × 480

MODE3/2/1: H/H/L MODE: H DWN: H VP: LLHLLLHH (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

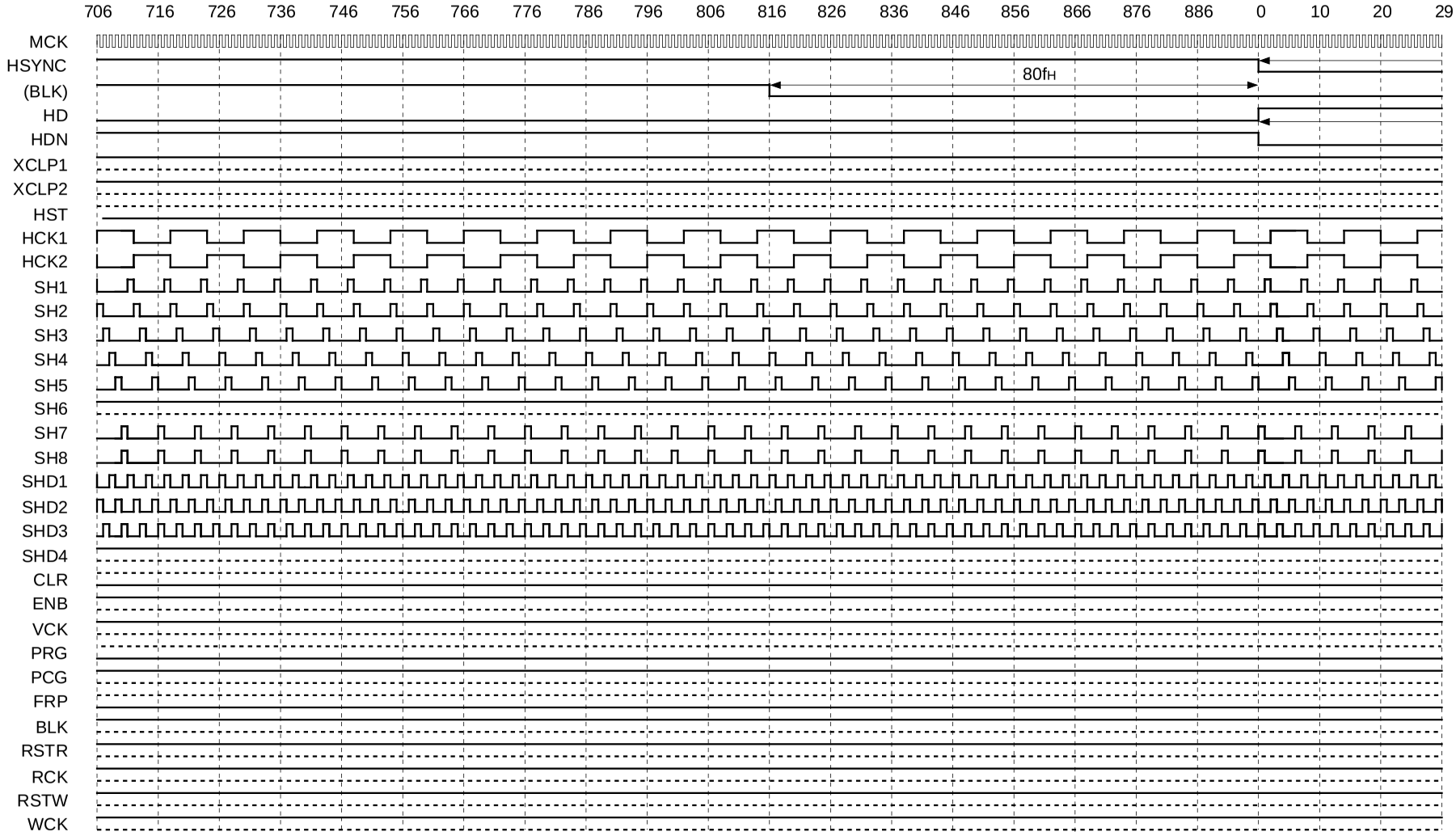


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX016 VGA_1 640 × 480

RGT: H PLLP: LHHLHHHHHHL (LSB) HP: HLHHHLLL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

Loop Counter: 896f_H
MCK f: 31.33MHz (31.92ns)

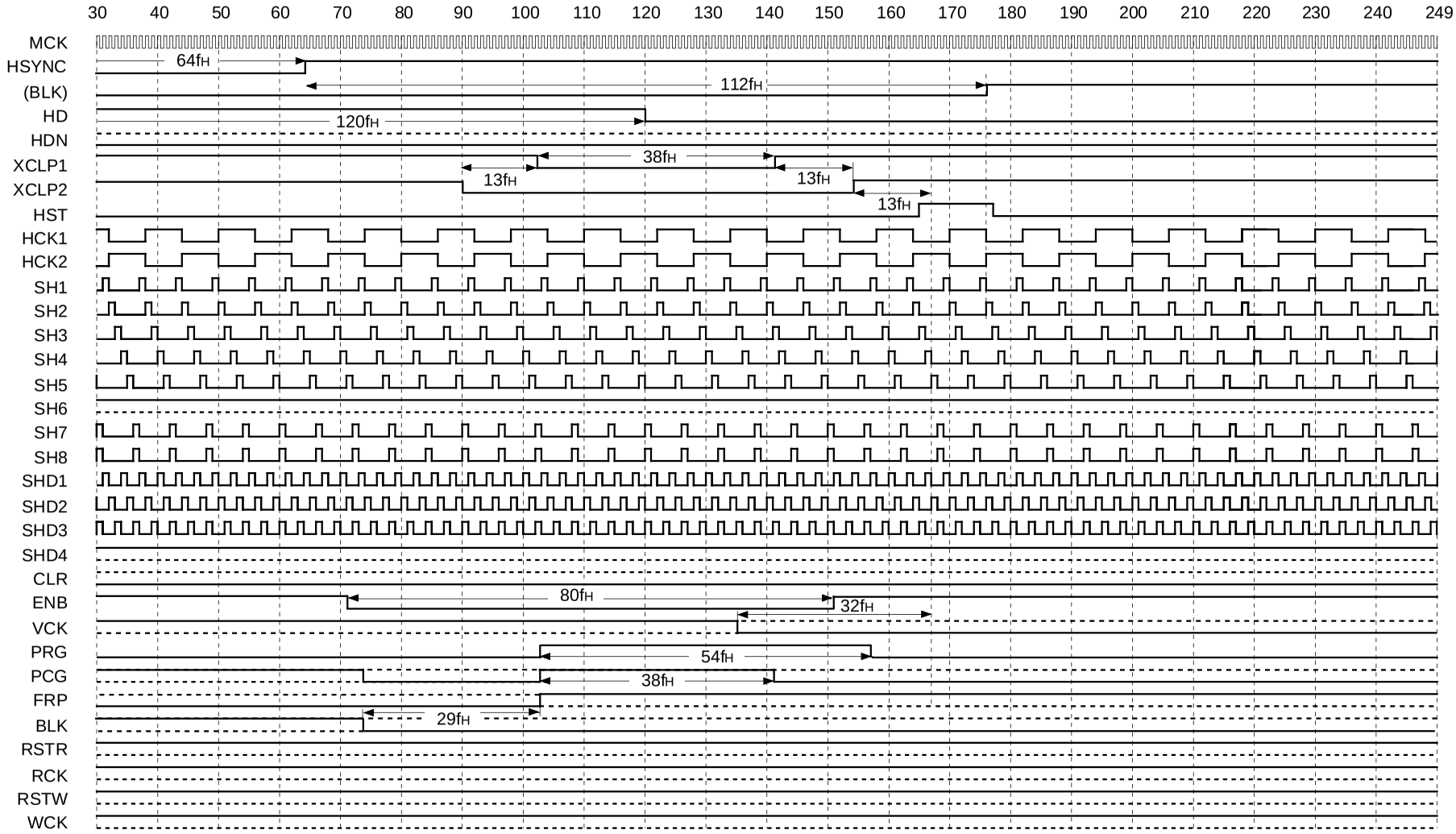


Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 VGA_1 640 × 480

RGT: H PLLP: LHHLHHHHHHL (LSB) HP: HLHHHLLL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

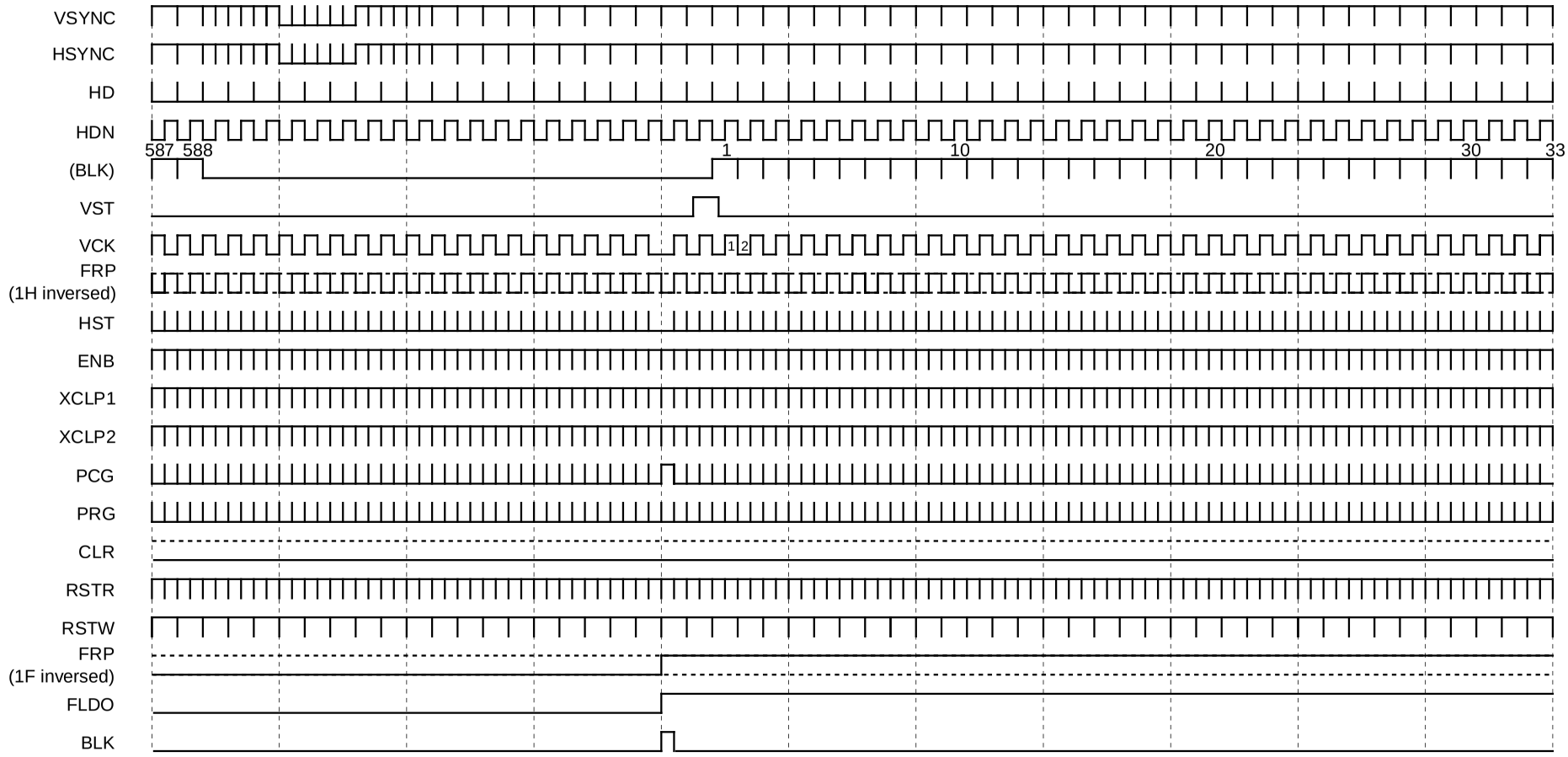
Loop Counter: 896f_H
MCK f: 31.33MHz (31.92ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC (ODD) 640 × 480

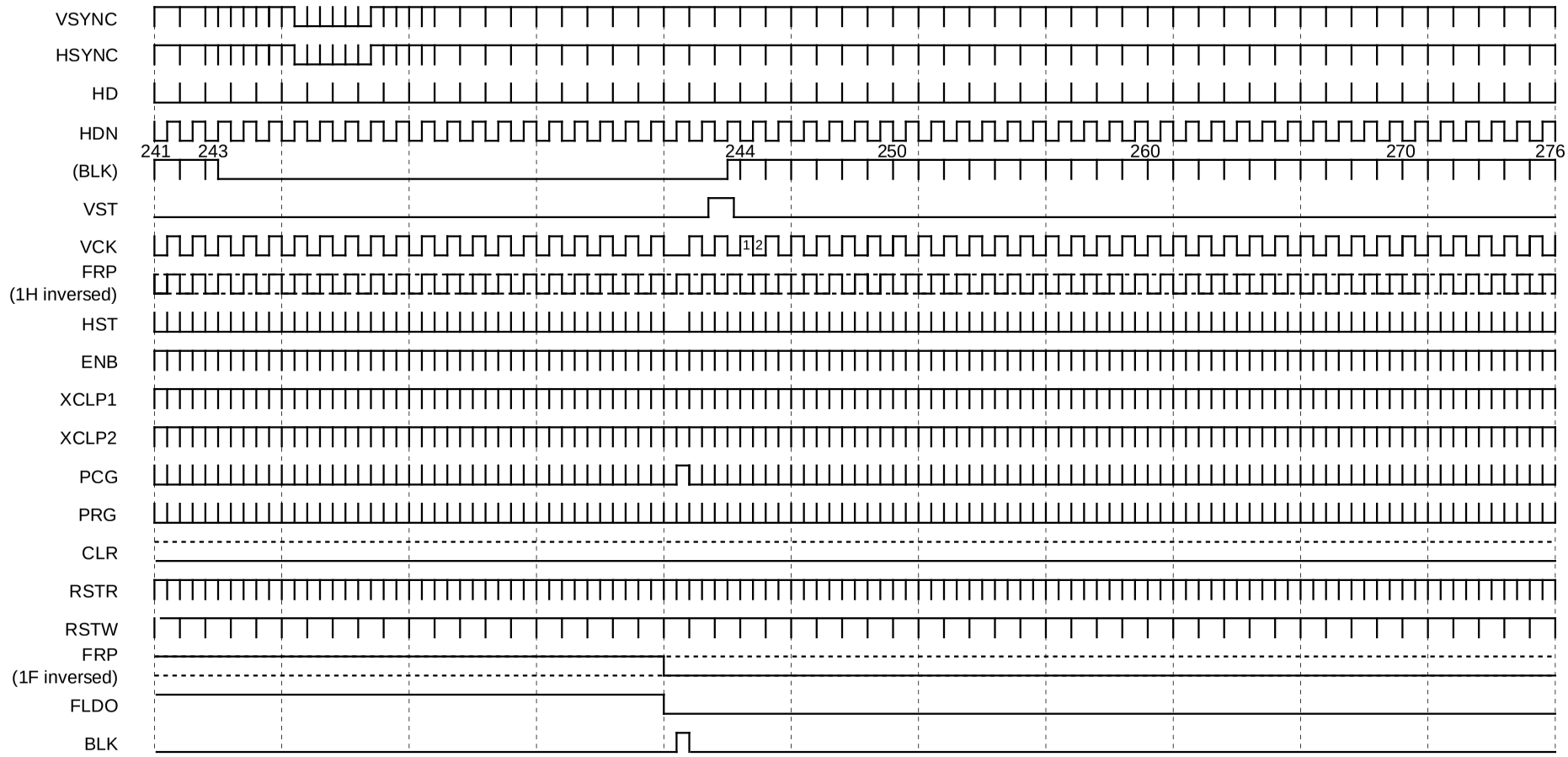
MODE3/2/1: H/H/L MODE: H DWN: H VP: LLLLHHLL (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H



Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX016 NTSC (EVEN) 640 × 480

MODE3/2/1: H/H/L MODE: H DWN: H VP: LLLLHHLL (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H

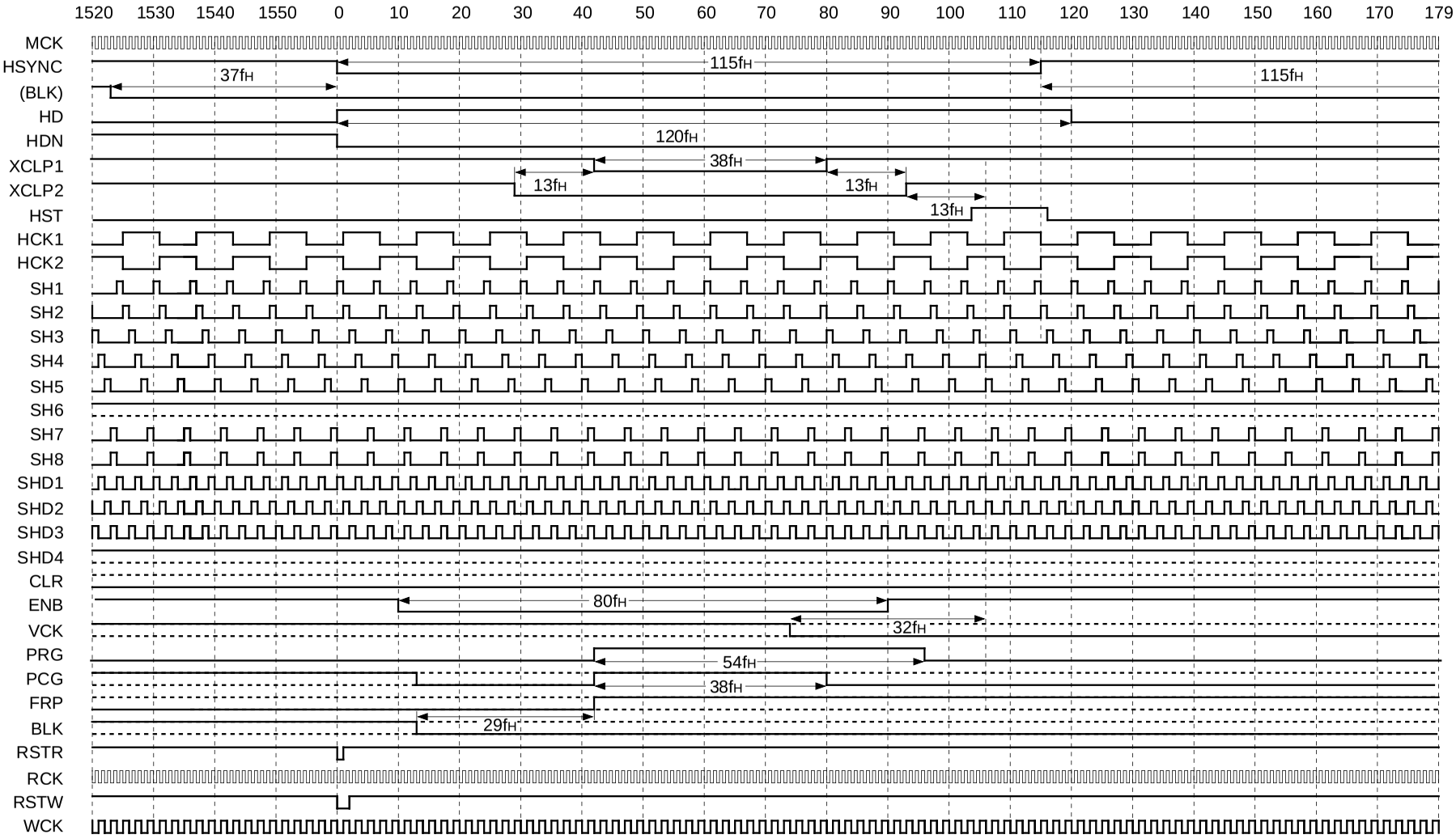


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX016 NTSC_1 640 × 480

RGT: H PLLP: HHLLLLHLHHL (LSB) HP: HHHHLHLH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

Loop Counter: 1560fH
MCK f: 24.54MHz (40.75ns)

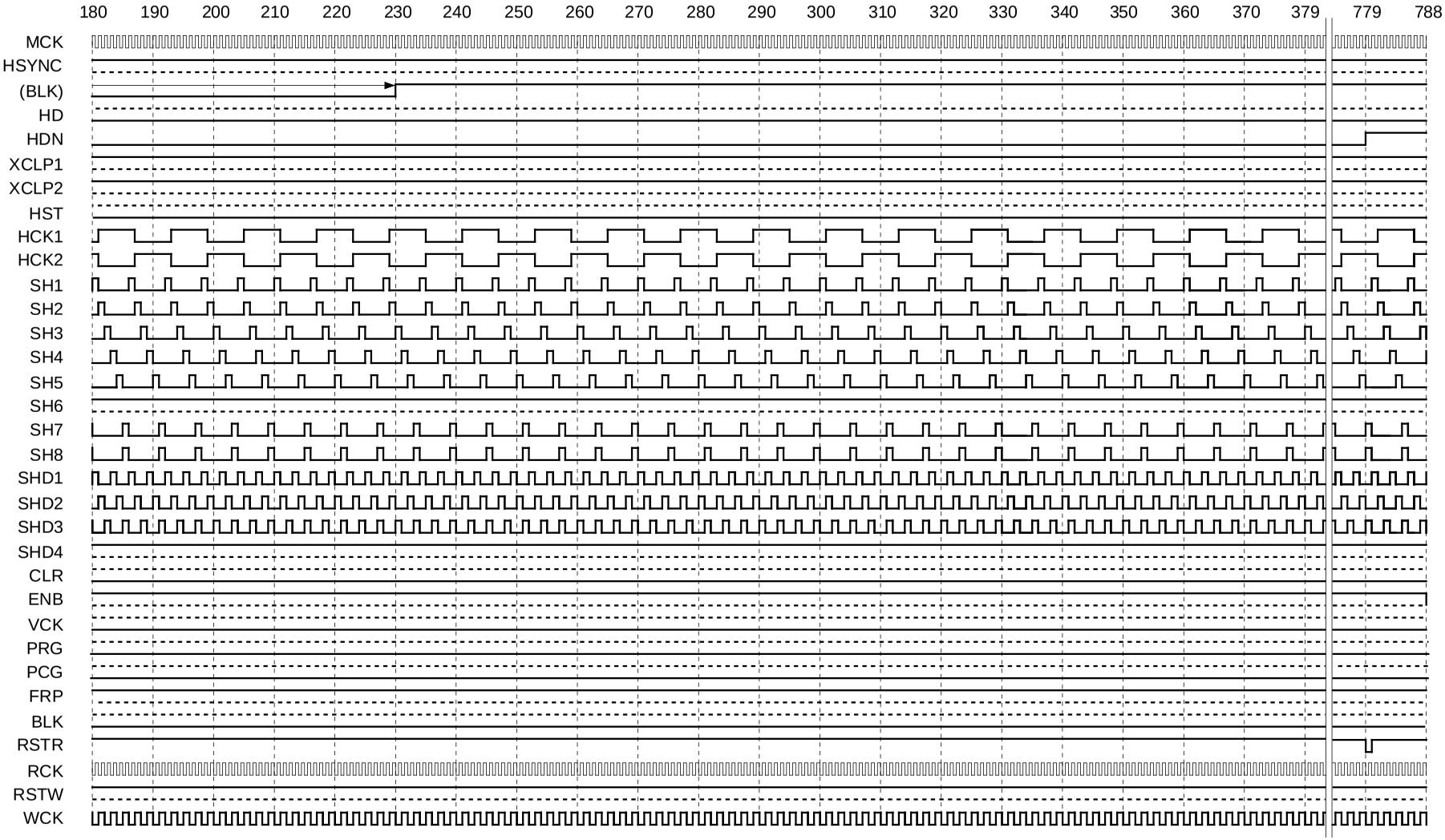


Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC_2 640 × 480

RGT: H PLLP: HHLLLLHLHHL (LSB) HP: HHHHLHLH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

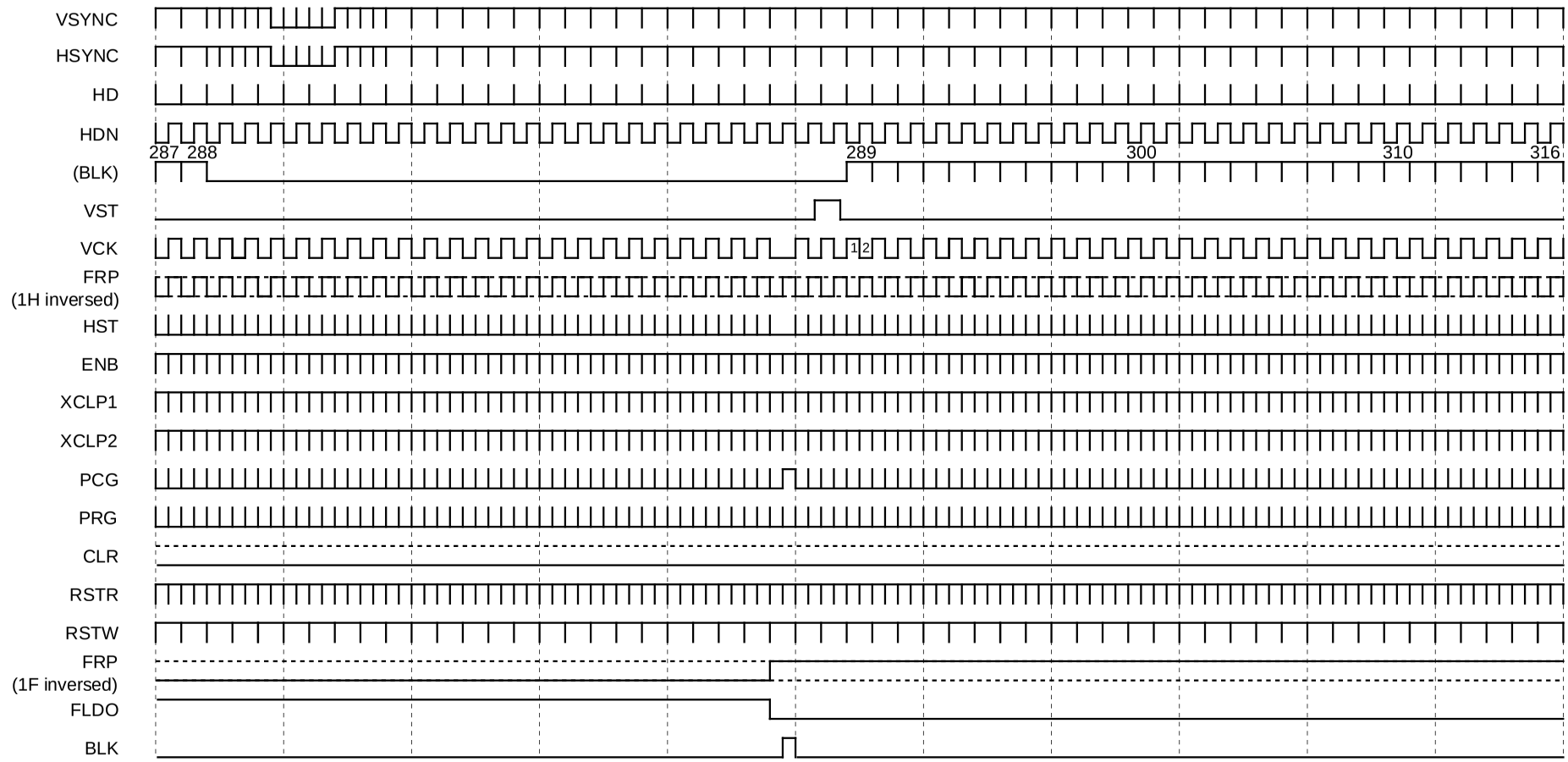
Loop Counter: 1560f_H
MCK f: 24.54MHz (40.75ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 PAL (ODD) 762 × 572

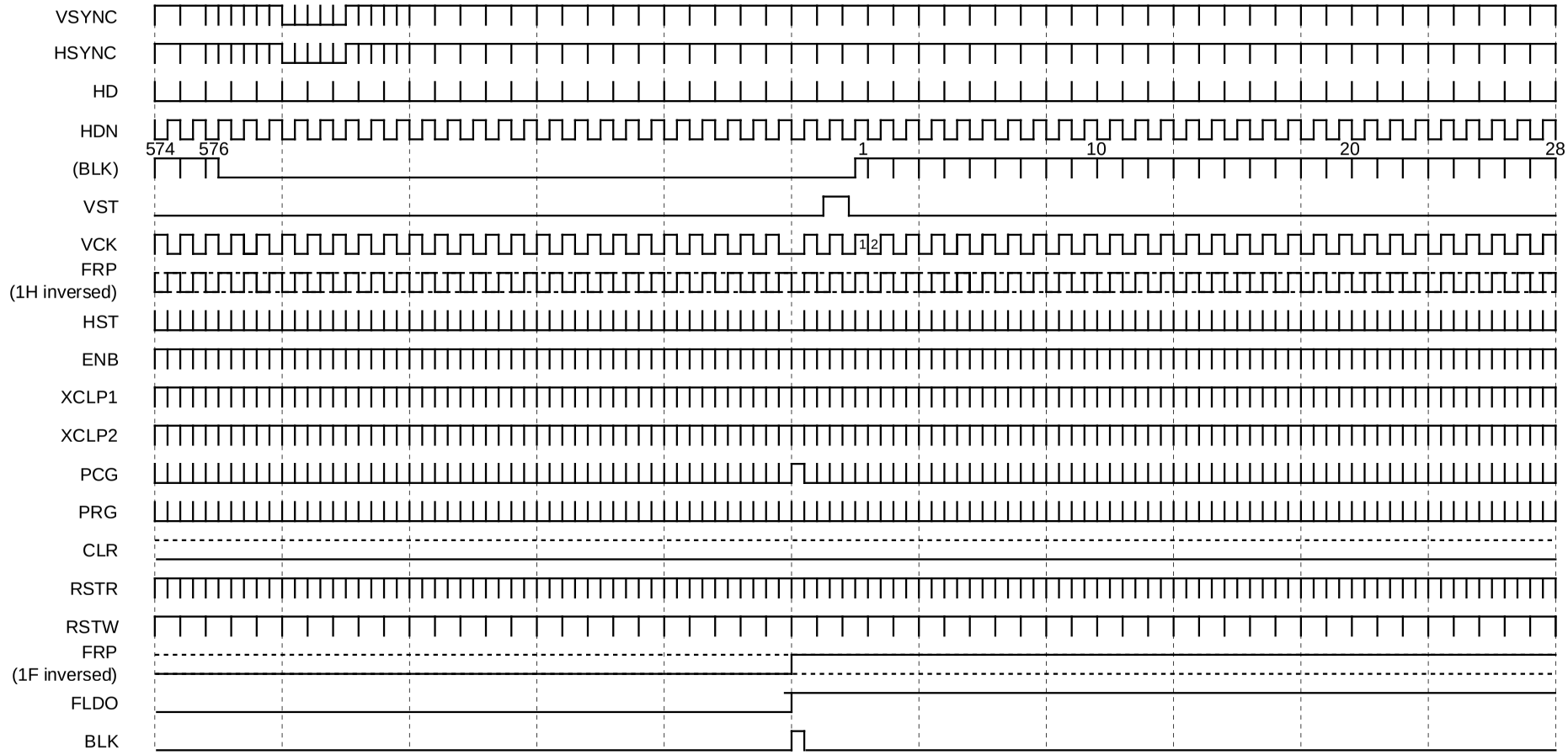
MODE3/2/1: L/H/L MODE: H DWN: H VP: LLLHLLLH (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H



Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX016 PAL (EVEN) 762 × 572

MODE3/2/1: L/H/L MODE: H DWN: H VP: LLLHLLLH (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

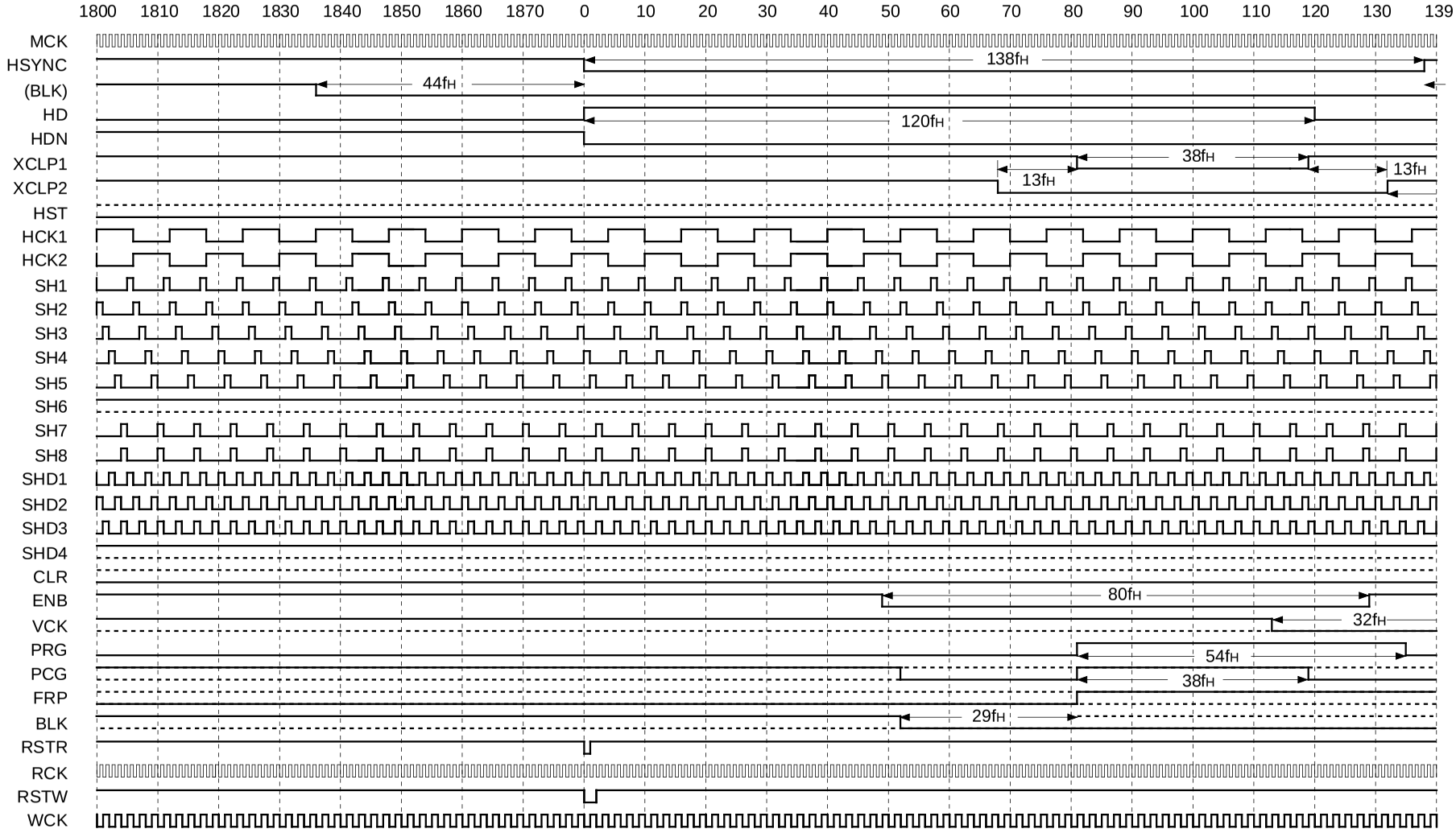


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX016 PAL_1 762 × 572

RGT: H PLLP: HHHLHLHLHHL (LSB) HP: HHLLHHHL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

Loop Counter: 1880fH
MCK f: 29.38MHz (34.04ns)

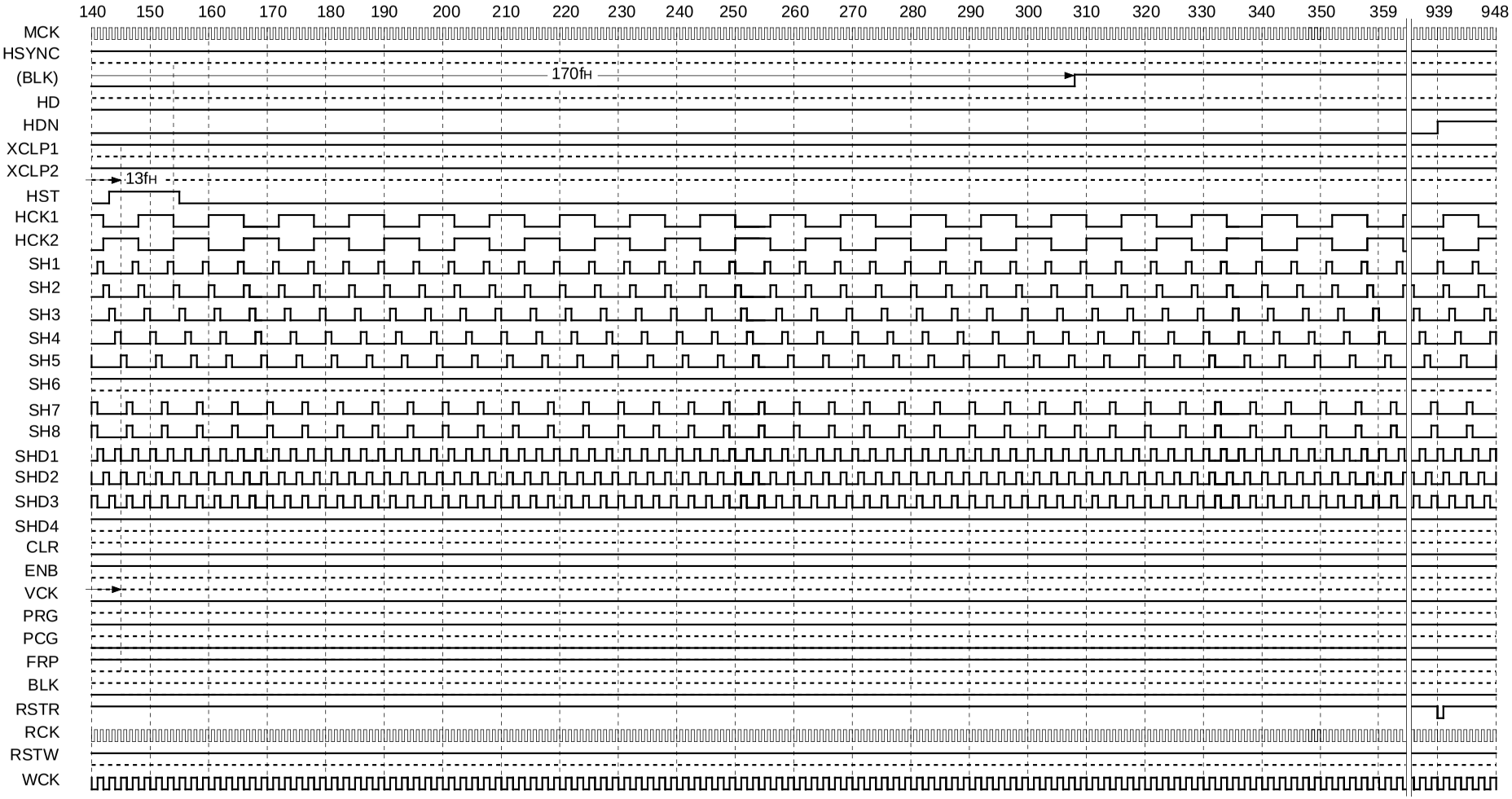


Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 PAL_2 762 × 572

RGT: H PLLP: HHHLHLHLHHL (LSB) HP: HHLLHHHL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

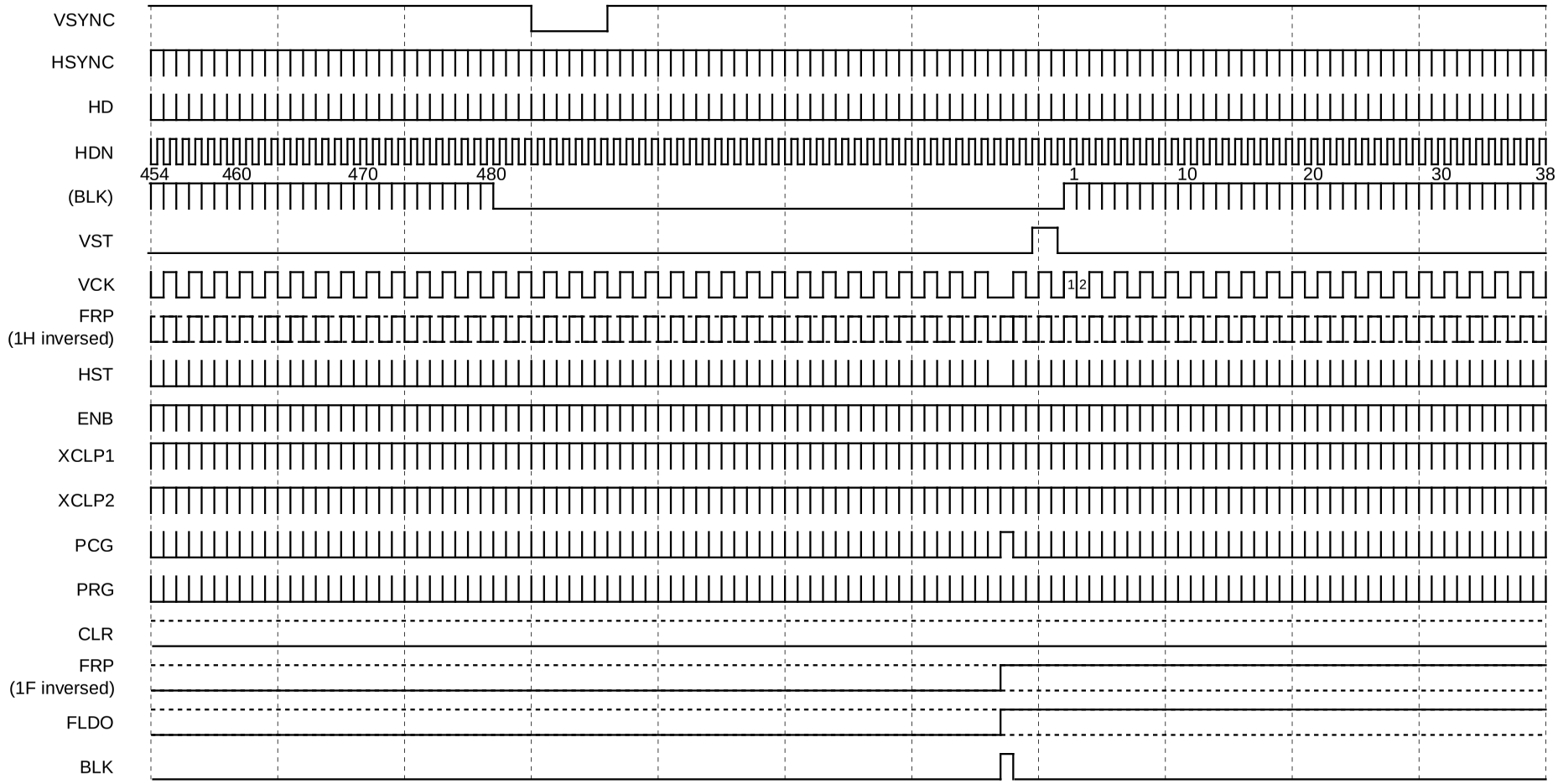
Loop Counter: 1880fH
MCK f: 29.38MHz (34.04ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC WIDE 832 × 480

MODE3/2/1: H/L/H MODE: H DWN: H VP: LLHLLLHH (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

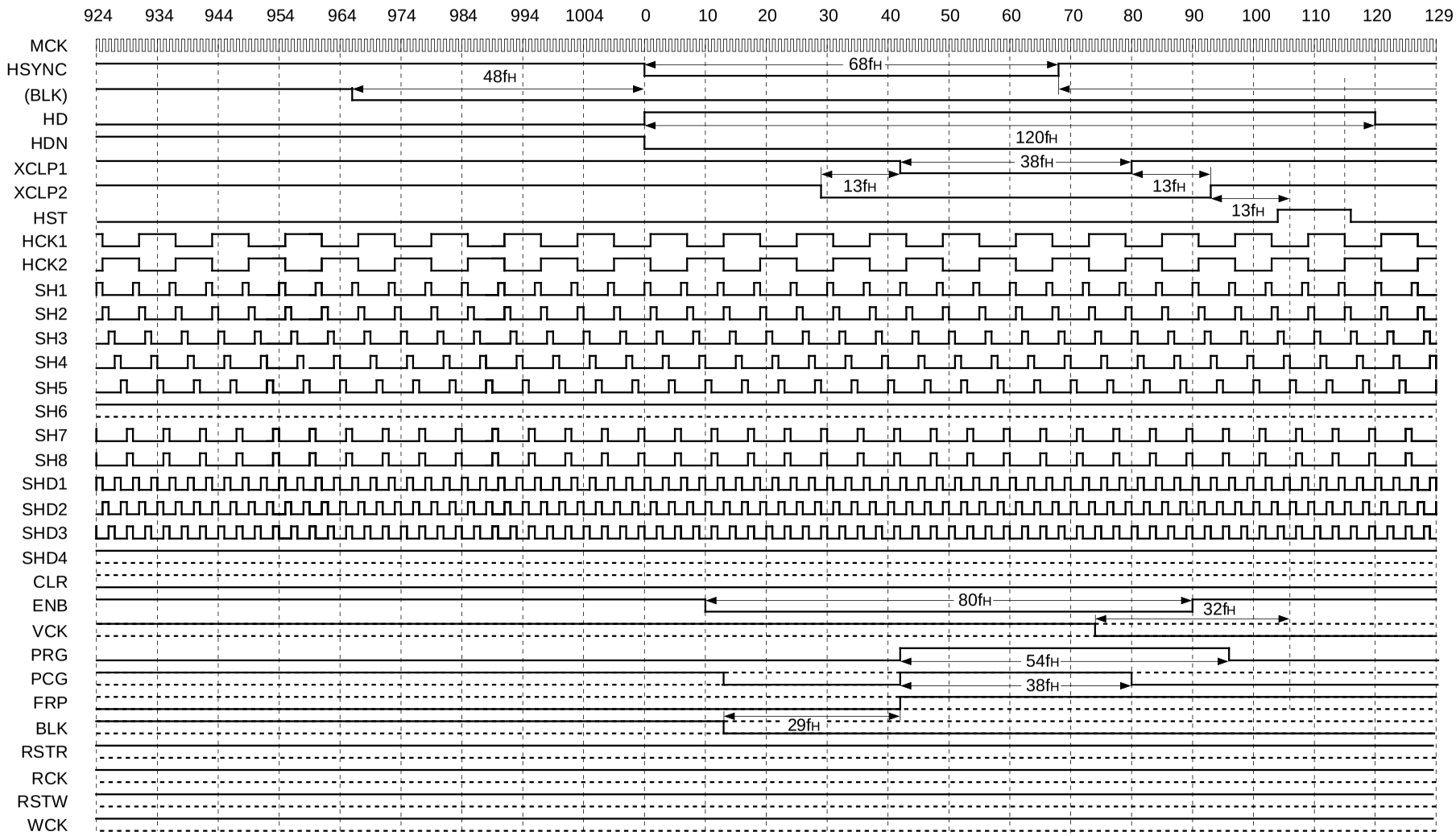


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX016 NTSC WIDE_1 832 × 480

RGT: H PLLP: LHHHHHHHLHLL (LSB) HP: HHHHLHLH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

Loop Counter: 1014fH
MCK f: 31.90MHz (31.35ns)

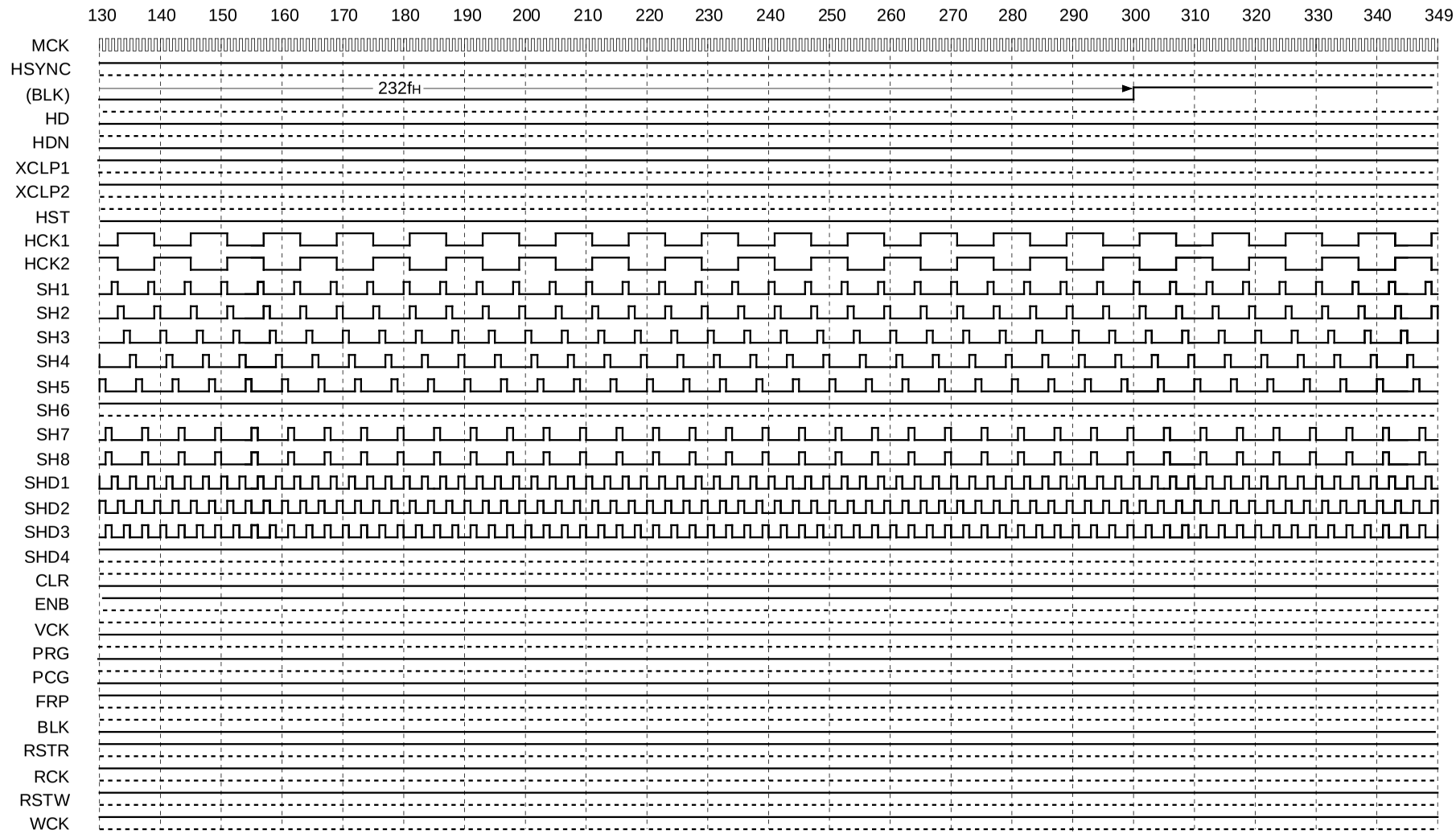


Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC WIDE_2 832 × 480

RGT: H PLLP: LHHHHHHLHLL (LSB) HP: HHHHLHLH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

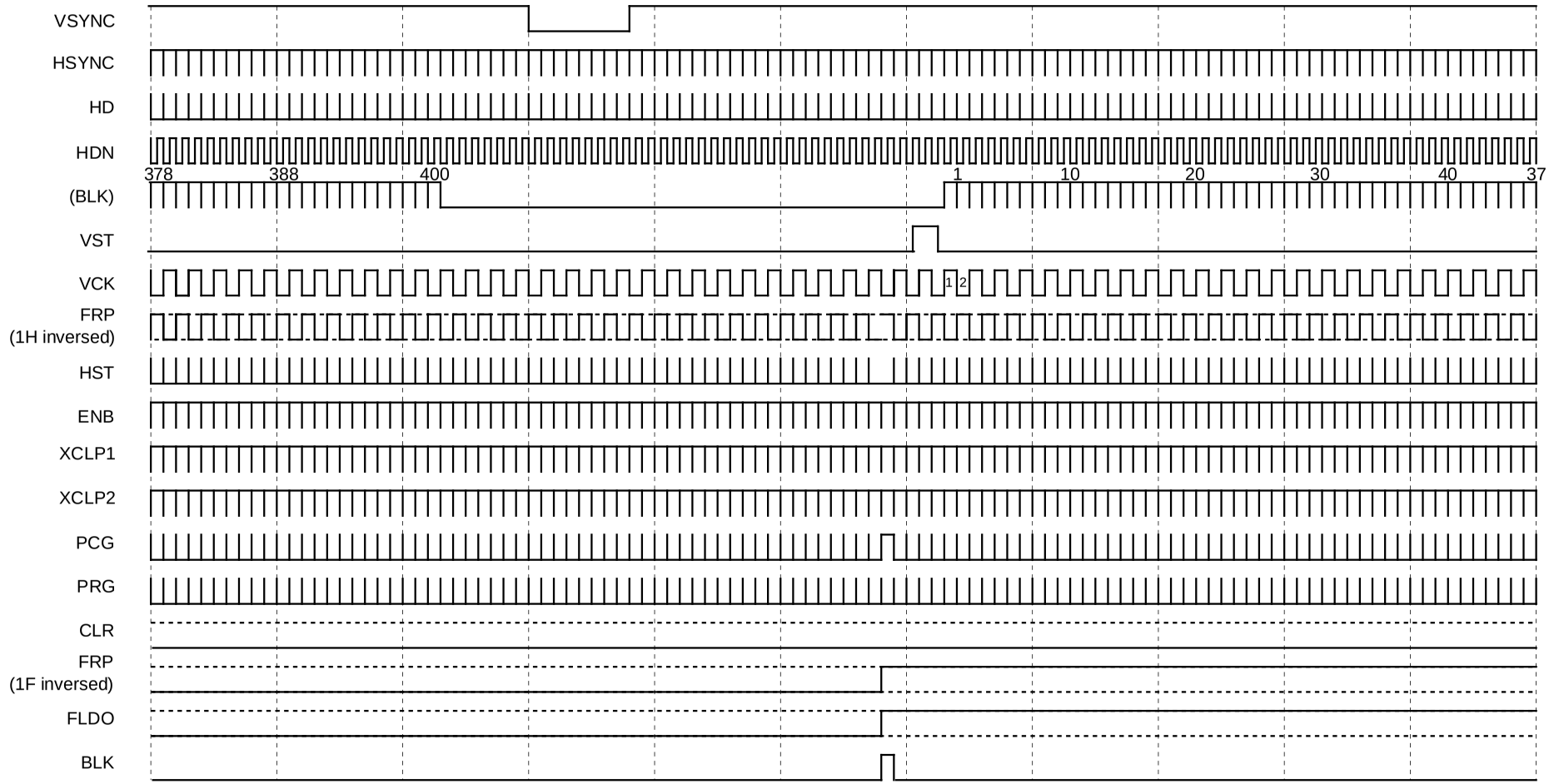
Loop Counter: 1014fH
MCK f: 31.90MHz (31.35ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 PC-98 640 × 400

MODE3/2/1: L/L/H MODE: H DWN: H VP: LLLHHLHL (LSB) MBK2/1/0/B/A: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

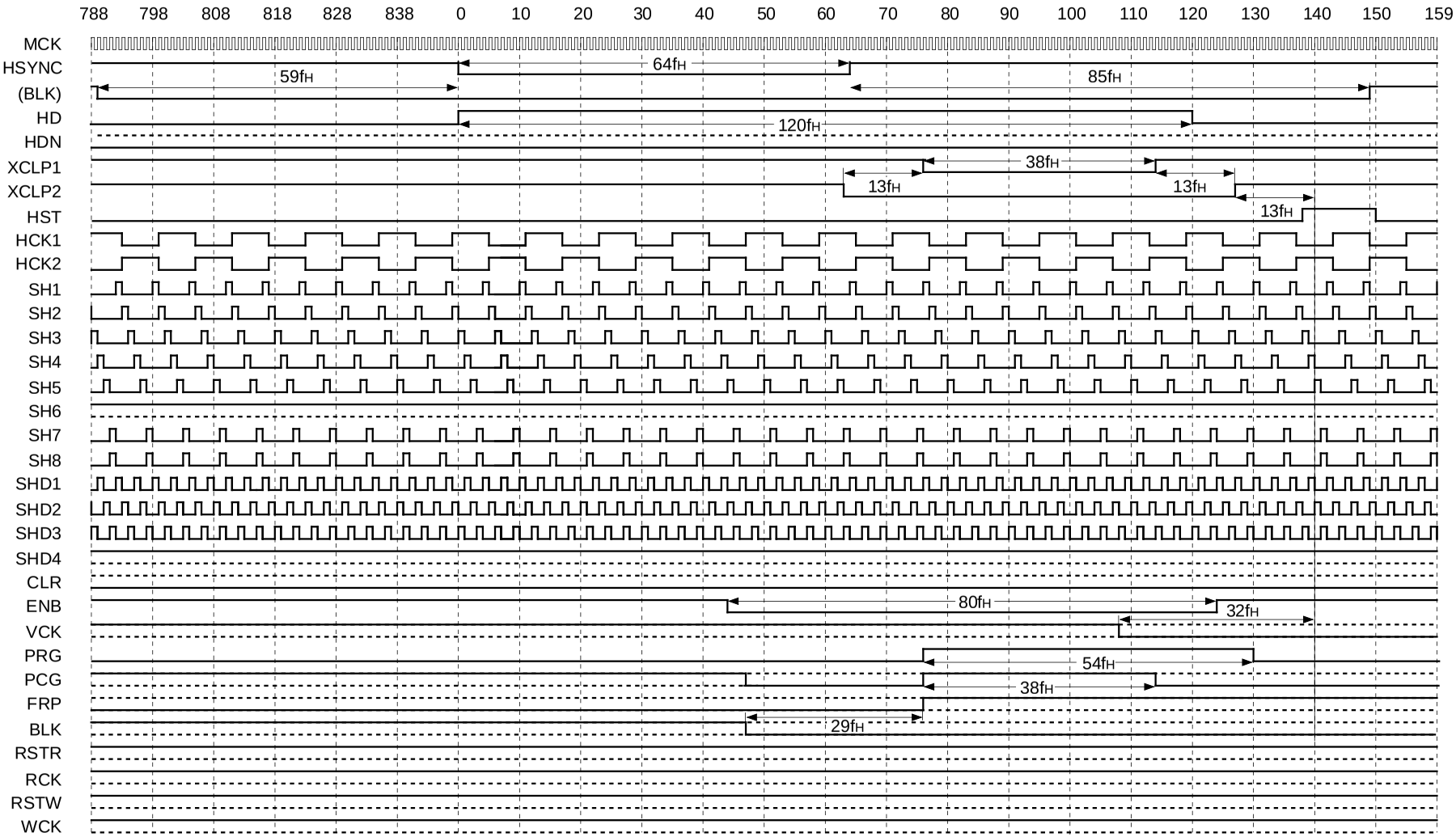


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX016 PC-98 640 × 400

RGT: H PLLP: LHHLHLLHHHL (LSB) HP: HHLHLLHH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

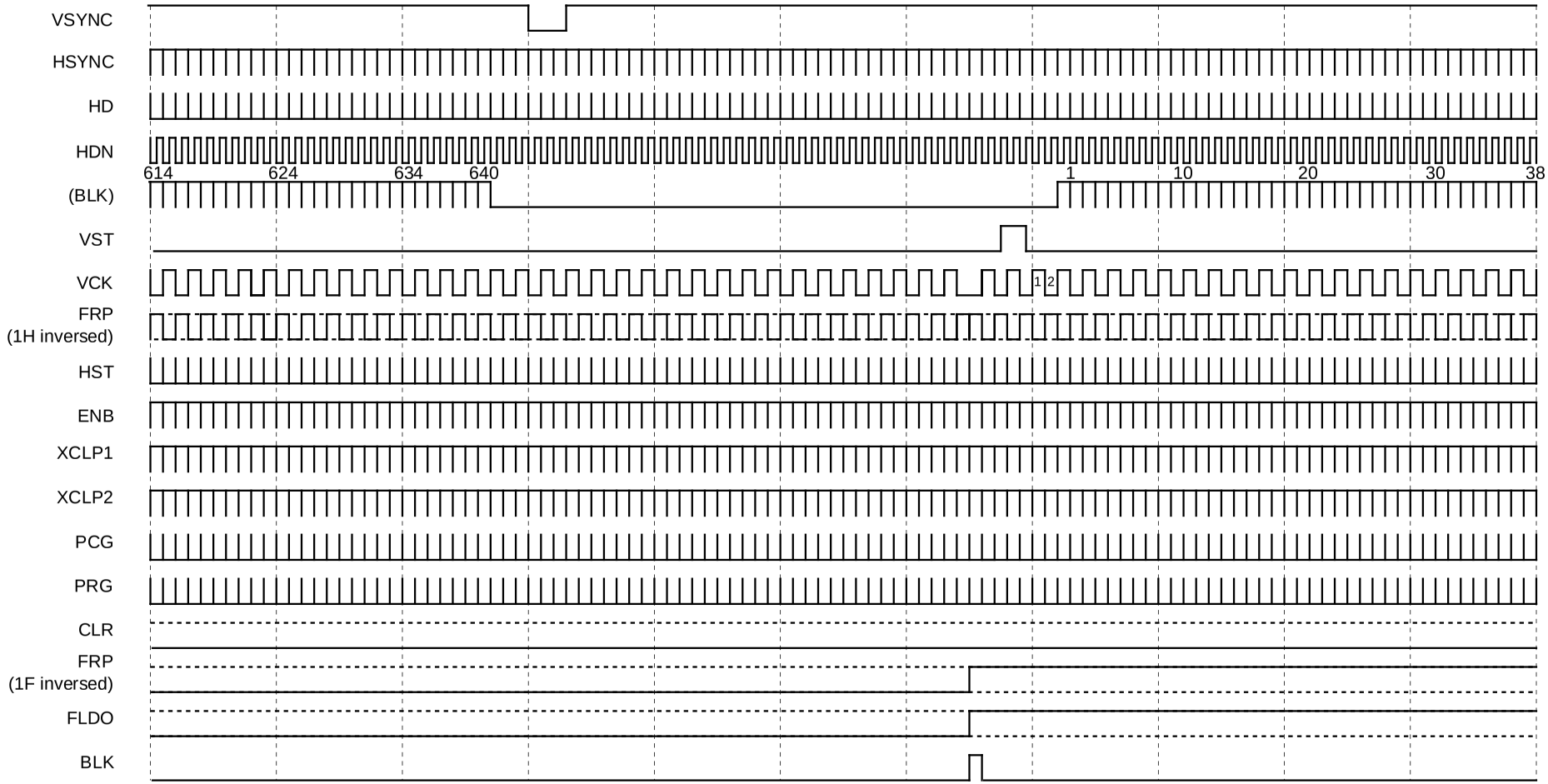
Loop Counter: 848f_H
MCK f: 21.053MHz (47.499ns)



Note) When RGT is Low, HCK1 and 2 are inversed, and pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL VGA 640 × 480

MODE3/2/1: H/H/L MODE: L DWN: H VP: LLHLLLLH (LSB) MBK2/1/0/A/B: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H

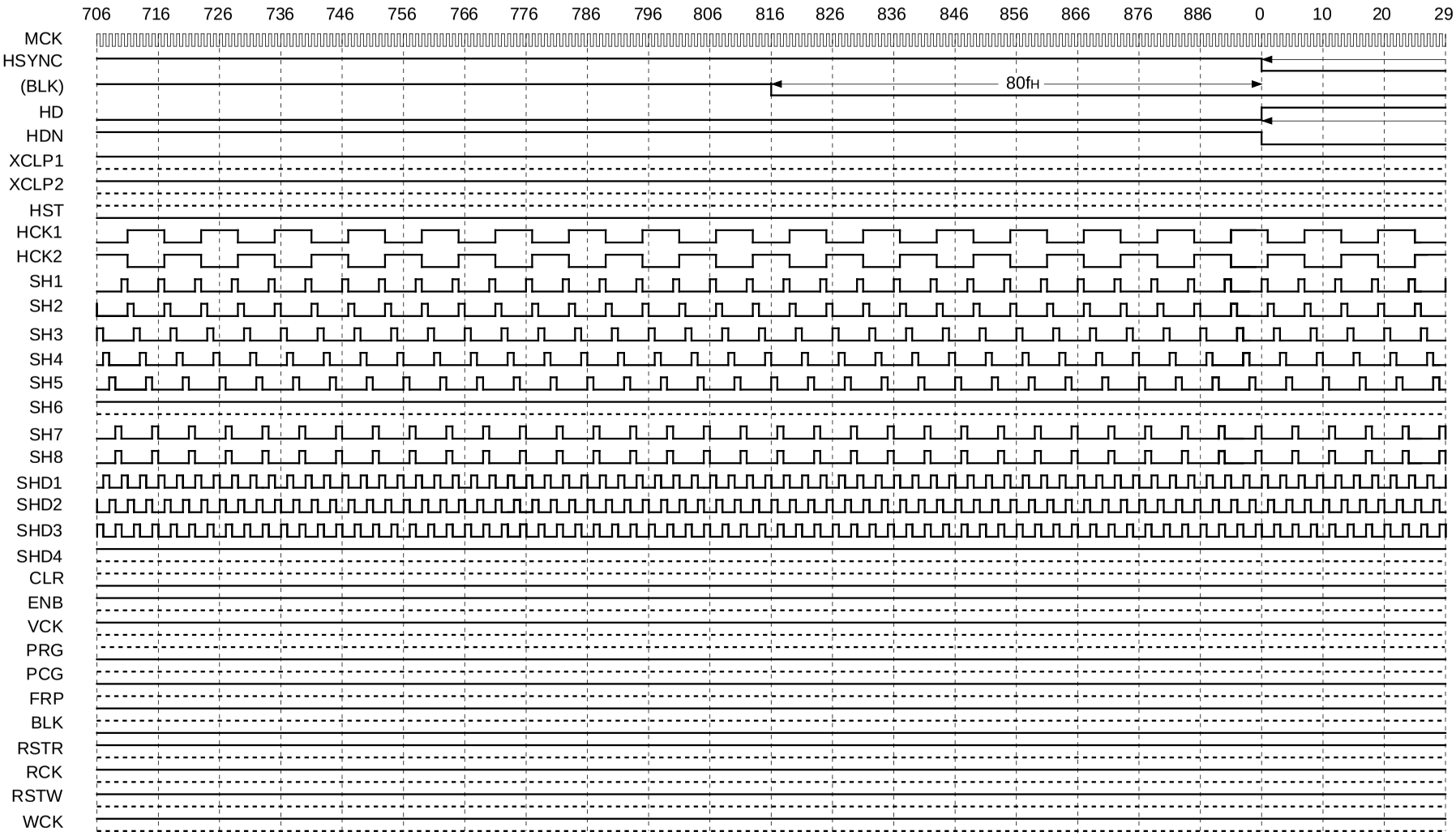


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX012BL VGA_1 640 × 480

RGT: H PLLP: LHHLHHHHHHL (LSB) HP: HLHHHHHH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

Loop Counter: 896f_H
MCK f: 31.333MHz (31.92ns)

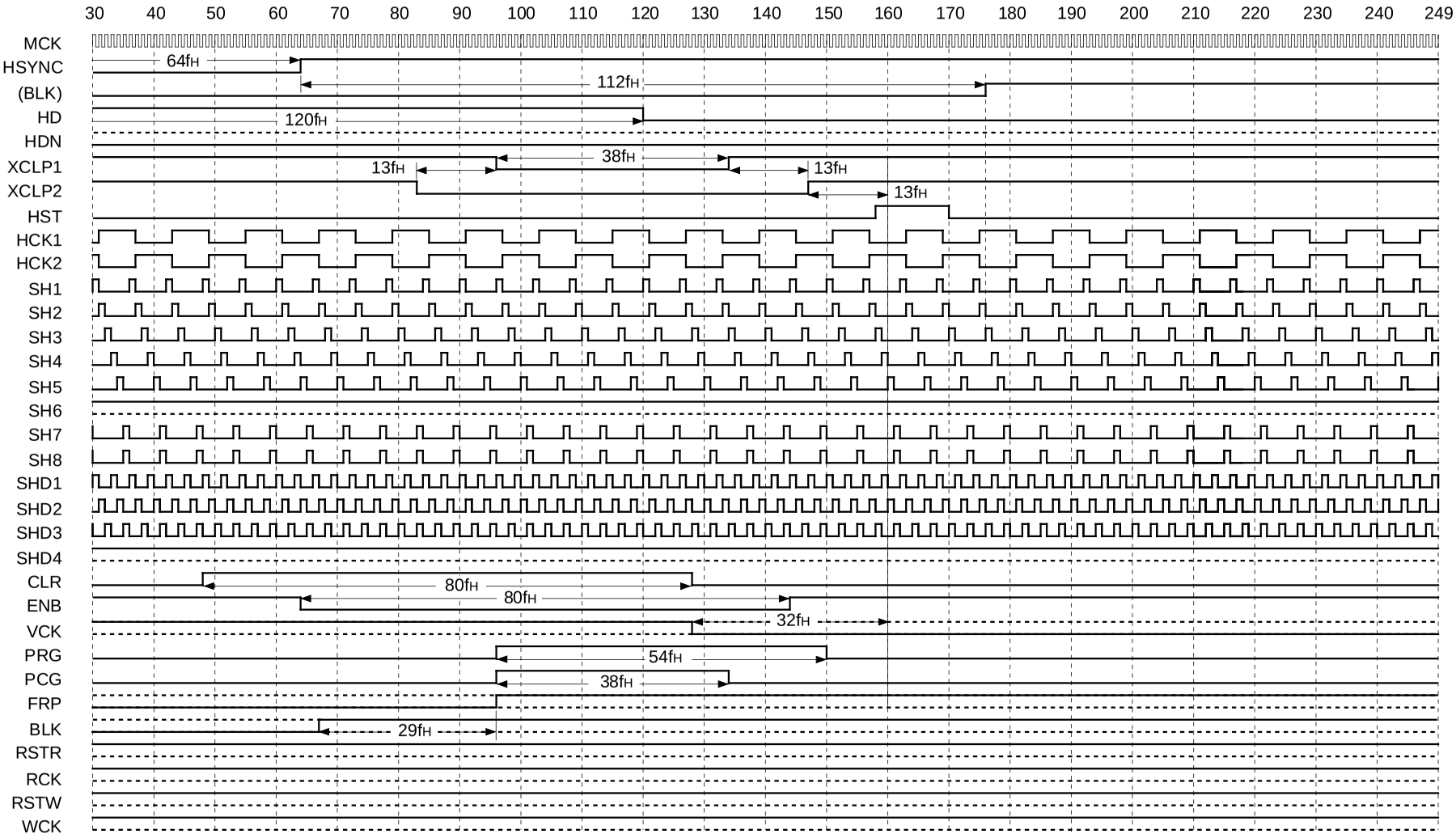


Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL VGA_2 640 × 480

RGT: H PLLP: LHHLHHHHHHL (LSB) HP: HLHHHHHH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

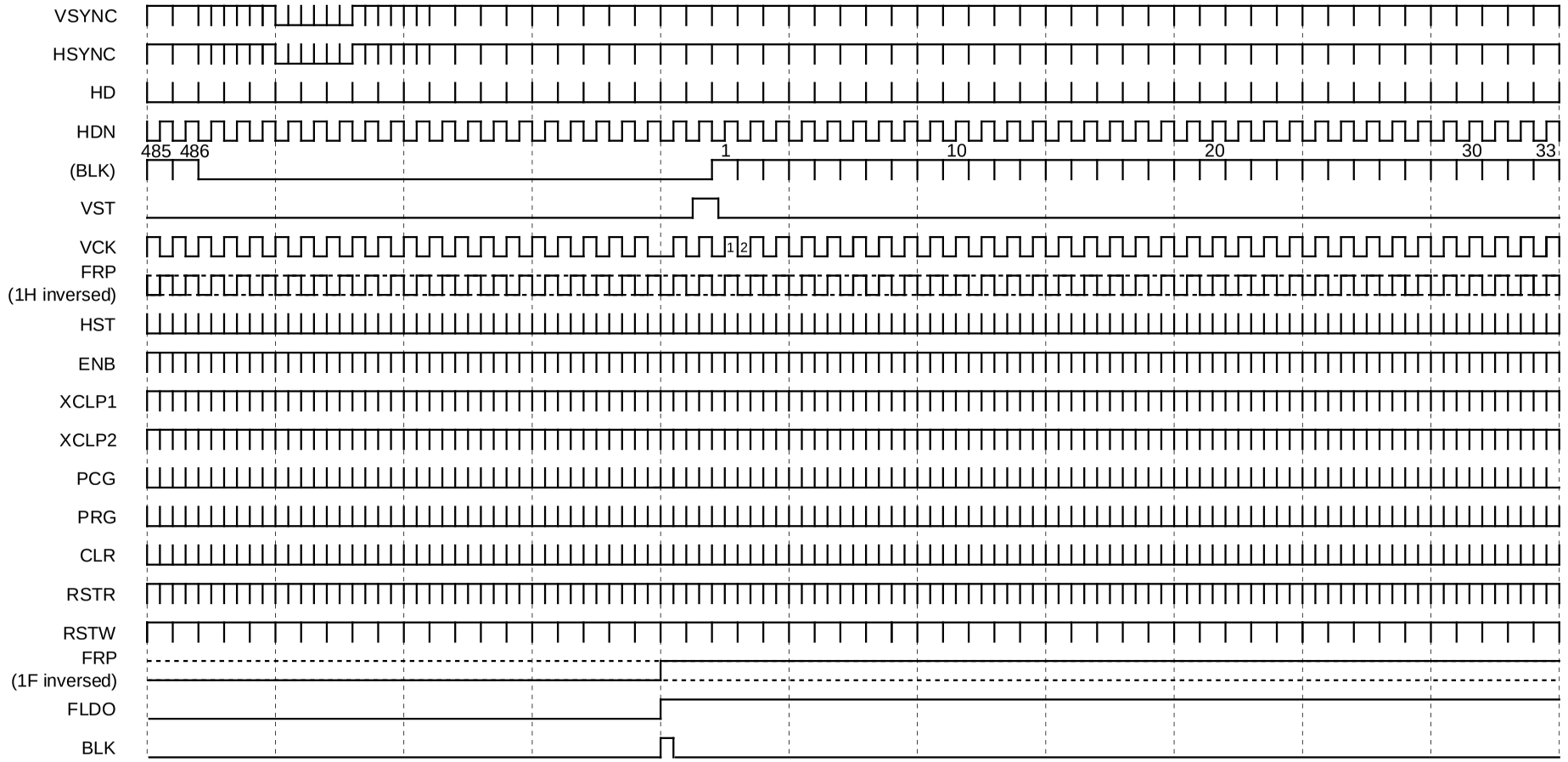
Loop Counter: 896f_H
MCK f: 31.333MHz (31.92ns)



Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL NTSC (ODD) 640 × 480

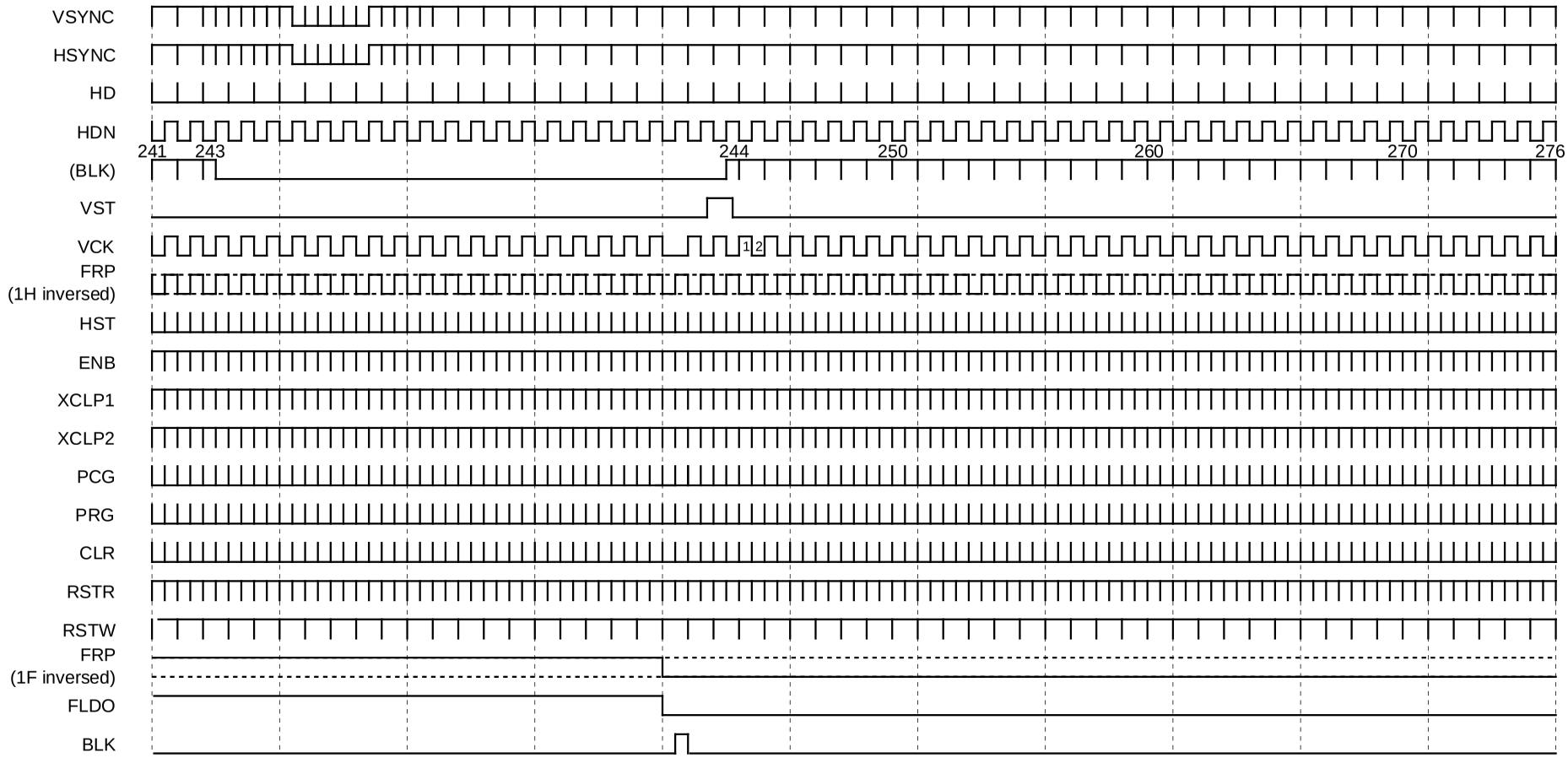
MODE3/2/1: H/H/L MODE: L DWN: H VP: LLLLHHLL (LSB) MBK2/1/0/A/B: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H



Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX012BL NTSC (EVEN) 640 × 480

MODE3/2/1: H/H/L MODE: L DWN: H VP: LLLLHHLL (LSB) MBK2/1/0/A/B: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H

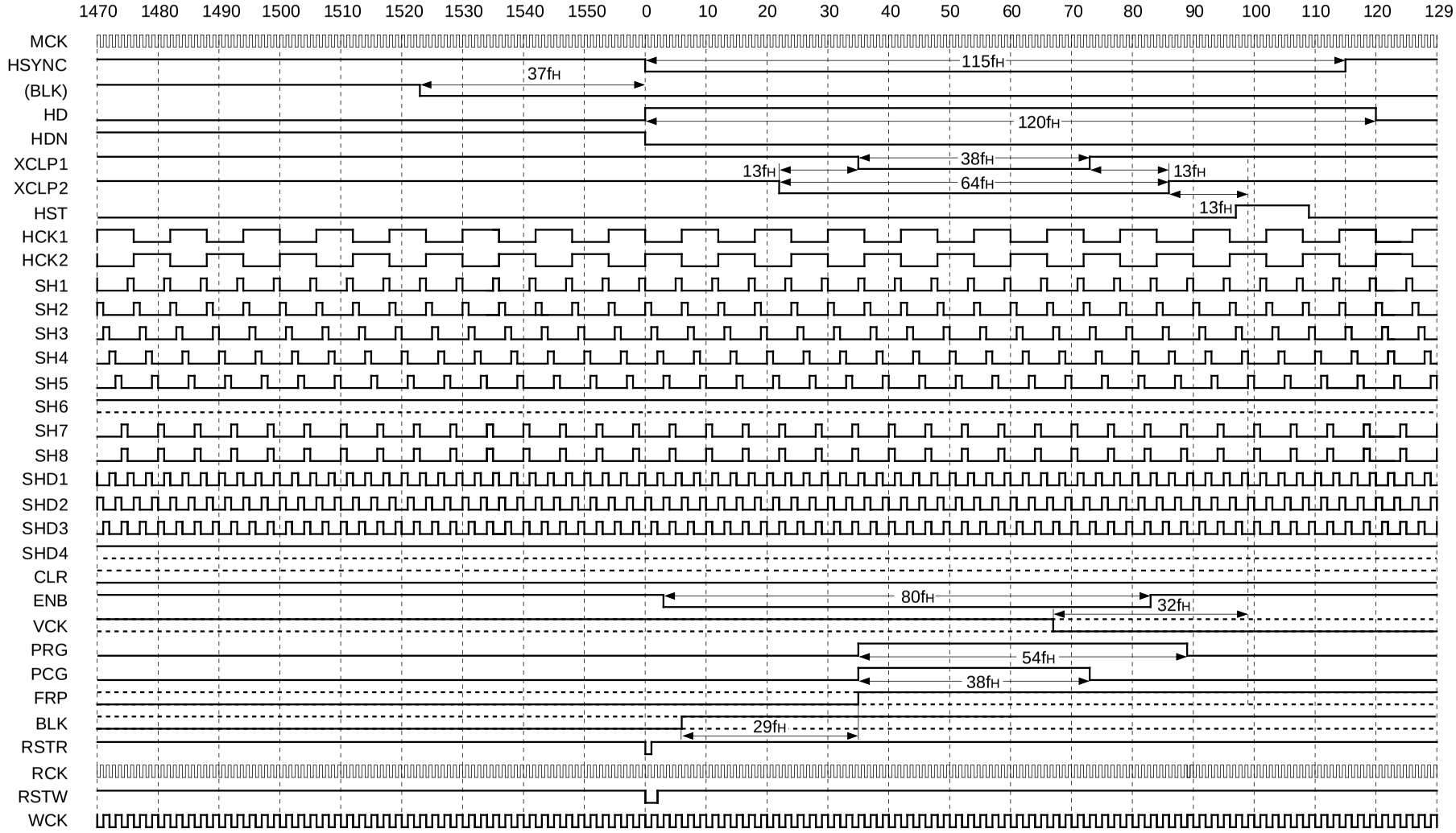


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX012BL NTSC_1 640 × 480

RGT: H PLLP: HHLLLLHLHHL (LSB) HP: HHHHHHLL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

Loop Counter: 1560fH
MCK f: 24.54MHz (40.75ns)

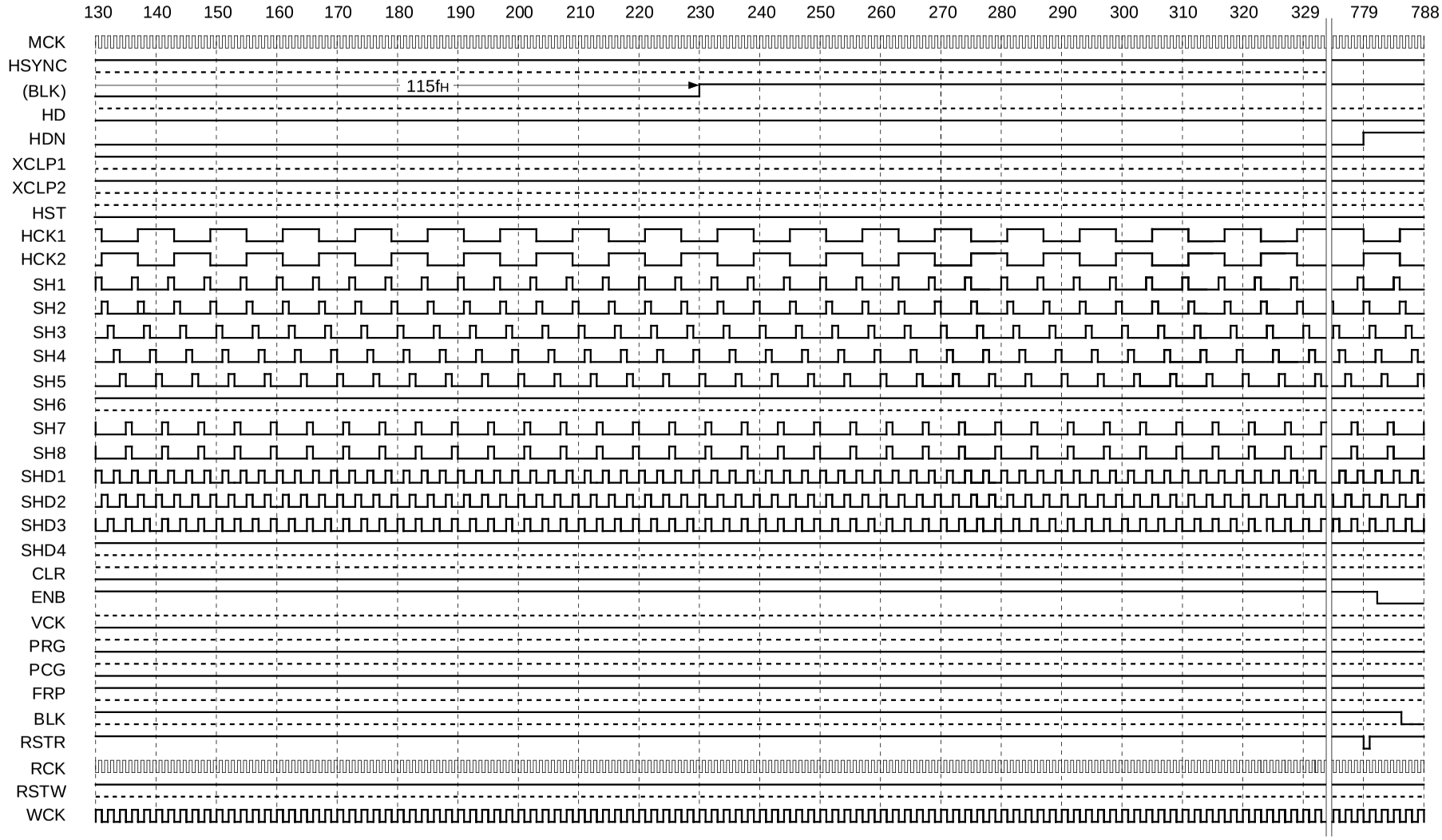


Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL NTSC_2 640 × 480

RGT: H PLLP: HHLLLLHLHHL (LSB) HP: HHHHHHLL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

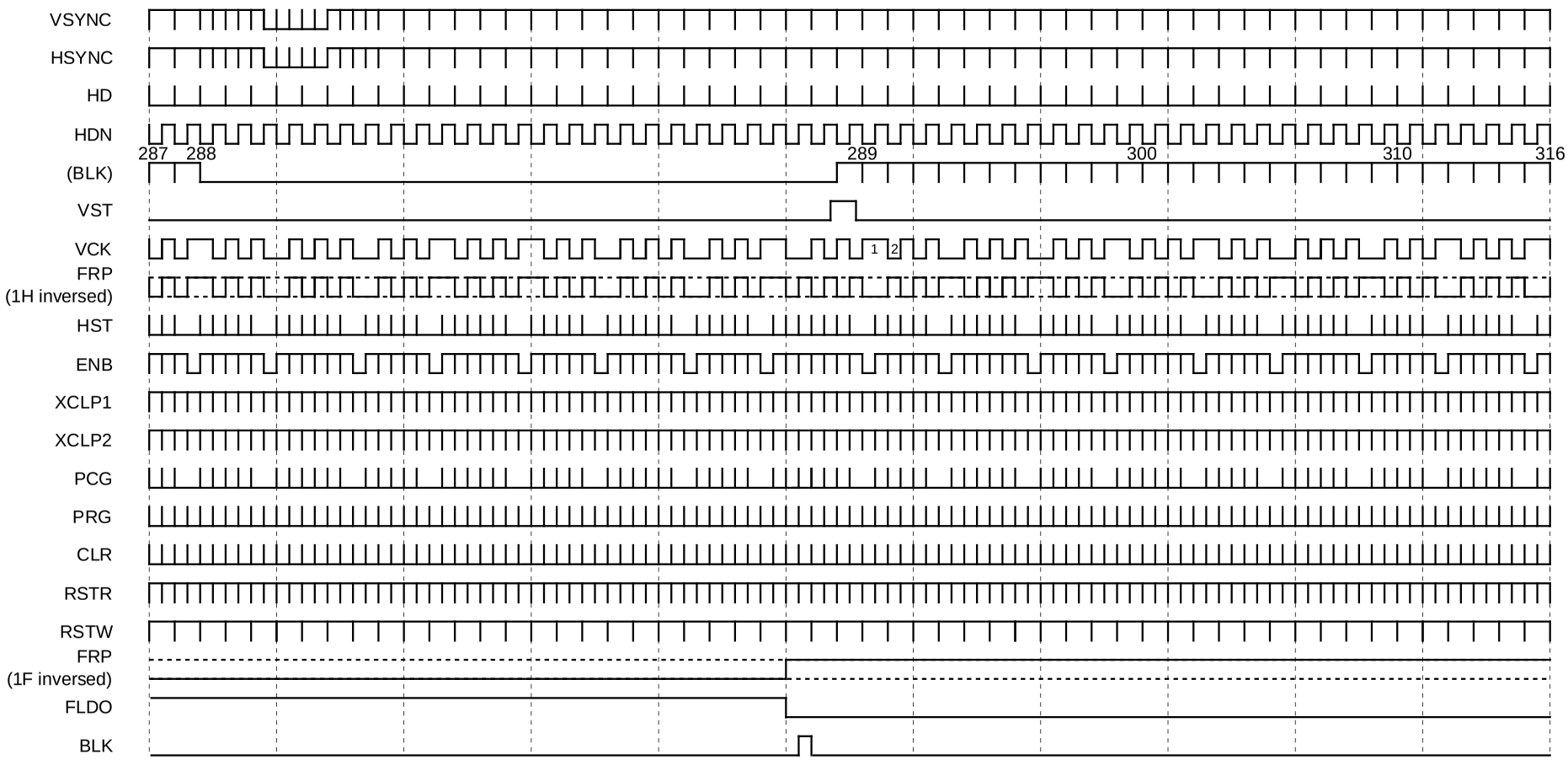
Loop Counter: 1560f_H
MCK f: 24.54MHz (40.75ns)



Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PAL (ODD) 640 × 480

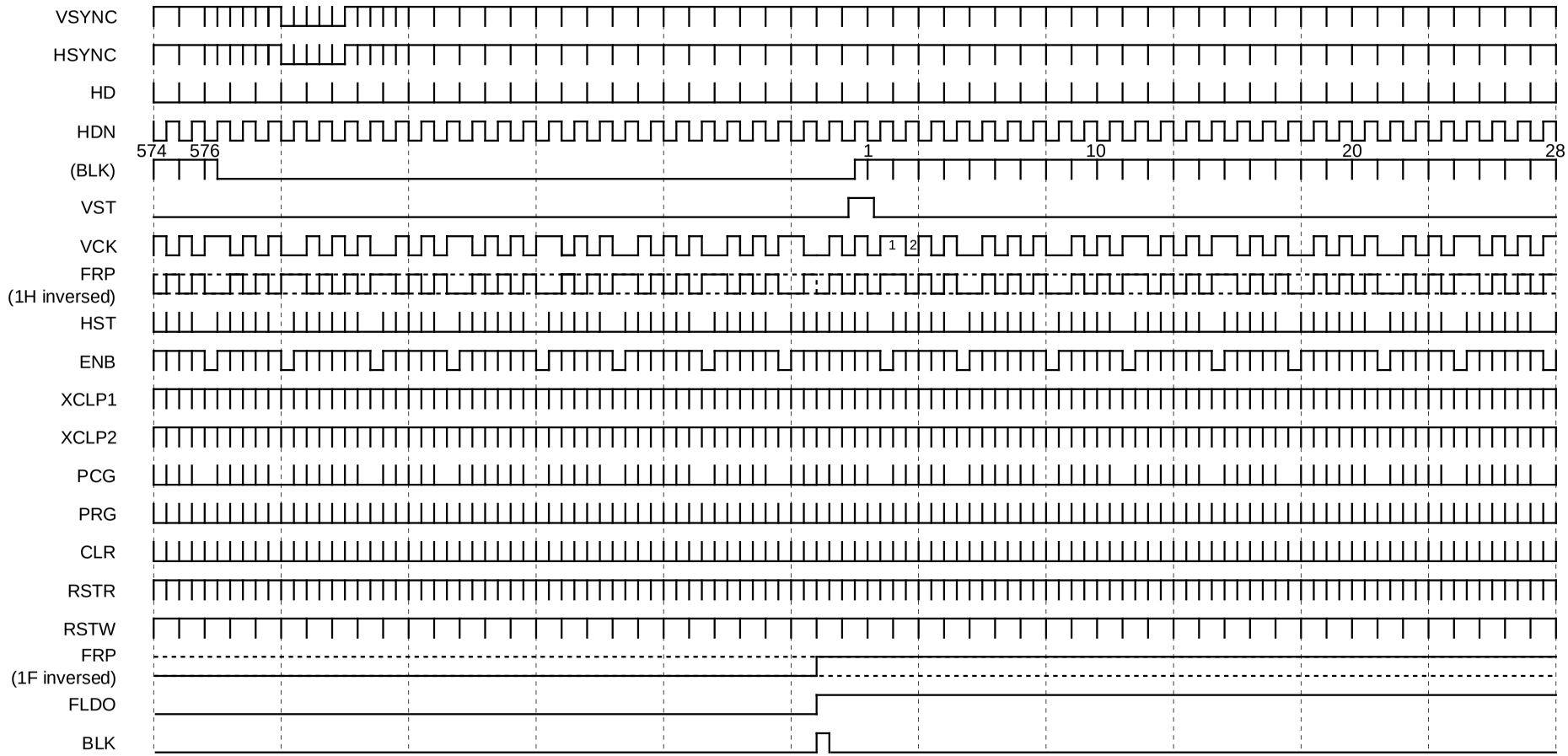
MODE3/2/1: H/H/L MODE: L DWN: H VP: LLLHLLHL (LSB) MBK2/1/0/A/B: H/L/L/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H



Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX012BL PAL (EVEN) 640 × 480

MODE3/2/1: H/H/L MODE: L DWN: H VP: LLLHLLHL (LSB) MBK2/1/0/A/B: H/L/L/L/L FRP1/0: H/H VPOL: L DSP: L PC98: H

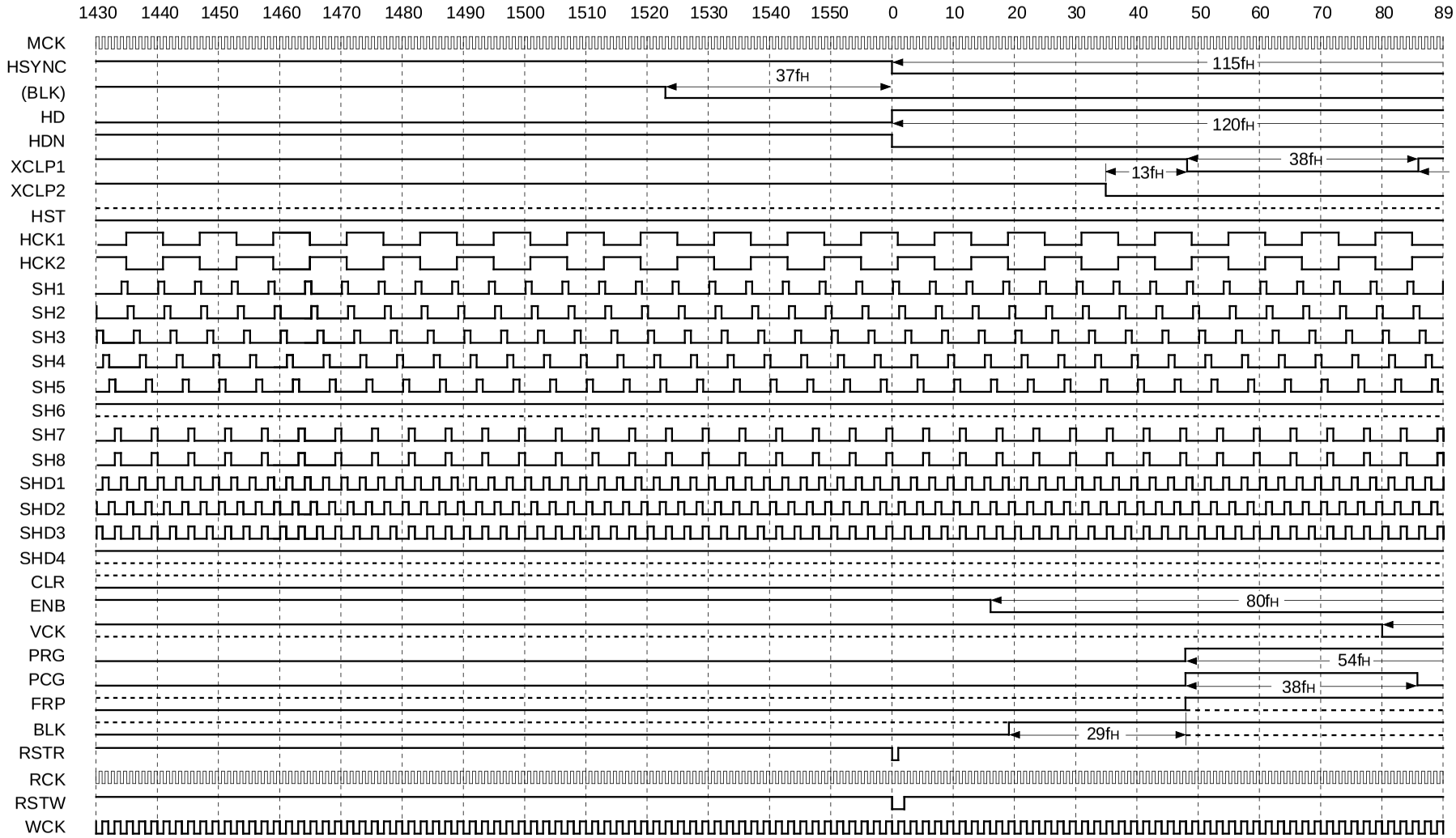


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP polarity is not specified.

LCX012BL PAL_1 640 × 480

RGT: H PLLP:HHLLLLHLHHL (LSB) HP: HHHLHHHH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

Loop Counter: 1560fH
MCK f: 24.38MHz (41.02ns)

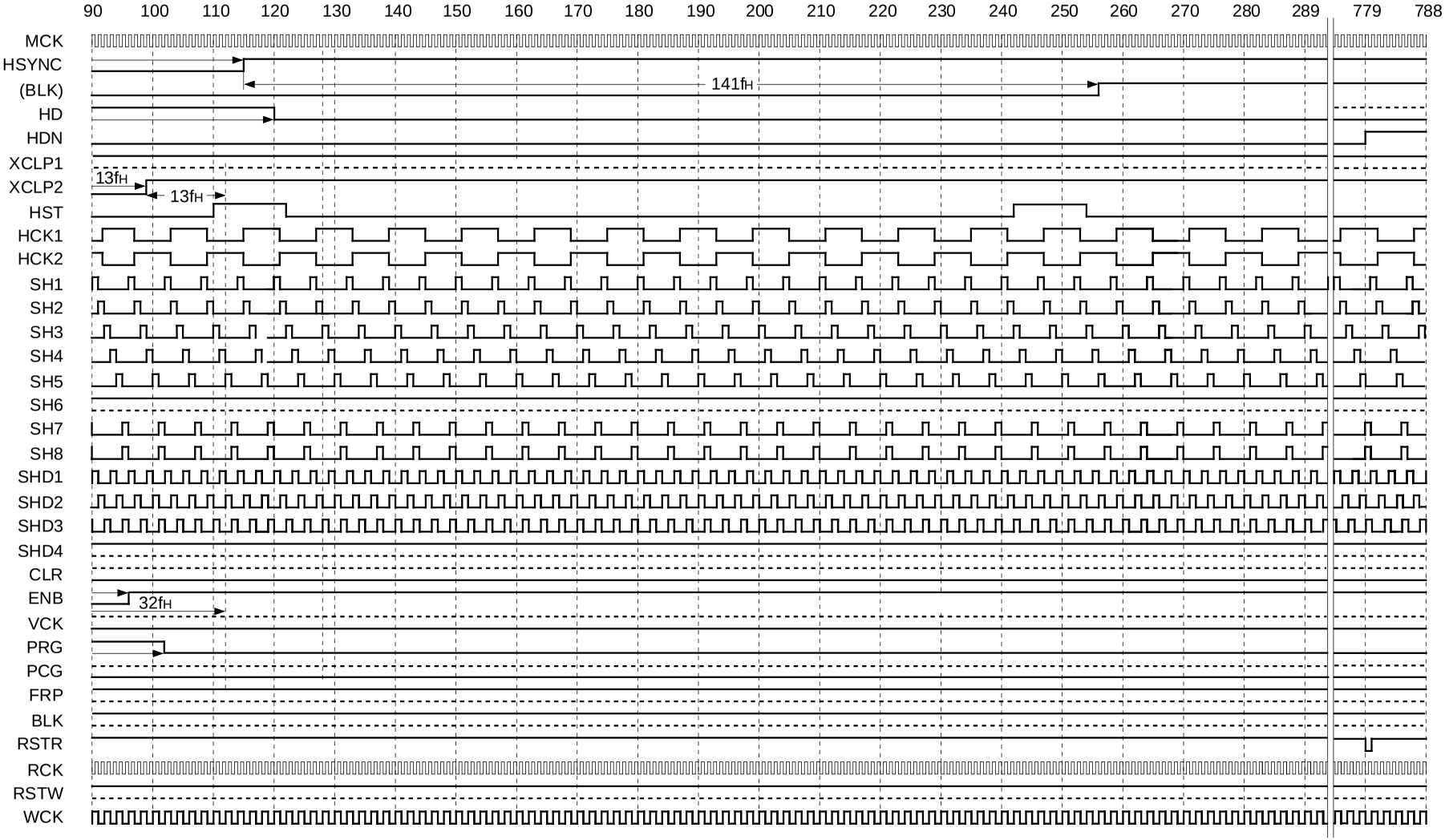


Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PAL_2 640 × 480

RGT: H PLLP: HHLLLLHLHHL (LSB) HP: HHHLHHHH (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: H HR: H HST: H PCG: H

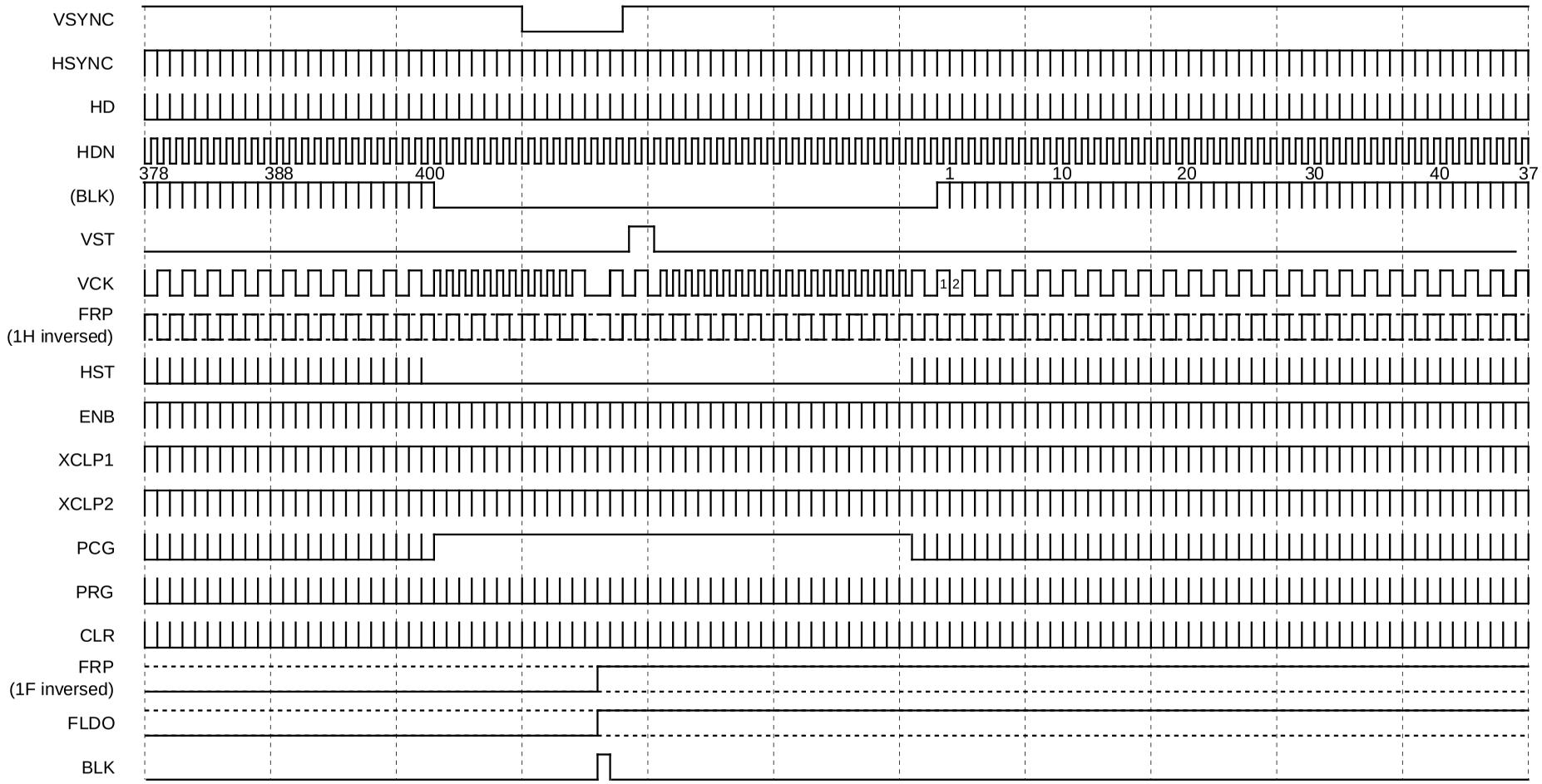
Loop Counter: 1560f_H
MCK f: 24.38MHz (41.02ns)



Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PC-98 640 × 400

MODE3/2/1: H/H/L MODE: L DWN: H VP: LLLLLHLL (LSB) MBK2/1/0/A/B: H/H/H/L/L FRP1/0: H/H VPOL: L DSP: H PC98: L

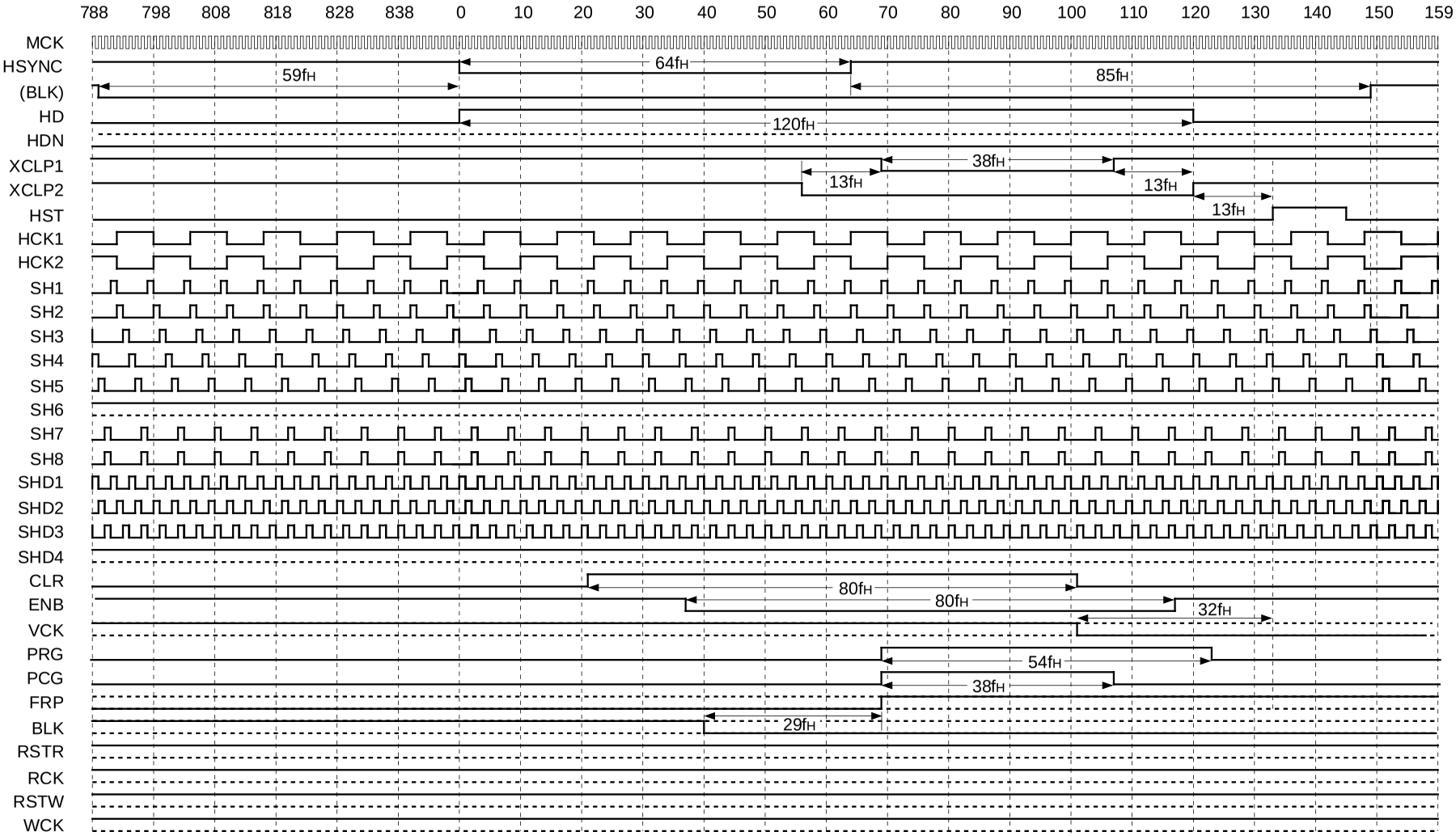


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX012BL PC-98 640 × 400

RGT: H PLLP: LHHLHLLHHHL (LSB) HP: HHLHHLHL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

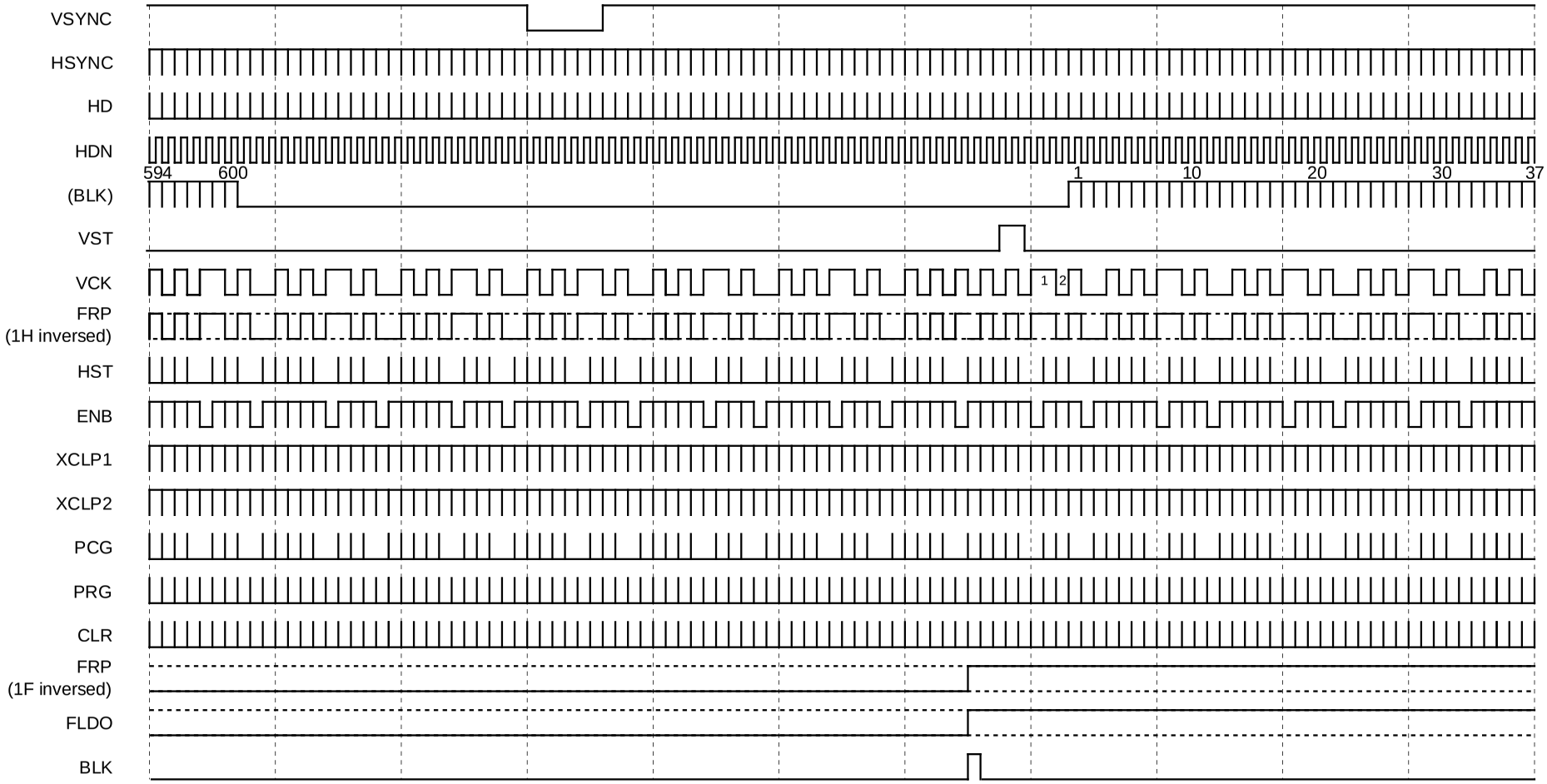
Loop Counter: 848fH
MCK f: 21.05MHz (47.50ns)



Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL SVGA 640 × 480

MODE3/2/1: H/H/L MODE: L DWN: H VP: LLHLLLLH (LSB) MBK2/1/0/A/B: H/H/L/L/L FRP1/0: H/H VPOL: L DSP: H PC98: H HPOL: L

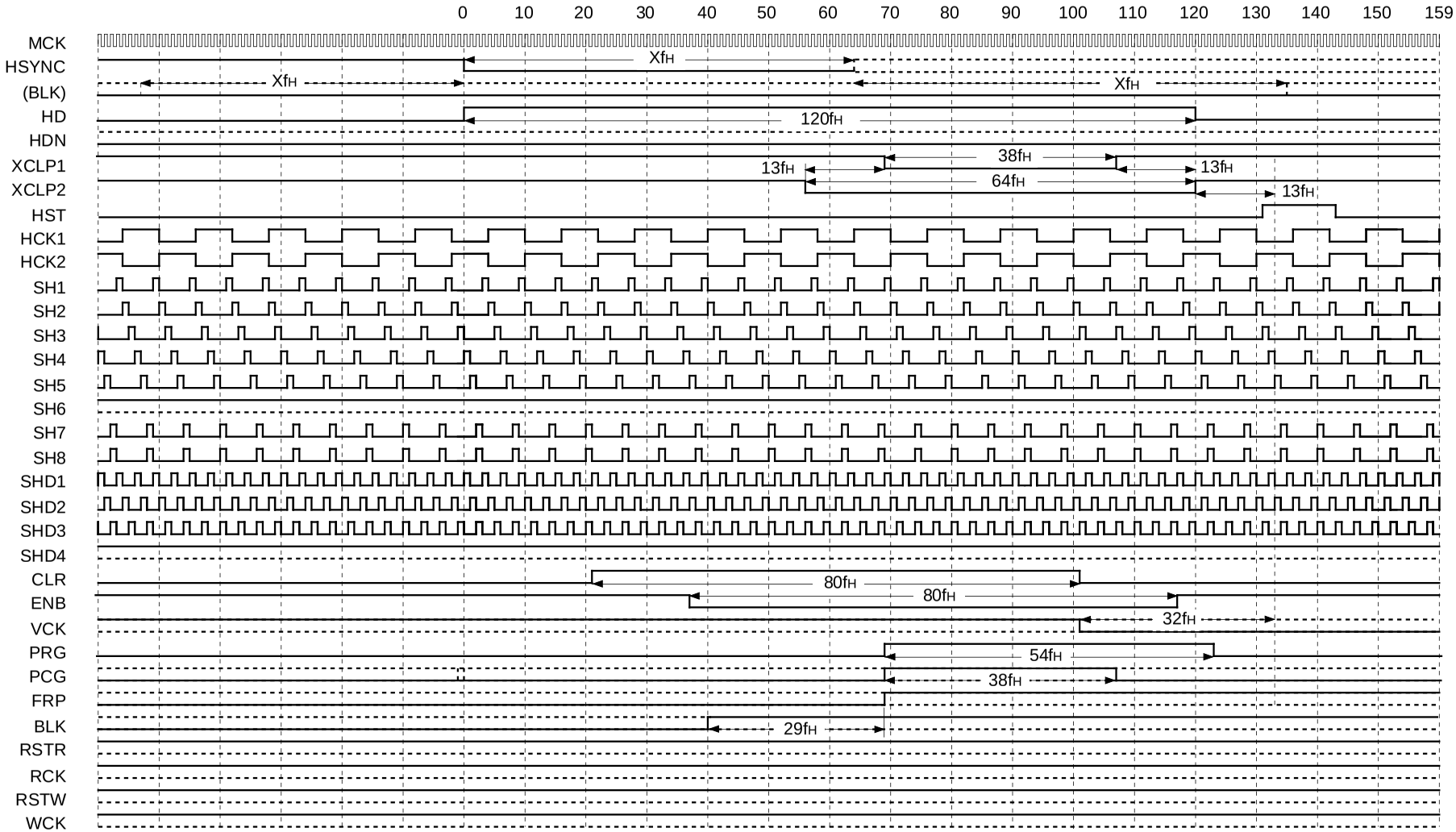


Note) When DWN is Low, VST is inversed.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The 1H and 1V cycle FRP and FLDO polarity are not specified.

LCX012BL SVGA 640 × 480

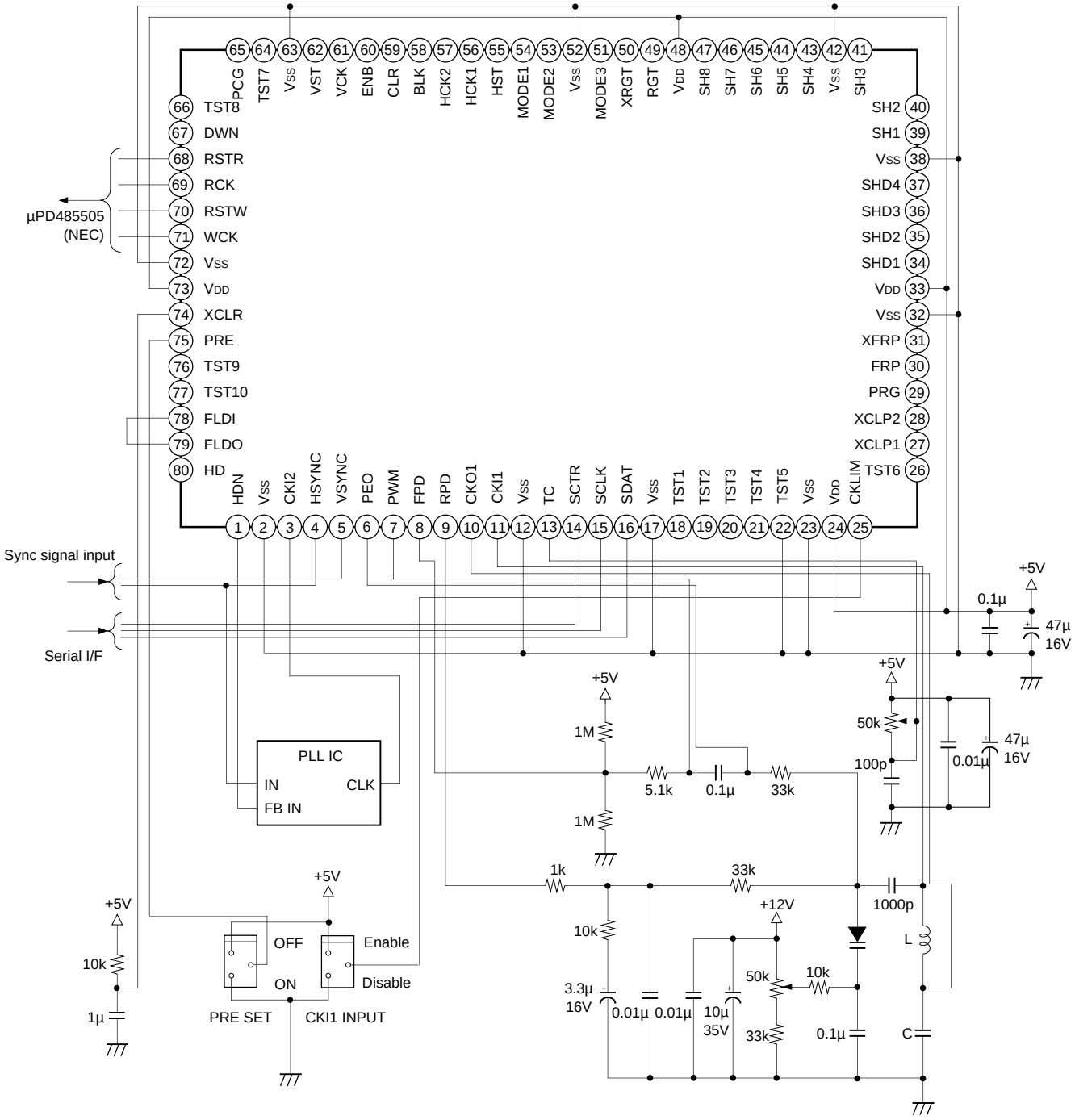
RGT: H HP: HHLHHLHL (LSB) HDNP: LLLLL (LSB) SHP: LLLLLLL (LSB) HCKP: LLLL (LSB)
HSTP: LLLH (LSB) CLPP: LL (LSB) SHD2/1/0: L/H/H SH2/1/0: H/L/H HPOL: L CK: L HR: H HST: H PCG: H

Loop Counter: 2048fH >
MCK f: 32MHz (31.25ns) >



Note) When RGT is Low, pulses SH1, 2, 3 are switched with SH6, 5, 4, and SHD1 with SHD3.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
The SVGA (LCX012BL) mode timing changes according to the signal processing (H direction) method.

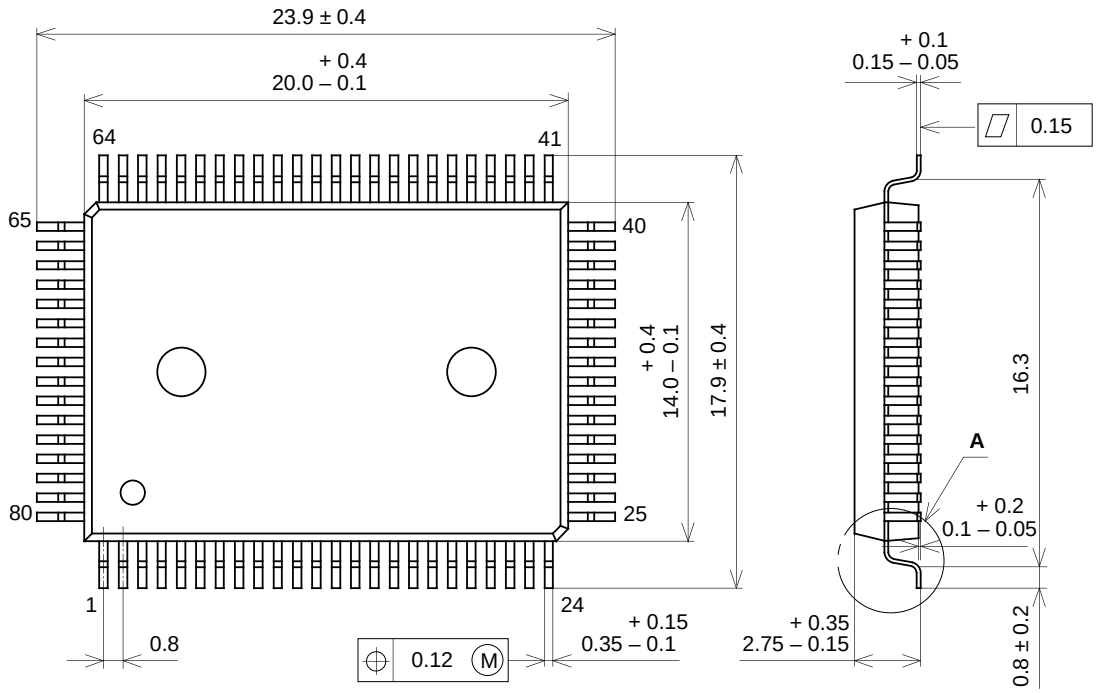
Application Circuit

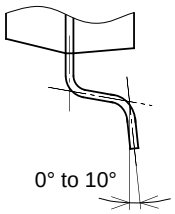


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g