SONY

CXD2498R

Timing Generator for Frame Readout CCD Image Sensor

Description

The CXD2498R is a timing generator IC which generates the timing pulses for performing frame readout using the ICX282 CCD image sensor.

Features

- Base oscillation frequency 45MHz
- Electronic shutter function
- Supports various drive modes such as draft and AF mode
- Horizontal driver for CCD image sensor
- Vertical driver for CCD image sensor

Applications

Digital still cameras

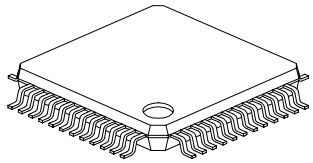
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX282 (Type 2/3, 5070K pixels)

48 pin LQFP (Plastic)



Absolute Maximum Ratings

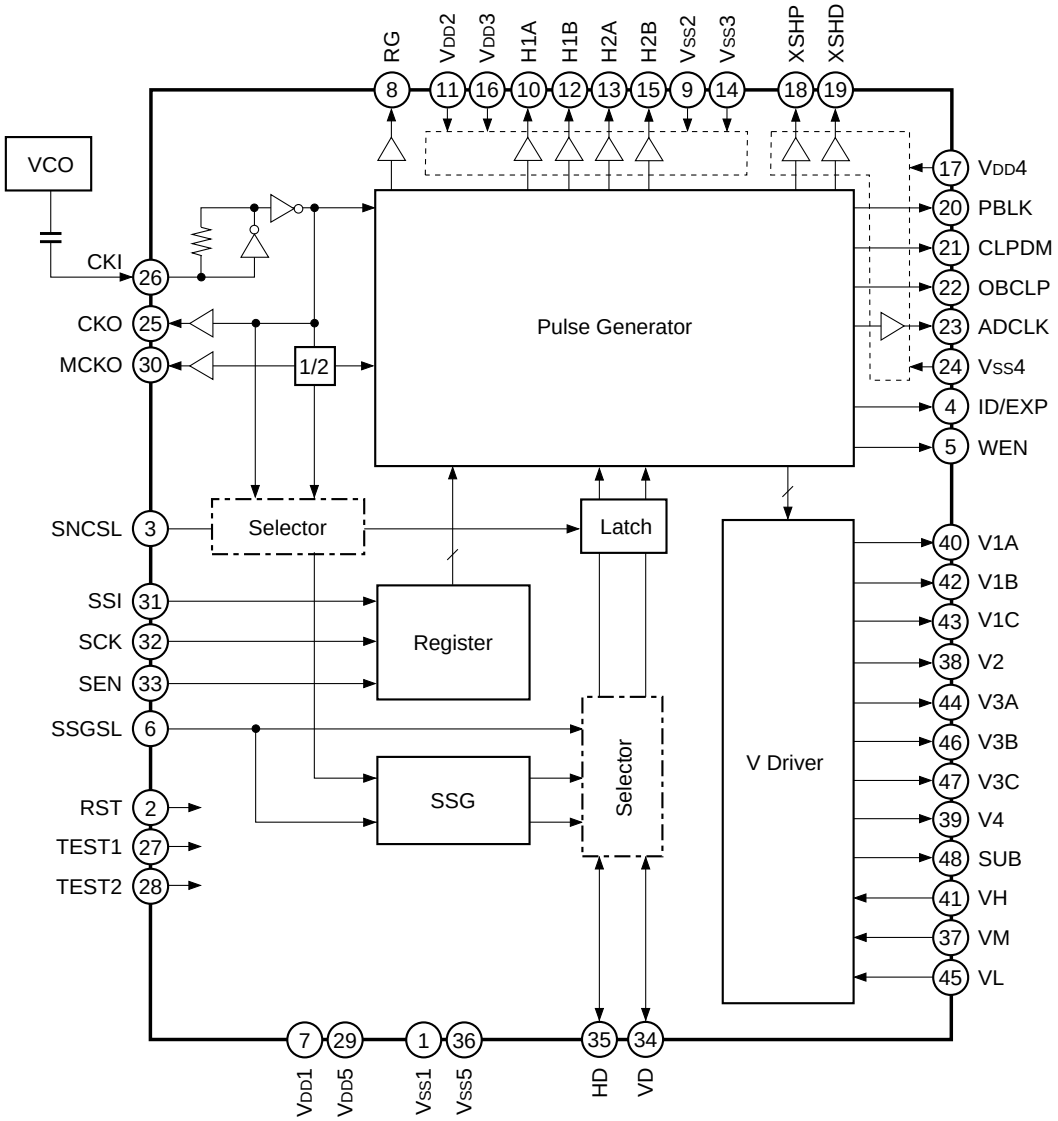
• Supply voltage	V_{DD}	V_{SS} – 0.3 to +7.0	V
	VL	–10.0 to V_{SS}	V
	VH	VL – 0.3 to +26.0	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_{O1}	V_{SS} – 0.3 to V_{DD} + 0.3	V
	V_{O2}	VL – 0.3 to V_{SS} + 0.3	V
	V_{O3}	VL – 0.3 to VH + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

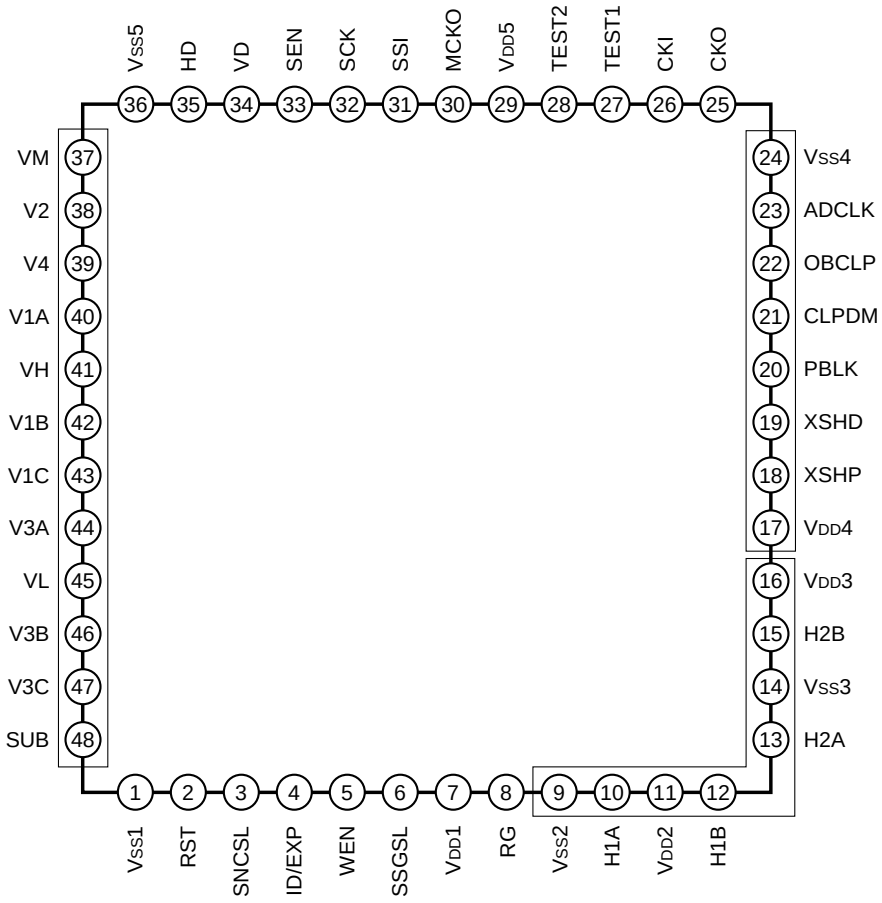
• Supply voltage			
	V_{DD}a, V_{DD}b, V_{DD}c	3.0 to 3.6	V
	VM	0.0	V
	VH	14.5 to 15.5	V
	VL	–7.0 to –8.0	V
• Operating temperature			
	Topr	–20 to +75	°C

E00X63-PS

Block Diagram



Pin Configuration



* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{SS}1$	—	GND
2	RST	I	Internal system reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input
3	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync With pull-down resistor
4	ID/EXP	O	Vertical direction line identification pulse output/exposure time identification pulse output. Switching possible using the serial interface data. (Default: ID)
5	WEN	O	Memory write timing pulse output.
6	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External sync valid With pull-down resistor
7	$V_{DD}1$	—	3.3V power supply. (Power supply for common logic block)
8	RG	O	CCD reset gate pulse output.
9	$V_{SS}2$	—	GND
10	H1A	O	CCD horizontal register clock output.
11	$V_{DD}2$	—	3.3V power supply. (Power supply for H block)
12	H1B	O	CCD horizontal register clock output.
13	H2A	O	CCD horizontal register clock output.
14	$V_{SS}3$	—	GND
15	H2B	O	CCD horizontal register clock output.
16	$V_{DD}3$	—	3.3V power supply. (Power supply for H block)
17	$V_{DD}4$	—	3.3V power supply. (Power supply for CDS block)
18	XSHP	O	CCD precharge level sample-and-hold pulse output.
19	XSHD	O	CCD data level sample-and-hold pulse output.
20	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
21	CLPDM	O	CCD dummy signal clamp pulse output.
22	OBCLP	O	CCD optical black signal clamp pulse output. The horizontal OB pattern can be changed using the serial interface data.
23	ADCLK	O	Clock output for analog/digital conversion IC. Logical phase adjustment possible using the serial interface data.
24	$V_{SS}4$	—	GND
25	CKO	O	Inverter output.
26	CKI	I	Inverter input.
27	TEST1	I	IC test pin 1; normally fixed to GND. With pull-down resistor
28	TEST2	I	IC test pin 2; normally fixed to GND. With pull-down resistor
29	$V_{DD}5$	—	3.3V power supply. (Power supply for common logic block)
30	MCKO	O	System clock output for signal processing IC.
31	SSI	I	Serial interface data input for internal mode settings. Schmitt trigger input

Pin No.	Symbol	I/O	Description
32	SCK	I	Serial interface clock input for internal mode settings. Schmitt trigger input
33	SEN	I	Serial interface strobe input for internal mode settings. Schmitt trigger input
34	VD	I/O	Vertical sync signal input/output.
35	HD	I/O	Horizontal sync signal input/output.
36	$V_{SS}5$	—	GND
37	VM	—	GND (GND for vertical driver)
38	V2	O	CCD vertical register clock output.
39	V4	O	CCD vertical register clock output.
40	V1A	O	CCD vertical register clock output.
41	VH	—	15.0V power supply. (Power supply for vertical driver)
42	V1B	O	CCD vertical register clock output.
43	V1C	O	CCD vertical register clock output.
44	V3A	O	CCD vertical register clock output.
45	VL	—	–7.5V power supply. (Power supply for vertical driver)
46	V3B	O	CCD vertical register clock output.
47	V3C	O	CCD vertical register clock output.
48	SUB	O	CCD electronic shutter pulse output.

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{DD}2$, $V_{DD}3$	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	$V_{DD}4$	$V_{DD}b$		3.0	3.3	3.6	V
Supply voltage 3	$V_{DD}1$, $V_{DD}5$	$V_{DD}c$		3.0	3.3	3.6	V
Input voltage 1*1	RST, SSI, SCK, SEN	V_{t+}		0.8$V_{DD}c$			V
		V_{t-}				0.2$V_{DD}c$	V
Input voltage 2*2	TEST1, TEST2, SNCSL, SSGSL	V_{IH1}		0.7$V_{DD}c$			V
		V_{IL1}				0.2$V_{DD}c$	V
Input/output voltage	VD, HD	V_{IH2}		0.8$V_{DD}c$			V
		V_{IL2}				0.2$V_{DD}c$	V
		V_{OH1}	Feed current where I_{OH} = –1.2mA	$V_{DD}c$ – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 1	H1A, H1B, H2A, H2B	V_{OH2}	Feed current where I_{OH} = –22.0mA	$V_{DD}a$ – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 14.4mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	$V_{DD}c$ – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4 mA			0.4	V
Output voltage 3	XSHP, XSHD, PBLK, OBCLP, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	$V_{DD}b$ – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	CKO	V_{OH5}	Feed current where I_{OH} = –6.9mA	$V_{DD}c$ – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 5	MCKO	V_{OH6}	Feed current where I_{OH} = –3.3mA	$V_{DD}c$ – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 6	ID/EXP, WEN	V_{OH7}	Feed current where I_{OH} = –2.4mA	$V_{DD}c$ – 0.8			V
		V_{OL7}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output current 1	V1A, V1B, V1C, V3A, V3B, V3C, V2, V4	I_{OL}	V1A/B/C, V2, V3A/B/C, V4 = –8.25V	10.0			mA
		I_{OM1}	V1A/B/C, V2, V3A/B/C, V4 = –0.25V			–5.0	mA
		I_{OM2}	V1A/B/C, V3A/B/C = 0.25V	5.0			mA
		I_{OH}	V1A/B/C, V3A/B/C = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 This input pin is a schmitt trigger input.

*2 This input pin is with pull-down registor in the IC.

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DDC}/2$		V
Input voltage		V_{IH}		$0.7V_{DDC}$			V
		V_{IL}				$0.3V_{DDC}$	V
Input amplitude		V_{IN}	fmax = 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source.
Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

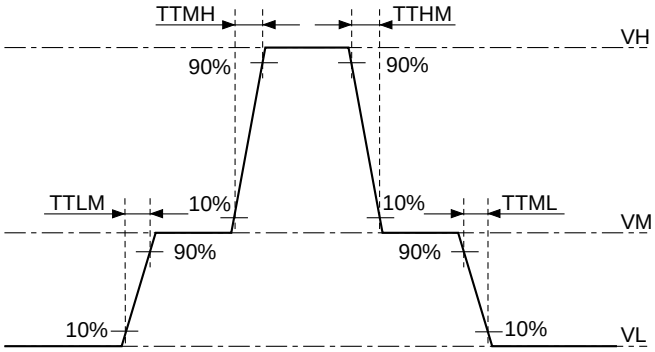
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

Note)

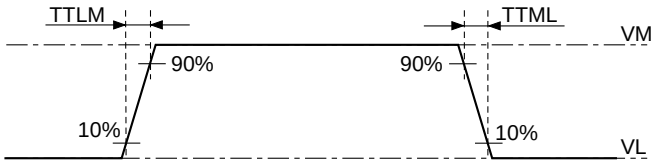
1) The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2) For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3) To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

Switching Waveforms

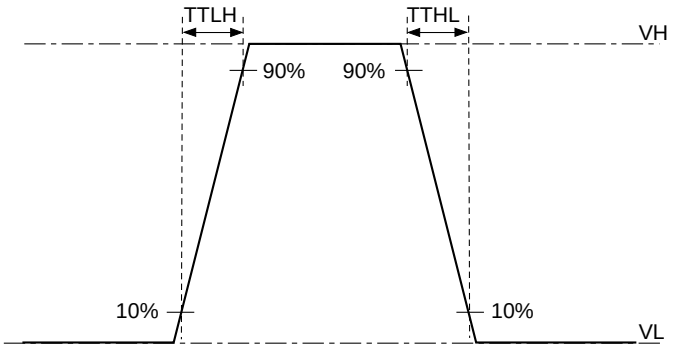
V1A (V1B, V1C, V3A, V3B, V3C)



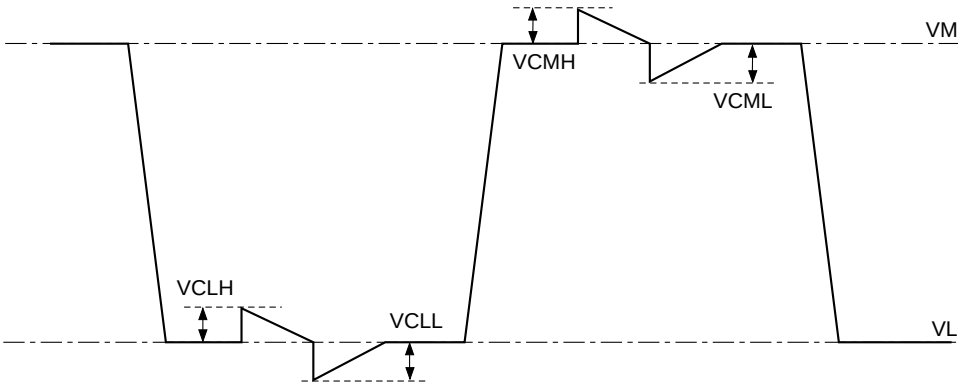
V2 (V4)



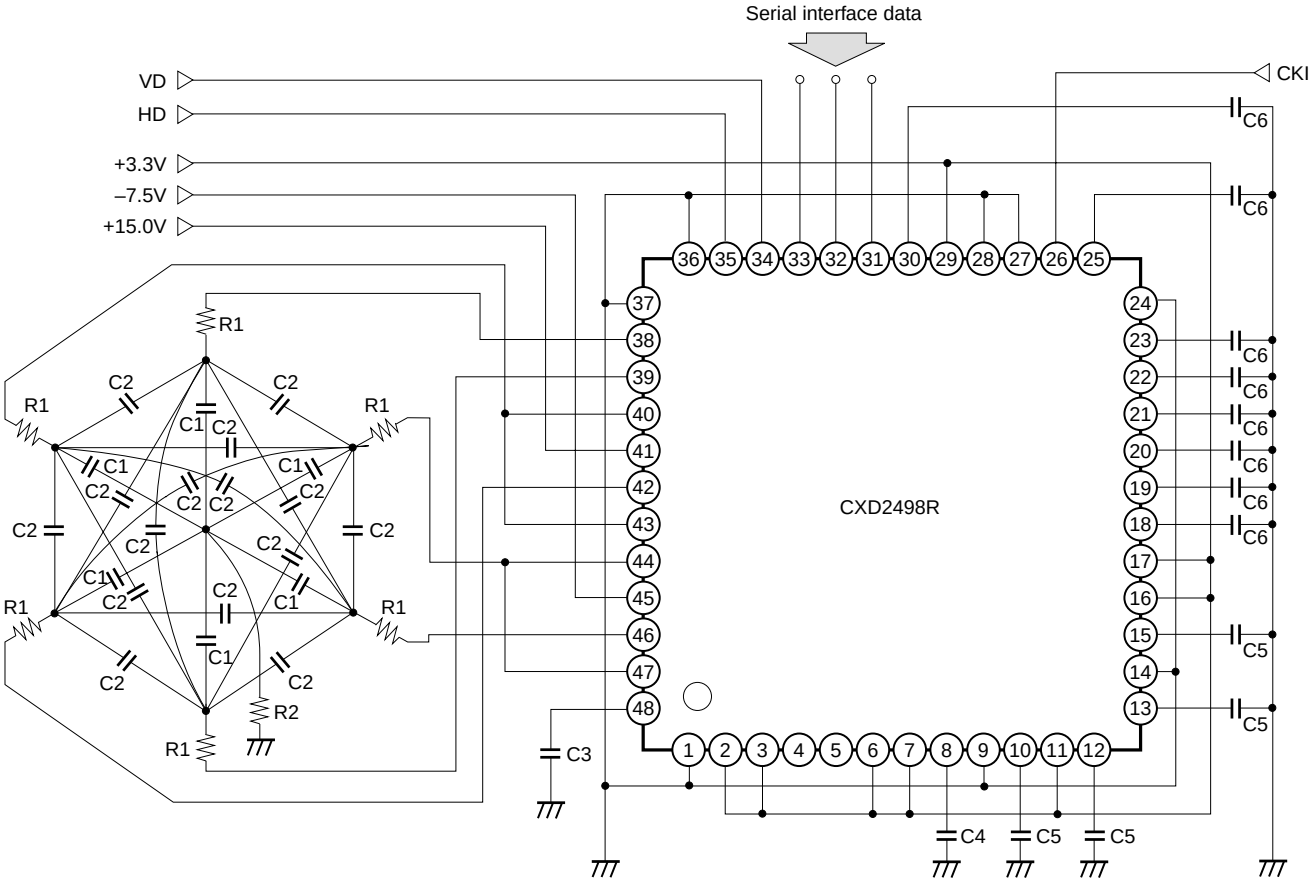
SUB



Waveform Noise



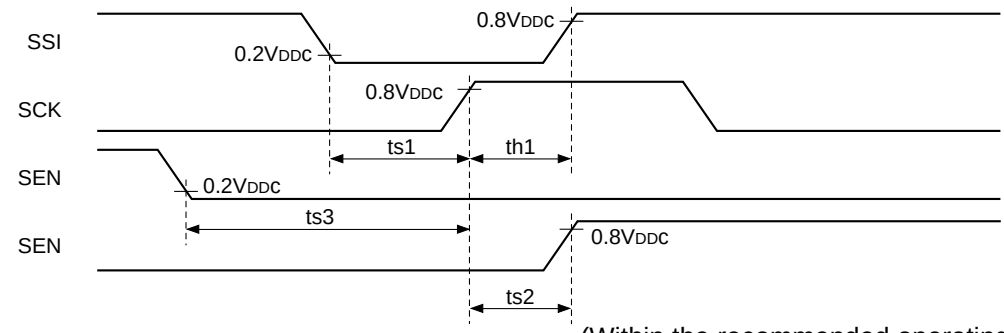
Measurement Circuit



C1: 3300pF C2: 560pF C3: 820pF C4: 8pF C5: 320pF C6: 10pF
R1: 30Ω R2: 10Ω

AC Characteristics

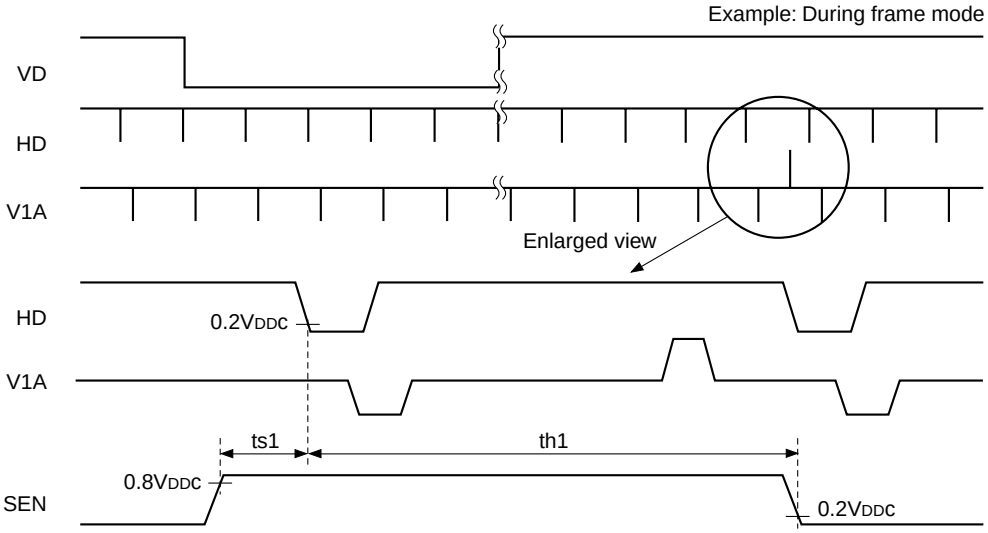
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SCK	20			ns
th1	SSI hold time, activated by the rising edge of SCK	20			ns
ts2	SCK setup time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SCK	20			ns

Serial interface clock internal loading characteristics (1)



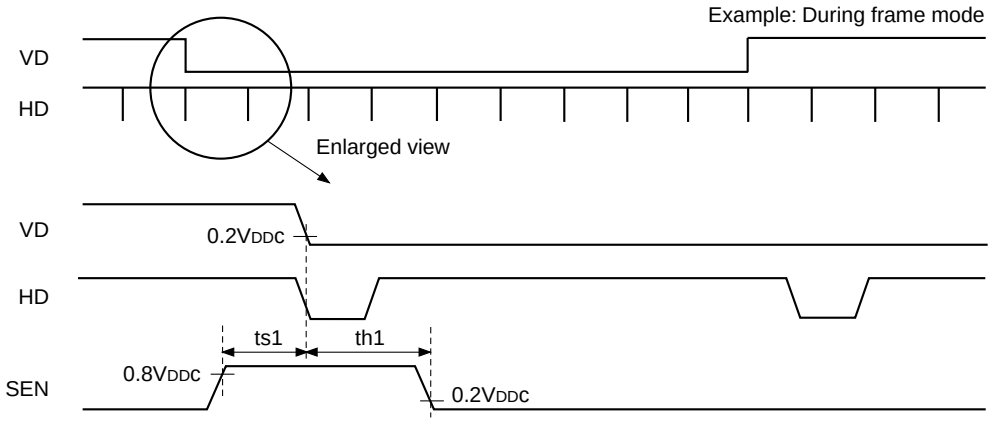
* Be sure to maintain a constantly high SEN logic level near the falling edge of the HD in the horizontal period during which V1A/B/C and V3A/B/C values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of HD	0			ns
th1	SEN hold time, activated by the falling edge of HD	134			µs

* Restriction in draft mode with an operating frequency of 22.5MHz.

Serial interface clock internal loading characteristics (2)



* Be sure to maintain a constantly high SEN logic level near the falling edge of VD.

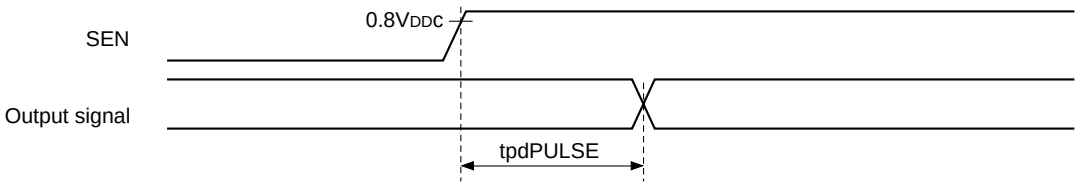
(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of VD	0			ns
th1	SEN hold time, activated by the falling edge of VD	200			ns

* Restriction with an operating frequency of 22.5MHz.

Serial interface clock output variation characteristics

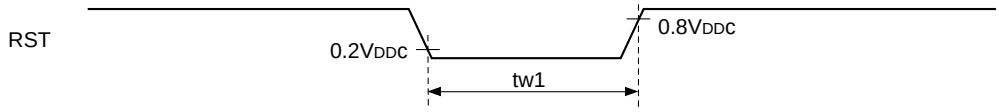
Normally, the serial interface data is loaded to the CXD2498R at the timing shown in “Serial interface clock internal loading characteristics (1)” above. However, one exception to this is when the data such as STB is loaded to the CXD2498R and controlled at the rising edge of SEN. See ”Description of Operation”.



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Uniy
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		70	ns

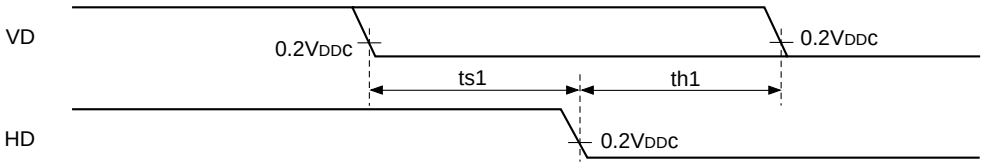
RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	22			ns

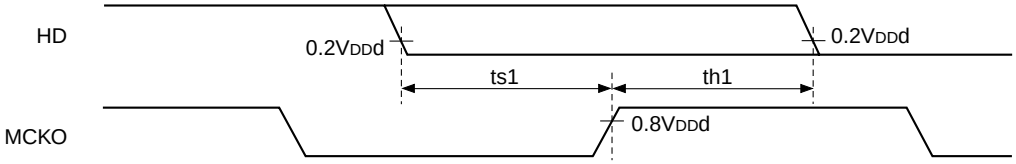
VD and HD phase characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VD setup time, activated by the falling edge of HD	0			ns
th1	VD hold time, activated by the falling edge of HD			44	ns

HD loading characteristics

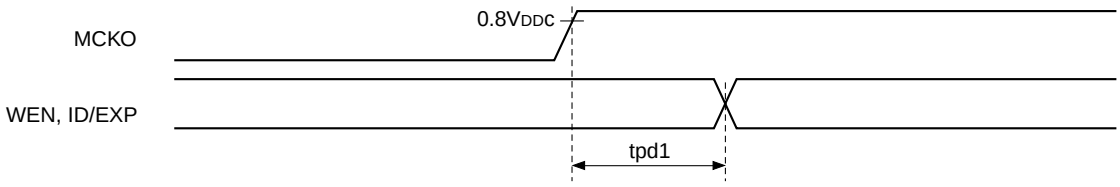


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	HD setup time, activated by the rising edge of MCKO	31			ns
th1	HD hold time, activated by the rising edge of MCKO	0			ns

Output variation characteristics



WEN and ID/EXP load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	23		33	ns

Description of Operation

Pulses output from the CXD2498R are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on the following pages.

Pin Status Table

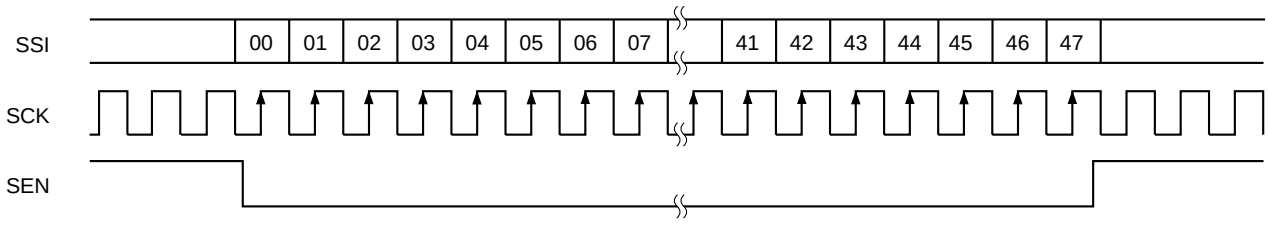
Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
1	$V_{SS}1$	—				25	CKO	ACT	ACT	L	ACT
2	RST	ACT	ACT	ACT	L	26	CKI	ACT	ACT	ACT	ACT
3	SNCSL	ACT	ACT	ACT	ACT	27	TEST1	—			
4	ID/EXP	ACT	L	L	L	28	TEST2	—			
5	WEN	ACT	L	L	L	29	VDD5	—			
6	SSGSL	ACT	ACT	ACT	ACT	30	MCKO	ACT	ACT	L	ACT
7	$V_{DD}1$	—				31	SSI	ACT	ACT	ACT	DIS
8	RG	ACT	L	L	ACT	32	SCK	ACT	ACT	ACT	DIS
9	$V_{SS}2$	—				33	SEN	ACT	ACT	ACT	DIS
10	H1A	ACT	L	L	ACT	34	VD*1	ACT	L	L	H
11	$V_{DD}2$	—				35	HD*1	ACT	L	L	H
12	H1B	ACT	L	L	ACT	36	$V_{SS}5$	—			
13	H2A	ACT	L	L	ACT	37	VM	—			
14	$V_{SS}3$	—				38	V2	ACT	VM	VM	VM
15	H2B	ACT	L	L	ACT	39	V4	ACT	VM	VM	VL
16	$V_{DD}3$	—				40	V1A	ACT	VH	VH	VM
17	$V_{DD}4$	—				41	VH	—			
18	XSHP	ACT	L	L	ACT	42	V1B	ACT	VH	VH	VM
19	XSHD	ACT	L	L	ACT	43	V1C	ACT	VH	VH	VM
20	PBLK	ACT	L	L	H	44	V3A	ACT	VH	VH	VL
21	CLPDM	ACT	L	L	H	45	VL	—			
22	OBCLP	ACT	L	L	H	46	V3B	ACT	VH	VH	VL
23	ADCLK	ACT	L	L	ACT	47	V3C	ACT	VH	VH	VL
24	$V_{SS}4$	—				48	SUB	ACT	VH	VH	VL

*1 It is for output. For input, all items are “ACT”.

Note) ACT means that the circuit is operating, and DIS means that loading is stopped. L indicates a low output level, and H a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin 41), VM (Pin 37) and VL (Pin 45), respectively, in the controlled status.

Serial Interface Control

The CXD2498R basically loads and reflects the serial interface data sent in the following format in the readout portion at the falling edge of HD. Here, readout portion specifies the horizontal period during which V1A/B/C and V3A/B/C, etc. take the ternary value.
Note that some items reflect the serial interface data at the falling edge of VD or the rising edge of SEN.



These are two categories of serial interface data : the CXD2498R drive control data (hereafter “control data”) and electronic shutter data (hereafter “shutter data”).
The details of each data are described below.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D11	MODE	Drive mode switching	See D10 to D11 MODE.		All 0
D12	—	—	—	—	0
D13	SMD	Electronic shutter mode switching*1	OFF	ON	0
D14	HTSG	HTSG control switching*1	OFF	ON	0
D15	—	—	—	—	0
D16 to D17	PTMD	Drive mode pattern switching	See D16 to D17 PTMD.		All 0
D18 to D32	—	—	—	—	All 0
D33	EXP	ID/EXP output switching	ID	EXP	0
D34 to D35	PTOB	OBCLP waveform pattern switching	See D34 to D35 PTOB.		All 0
D36 to D37	LDAD	ADCLK logic phase adjustment	See D36 to D37 LDAD.		1 0
D38 to D39	STB	Standby control	See D38 to D39 STB.		All 0
D40 to D47	—	—	—	—	All 0

*1 See D13 SMD.

Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D19	SVD	Electronic shutter vertical period specification	See D10 to D19 SVD.		All 0
D20 to D31	SHD	Electronic shutter horizontal period specification	See D20 to D31 SHD.		All 0
D32 to D41	SPL	High-speed shutter position specification	See D32 to D41 SPL.		All 0
D42 to D47	—		—	—	0

Detailed Description of Each Data

Shared data: D08 to D09 CTG [Category]

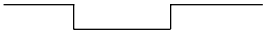
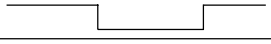
Of the data provided to the CXD2498R by the serial interface, the CXD2498R loads D10 and subsequent data to each data register as shown in the table below according to the combination of D08 and D09 .

D09	D08	Description of operation
0	0	Loading to control data register
0	1	Loading to shutter data register
1	X	Test mode

Note that the CXD2498R can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D34 to D35 PTOB [OBCLP waveform pattern]

This specifies the OBCLP waveform pattern. The default is “Normal”. See the Timing Charts for details.

D35	D34	Waveform pattern
0	0	 (Normal)
0	1	 (Rearward)
1	0	 (Forward)
1	1	 (Wide)

Control data: D36 to D37 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is 90° relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: D38 to D39 STB [Standby]

The operating mode is switched as follows. However, the standby bits are loaded to the CXD2498R and control is applied immediately at the rising edge of SEN.

D39	D38	Symbol	Operating mode
X	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	1	STB	Standby mode

See the Pin Status Table for the pin status in each mode.

Control data: [Drive mode]

The CXD2498R realizes various drive modes by using control data D10 to D11 MODE and D16 to D17 PTMD. The drive mode bits are loaded to the CXD2498R and reflected at the falling edge of VD. These details are described below.

First, the basic drive mode is assigned using the control data D10 to D11 MODE.

D11	D10	Description of operation
0	0	Draft mode (default)
0	1	Progressive scan mode
1	0	Double speed mode
1	1	Frame mode

Draft mode is the pulse eliminator drive mode called octuple speed mode in the ICX282. This is a high frame rate drive mode that can be used for purposes such as monitoring and auto focus (AF).

Progressive scan mode is the pulse eliminator drive mode called double speed mode (1) in the ICX282. Pulse elimination is performed, but the frame data is obtained over one field period and corresponds to progressive scan drive, so it is called progressive scan mode in this data sheet.

Double speed mode is the pulse eliminator drive mode called double speed mode (2) in the ICX282. Readout is applied with two lines added to provide an image which appears like frame mode with an increased frame rate. This drive mode is comprised of A and B Fields, so when it is established, repeated drive is performed in the manner of A → B → A → and so on.

Frame mode is the ICX282 drive mode in which the data for all lines are read. This drive mode is also comprised of A and B Fields, so when it is established, repeated drive is performed in the manner of A → B → A → and so on like double speed mode.

[Special drive modes]

Of the above basic drive modes, when a drive mode other than double speed mode is specified, special drive modes can be specified using the control data D16 to D17 PTMD.

D17	D16	Description of operation		
		Draft mode	Progressive scan mode	Frame mode
0	X	Draft mode	Progressive scan mode	Frame mode
1	0	AF1 mode	Center scan 1 mode	Center scan 1 mode
1	1	AF2 mode	Center scan 2 mode	Center scan 2 mode

See the Timing Charts for details of all drive modes. Note that center scan modes (3) and (4) in the ICX282 correspond to center scan 1 and 2 in frame mode, and center scan modes (1) and (2) in the ICX282 correspond to center scan 1 and 2 in progressive scan mode.

Control data/shutter data: [Electronic shutter]

The CXD2498R realizes various electronic shutter functions by using control data D13 SMD and D14 HTSG and shutter data D10 to D19 SVD, D20 to D31 SHD and D32 to D41 SPL. These functions are described in detail below.

First, the various modes are shown below. These modes are switched using control data D13 SMD.

D13	Description of operation
0	Electronic shutter stopped mode
1	Electronic shutter mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHD as an example. However, MSB (D31) is a reserve bit for the future specification, and it is handled as a dummy on this IC.

MSB D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	LSB D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

→ SHD is expressed as 1C3H .

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[Electronic shutter mode]

During this mode, the shutter data items have the following meanings.

Symbol	Data	Description
SVD	D10 to D19	Number of vertical periods specification (000h ≤ SVD ≤ 3FFh)
SHD	D20 to D31	Number of horizontal periods specification (000h ≤ SHD ≤ 7FFh)
SPL	D32 to D41	Vertical period specification for high-speed shutter operation (000h ≤ SPL ≤ 3FFh)

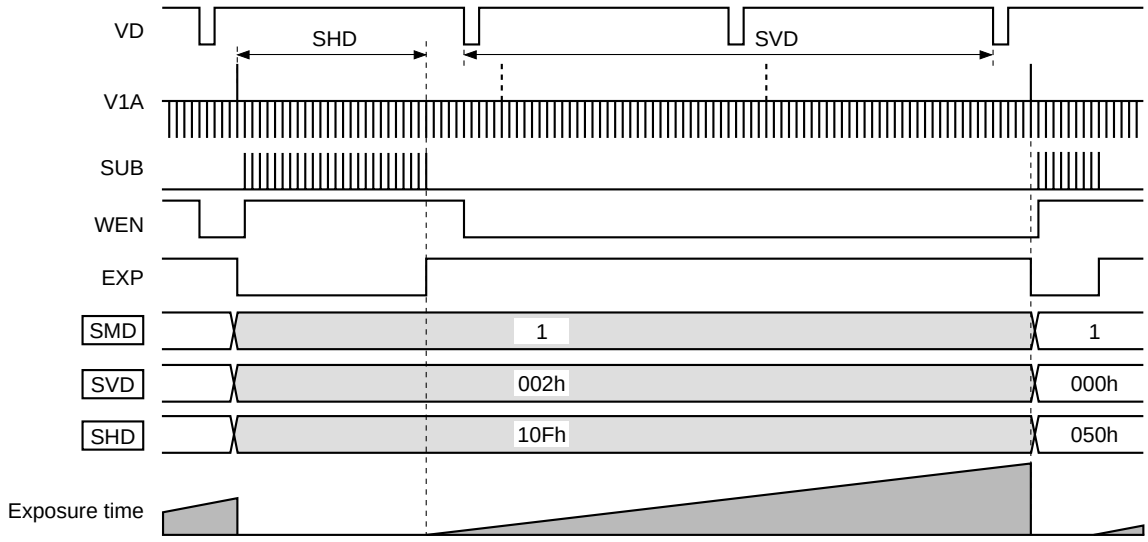
Note) The bit data definition area is assured in terms of the CXD2498R functions, and does not assure the CCD characteristics.

The period during which SVD and SHD are specified together is the shutter speed. An image of the exposure time calculation formula is shown below. In actual operation, the precise exposure time is calculated from the operating frequency, VD and HD periods, decoding value during the horizontal period, and other factors.

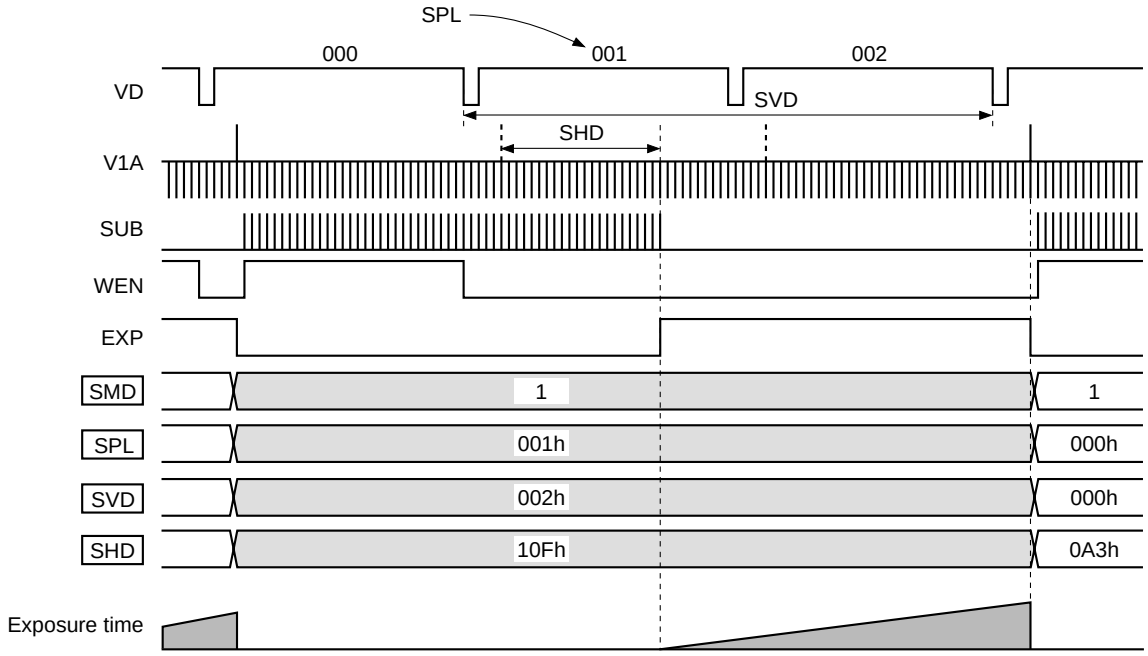
(Exposure time) = SVD + {(number of HD per 1V) – (SHD + 1)}

Concretely, when specifying high-speed shutter, SVD is set to “000h”. (See the figure.) During low-speed shutter, or in other words when SVD is set to “001h” or higher, the serial interface data is not loaded until this period is finished.

The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1).



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.
In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.

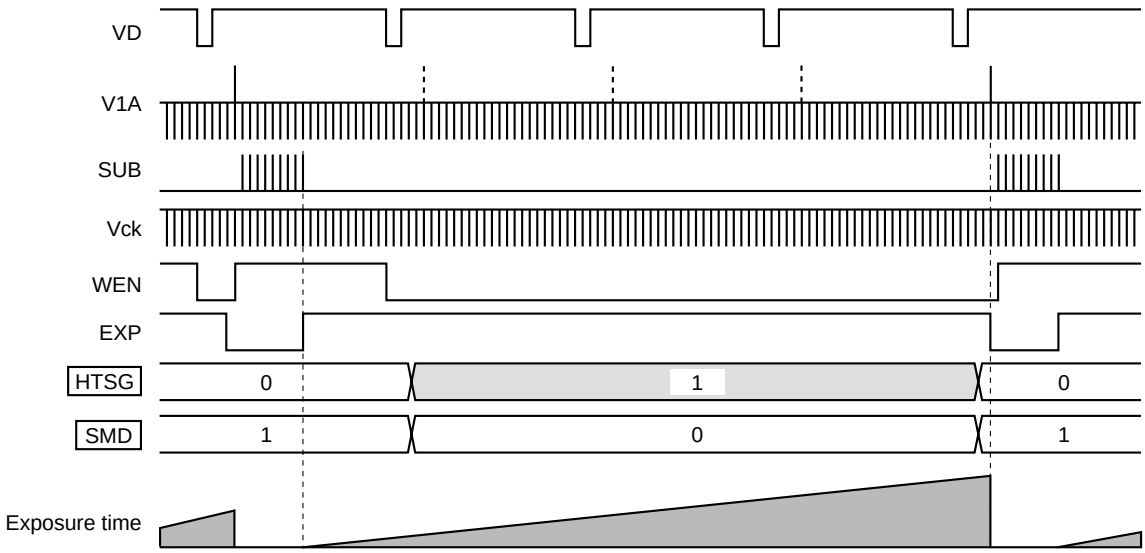


Incidentally, SPL is counted as “000h”, “001h”, “002h” and so on in conformance with SVD.
Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

[HTSG control mode]

This mode controls the V1A/B/C and V3A/B/C ternary level outputs (readout pulse block) using D14 HTSG. When control is applied, V pulse modulation does not occur during the readout period, and only normal V transfer is performed.

D14	Description of operation
0	Readout pulse (SG) normal operation
1	HTSG control mode



[EXP pulse]

The ID/EXP pin (Pin 4) output can be switched between the ID pulse or the EXP pulse using D33 EXP. The default is the “ID” pulse. See the Timing Charts for the ID pulse. The EXP pulse indicates the exposure time when it is high. The transition point is midpoint value (1515ck) of the last SUB pulse falling edge and each V1A/B/C and V3A/B/C ternary output falling edge. When there is no SUB pulse, the later ternary output falling edge (1590ck) is used. See the EXP pulse indicated in the explanatory diagrams under [Electronic shutter] for an image of operation.

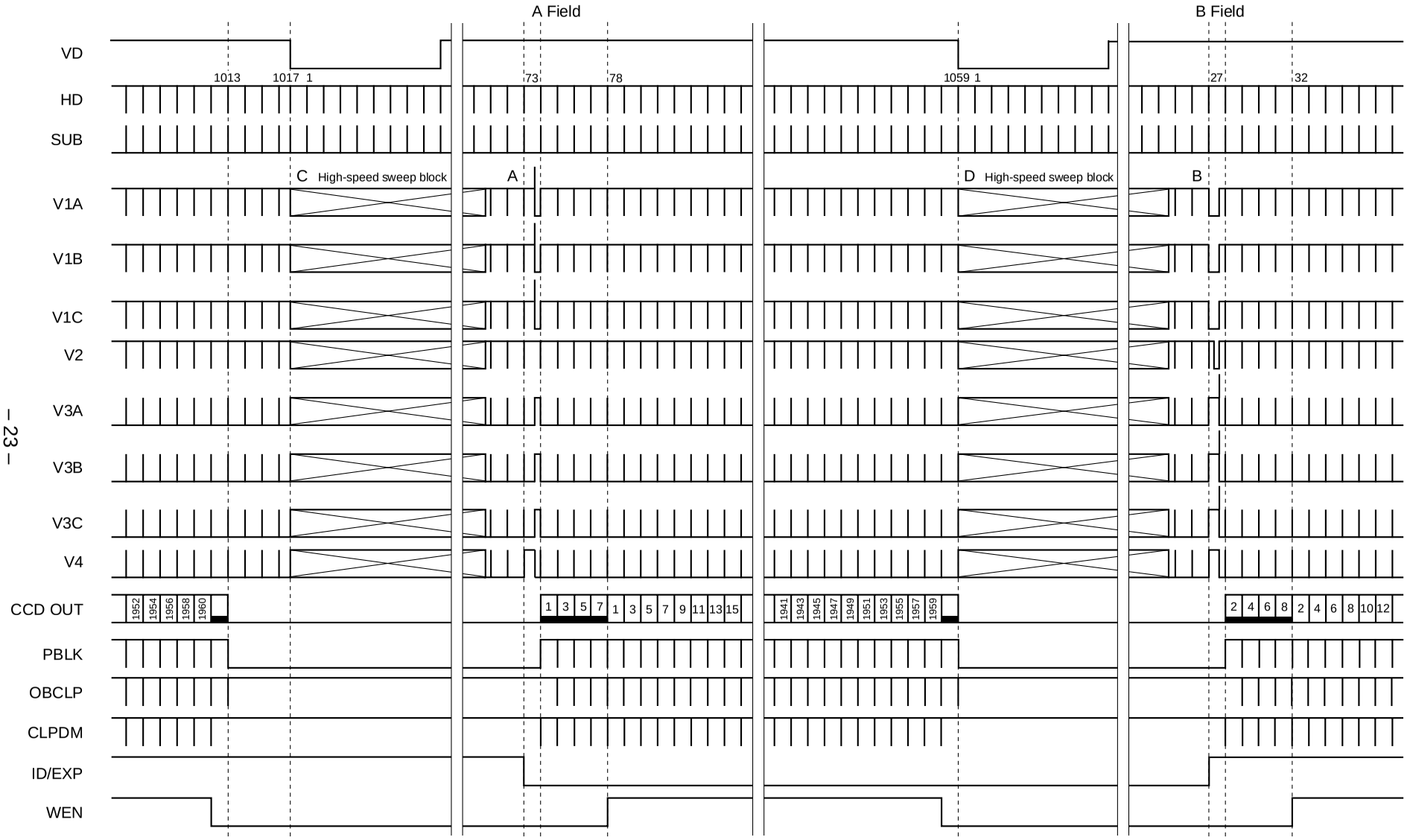
Chart-1 Vertical Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 1059H in the A Field and 1017H in the B Field (2894ck in both cases). The B Field 1016H only has a 950ck period.

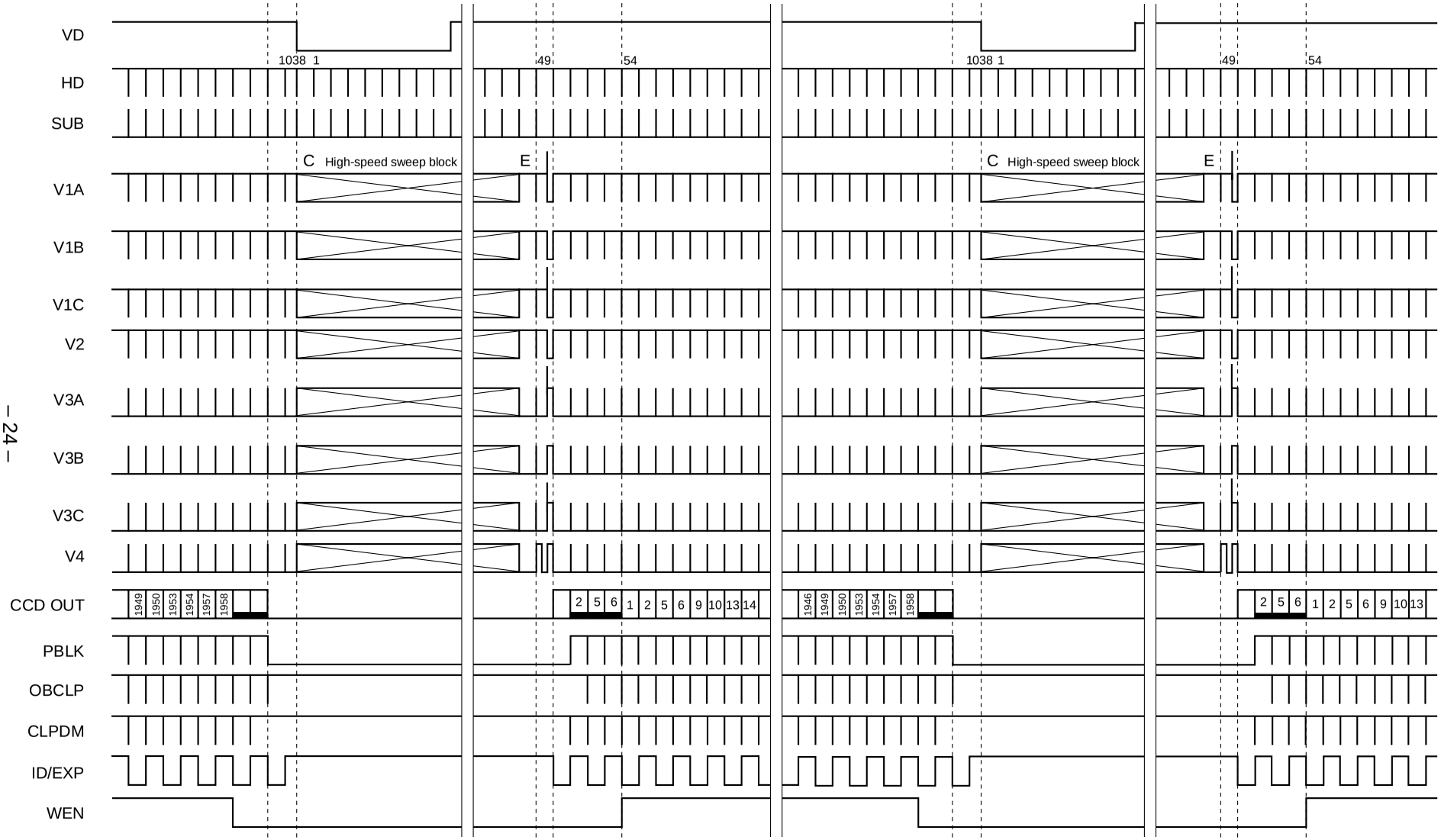
Chart-2 **Vertical Direction Timing Chart**

MODE

Progressive scan mode

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 1038H period (2894ck). 1037H only has a 1922ck period.

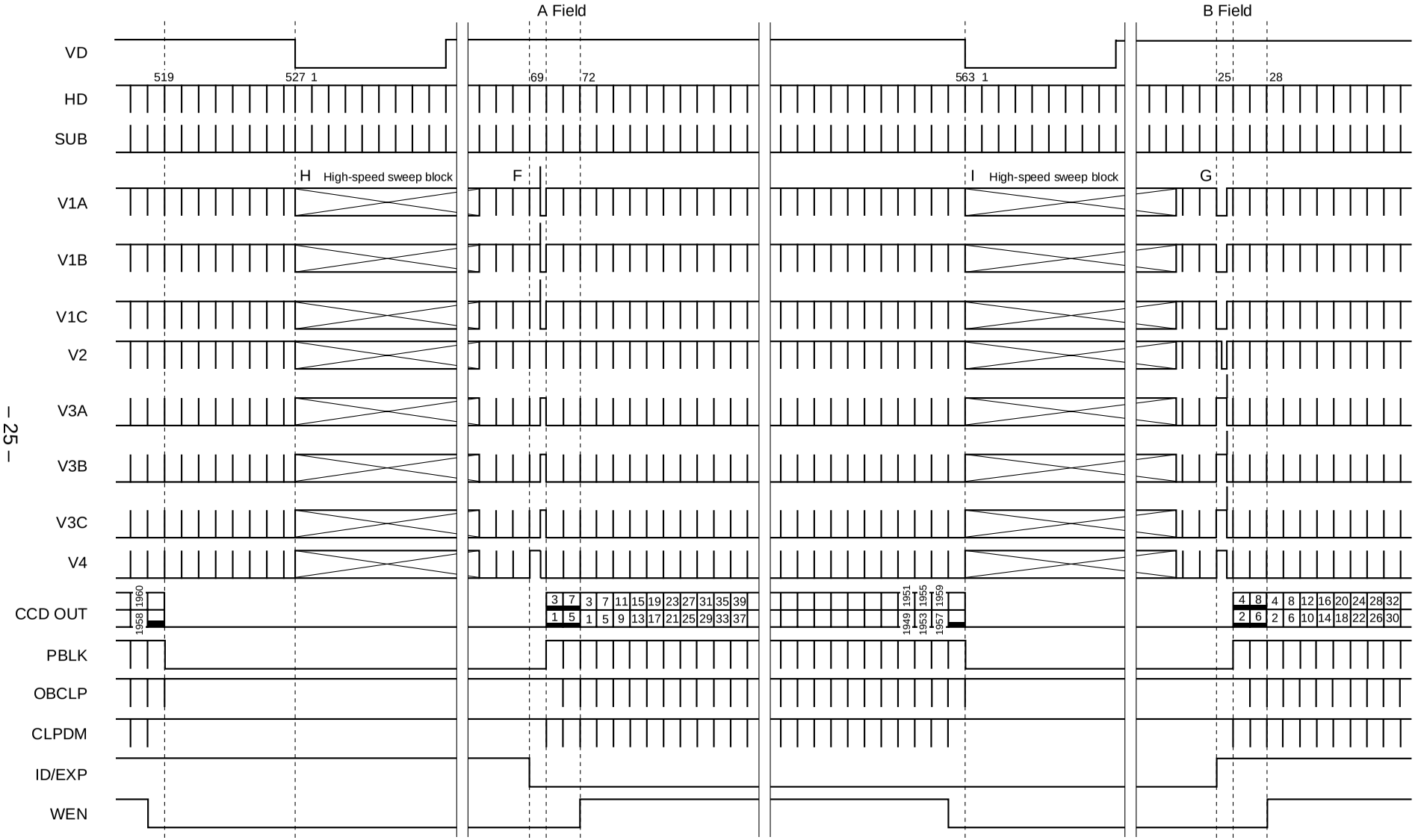
Chart-3 **Vertical Direction Timing Chart**

MODE

Double speed mode

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 563H in the A Field and 527H in the B Field (3102ck in both cases). The B Field 525H has a 1700ck period and 526H has a 1699ck period.

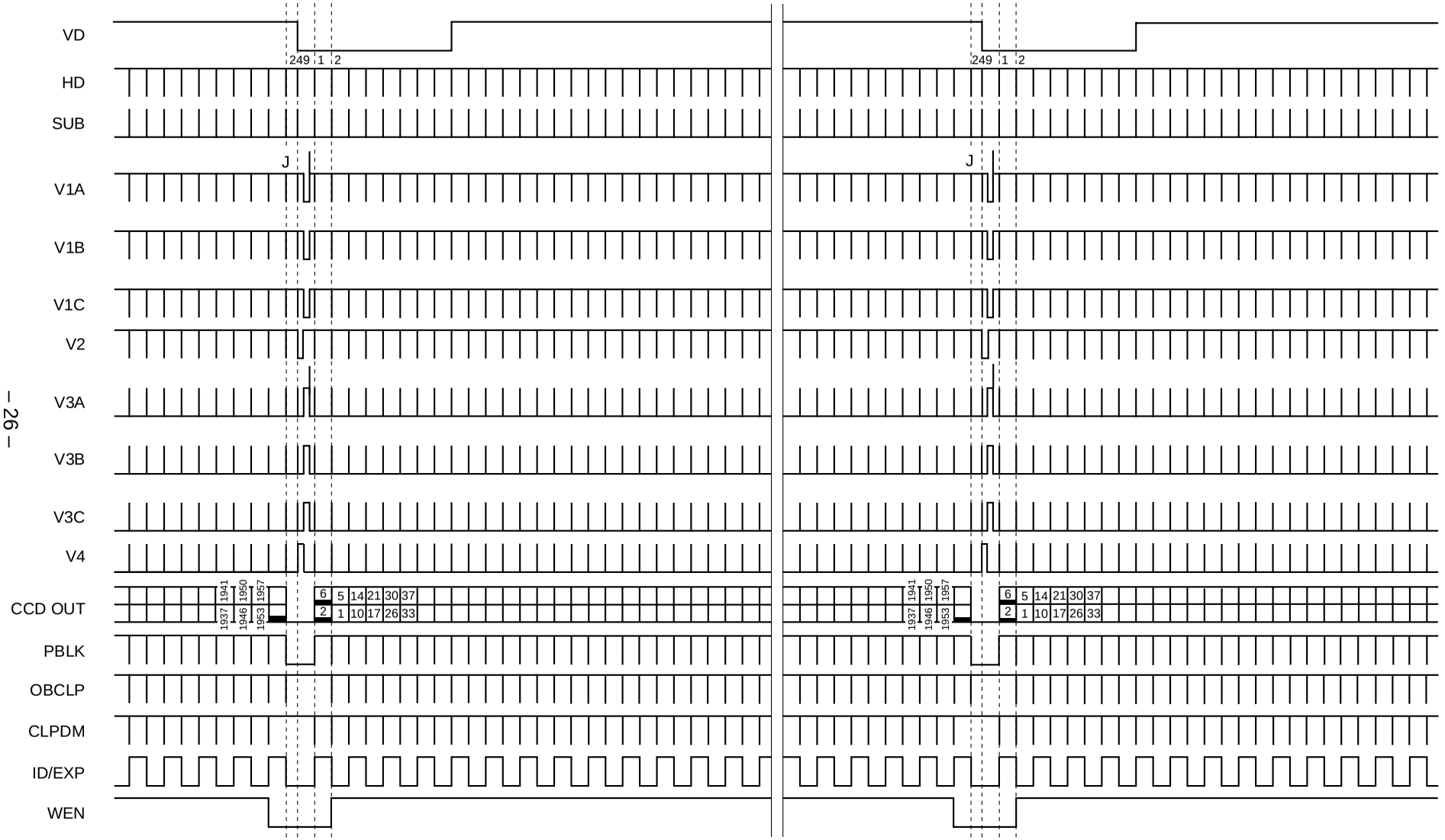
Chart-4 **Vertical Direction Timing Chart**

MODE

Draft mode

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 249H (3022ck) period. 248H only has a 1294ck period.

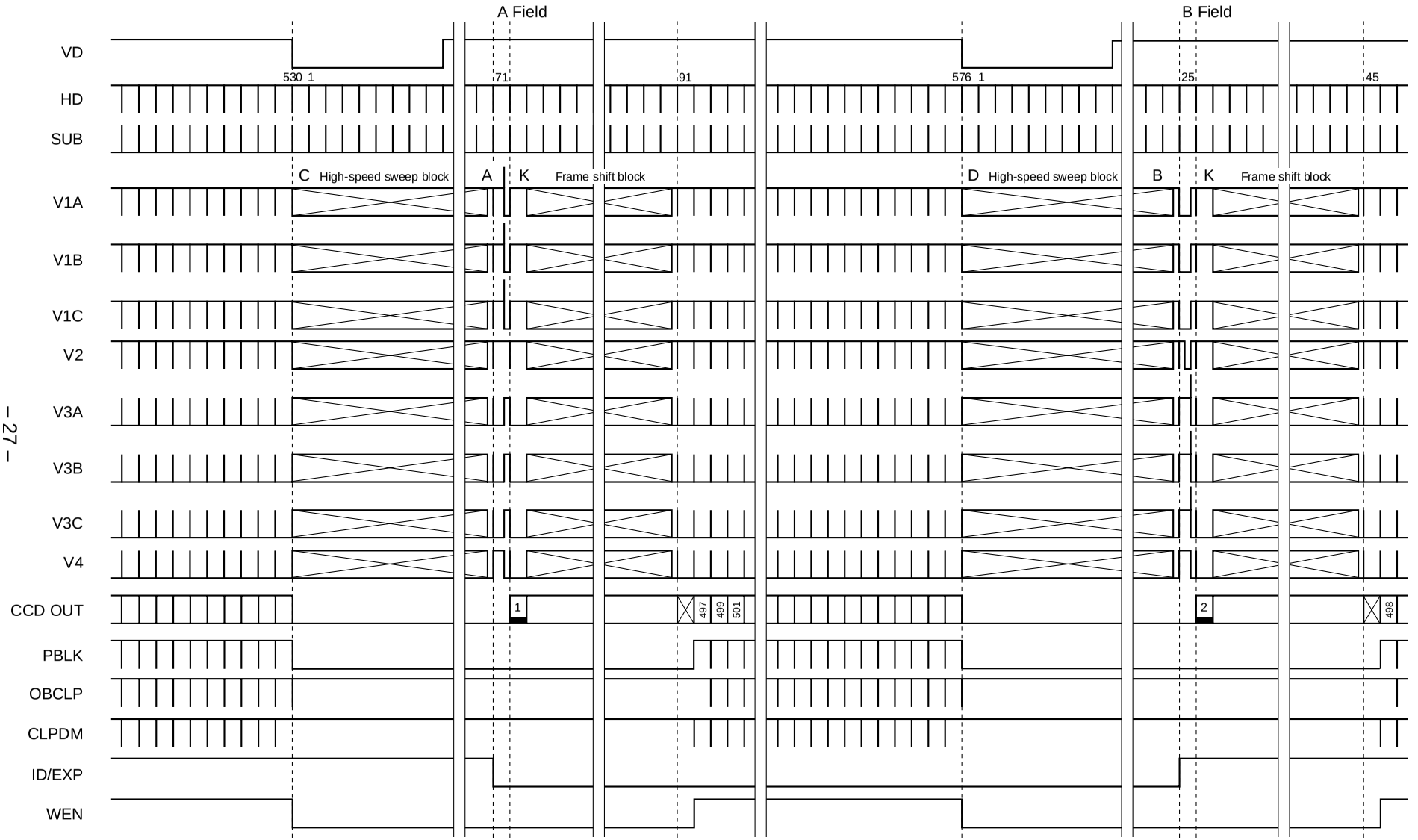
Chart-5 **Vertical Direction Timing Chart**

MODE

Frame mode (center scan 1)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 576H in the A Field and 530H in the B Field (2894ck in both cases).

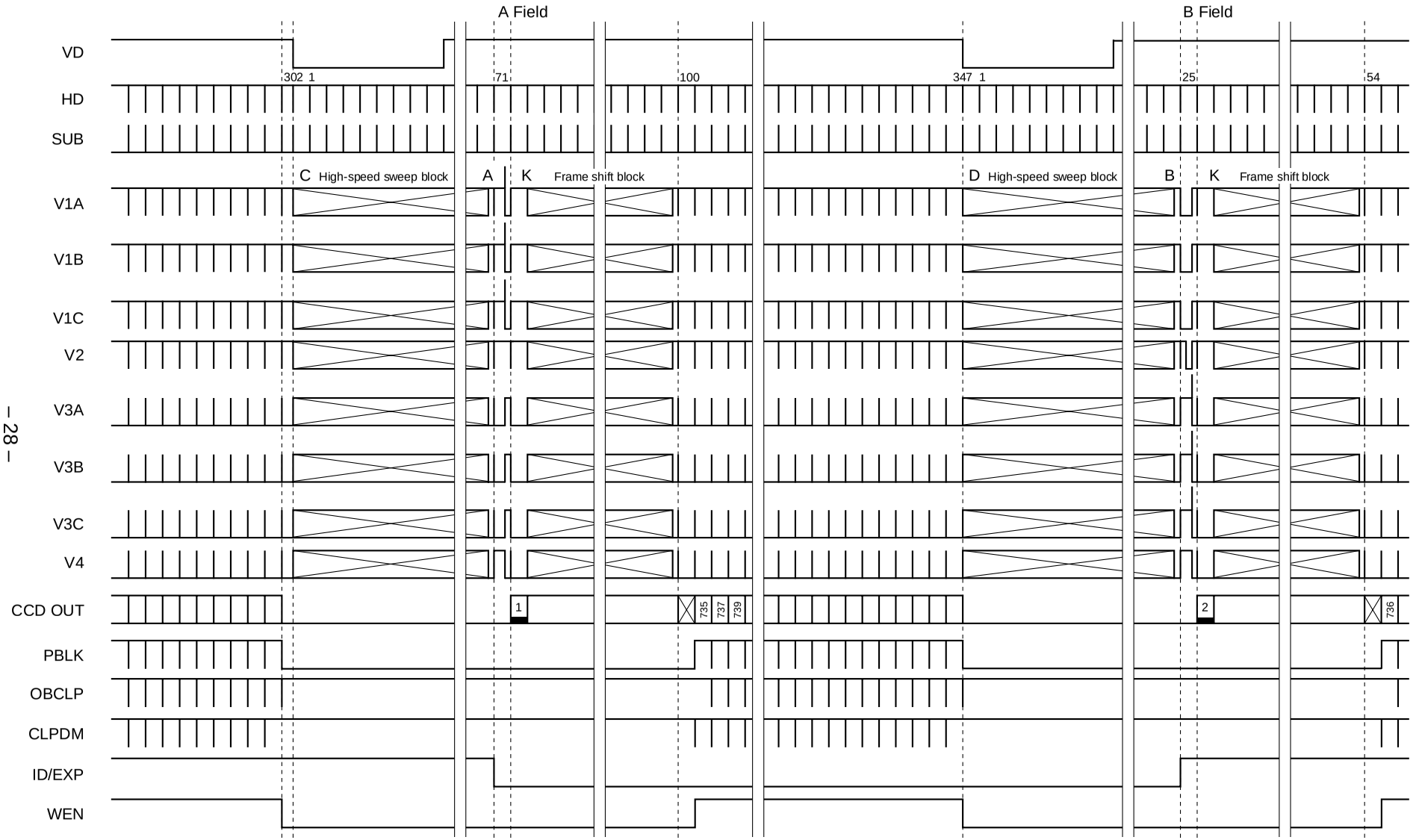
Chart-6 **Vertical Direction Timing Chart**

MODE

Frame mode (center scan 2)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 347H in the A Field and 302H in the B Field (2894ck in both cases). The B Field 301H only has a 1563ck period.

SONY

CXD2498R

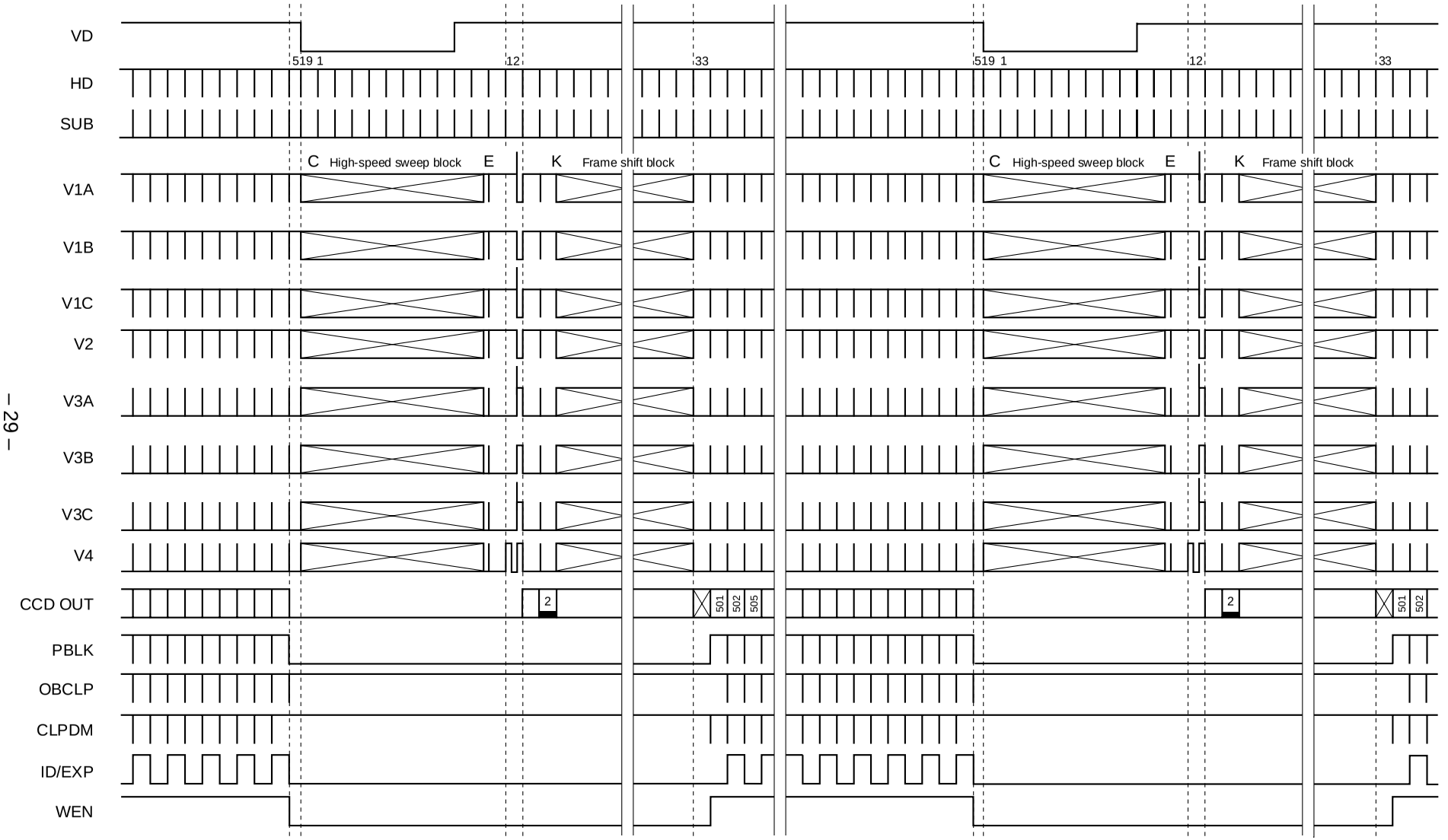
Chart-7 **Vertical Direction Timing Chart**

MODE

Progressive scan mode (center scan 1)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 519H (2894ck) period. 518H only has a 2408ck period.

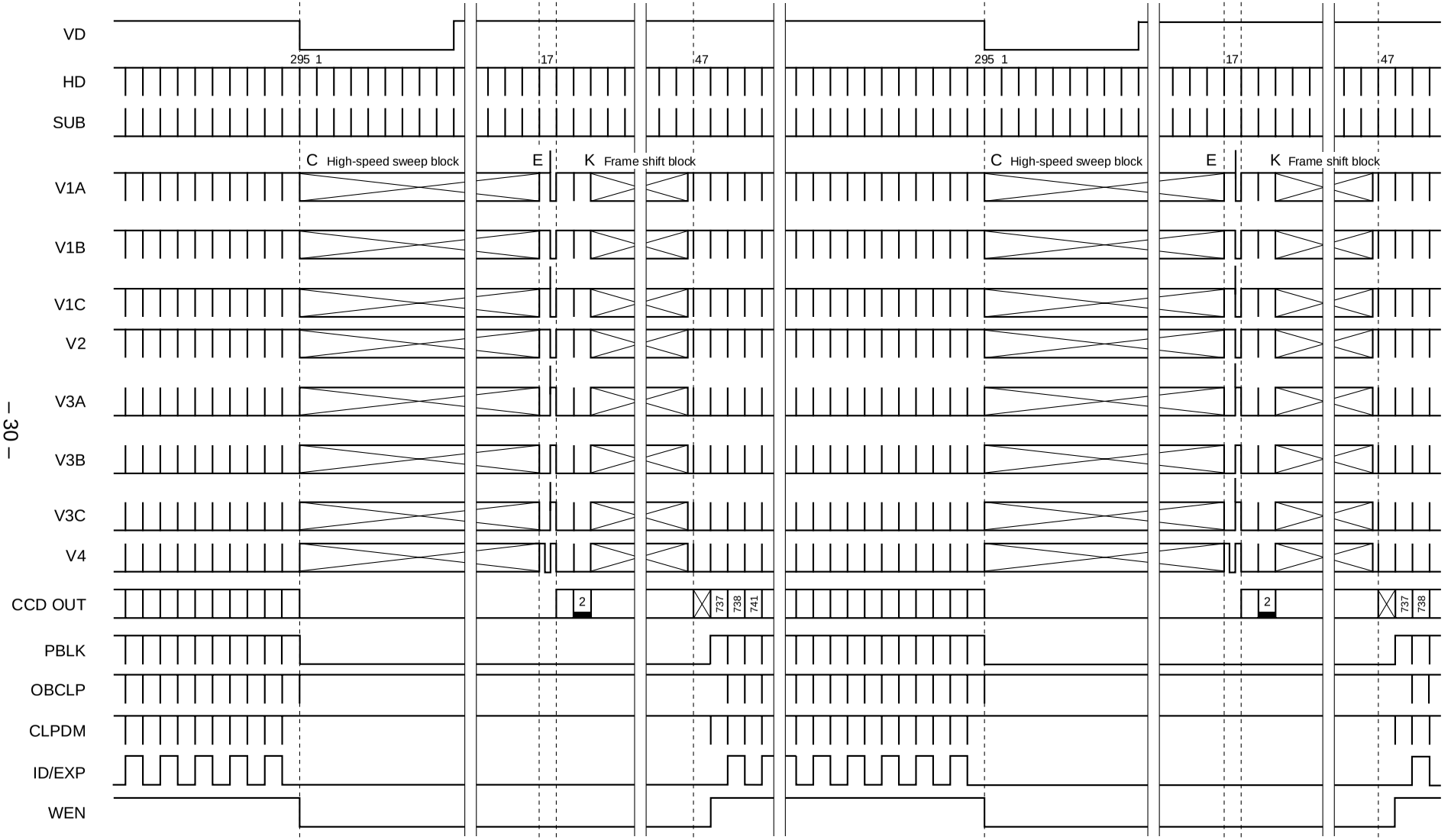
Chart-8 **Vertical Direction Timing Chart**

MODE

Progressive scan mode (center scan 2)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 295H (2894ck) period.

SONY

CXD2498R

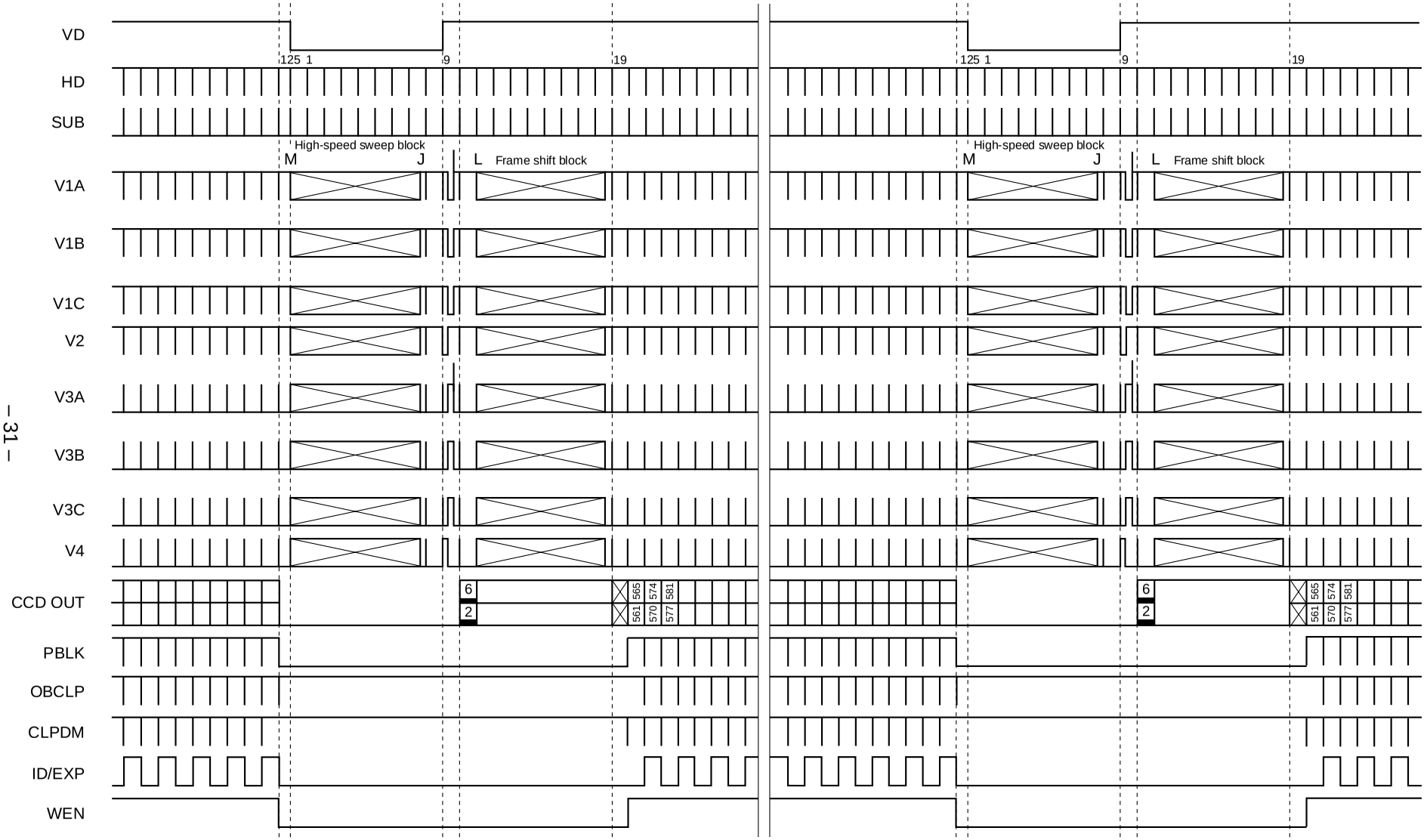
Chart-9 **Vertical Direction Timing Chart**

MODE

Draft mode (AF1)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 125H (3022ck) period. 124H only has a 647ck period.

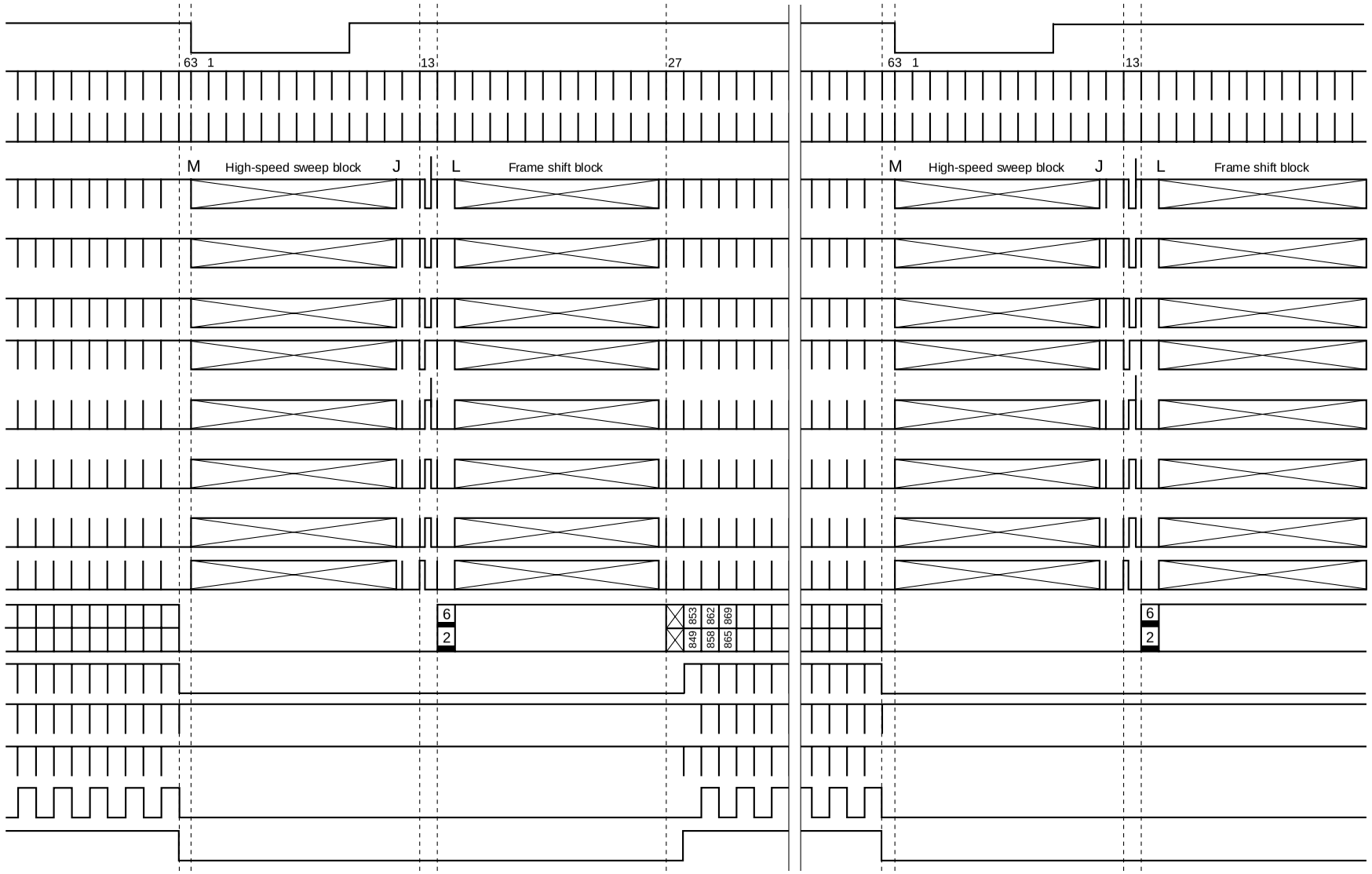
Chart-10 Vertical Direction Timing Chart

MODE

Draft mode (AF2)

Applicable CCD image sensor

• ICX282



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

* VD of this chart is 63H (3022ck) period. 62H only has a 324ck period.

Chart-11 Horizontal Direction Timing Chart

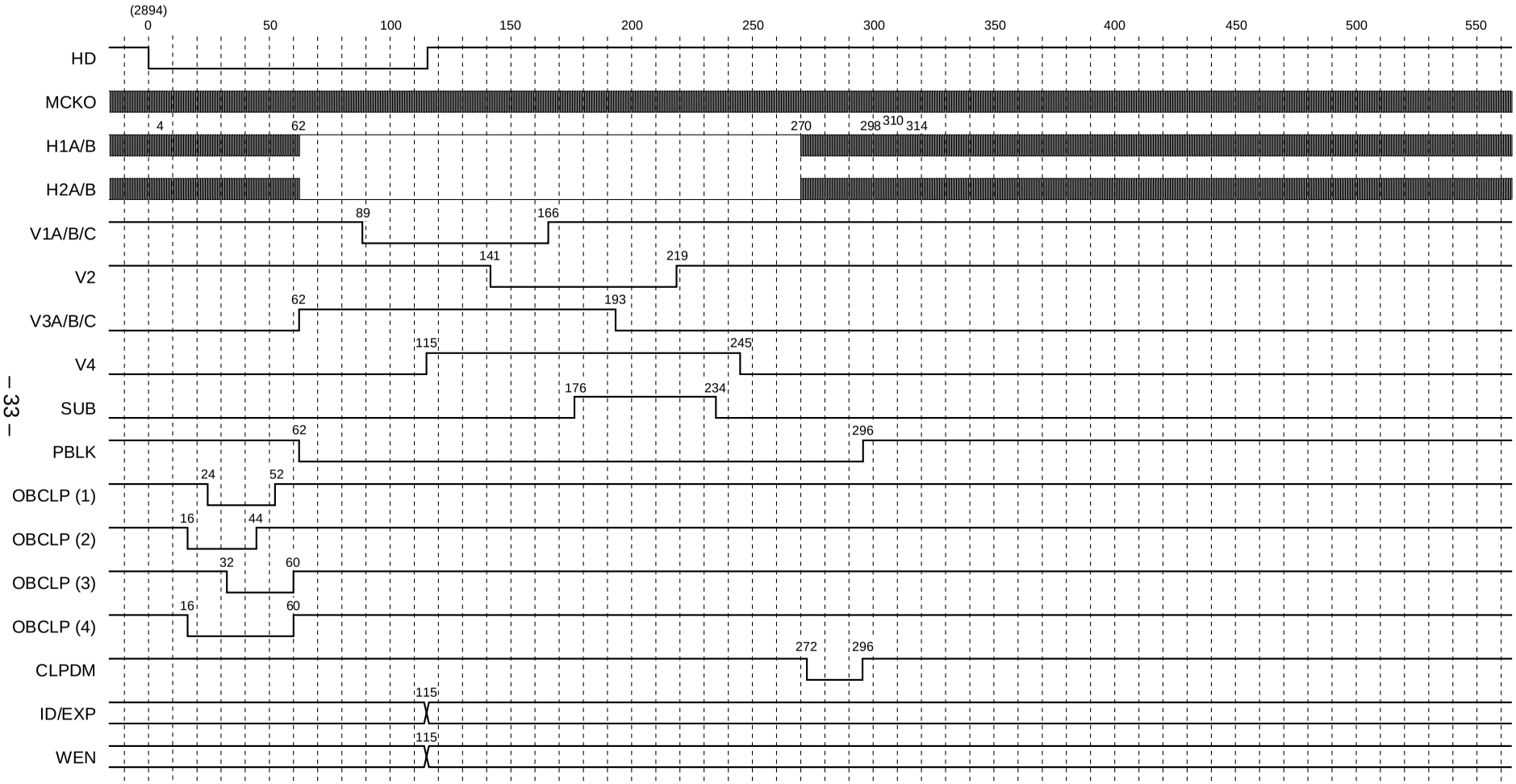
MODE

Frame mode (including center scan 1 and 2)

Progressive scan mode (including center scan 1 and 2)

Applicable CCD image sensor

• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows a period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID/EXP and WEN are output at the timing shown above at the position shown in Chart-1, 2, 5, 6, 7 and 8.

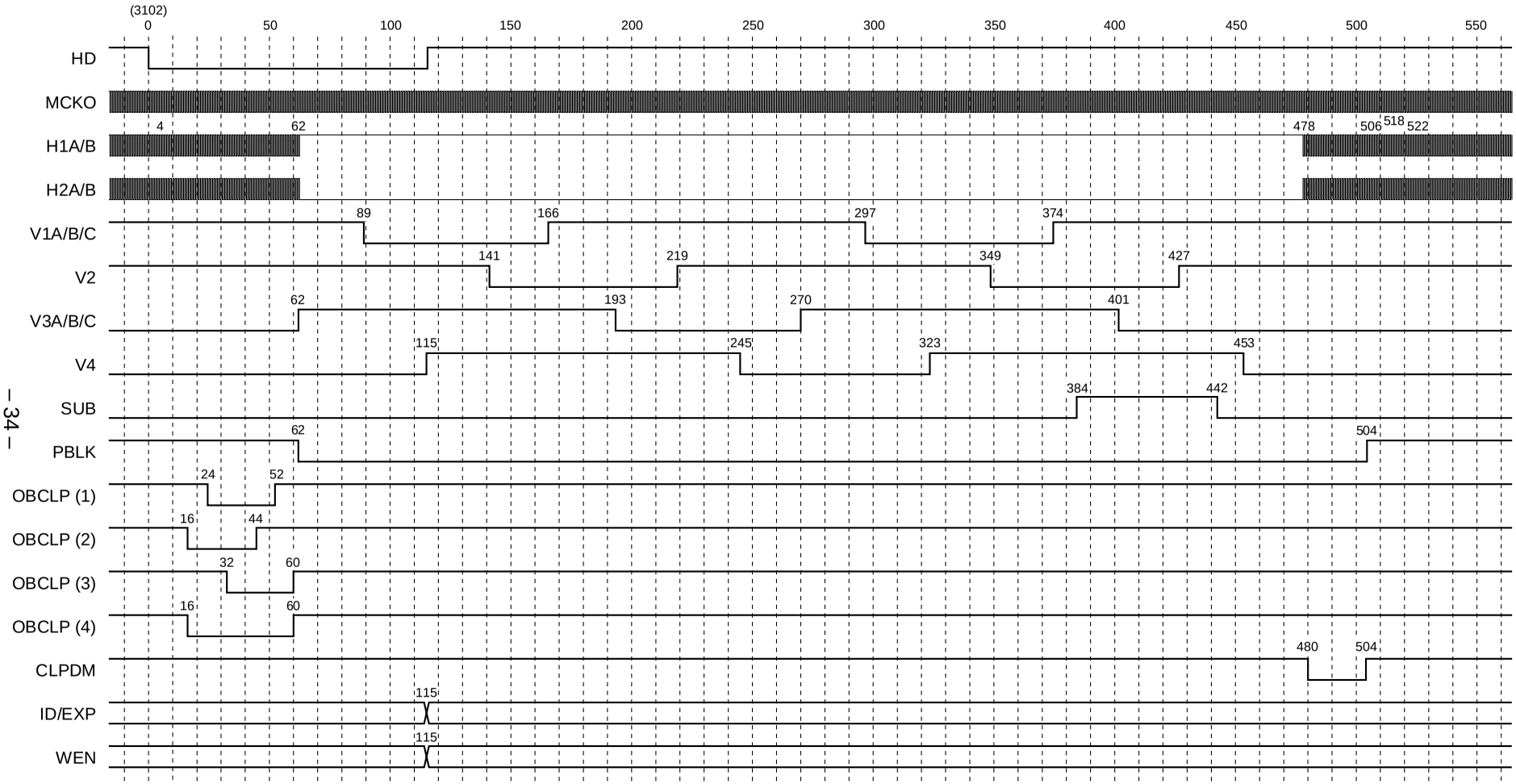
Chart-12 Horizontal Direction Timing Chart

MODE

Double speed mode

Applicable CCD image sensor

• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows a period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID/EXP and WEN are output at the timing shown above at the position shown in Chart-3.

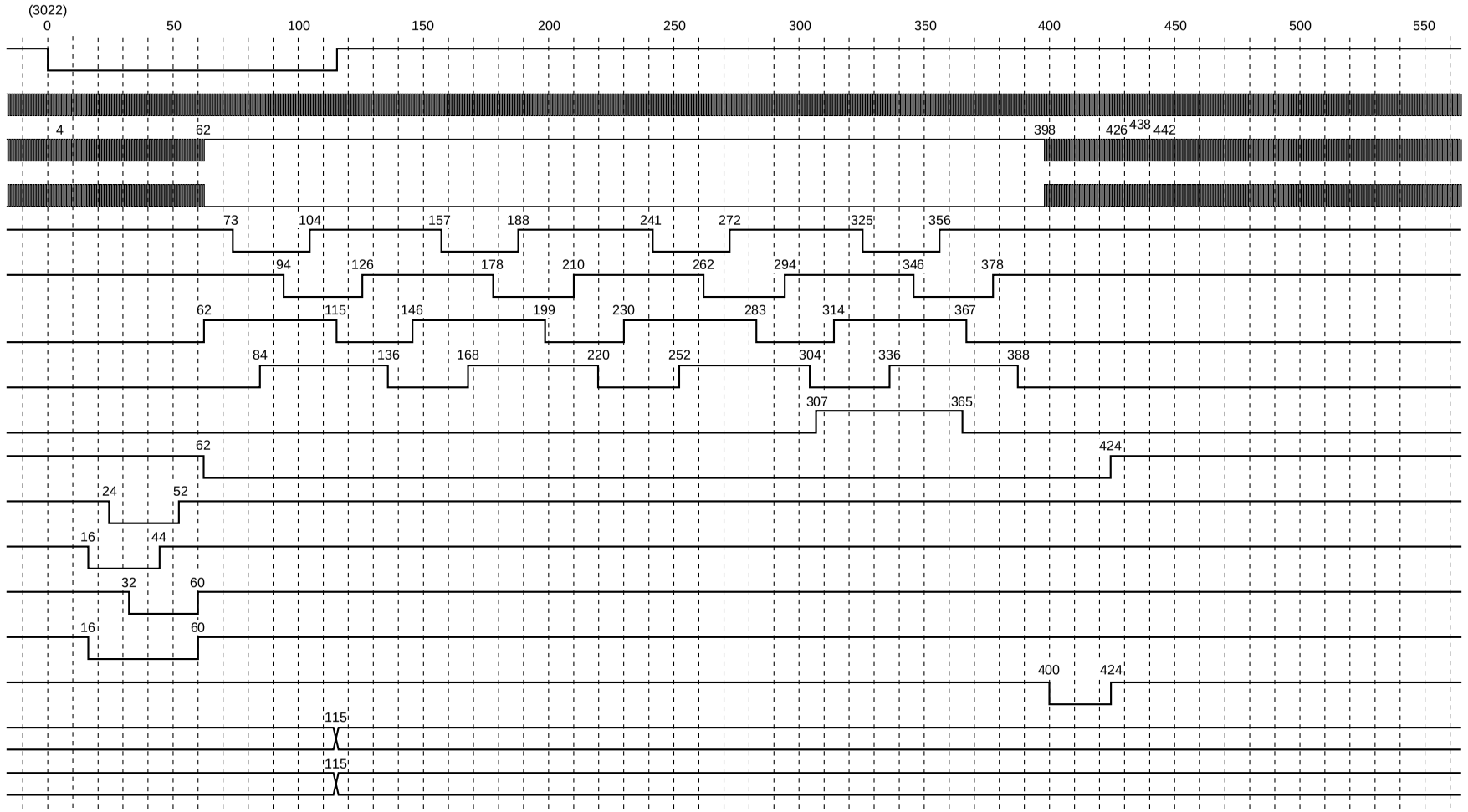
Chart-13 Horizontal Direction Timing Chart

MODE

Draft mode (including AF1 and 2)

Applicable CCD image sensor

• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows a period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID/EXP and WEN are output at the timing shown above at the position shown in Chart-4, 9 and 10.

Chart-14 Horizontal Direction Timing Chart (High-speed sweep: C)

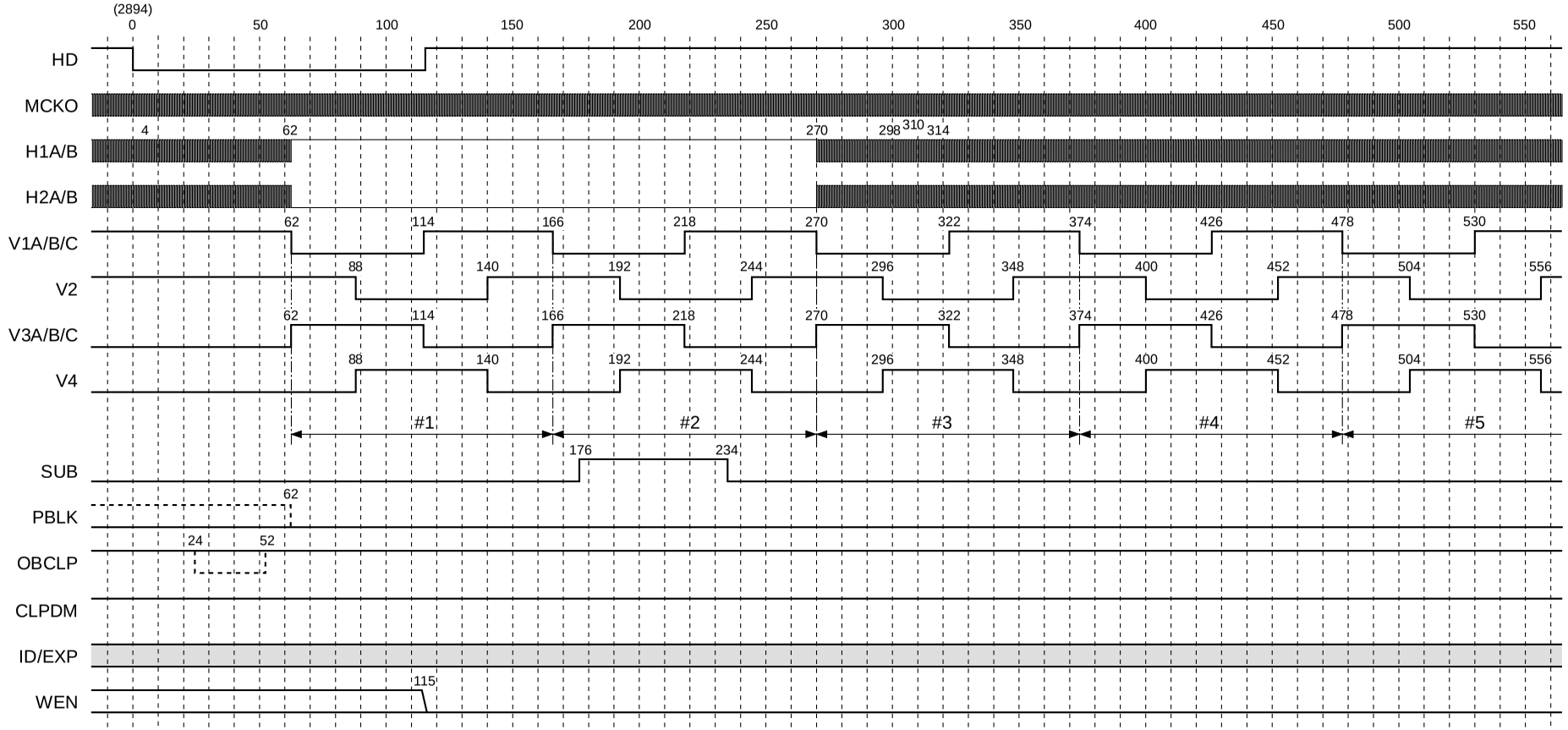
MODE

Frame mode (including center scan 1 and 2)

Progressive scan mode (including center scan 1 and 2)

Applicable CCD image sensor

• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.

* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.

* SUB is output at the timing shown above when output is controlled by the serial interface data.

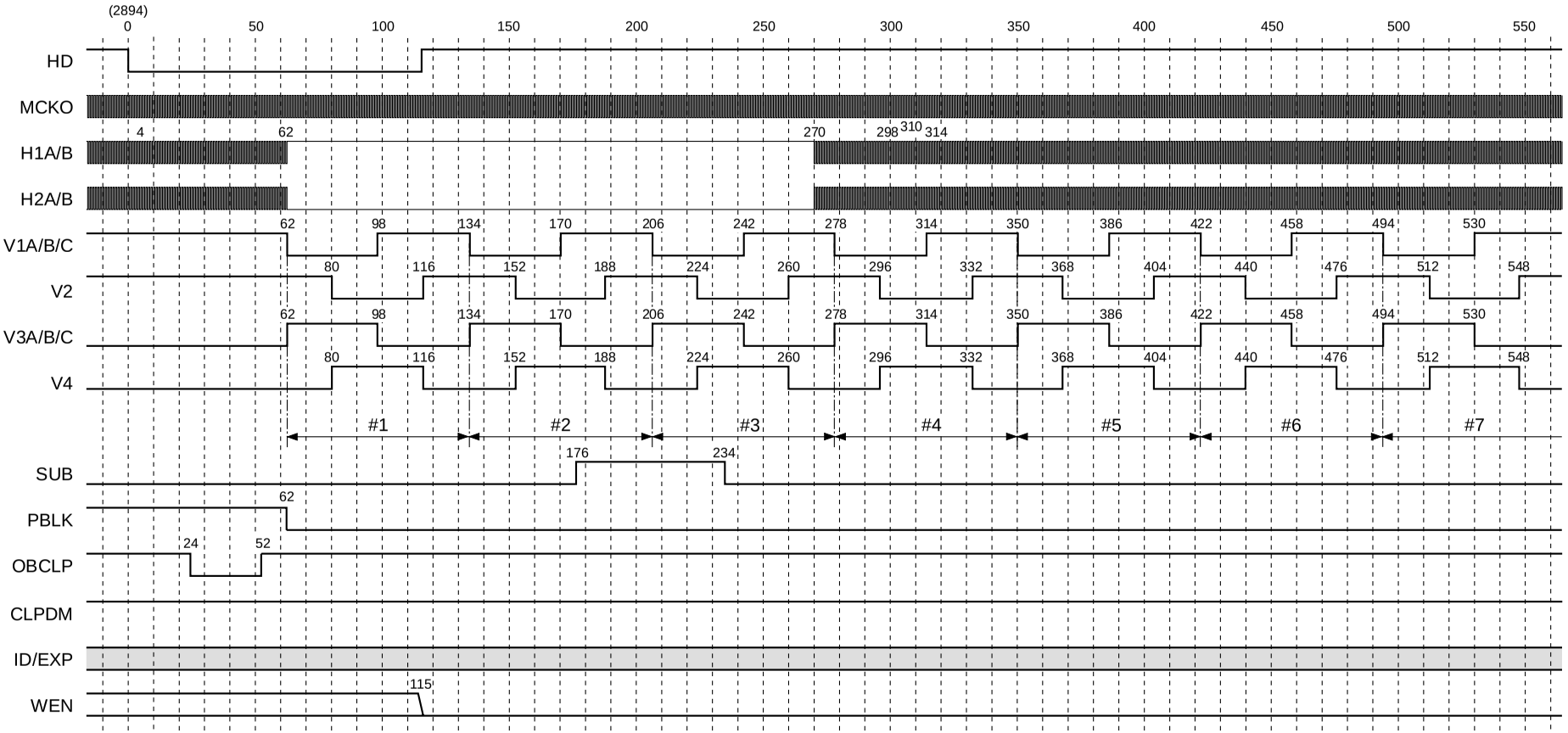
* PBLK, OBCLP, ID/EXP and WEN are output at the timing shown above at the position shown in Chart-1, 2, 5, 6, 7 and 8.

* High-speed sweep of V1A/B/C, V2, V3A/B/C and V4 is performed up to 70H 2362ck (#1970) in the A Field of frame mode (including center scan 1 and 2), 47H 2884ck (#1335) in progressive scan mode, 10H 2842ck (#305) in progressive scan mode (center scan 1), and 16H 2846ck (#472) in progressive scan mode (center scan 2).

Chart-15 **Horizontal Direction Timing Chart**
(High-speed sweep: D)

MODE
Frame mode (including center scan 1 and 2)

Applicable CCD image sensor
• ICX282

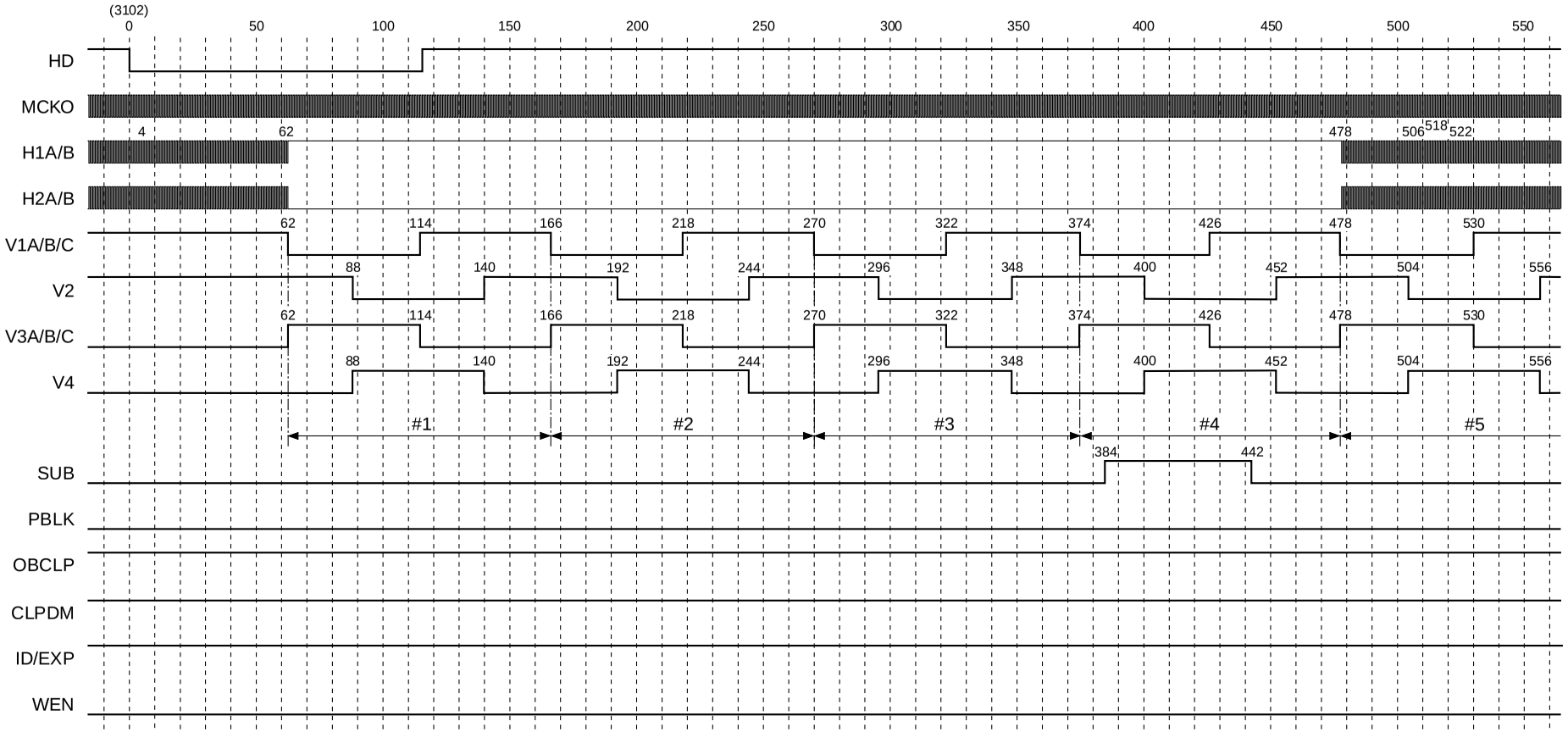


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* PBLK, ID/EXP and WEN are output at the timing shown above at the position shown in Chart-1, 5, and 6.
* High-speed sweep of V1A/B/C, V2, V3A/B/C and V4 is performed up to 24H 1670ck (#986) in the B Field of frame mode (including center scan 1 and 2).

Chart-16 **Horizontal Direction Timing Chart (High-speed sweep: H)**

MODE
Double speed mode

Applicable CCD image sensor
• ICX282

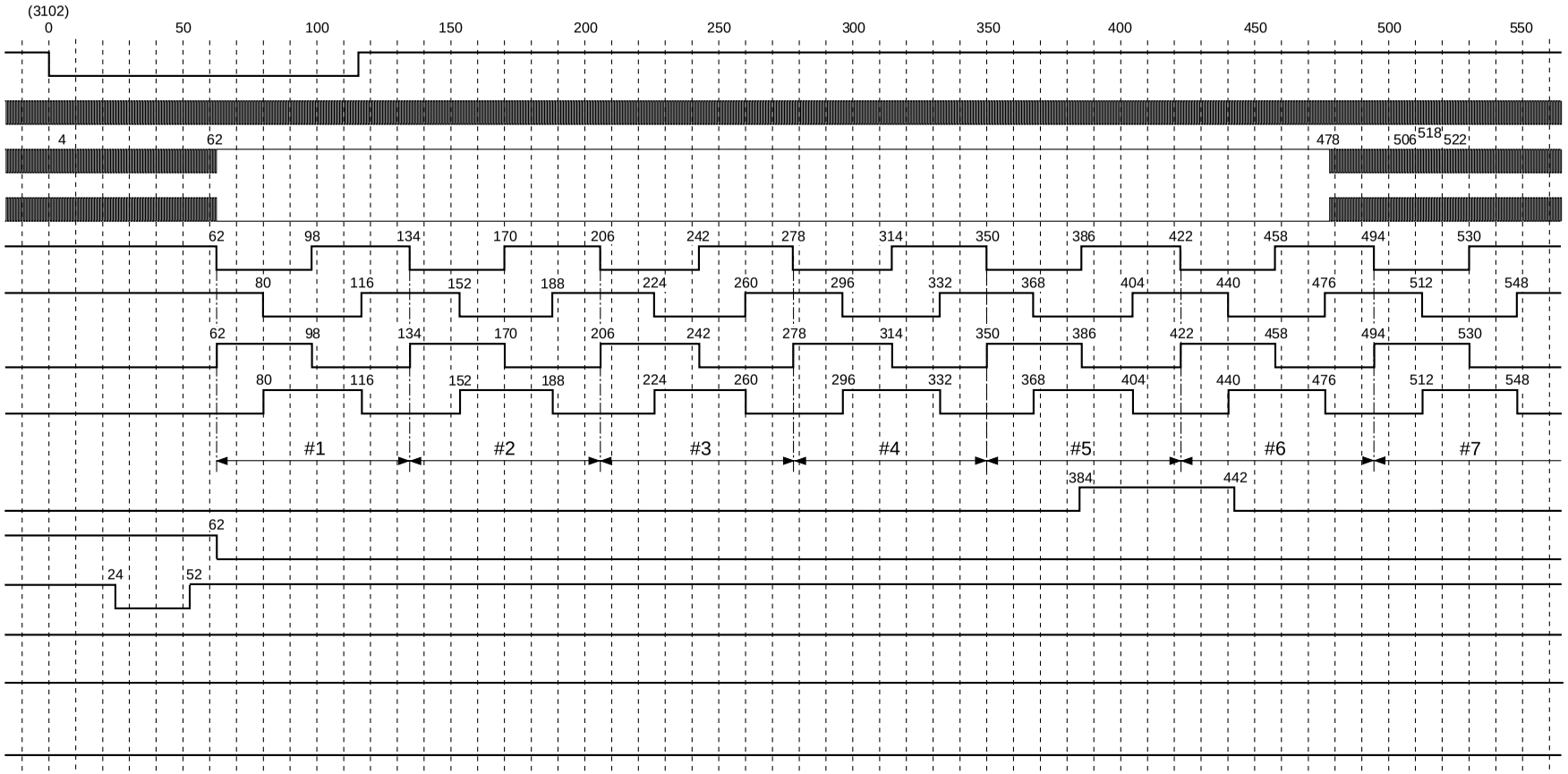


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1A/B/C, V2, V3A/B/C and V4 is performed up to 66H 314ck (#1970).

Chart-17 Horizontal Direction Timing Chart (High-speed sweep: I)

MODE
Double speed mode

Applicable CCD image sensor
• ICX282

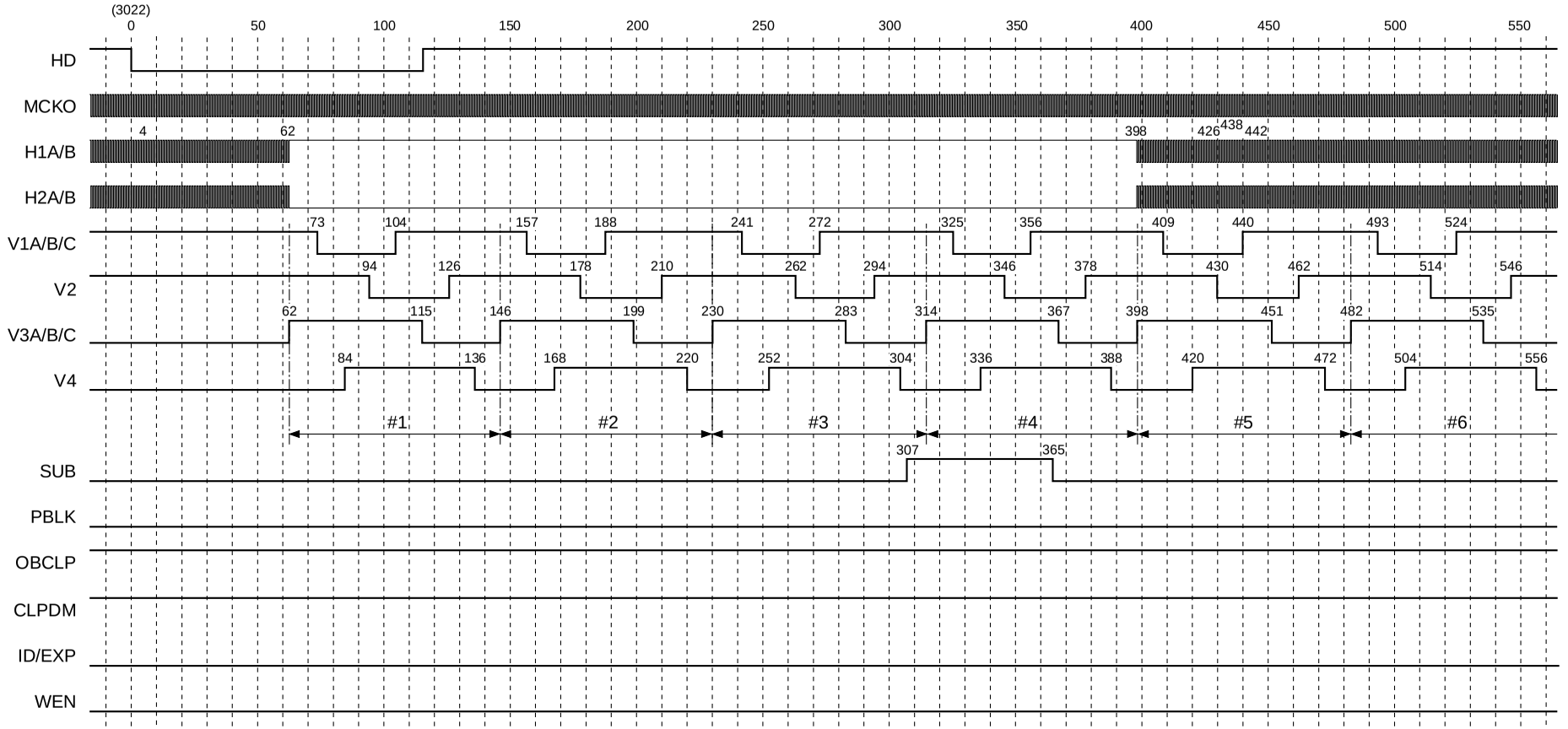


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1A/B/C, V2, V3A/B/C and V4 is performed up to 22H 2810ck (#986).

Chart-18 **Horizontal Direction Timing Chart (High-speed sweep: M)**

MODE
Draft mode (AF1 and 2)

Applicable CCD image sensor
• ICX282

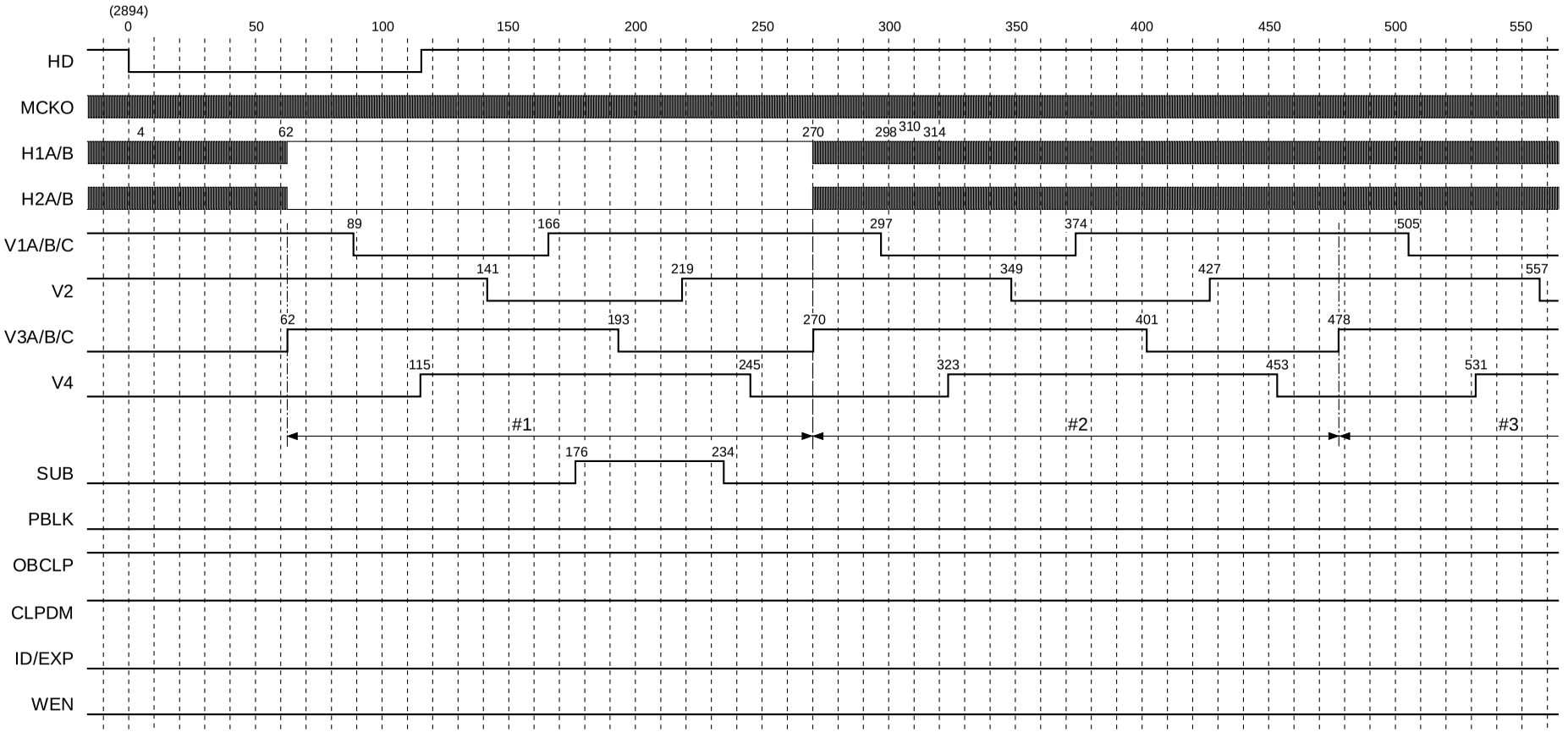


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1A/B/C, V2, V3A/B/C and V4 is performed up to 7H 2848ck (#285) in draft mode (AF1), 11H 2184ck (#421) in draft mode (AF2).

Chart-19 **Horizontal Direction Timing Chart**
(Frame shift : K)

MODE
Frame mode (including center scan 1 and 2)
Progressive scan mode (including center scan 1 and 2)

Applicable CCD image sensor
• ICX282

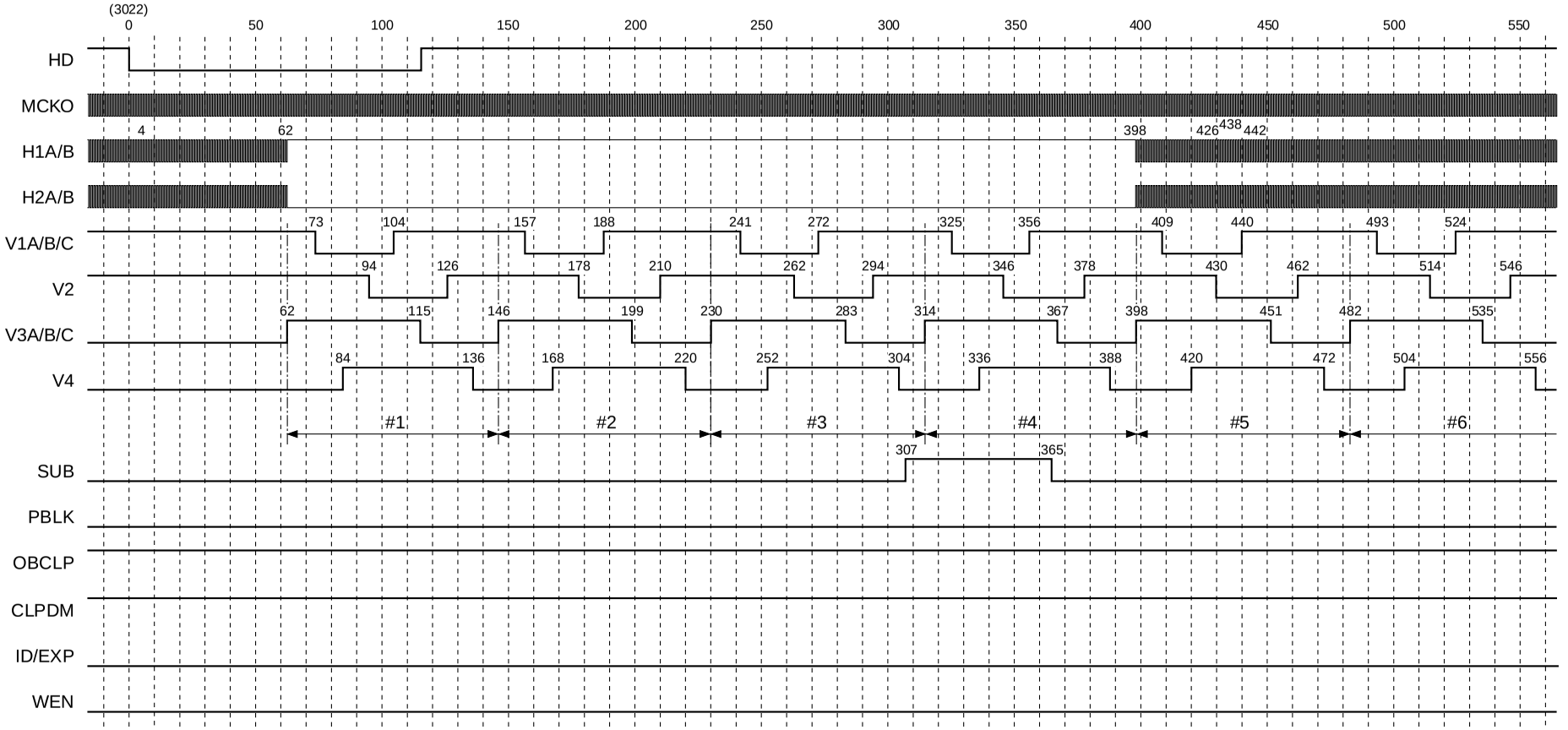


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows a period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* Frame shift of V1A/B/C, V2, V3A/B/C and V4 is performed up to 90H 2864ck (#250) in the A Field of frame mode (center scan 1), 44H 2864ck (#250) in the B Field, 99H 1570ck (#369) in the A Field of frame mode (center scan 2), 53H 1570ck (#369) in the B Field, 32H 2864ck (#250) in progressive scan mode (center scan 1), and 46H 1646ck (#369) in progressive scan mode (center scan 2).

Chart-20 **Horizontal Direction Timing Chart**
(Frame shift: L)

MODE
Draft mode (AF1 and 2)

Applicable CCD image sensor
• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* Frame shift of V1A/B/C, V2, V3A/B/C and V4 is performed up to 18H 2092ck (#276) in draft mode (AF1), 22H 2100ck (#420) in draft mode (AF2).

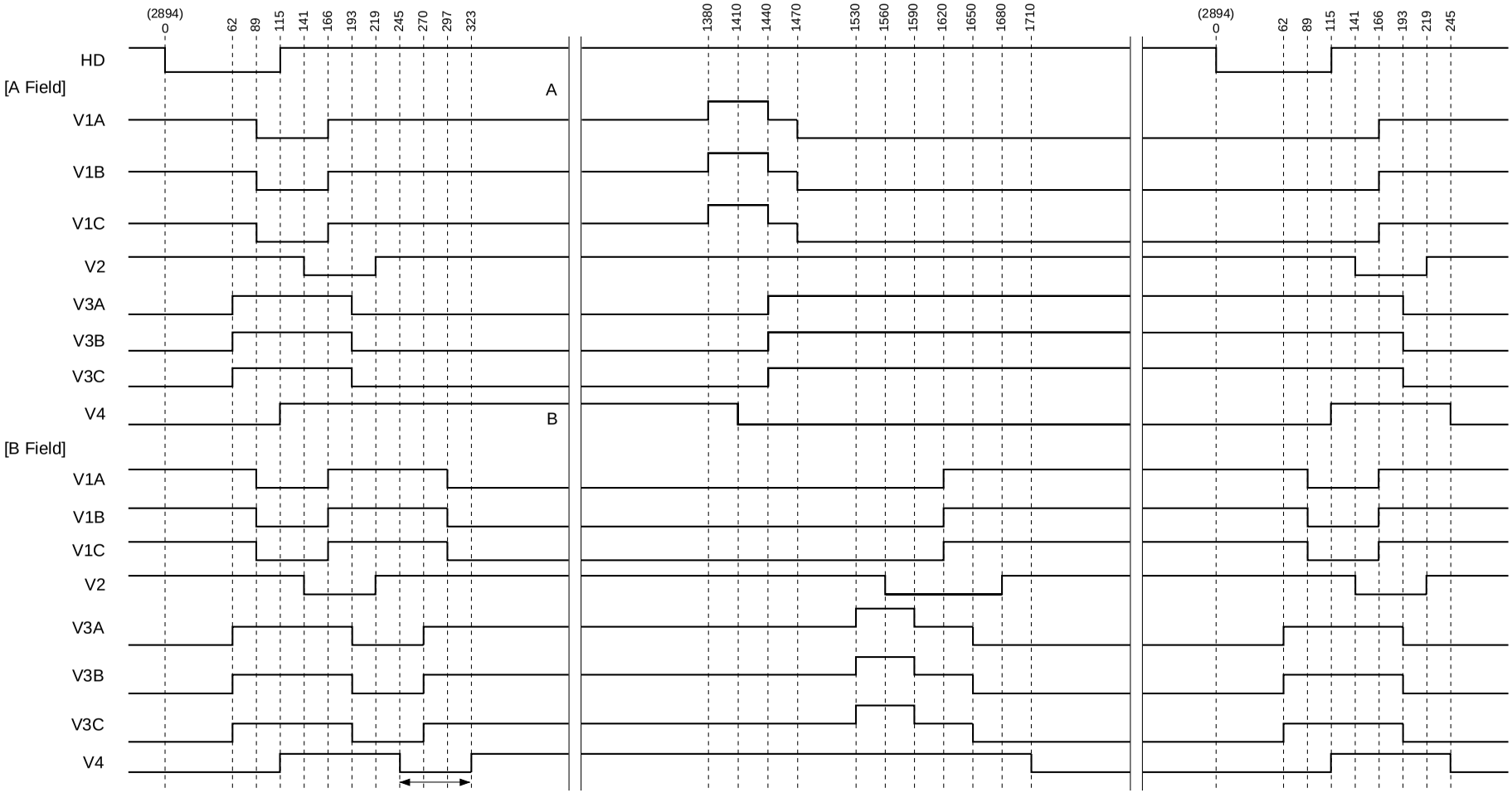
Chart-21 Horizontal Direction Timing Chart

MODE

Frame mode (including center scan 1 and 2)

Applicable CCD image sensor

• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.

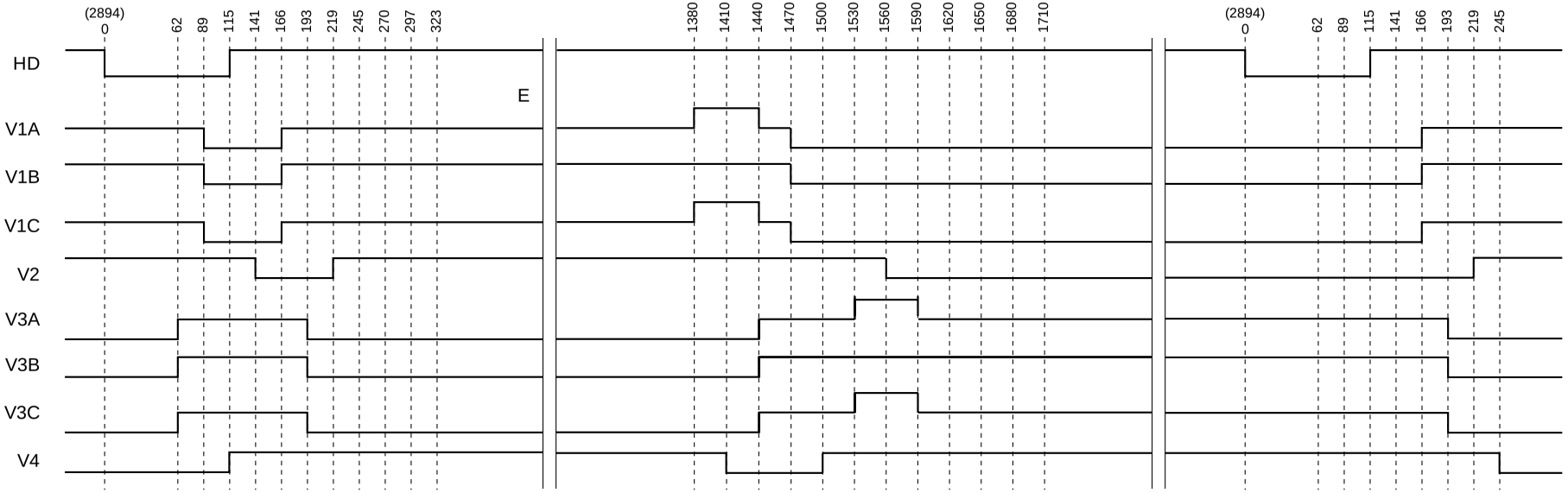
Chart-22 Horizontal Direction Timing Chart

MODE

Progressive scan mode (including center scan 1 and 2)

Applicable CCD image sensor

• ICX282

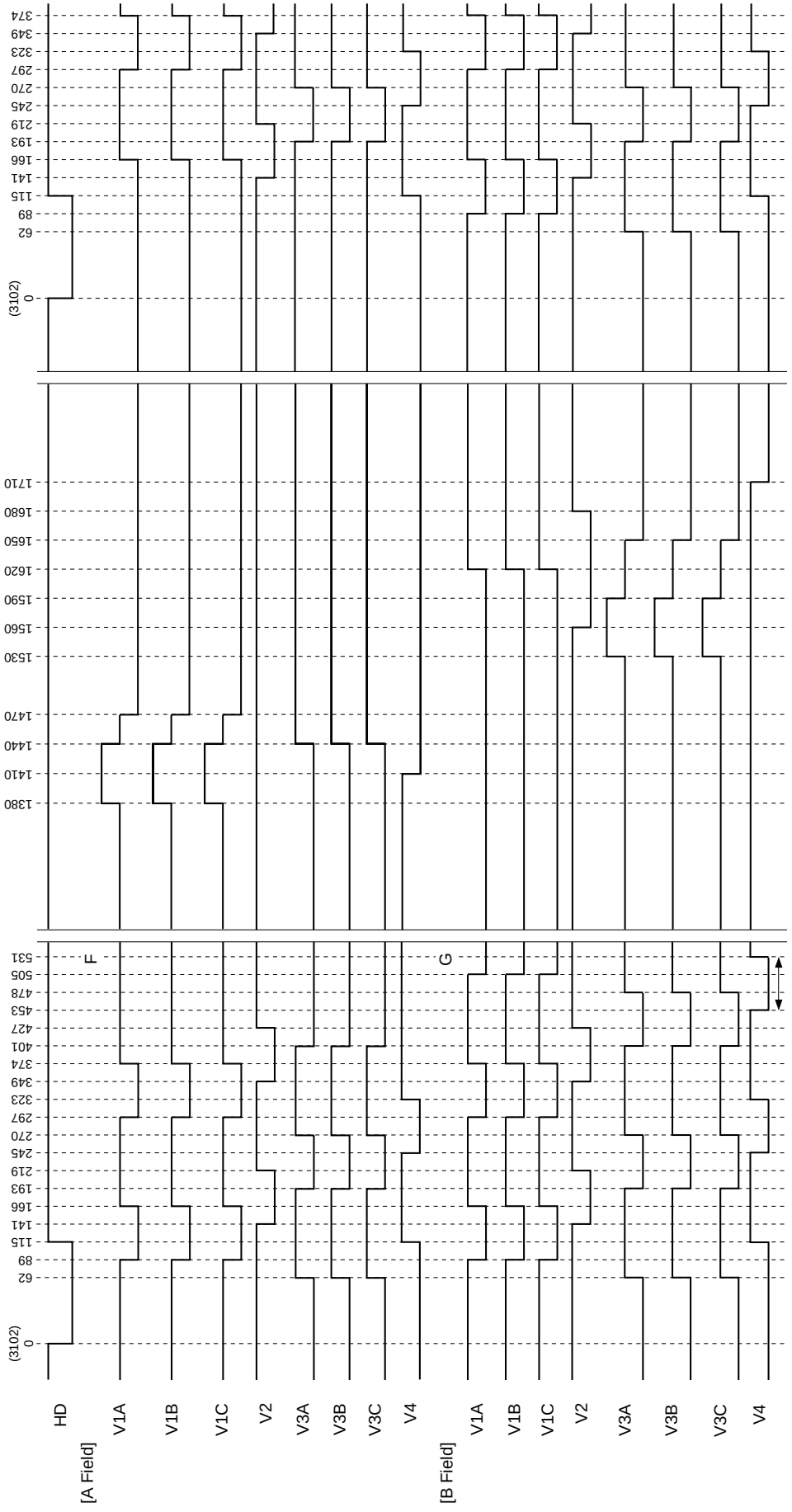


* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.

Chart-23 Horizontal Direction Timing Chart

MODE
Double speed mode

Applicable CCD image sensor
• ICX282



* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.

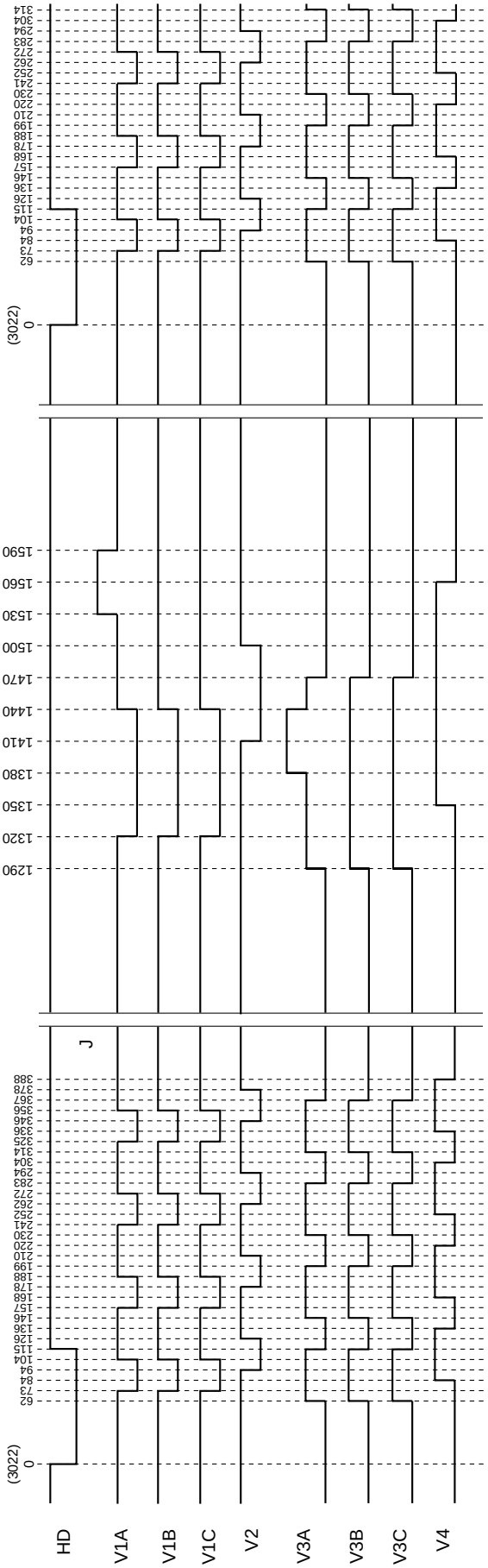
Chart-24 Horizontal Direction Timing Chart

MODE

Draft mode (including AF1 and 2)

Applicable CCD image sensor

• ICX282



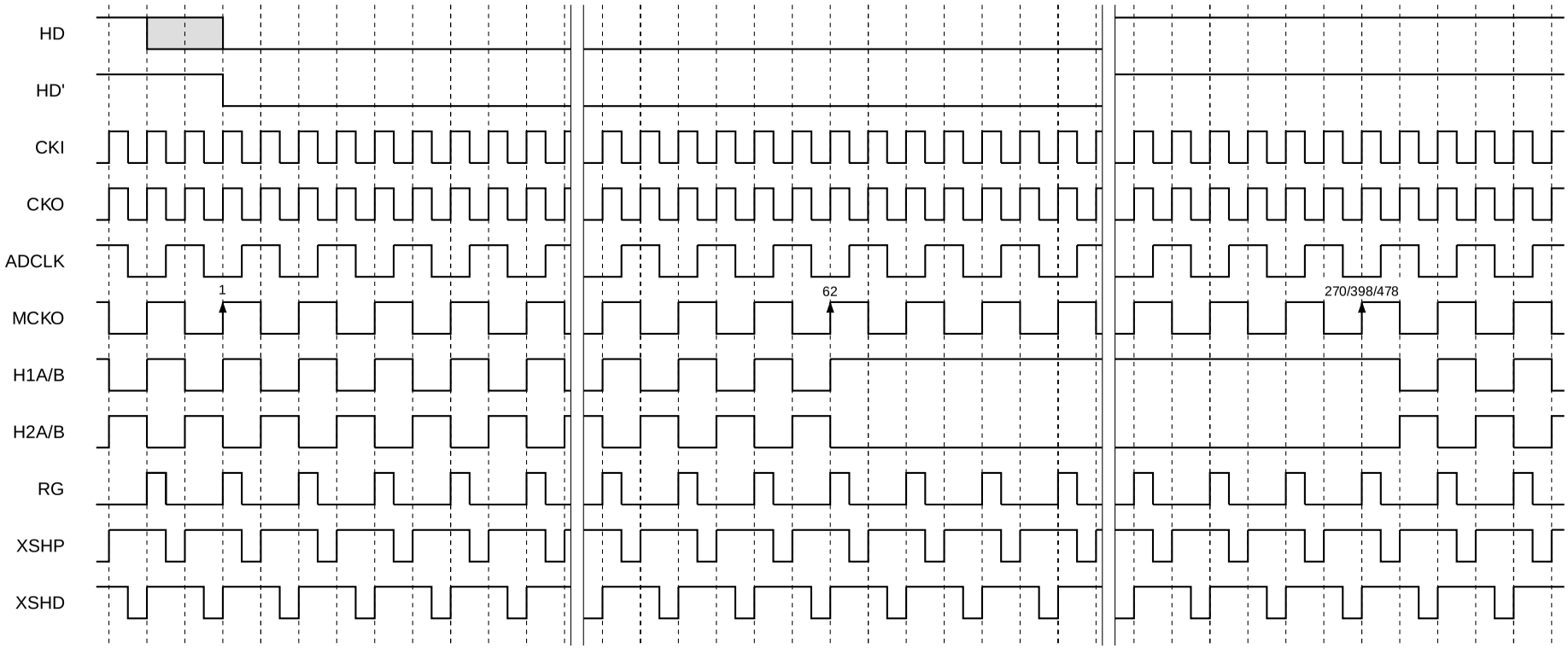
* The HD of this chart indicates the actual CXD2498R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.8 to 12.0µs (when the drive frequency is 22.5MHz). This chart shows an period of 115ck (5.1µs). Internal SSG is at this timing.

Chart-25 High-Speed Phase Timing Chart

MODE

Applicable CCD image sensor

• ICX282



* HD' indicates the HD which is the actual CXD2498R load timing.
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phase of ADCLK can be specified by the serial interface data.

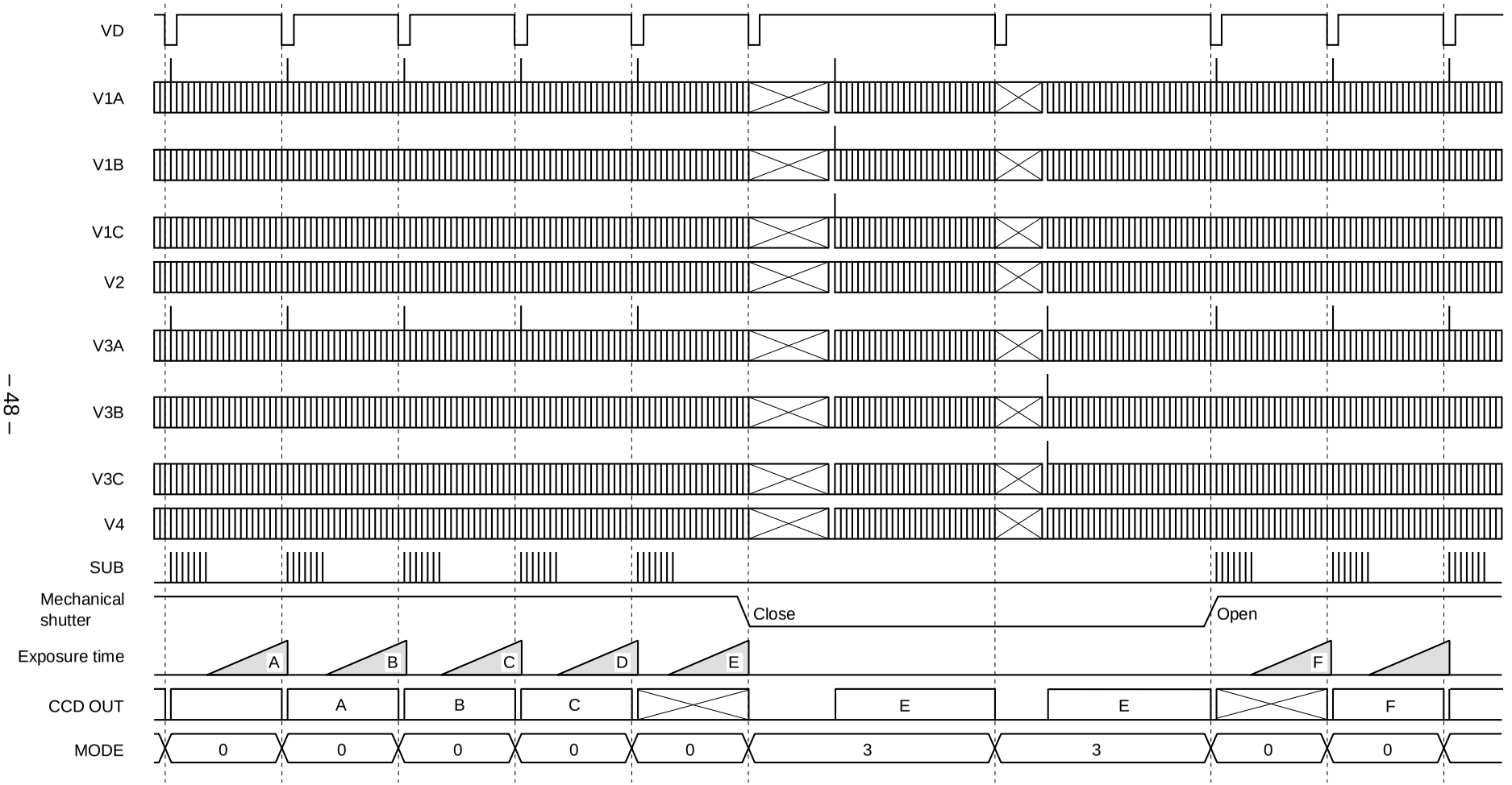
Chart-A1 Vertical Direction Sequence Chart

MODE

Draft → Frame (or double speed) → Draft

Applicable CCD image sensor

• ICX282



* This chart is a drive timing chart example of electronic shutter normal operation.
* Data exposed at D includes the blooming component. For details, see the CCD image sensor data sheet.
* The CXD2498R does not generate the pulse to control mechanical shutter operation.
* The switching timing of drive mode and electronic shutter data are not the same.

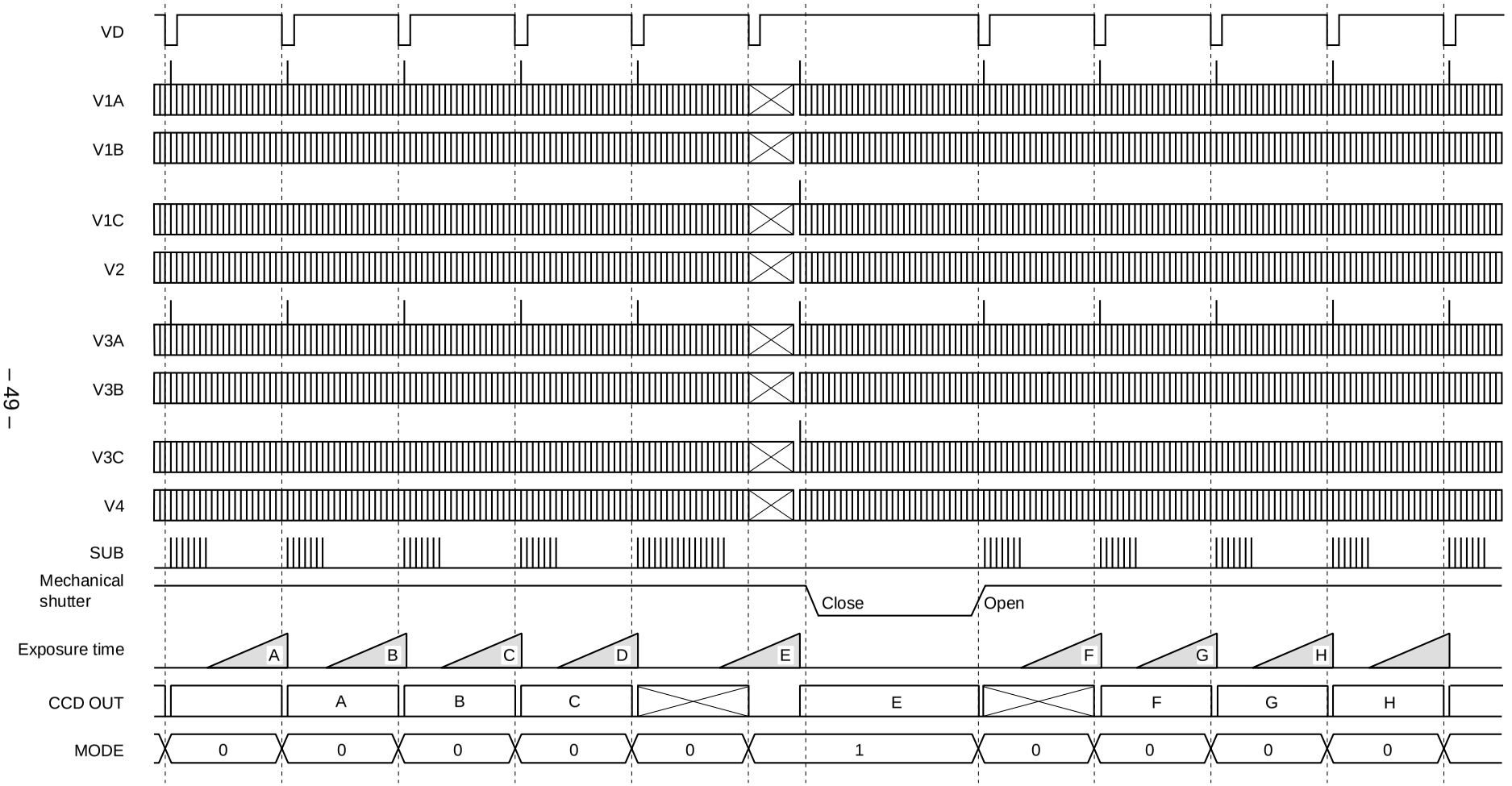
Chart-A2 Vertical Direction Sequence Chart

MODE

Draft → Progressive scan → Draft

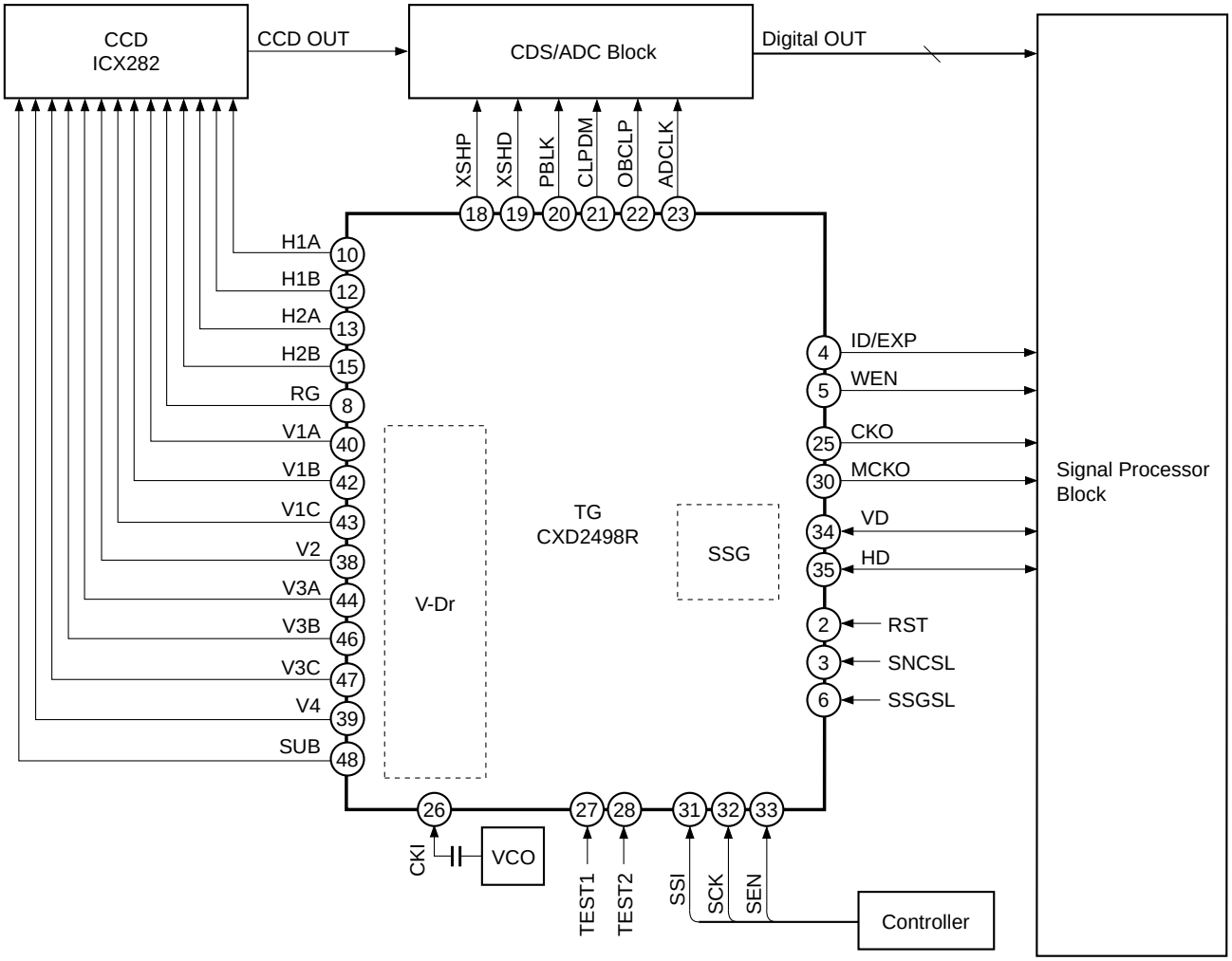
Applicable CCD image sensor

• ICX282



* This chart is a drive timing chart example of electronic shutter normal operation.
* Data exposed at D includes the blooming component. For details, see the CCD image sensor data sheet.
* The CXD2498R does not generate the pulse to control mechanical shutter operation.
* The switching timing of drive mode and electronic shutter data are not the same.

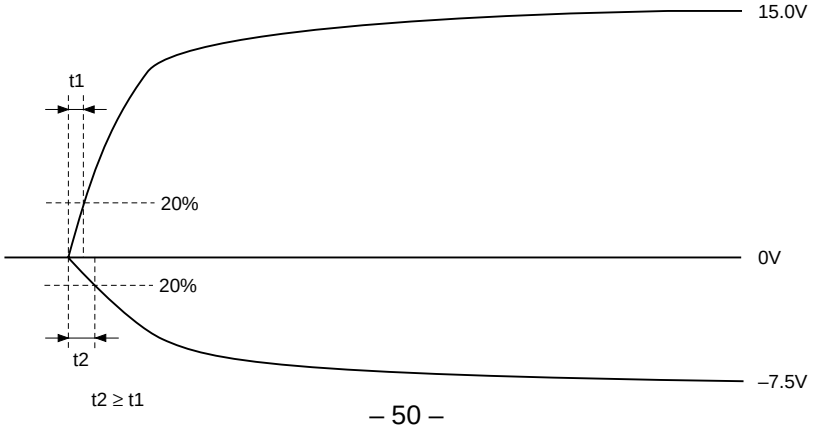
Application Circuit Block diagram



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

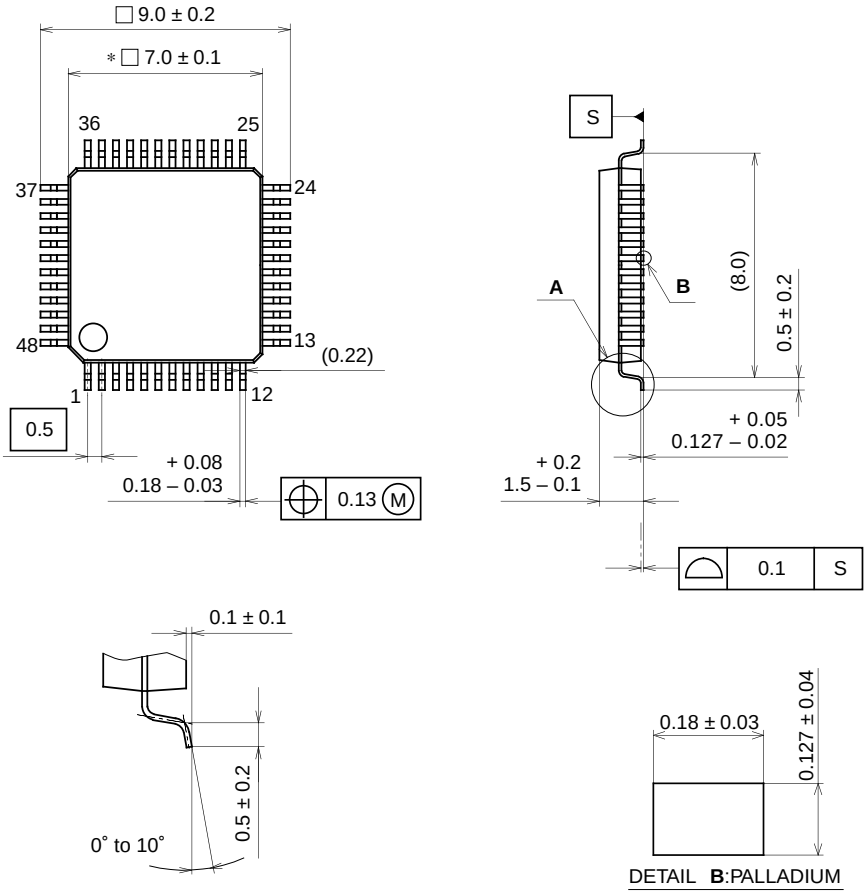
Notes for Power-on

Of the three –7.5V, +15.0V, +3.3V power supplies, be sure to start up the –7.5V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**:PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g