

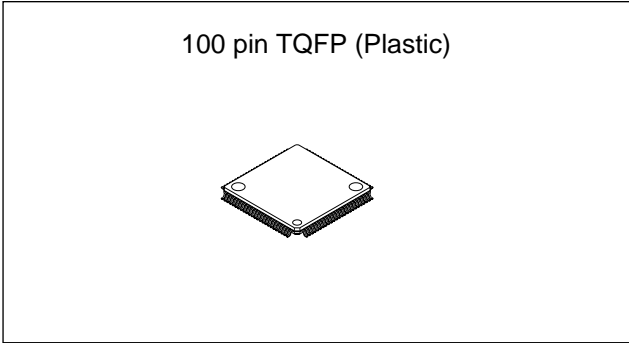
**LCD Interface IC**

**Description**

The CXD3508BTQ is a LCD interface IC for the color LCD module ACX704AKM driver.

**Features**

- Generates the color LCD module ACX704AKM drive pulse.
- Standby mode function
- Thin package (100-pin TQFP)



**Applications**

PDA, compact LCD monitor, etc.

**Structure**

Silicon gate CMOS IC

**Absolute Maximum Ratings** (Ta = 25°C)

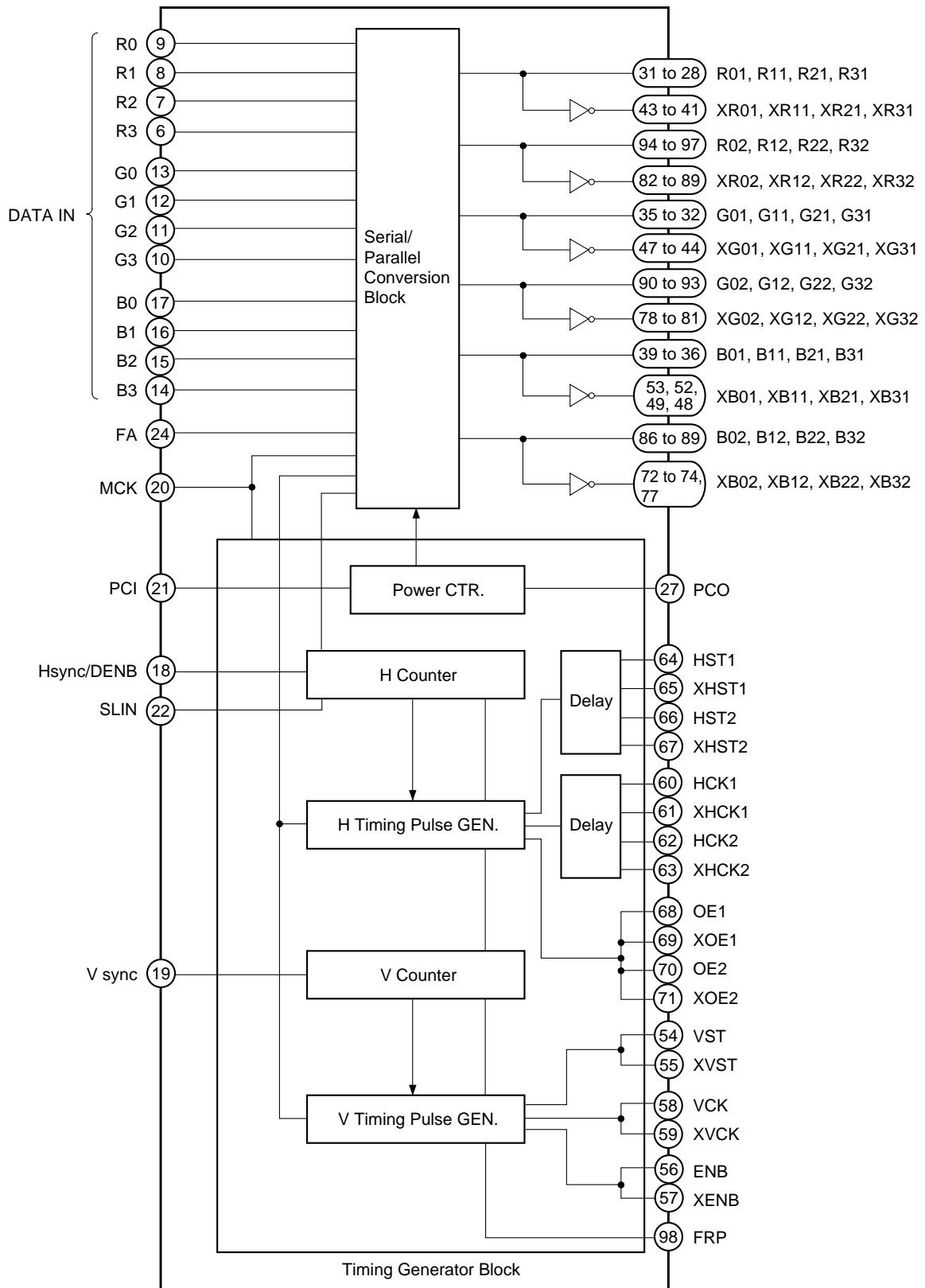
- |                         |                  |  |    |
|-------------------------|------------------|--|----|
| • Supply voltage        | V <sub>DD</sub>  | V <sub>SS</sub> – 0.5 to +4.0                  | V  |
| • Input voltage         | V <sub>I</sub>   | V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5 | V  |
| • Output voltage        | V <sub>O</sub>   | V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5 | V  |
| • Operating temperature | T <sub>opr</sub> | –25 to +75                                     | °C |
| • Storage temperature   | T <sub>stg</sub> | –55 to +125                                    | °C |

**Recommended Operating Conditions**

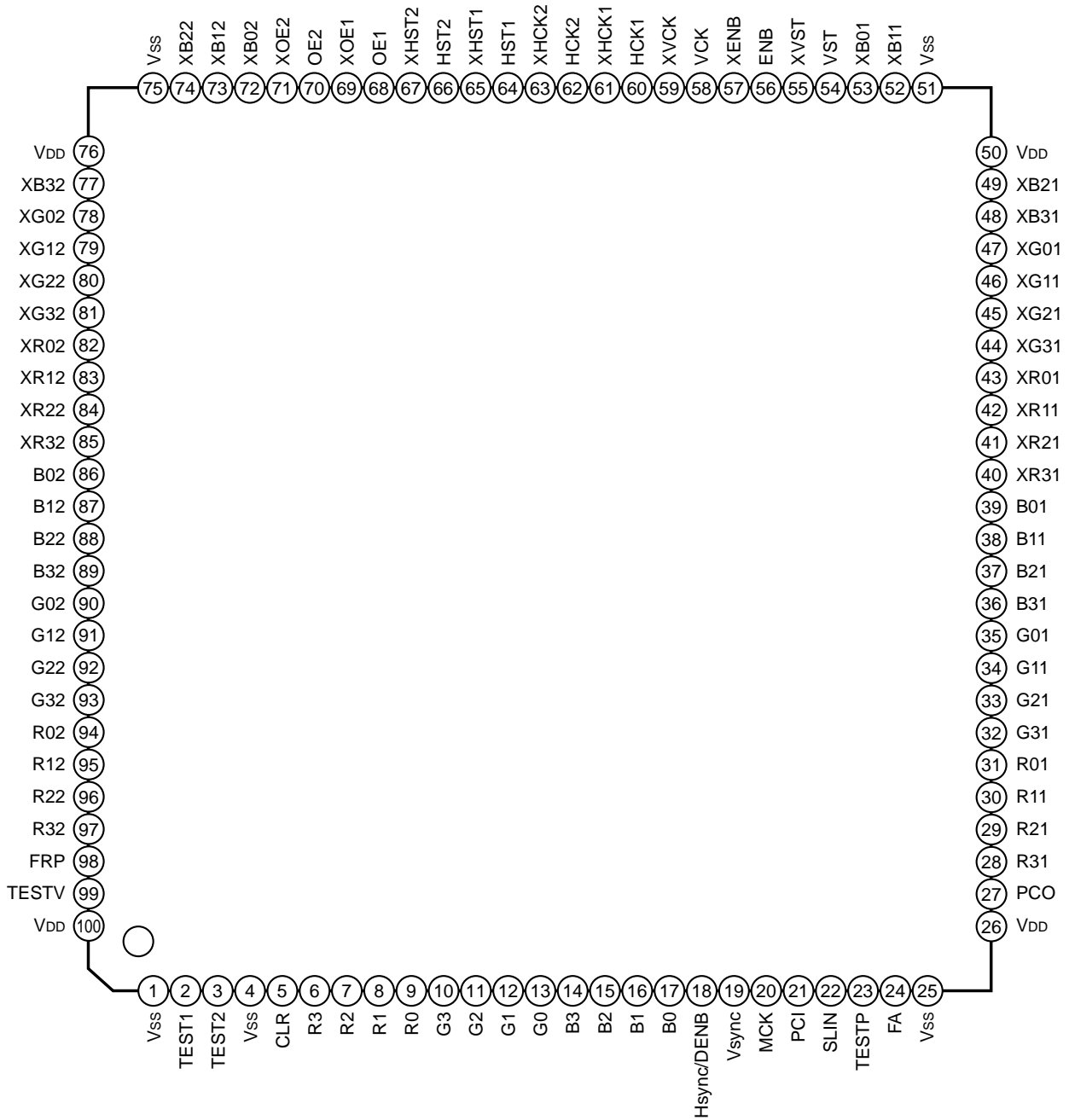
- |                         |                  |            |    |
|-------------------------|------------------|------------|----|
| • Supply voltage        | V <sub>DD</sub>  | 3.0 to 3.6 | V  |
| • Operating temperature | T <sub>opr</sub> | –10 to +60 | °C |

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Configuration



## Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	V <sub>SS</sub>	—	GND	—
2	TEST1	I	Test signal input (Connect to GND)	DWN*1
3	TEST2	I	Test signal input (Connect to GND)	DWN*1
4	V <sub>SS</sub>	—	GND	—
5	CLR	I	System reset	UP*2
6	R3	I	Red signal input (MSB)	—
7	R2	I	Red signal input	—
8	R1	I	Red signal input	—
9	R0	I	Red signal input (LSB)	—
10	G3	I	Green signal input (MSB)	—
11	G2	I	Green signal input	—
12	G1	I	Green signal input	—
13	G0	I	Green signal input (LSB)	—
14	B3	I	Blue signal input (MSB)	—
15	B2	I	Blue signal input	—
16	B1	I	Blue signal input	—
17	B0	I	Blue signal input (LSB)	—
18	Hsync/DENB	I	Hsync/data enable pulse input	—
19	Vsync	I	Vsync pulse input	—
20	MCK	I	Dot clock input	—
21	PCI	I	Power control signal input	—
22	SLIN	I	Sync input signal mode switch	—
23	TESTP	I	Test signal input (Connect to V <sub>DD</sub> )	—
24	FA	I	Data phase adjustment (Connect to GND)	—
25	V <sub>SS</sub>	—	GND	—
26	V <sub>DD</sub>	—	Power supply	—
27	PCO	O	Power control signal output	—
28	R31	O	Red signal output	—
29	R21	O	Red signal output	—
30	R11	O	Red signal output	—
31	R01	O	Red signal output	—
32	G31	O	Green signal output	—
33	G21	O	Green signal output	—

\*1 Built-in pull-down resistor (50kΩ typ.)

\*2 Built-in pull-up resistor (50kΩ typ.)

Pin No.	Symbol	I/O	Description	Input pin for open status
34	G11	O	Green signal output	—
35	G01	O	Green signal output	—
36	B31	O	Blue signal output	—
37	B21	O	Blue signal output	—
38	B11	O	Blue signal output	—
39	B01	O	Blue signal output	—
40	XR31	O	Red signal output (inverse)	—
41	XR21	O	Red signal output (inverse)	—
42	XR11	O	Red signal output (inverse)	—
43	XR01	O	Red signal output (inverse)	—
44	XG31	O	Green signal output (inverse)	—
45	XG21	O	Green signal output (inverse)	—
46	XG11	O	Green signal output (inverse)	—
47	XG01	O	Green signal output (inverse)	—
48	XB31	O	Blue signal output (inverse)	—
49	XB21	O	Blue signal output (inverse)	—
50	V <sub>DD</sub>	—	Power supply	—
51	V <sub>SS</sub>	—	GND	—
52	XB11	O	Blue signal output (inverse)	—
53	XB01	O	Blue signal output (inverse)	—
54	VST	O	VST pulse output	—
55	XVST	O	VST pulse output (inverse)	—
56	ENB	O	ENB pulse output	—
57	XENB	O	ENB pulse output (inverse)	—
58	VCK	O	VCK pulse output	—
59	XVCK	O	VCK pulse output (inverse)	—
60	HCK1	O	HCK1 pulse output	—
61	XHCK1	O	HCK1 pulse output (inverse)	—
62	HCK2	O	HCK2 pulse output	—
63	XHCK2	O	HCK2 pulse output (inverse)	—
64	HST1	O	HST1 pulse output	—
65	XHST1	O	HST1 pulse output (inverse)	—
66	HST2	O	HST2 pulse output	—
67	XHST2	O	HST2 pulse output (inverse)	—

Pin No.	Symbol	I/O	Description	Input pin for open status
68	OE1	O	OE1 pulse output	—
69	XOE1	O	OE1 pulse output (inverse)	—
70	OE2	O	OE2 pulse output	—
71	XOE2	O	OE2 pulse output (inverse)	—
72	XB02	O	Blue signal output (inverse)	—
73	XB12	O	Blue signal output (inverse)	—
74	XB22	O	Blue signal output (inverse)	—
75	V <sub>SS</sub>	—	GND	—
76	V <sub>DD</sub>	—	Power supply	—
77	XB32	O	Blue signal output (inverse)	—
78	XG02	O	Green signal output (inverse)	—
79	XG12	O	Green signal output (inverse)	—
80	XG22	O	Green signal output (inverse)	—
81	XG32	O	Green signal output (inverse)	—
82	XR02	O	Red signal output (inverse)	—
83	XR12	O	Red signal output (inverse)	—
84	XR22	O	Red signal output (inverse)	—
85	XR32	O	Red signal output (inverse)	—
86	B02	O	Blue signal output	—
87	B12	O	Blue signal output	—
88	B22	O	Blue signal output	—
89	B32	O	Blue signal output	—
90	G02	O	Green signal output	—
91	G12	O	Green signal output	—
92	G22	O	Green signal output	—
93	G32	O	Green signal output	—
94	R02	O	Red signal output	—
95	R12	O	Red signal output	—
96	R22	O	Red signal output	—
97	R32	O	Red signal output	—
98	FRP	O	Polarity inversion pulse signal output	—
99	TESTV	I	Test signal input (Connect to GND)	—
100	V <sub>DD</sub>	—	Power supply	—

Electrical Characteristics

DC Characteristics

(V<sub>DD</sub> = 3.0 to 3.6V, Ta = -25 to + 75°C)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	—	3.0	3.3	3.6	V
Current consumption	I <sub>DD</sub>	—	No load, Ta = 25°C, V <sub>DD</sub> = 3.3V, MCK: 5.58MHz	—	0.9	—	mA
Input voltage 1	V <sub>IH1</sub>	MCK	LVTTTL input cell	2.0	—	—	V
	V <sub>IL1</sub>			—	—	0.8	
Input voltage 2	V <sub>t+</sub>	All output pins excluding MCK	LVTTTL Schmitt trigger input cell	—	—	2.0	V
	V <sub>t-</sub>			0.5	—	—	
	V <sub>t+</sub> - V <sub>t-</sub>			0.2	—	—	
Input current 1	I <sub>IL1</sub>	R0, R1, R2, R3, G0, G1, G2, G3, B0, B1, B2, B3, Hsync/DENB, Vsync, MCK, PCI, SLIN, FA, TESTV, TESTP	V <sub>I</sub> = 0V	—	—	5.0	μA
	I <sub>IH1</sub>		V <sub>I</sub> = V <sub>DD</sub>	—	—	5.0	
Input current 2	I <sub>IL2</sub>	CLR	V <sub>I</sub> = 0V	8	—	100	μA
	I <sub>IH2</sub>		V <sub>I</sub> = V <sub>DD</sub>	—	—	5.0	
Input current 3	I <sub>IL3</sub>	TEST1, TEST2,	V <sub>I</sub> = 0V	—	—	5.0	μA
	I <sub>IH3</sub>		V <sub>I</sub> = V <sub>DD</sub>	10	—	100	
Output voltage 1	V <sub>OL1</sub>	ENB, XENB	I <sub>OL1</sub> = 0.75mA	—	—	0.2	V
	V <sub>OH1</sub>		I <sub>OH1</sub> = -0.50mA	V <sub>DD</sub> - 0.2	—	—	
Output voltage 2	V <sub>OL2</sub>	R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32, PCO, VST, XVST, VCK, XVCK, OE1, XOE1, OE2, XOE2, FRP	I <sub>OL2</sub> = 1.5mA	—	—	0.2	V
	V <sub>OH2</sub>		I <sub>OH2</sub> = -1.0mA	V <sub>DD</sub> - 0.2	—	—	
Output voltage 3	V <sub>OL3</sub>	HST1, XHST1, HST2, XHST2	I <sub>OL3</sub> = 3.0mA	—	—	0.2	V
	V <sub>OH3</sub>		I <sub>OH3</sub> = -2.0mA	V <sub>DD</sub> - 0.2	—	—	
Output voltage 4	V <sub>OL4</sub>	HCK1, XHCK1, HCK2, XHCK2	I <sub>OL4</sub> = 4.5mA	—	—	0.2	V
	V <sub>OH4</sub>		I <sub>OH4</sub> = -3.0mA	V <sub>DD</sub> - 0.2	—	—	

AC Characteristics

(V<sub>DD</sub> = 3.0 to 3.6V, T<sub>a</sub> = -10 to +60°C)

Item	Symbol	Applicable pins	Conditions*1	Min.	Typ.	Max.	Unit
HCK, HST time difference	$\Delta t_{\text{HST-HCKU}}$ $\Delta t_{\text{HST-HCKD}}$	HCK1, HCK2, XCHK1, XHCK2, HST1, HST2, XHST1, XHST2	—	—	—	15*2	ns
Data output rise time	t <sub>RD</sub>	R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32	GND – V <sub>DD</sub> (0 – 90%)	—	—	40	ns
Data output fall time	t <sub>FD</sub>		V <sub>DD</sub> – GND (100 – 10%)	—	—	40	
H pulse output rise time	t <sub>RHP</sub>	HCK1, HCK2, XCHK1, XHCK2, HST1, HST2, XHST1, XHST2	GND – V <sub>DD</sub> (0 – 90%)	—	—	30	ns
H pulse output fall time	t <sub>FHP</sub>		V <sub>DD</sub> – GND (100 – 10%)	—	—	30	
V pulse output rise time	t <sub>RVP</sub>	VCK, XVCK, VST, XVST, OE1, OE2, XOE1, XOE2, FRP, PCO	GND – V <sub>DD</sub> (0 – 90%)	—	—	60	ns
V pulse output fall time	t <sub>FVP</sub>		V <sub>DD</sub> – GND (100 – 10%)	—	—	60	
ENB pulse output rise time	t <sub>REP</sub>	ENB, XENB	GND – V <sub>DD</sub> (0 – 90%)	—	—	80	ns
ENB pulse output fall time	t <sub>FEP</sub>		V <sub>DD</sub> – GND (100 – 10%)	—	—	80	
HCK1, HCK2, XHCK1, XHCK2, DATA setup time	t <sub>STP</sub>	HCK1, HCK2, XHCK1, XHCK2, R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32	*3	35	50	120	ns
HCK, VCK duty	dHCK dVCK	HCK1, HCK2, XHCK1, XHCK2, VCK, XVCK	*4	48	50	52	%

\*1 CL of each output pin is shown below.

- R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32, ENB, XENB: CL = 70pF
- HCK1, HCK2, XHCK1, XHCK2 : CL = 150pF
- HST, XHST, VCK, XVCK : CL = 100pF
- VST, XVST : CL = 85pF
- OE1, XOE1, OE2, XOE2, PCO, FRP : CL = 60pF

\*2 The absolute value of time difference (HST1, XHST1, HCK1, XHCK1) is within 15ns.

In the same manner, the absolute value of time difference (HST2, XHST2, HCK2, XHCK2) is within 15ns.

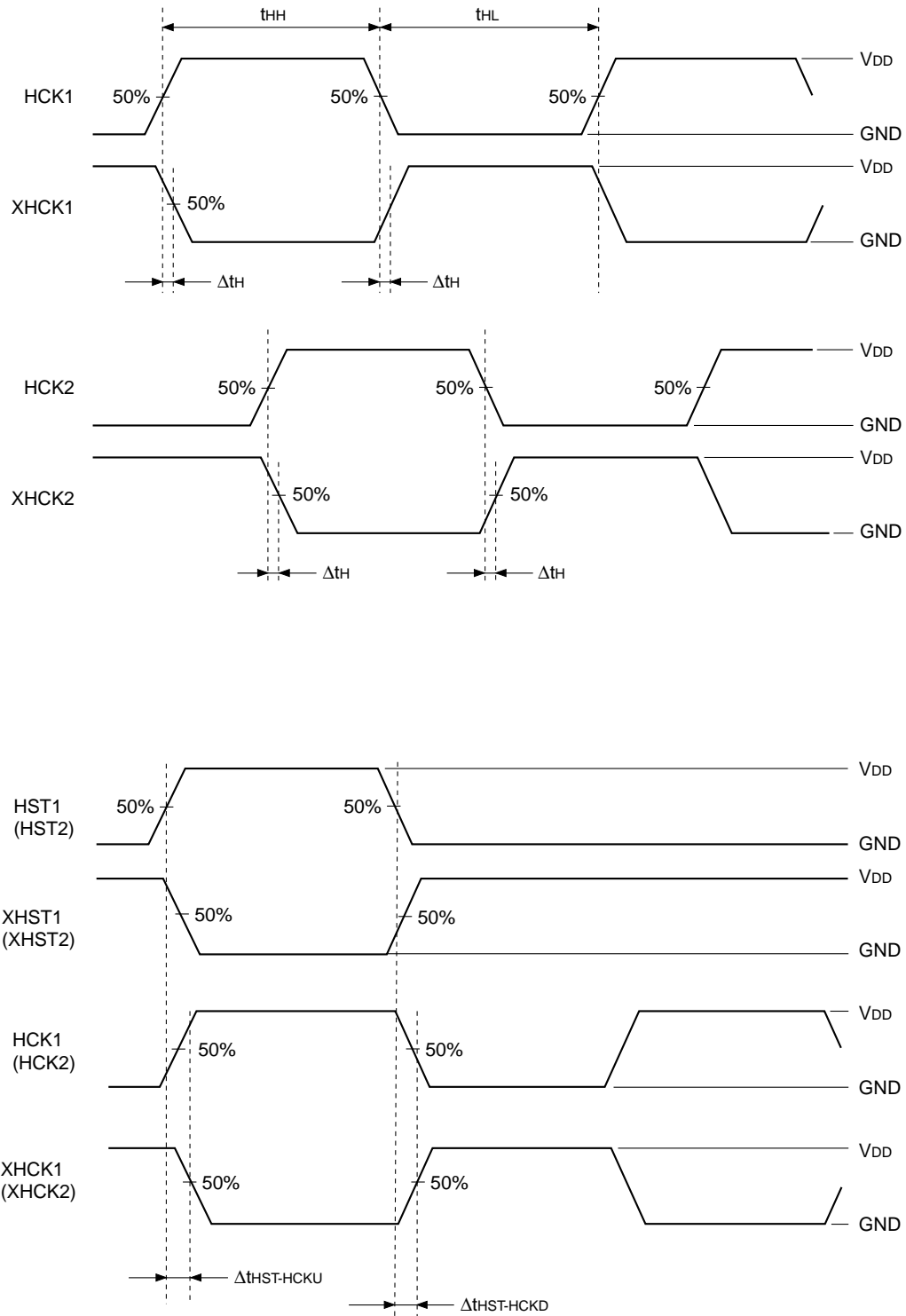
\*3 t<sub>STP</sub>: t<sub>ST1D</sub>, t<sub>ST1U</sub>, t<sub>ST2D</sub>, t<sub>ST2U</sub>

\*4 dHCK = (t<sub>HH</sub>/(t<sub>HH</sub> + t<sub>HL</sub>)) × 100, dVCK = (t<sub>VH</sub>/(t<sub>VH</sub> + t<sub>VL</sub>)) × 100

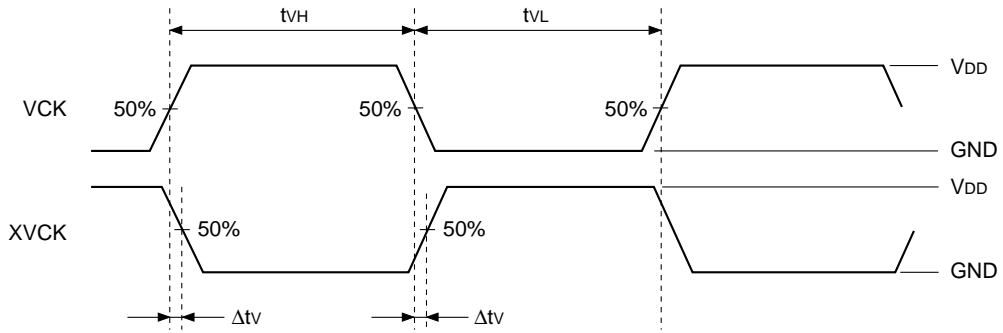


Timing Definition

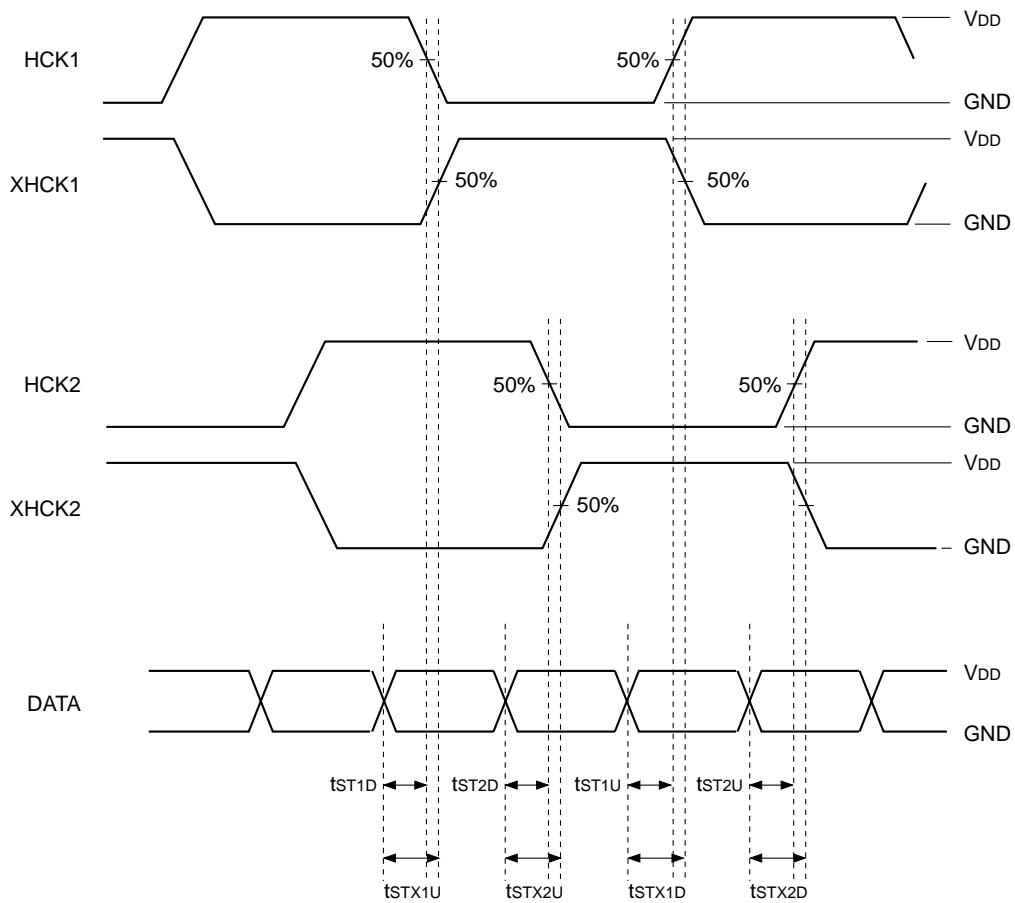
H system



V system



DATA



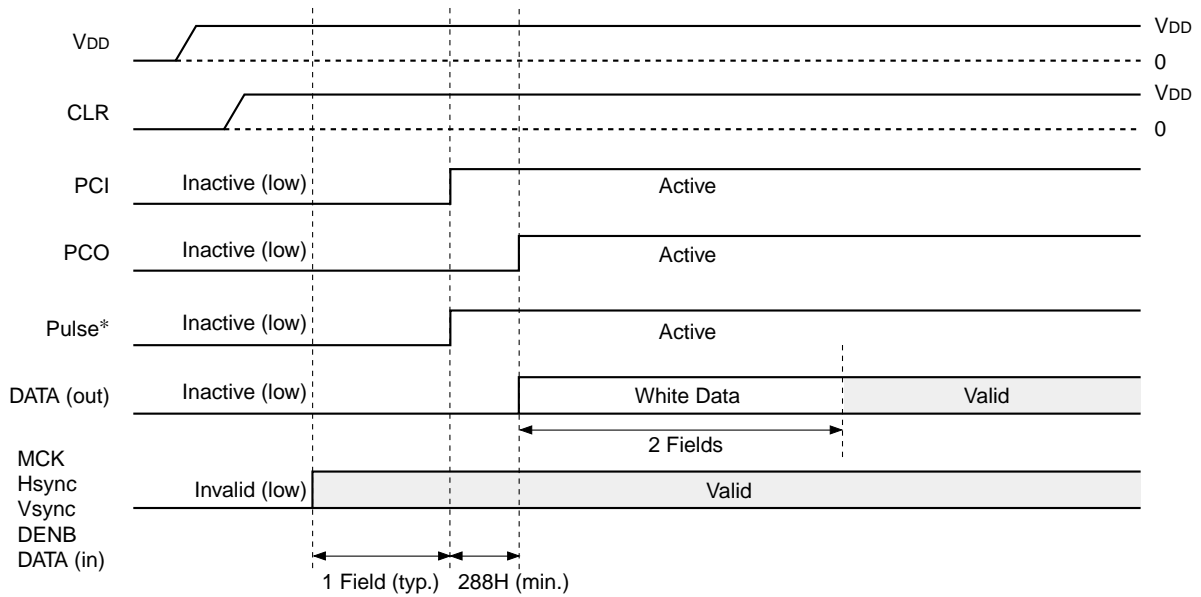
**PCI, PCO**

These pins control to turn power on/off of the ACX704AKM and the CXD3519TQ when the LCD is turned on/off.

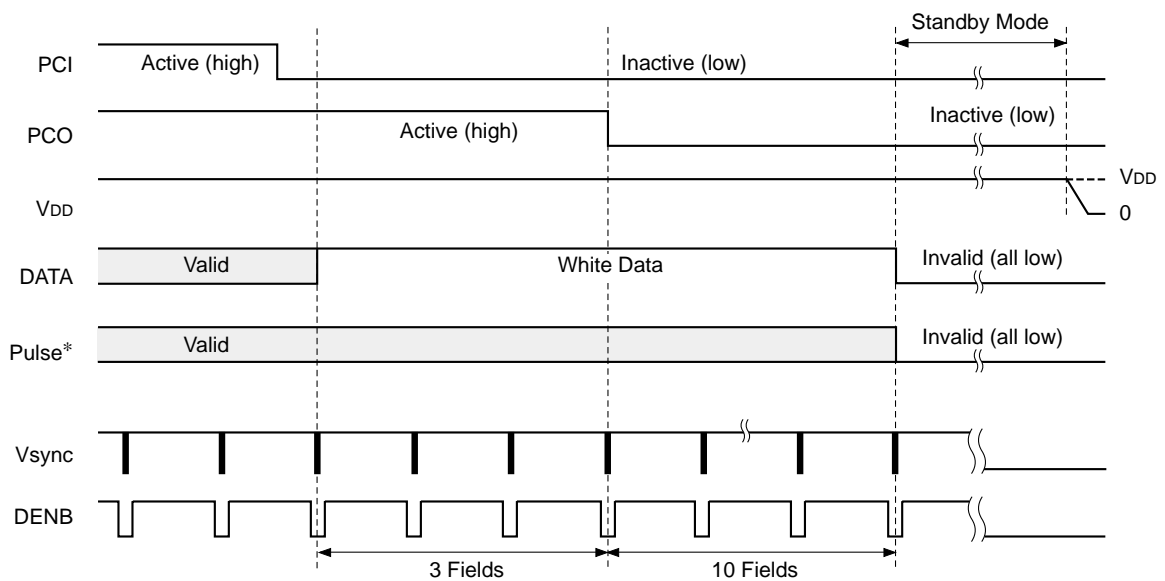
Connect PCO to DC-DC converter that can control power on/off of the ACX704AKM and the CXD3519TQ.

- When LCD is on, effective screen is displayed after entire white display (2 fields).
- When LCD is off, LCD is off after entire white display.

**Power On Sequence**



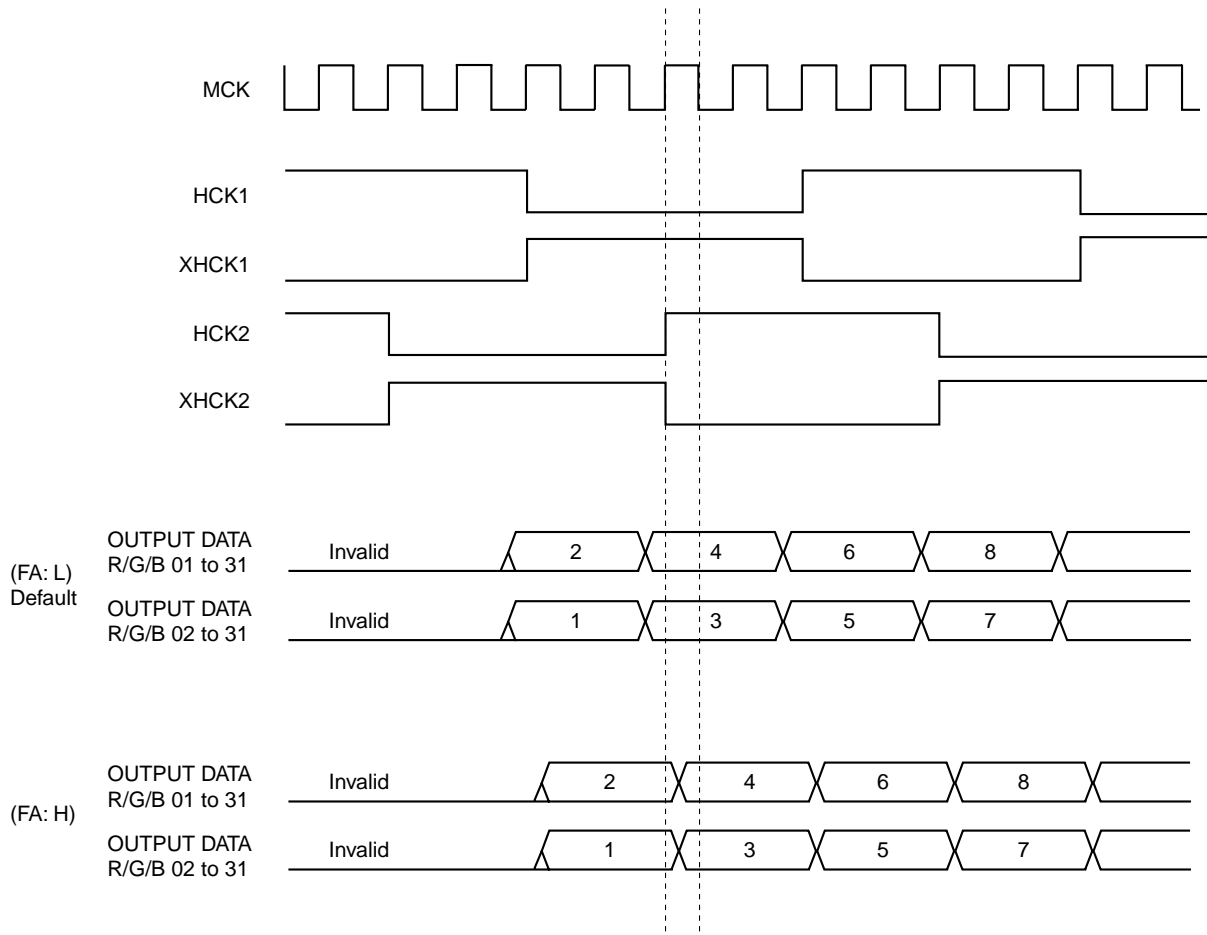
**Power Off Sequence (Standby)**



\* HST1, HST2, XHST1, XHST2, HCK1, HCK2, XHCK1, XHCK2, VST, XVST, VCK, XVCK, ENB, XENB, OE1, XOE1, OE2, XOE2, FRP

**FA**

This is a selector switch for phase relationship between data and other pulses.  
 (Normally, set to low.)

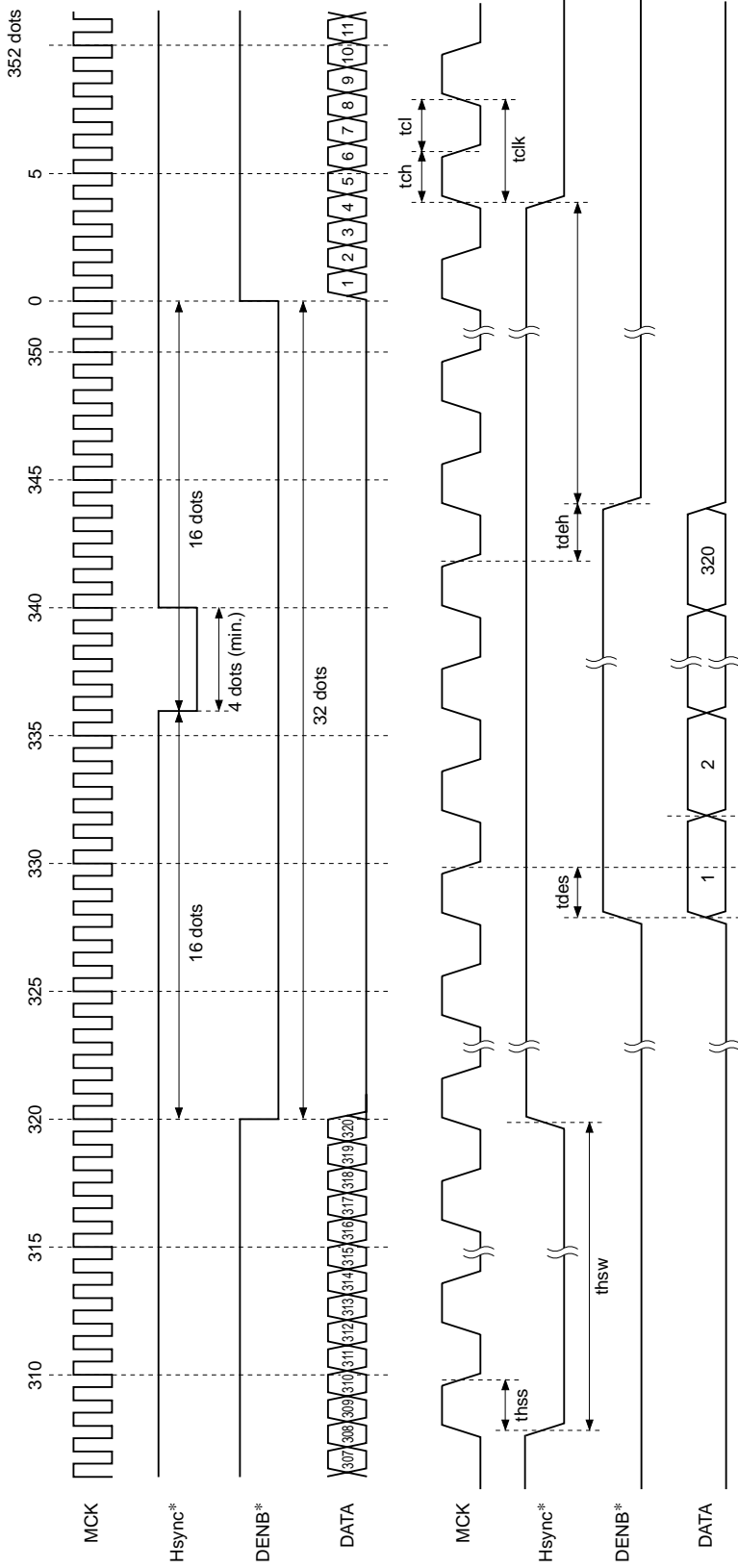


**SLIN**

This is a selector switch for input sync signal mode.

- SLIN: LOW → Hsync + Vsync Mode
- SLIN: HIGH → DENB ONLY Mode (Vsync input is invalid.)

Horizontal Direction Input Signal Timing Chart



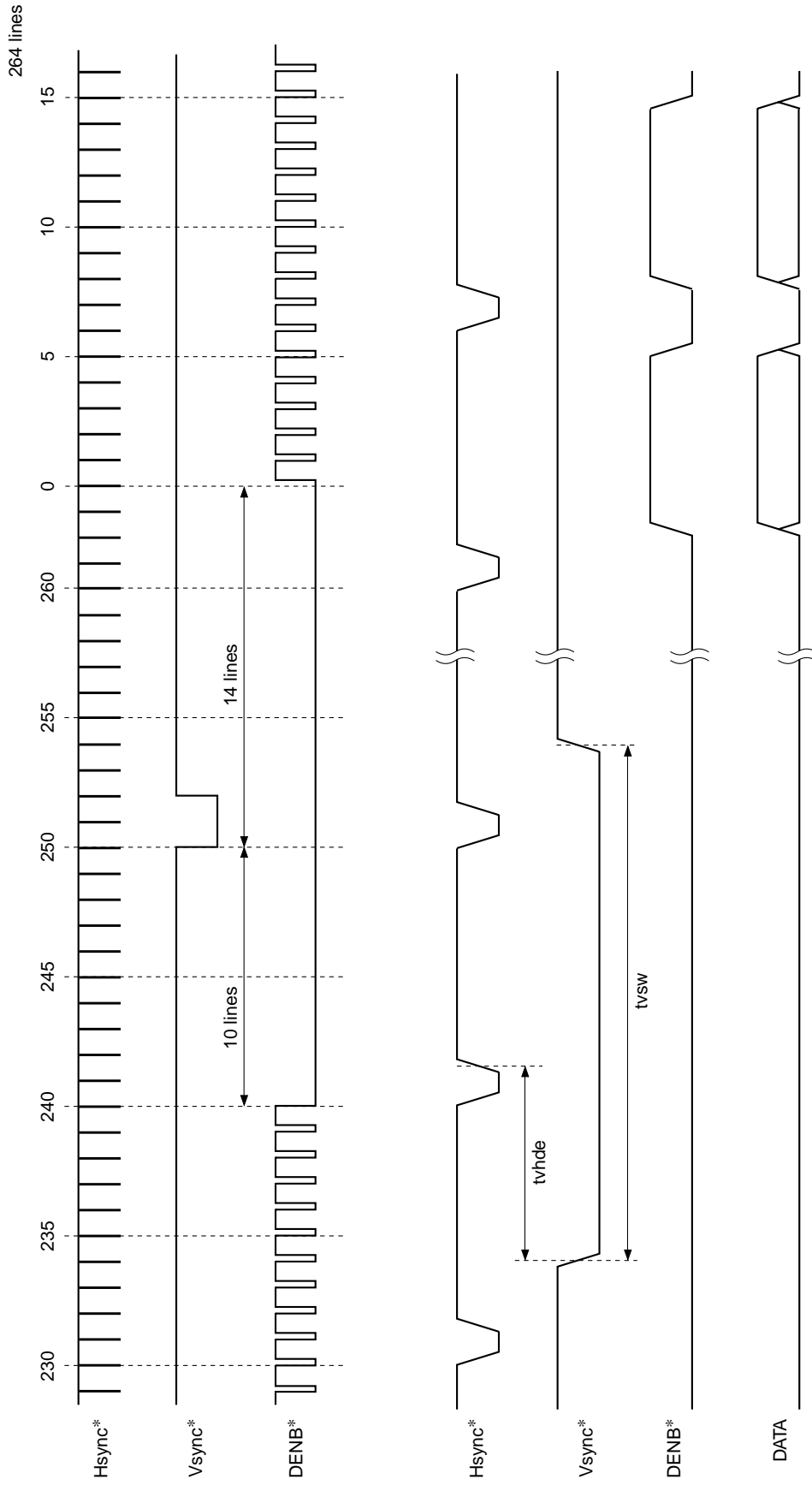
Input Signal AC Characteristics

(V<sub>DD</sub> = 3.0 to 3.6V, T<sub>a</sub> = -25 to +75°C)

Item	Symbol	Min.	Typ.	Max.
MCK frequency	fch	3MHz	5.58MHz	8MHz
MCK low, high pulse width	tch, tcl	-	0.5tclk	-
DATA setup time	tds	10ns	-	-
DATA hold time	tdh	15ns	-	-
DENB setup time	tdes	10ns	-	-
DENB hold time	tdeh	15ns	-	-
Hsync setup time	thss	10ns	-	-
Hsync low pulse width	thsw	4tclk	-	16tclk

\* Input either Hsync + Vsync or DENB as sync signal input.

Vertical Direction Input Signal Timing Chart



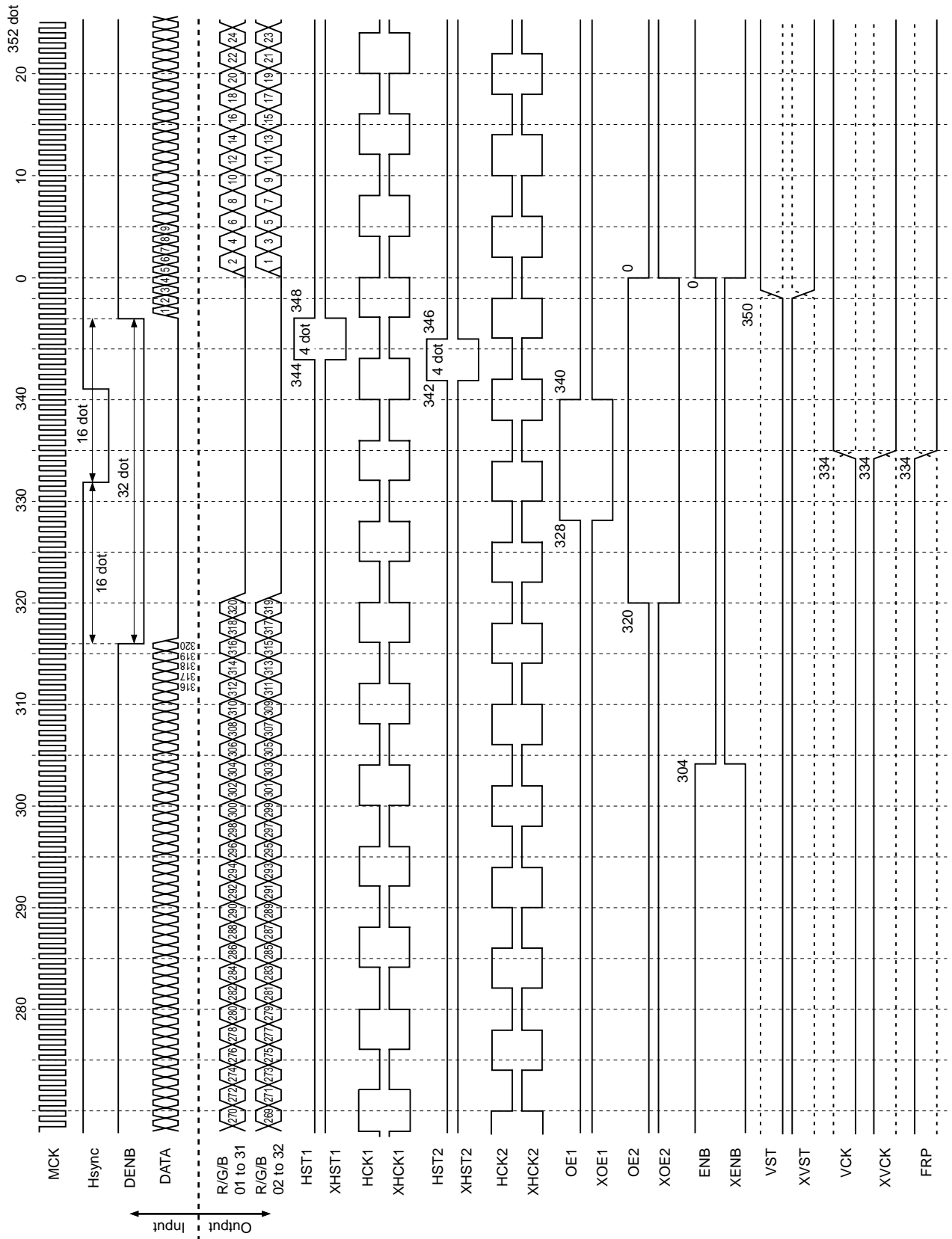
\* Input either Hsync + Vsync or DENB as sync signal input.

Input Signal AC Characteristics

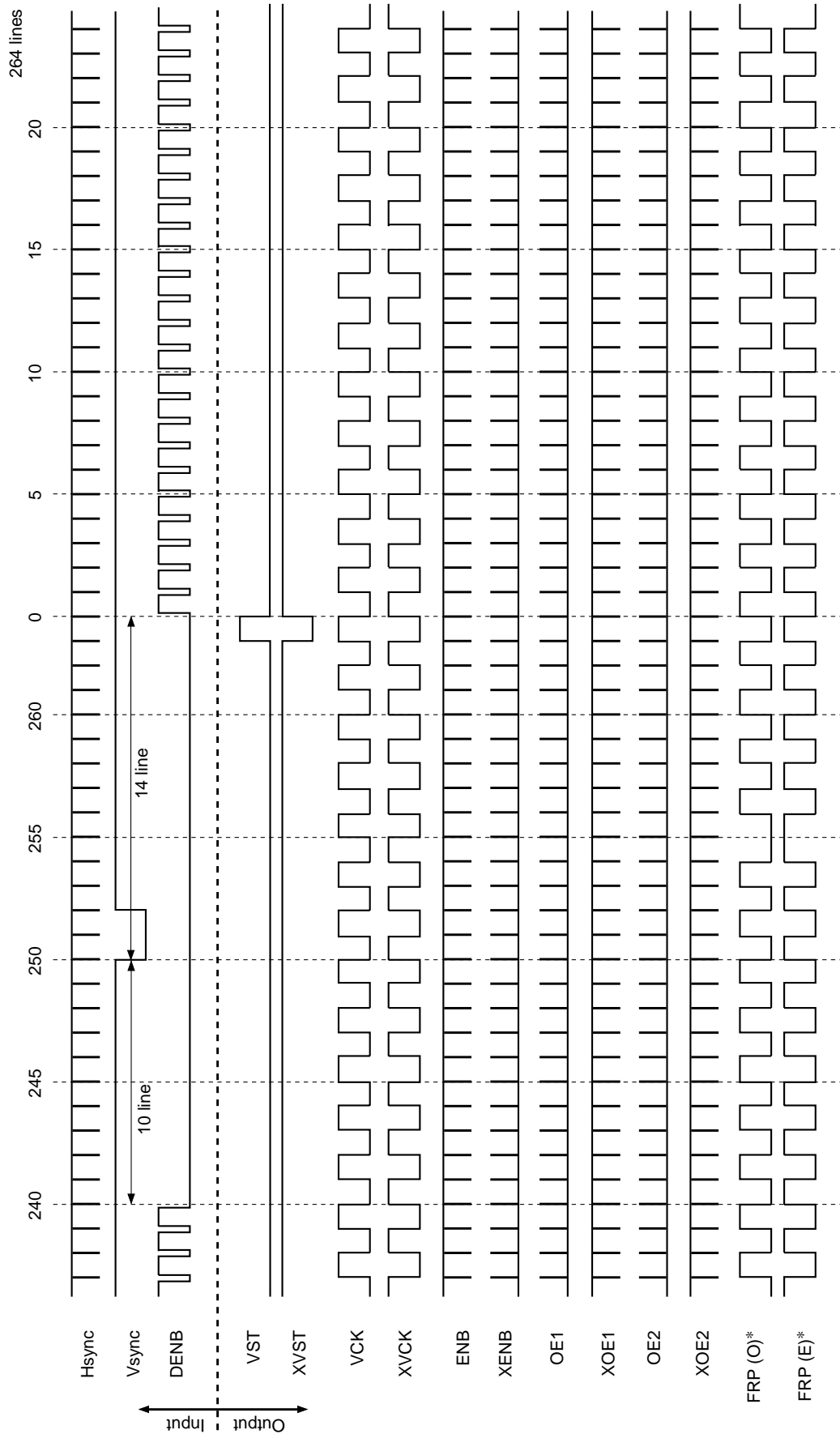
(V<sub>DD</sub> = 3.0 to 3.6V, Ta = -25 to +75°C)

Item	Symbol	Min.	Typ.	Max.
Vsync falling edge → Hsync rising edge	tvhde	334tclk	-	349tclk
Vsync low pulse width	tvsw	2 lines	-	14 lines

Horizontal Direction Timing Chart



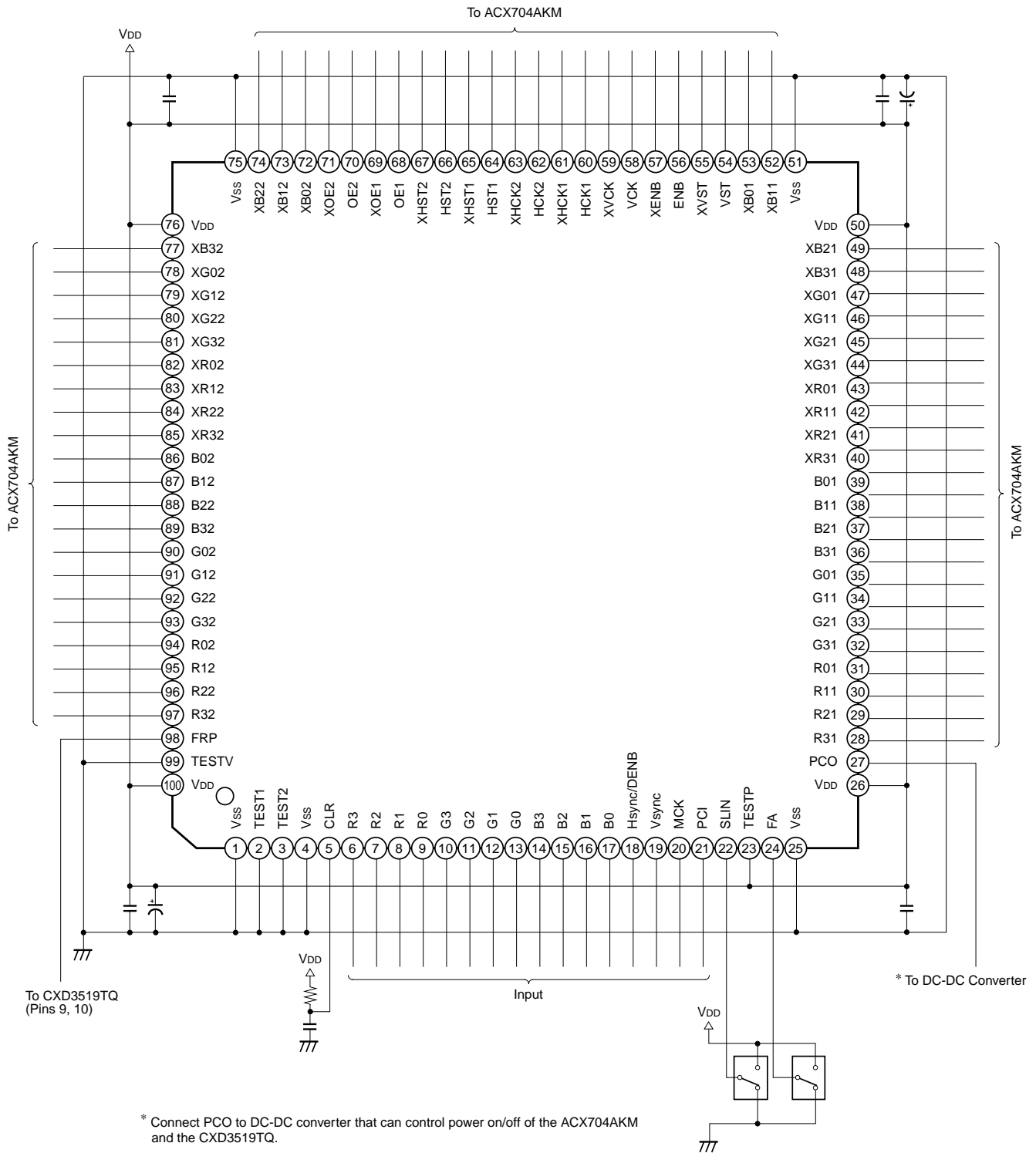
Vertical Direction Timing Chart



\* FRP (O): FRP output timing at odd field.  
FRP (E): FRP output timing at even field.



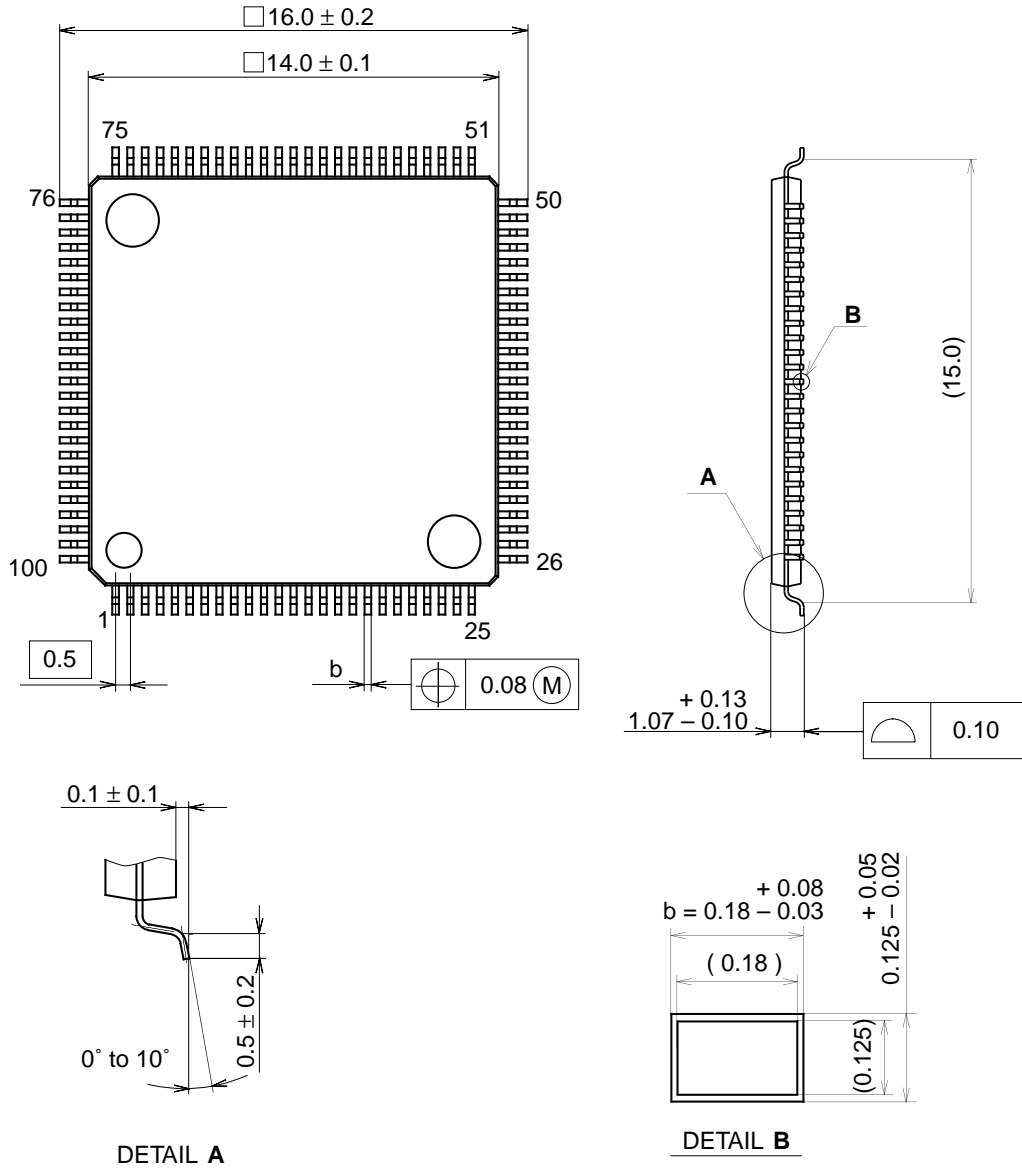
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN TQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	TQFP-100P-L021
EIAJ CODE	P-TQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.46g