

Interface and Driver IC for LCD

Description

The CXD3521GG is an interface and driver IC for the color LCD module ACX704AKM/BKM.

Features

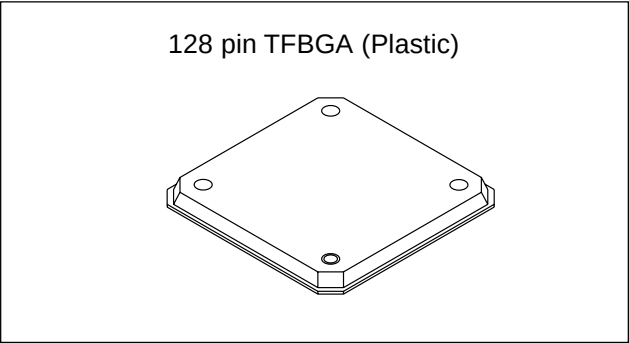
- Generates the color LCD module ACX704AKM/BKM drive pulse.
- Supports standby mode
- Built-in 9-channel reference voltage driver
- Built-in common voltage driver

Applications

PDA, compact LCD monitor, etc.

Structure

Silicon gate CMOS IC



Absolute Maximum Ratings (Ta = 25°C)

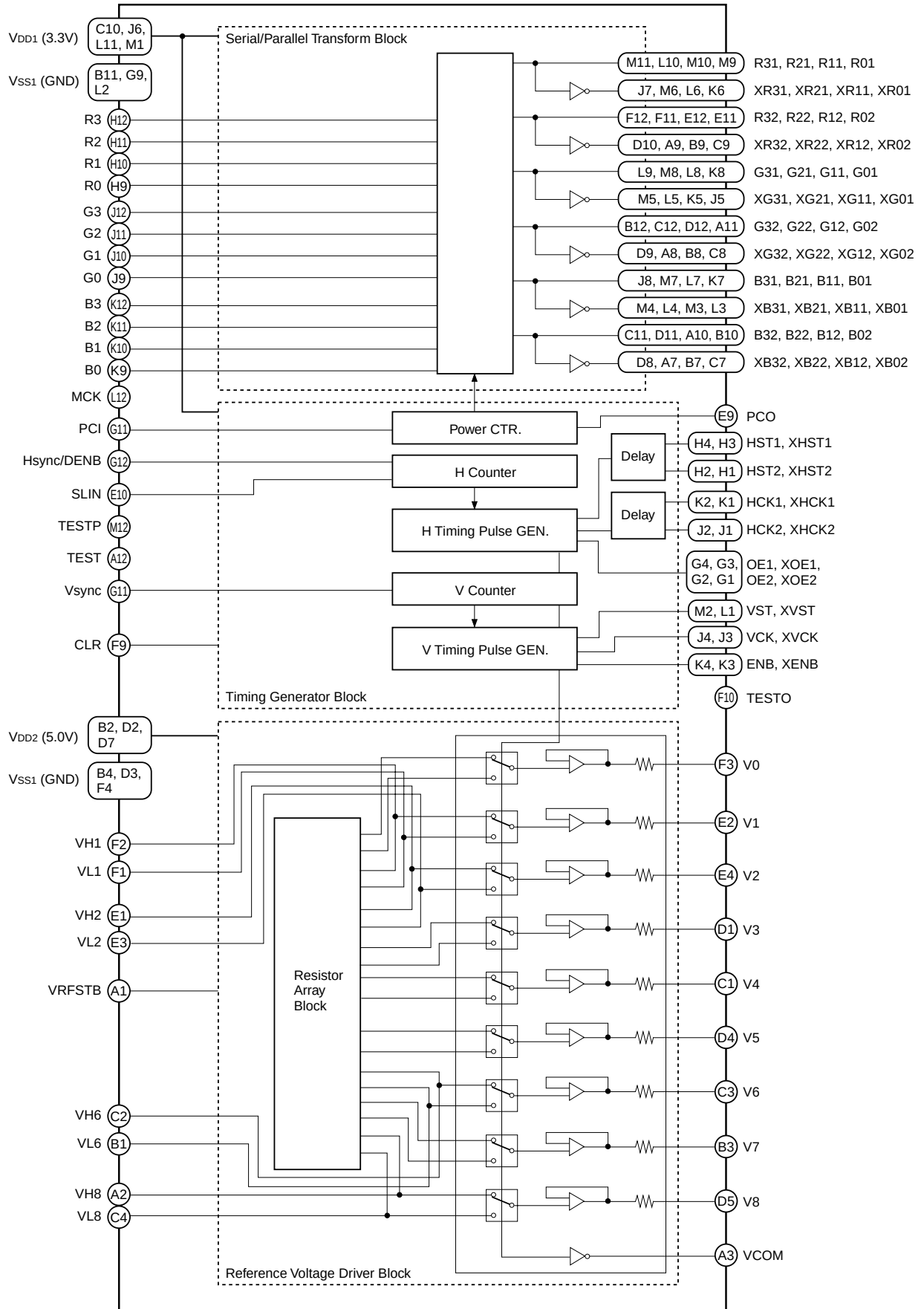
- Supply voltage 1 VDD1 VSS – 0.3 to +4.6 V
- Supply voltage 2 VDD2 VSS – 0.3 to +6.0 V
- Input voltage VI VSS – 0.3 to VDD + 0.3 V
- Output voltage VO VSS – 0.3 to VDD + 0.3 V
- Storage temperature Tstg –55 to +125 °C

Recommended Operating Conditions

- Supply voltage 1 VDD1 3.0 to 3.6 V
- Supply voltage 2 VDD2 4.7 to 5.3 V
- Operating temperature Topr –25 to +75 °C

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Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	 VRFSTB	 VH8	 VCOM	 TESTL1	 TESTL7	 TESTL5	 XB22	 XG22	 XR22	 B12	 G02	 TEST1
B	 VL6	 VDD2	 V7	 VSS2	 TESTL8	 TESTL4	 XB12	 XG12	 XR12	 B02	 VSS1	 G32
C	 V4	 VH6	 V6	 VL8	 TESTL2	 TESTL6	 XB02	 XG02	 XR02	 VDD1	 B32	 G22
D	 V3	 VDD2	 VSS2	 V5	 V8	 TESTL3	 VDD2	 XB32	 XG32	 XR32	 B22	 G12
E	 VH2	 V1	 VL2	 V2					 PCO	 SLIN	 R02	 R12
F	 VL1	 VH1	 V0	 VSS2					 CLR	 TESTO	 R22	 R32
G	 XOE2	 OE2	 XOE1	 OE1					 VSS1	 PCI	 Vsync	 Hsync/ DENB
H	 XHST2	 HST2	 XHST1	 HST1					 R0	 R1	 R2	 R3
J	 XHCK2	 HCK2	 XVCK	 VCK	 XG01	 VDD1	 XR31	 B31	 G0	 G1	 G2	 G3
K	 XHCK1	 HCK1	 XENB	 ENB	 XG11	 XR01	 B01	 G01	 B0	 B1	 B2	 B3
L	 XVST	 VSS1	 XB01	 XB21	 XG21	 XR11	 B11	 G11	 G31	 R21	 VDD1	 MCK
M	 VDD1	 VST	 XB11	 XB31	 XG31	 XR21	 B21	 G21	 R01	 R11	 R31	 TESTP

Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
B11	V _{SS1}	—	GND (Logic)	—
G9	V _{SS1}	—	GND (Logic)	—
L2	V _{SS1}	—	GND (Logic)	—
C10	V _{DD1}	—	Power supply (3.3V)	—
J6	V _{DD1}	—	Power supply (3.3V)	—
L11	V _{DD1}	—	Power supply (3.3V)	—
M1	V _{DD1}	—	Power supply (3.3V)	—
F9	CLR	I	System reset (Cleared at 0V)	UP*
H12	R3	I	Red signal input (MSB)	—
H11	R2	I	Red signal input	—
H10	R1	I	Red signal input	—
H9	R0	I	Red signal input (LSB)	—
J12	G3	I	Green signal input (MSB)	—
J11	G2	I	Green signal input	—
J10	G1	I	Green signal input	—
J9	G0	I	Green signal input (LSB)	—
K12	B3	I	Blue signal input (MSB)	—
K11	B2	I	Blue signal input	—
K10	B1	I	Blue signal input	—
K9	B0	I	Blue pulse input (LSB)	—
G12	Hsync/DENB	I	Hsync pulse input/Data enable signal input	—
G11	Vsync	I	Vsync pulse input	—
L12	MCK	I	Dot clock input	—
G10	PCI	I	Power control signal input	—
E10	SLIN	I	Sync input signal mode selector switch	—
F10	TESTO	O	Test output (Leave it open.)	—
E9	PCO	O	Power control signal output	—
M11	R31	O	Red signal output	—
L10	R21	O	Red signal output	—
M10	R11	O	Red signal output	—
M9	R01	O	Red signal output	—
L9	G31	O	Green signal output	—
M8	G21	O	Green signal output	—
L8	G11	O	Green signal output	—
K8	G01	O	Green signal output	—
J8	B31	O	Blue signal output	—

* UP: Pull-up (typ. 160kΩ)

Pin No.	Symbol	I/O	Description	Input pin for open status
M7	B21	O	Blue signal output	—
L7	B11	O	Blue signal output	—
K7	B01	O	Blue signal output	—
J7	XR31	O	R31 signal inversion output	—
M6	XR21	O	R21 signal inversion output	—
L6	XR11	O	R11 signal inversion output	—
K6	XR01	O	R01 signal inversion output	—
M5	XG31	O	G31 signal inversion output	—
L5	XG21	O	G21 signal inversion output	—
K5	XG11	O	G11 signal inversion output	—
J5	XG01	O	G01 signal inversion output	—
M4	XB31	O	B31 signal inversion output	—
L4	XB21	O	B21 signal inversion output	—
M3	XB11	O	B11 signal inversion output	—
L3	XB01	O	B01 signal inversion output	—
M12	TESTP	I	Test input (Connect to GND.)	—
A12	TEST	I	Test input (Connect to GND.)	DWN*
M2	VST	O	VST pulse output	—
L1	XVST	O	VST pulse inversion output	—
K4	ENB	O	ENB pulse output	—
K3	XENB	O	ENB pulse inversion output	—
J4	VCK	O	VCK pulse output	—
J3	XVCK	O	VCK pulse inversion output	—
K2	HCK1	O	HCK1 pulse output	—
K1	XHCK1	O	HCK1 pulse inversion output	—
J2	HCK2	O	HCK2 pulse output	—
J1	XHCK2	O	HCK2 pulse inversion output	—
H4	HST1	O	HST1 pulse output	—
H3	XHST1	O	HST1 pulse inversion output	—
H2	HST2	O	HST2 pulse output	—
H1	XHST2	O	HST2 pulse inversion output	—
G4	OE1	O	OE1 pulse output	—
G3	XOE1	O	OE1 pulse inversion output	—
G2	OE2	O	OE2 pulse output	—
G1	XOE2	O	OE2 pulse inversion output	—
D8	XB32	O	B32 signal inversion output	—
A7	XB22	O	B22 signal inversion output	—

* DWN: Pull-down (typ. 180k Ω)

Pin No.	Symbol	I/O	Description	Input pin for open status
B7	XB12	O	B12 signal inversion output	—
C7	XB02	O	B02 signal inversion output	—
D9	XG32	O	G32 signal inversion output	—
A8	XG22	O	G22 signal inversion output	—
B8	XG12	O	G12 signal inversion output	—
C8	XG02	O	G02 signal inversion output	—
D10	XR32	O	R32 signal inversion output	—
A9	XR22	O	R22 signal inversion output	—
B9	XR12	O	R12 signal inversion output	—
C9	XR02	O	R02 signal inversion output	—
C11	B32	O	Blue signal output	—
D11	B22	O	Blue signal output	—
A10	B12	O	Blue signal output	—
B10	B02	O	Blue signal output	—
B12	G32	O	Green signal output	—
C12	G22	O	Green signal output	—
D12	G12	O	Green signal output	—
A11	G02	O	Green signal output	—
F12	R32	O	Red signal output	—
F11	R22	O	Red signal output	—
E12	R12	O	Red signal output	—
E11	R02	O	Red signal output	—
B4	V _{SS2}	—	GND (Analog)	—
D3	V _{SS2}	—	GND (Analog)	—
F4	V _{SS2}	—	GND (Analog)	—
B2	V _{DD2}	—	Power supply (5.0V)	—
D2	V _{DD2}	—	Power supply (5.0V)	—
D7	V _{DD2}	—	Power supply (5.0V)	—
A4	TESTL1	O	Test output (Leave it open.)	—
C5	TESTL2	O	Test output (Leave it open.)	—
D6	TESTL3	I	Test input (Connect to GND.)	DWN*
B6	TESTL4	I	Test input (Connect to GND.)	—
A6	TESTL5	O	Test output (Leave it open.)	—
A5	TESTL6	I	Test input (Connect to GND.)	—
C6	TESTL7	I	Test input (Connect to GND.)	—
B5	TESTL8	I	Test input (Connect to GND.)	—
F3	V0	O	V0 output	—

* DWN: Pull-down (typ. 180kΩ)

Pin No.	Symbol	I/O	Description	Input pin for open status
E2	V1	O	V1 output	—
E4	V2	O	V2 output	—
D1	V3	O	V3 output	—
C1	V4	O	V4 output	—
D4	V5	O	V5 output	—
C3	V6	O	V6 output	—
B3	V7	O	V7 output	—
D5	V8	O	V8 output	—
A3	VCOM	O	VCOM output	—
A1	VRFSTB	I	Reference voltage driver on/off selector switch	DWN*
F2	VH1	I	VH1 input	—
F1	VL1	I	VL1 input	—
E1	VH2	I	VH2 input	—
E3	VL2	I	VL2 input	—
C2	VH6	I	VH6 input	—
B1	VL6	I	VL6 input	—
A2	VH8	I	VH8 input	—
C4	VL8	I	VL8 input	—

* DWN: Pull-down (typ. 180k Ω)

Electrical Characteristics (Serial/parallel conversion block, timing generator block)

DC Characteristics

(V_{DD1} = 3.0 to 3.6V, Ta = -25 to +75°C)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD1}	V _{DD1}	—	3.0	3.3	3.6	V
Current consumption	I _{DD1}	V _{DD1}	No load, Ta = 25°C V _{DD1} = 3.3V, MCK: 5.62MHz	—	1.5	—	mA
Input voltage 1	V _{IH1}	MCK, VRFSTB, TESTL1, TESTL2, TESTL3, TESTL4	CMOS input cell	0.7V _{DD1}	—	—	V
	V _{IL1}			—	—	0.2V _{DD1}	
Input voltage 2	V _{t+}	All input pins excluding MCK, VRFSTB, TESTL1, TESTL2, TESTL3, TESTL4	CMOS Schmitt trigger input cell	—	—	0.75V _{DD1}	V
	V _{t-}			0.15V _{DD1}	—	—	
Input current 1	I _{IL1}	R0, R1, R2, R3, G0, G1, G2, G3, B0, B1, B2, B3, Hsync/DENB, Vsync, MCK, PCI	V _I = 0V	—	—	1.0	μA
	I _{IH1}		V _I = V _{DD}	—	—	1.0	
Input current 2	I _{IL2}	CLR	V _I = 0V	10	—	100	μA
	I _{IH2}		V _I = V _{DD}	—	—	3.0	
Input current 3	I _{IL3}	TEST, TESTP, SLIN	V _I = 0V	—	—	3.0	μA
	I _{IH3}		V _I = V _{DD}	10	—	100	
Output voltage 1	V _{OL1}	R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32, VST, XVST, ENB, XENB, OE1, XOE1, OE2, XOE2, TESTO	I _{OL1} = 4.0mA	—	—	0.2	V
	V _{OH1}		I _{OH1} = -4.0mA	V _{DD} - 0.8	—	—	
Output voltage 2	V _{OL2}	HST1, XHST1, HST2, XHST2, VCK, XVCK, PCO	I _{OL2} = 6.0mA	—	—	0.2	V
	V _{OH2}		I _{OH2} = -6.0mA	V _{DD} - 0.8	—	—	
Output voltage 3	V _{OL3}	HCK1, XHCK1, HCK2, XHCK2	I _{OL3} = 10.0mA	—	—	0.4	V
	V _{OH3}		I _{OH3} = -10.0mA	V _{DD} - 0.8	—	—	

AC Characteristics

(V_{DD} = 3.0 to 3.6V, T_a = –25 to +75°C)

Item	Symbol	Applicable pins	Conditions*1	Min.	Typ.	Max.	Unit
HCK/HST time difference	$\Delta t_{\text{HST-HCKU}}$ $\Delta t_{\text{HST-HCKD}}$	HCK1, HCK2, XHCK1, XHCK2, HST1, HST2, XHST1, XHST2	—	—	—	15*2	ns
Data output rise time	t_{RD}	R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32	GND – V _{DD} (0 – 90%)	—	—	35	ns
Data output fall time	t_{FD}		V _{DD} – GND (100 – 10%)	—	—	35	
Horizontal pulse output rise time	t_{RHP}	HCK1, HCK2, XHCK1, XHCK2, HST1, HST2, XHST1, XHST2	GND – V _{DD} (0 – 90%)	—	—	35	ns
Horizontal pulse output fall time	t_{FHP}		V _{DD} – GND (100 – 10%)	—	—	35	
Vertical pulse output rise time	t_{RVP}	VCK, XVCK, VST, XVST, ENB, XENB, OE1, OE2, XOE1, XOE2, PCO, TESTO	GND – V _{DD} (0 – 90%)	—	—	50	ns
Vertical pulse output fall time	t_{FVP}		V _{DD} – GND (100 – 10%)	—	—	50	
HCK1, HCK2, XHCK1, XHCK2/ DATA setup time	t_{STP}	HCK1, HCK2, XHCK1, XHCK2, R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32	*3	35	55	100	ns
HCK, VCK duty	dHCK dVCK	HCK1, HCK2, XHCK1, XHCK2, VCK, XVCK	*4	48	50	52	%

*1 Load capacitance CL of each output pin is shown below.

- R01, R11, R21, R31, R02, R12, R22, R32, XR01, XR11, XR21, XR31, XR02, XR12, XR22, XR32, G01, G11, G21, G31, G02, G12, G22, G32, XG01, XG11, XG21, XG31, XG02, XG12, XG22, XG32, B01, B11, B21, B31, B02, B12, B22, B32, XB01, XB11, XB21, XB31, XB02, XB12, XB22, XB32, OE1, XOE1, OE2, XOE2, TESTO, ENB, XENB : CL = 70pF
- HCK1, HCK2, XHCK1, XHCK2 : CL = 180pF
- VCK, XVCK : CL = 150pF
- HST1, HST2, XHST1, XHST2, VST, XVST, PCO : CL = 100pF

*2 Absolute value of the time difference of the change point at HST1, XHST1, HCK1 and XHCK1 (50%) is within 15ns.

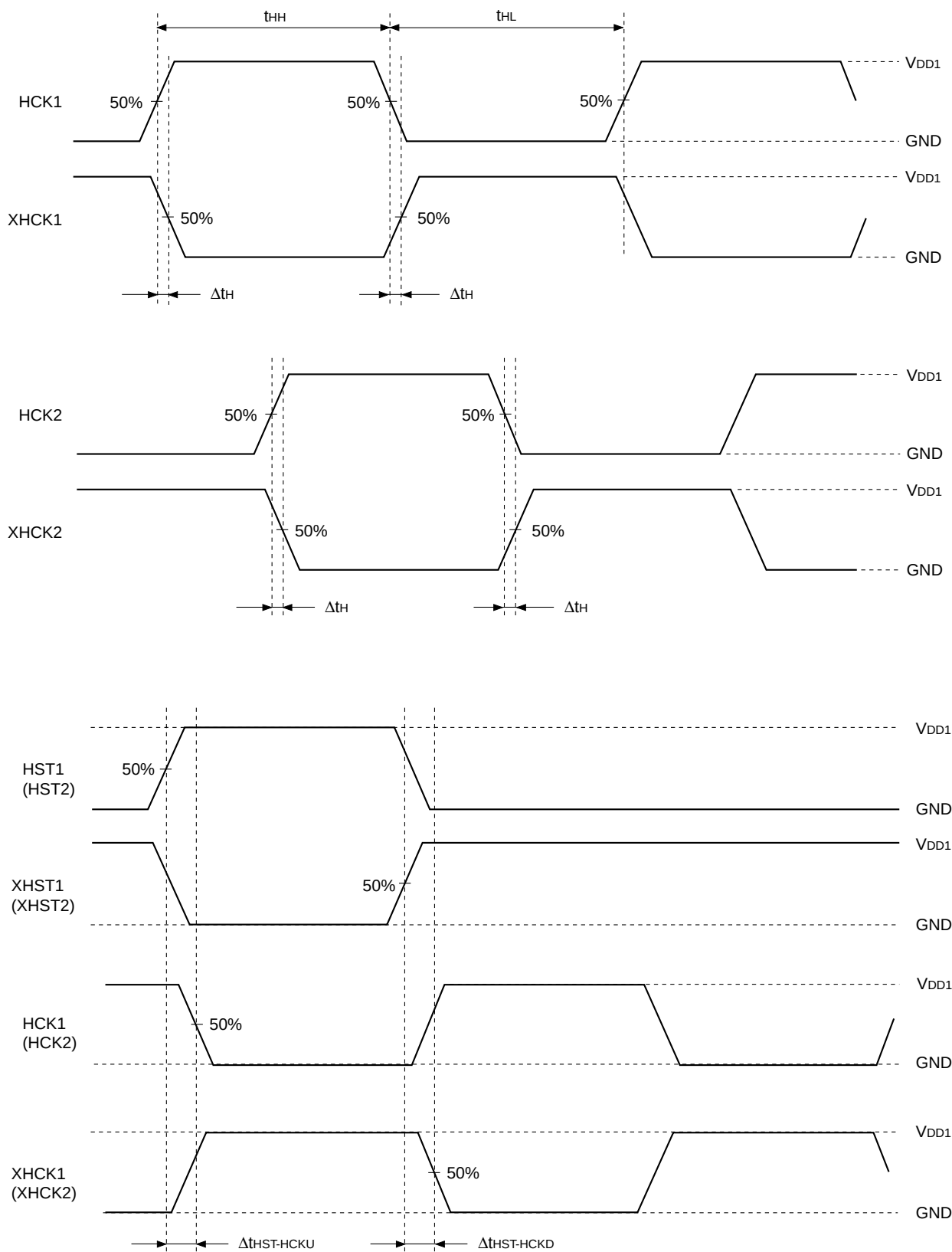
Similarly, absolute value of the time difference of the change point at HST2, XHST2, HCK2 and XHCK2 (50%) is within 15ns.

*3 t_{STP} : t_{ST1D} , t_{ST1U} , t_{ST2D} , t_{ST2U}

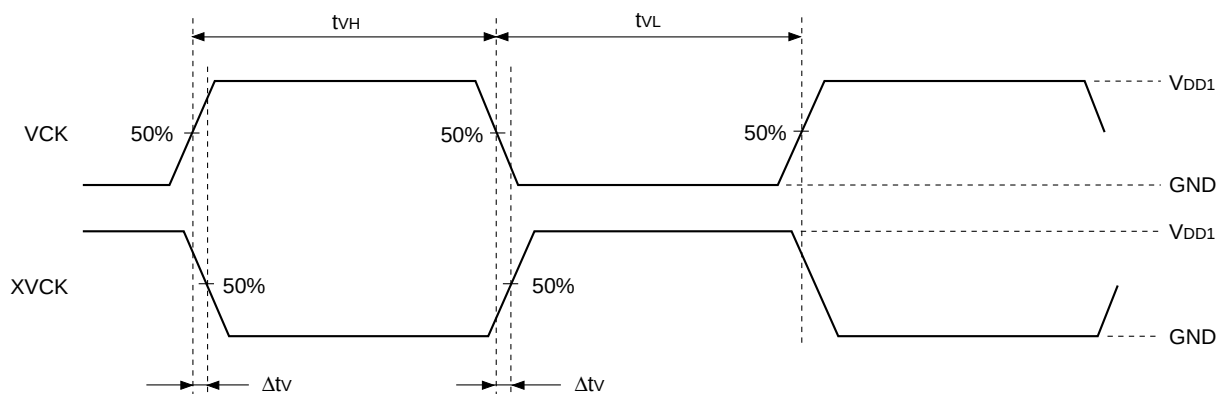
*4 $d\text{HCK} = (t_{\text{HH}}/(t_{\text{HH}} + t_{\text{HL}})) \times 100$, $d\text{VCK} = (t_{\text{VH}}/(t_{\text{VH}} + t_{\text{VL}})) \times 100$

Timing Definition

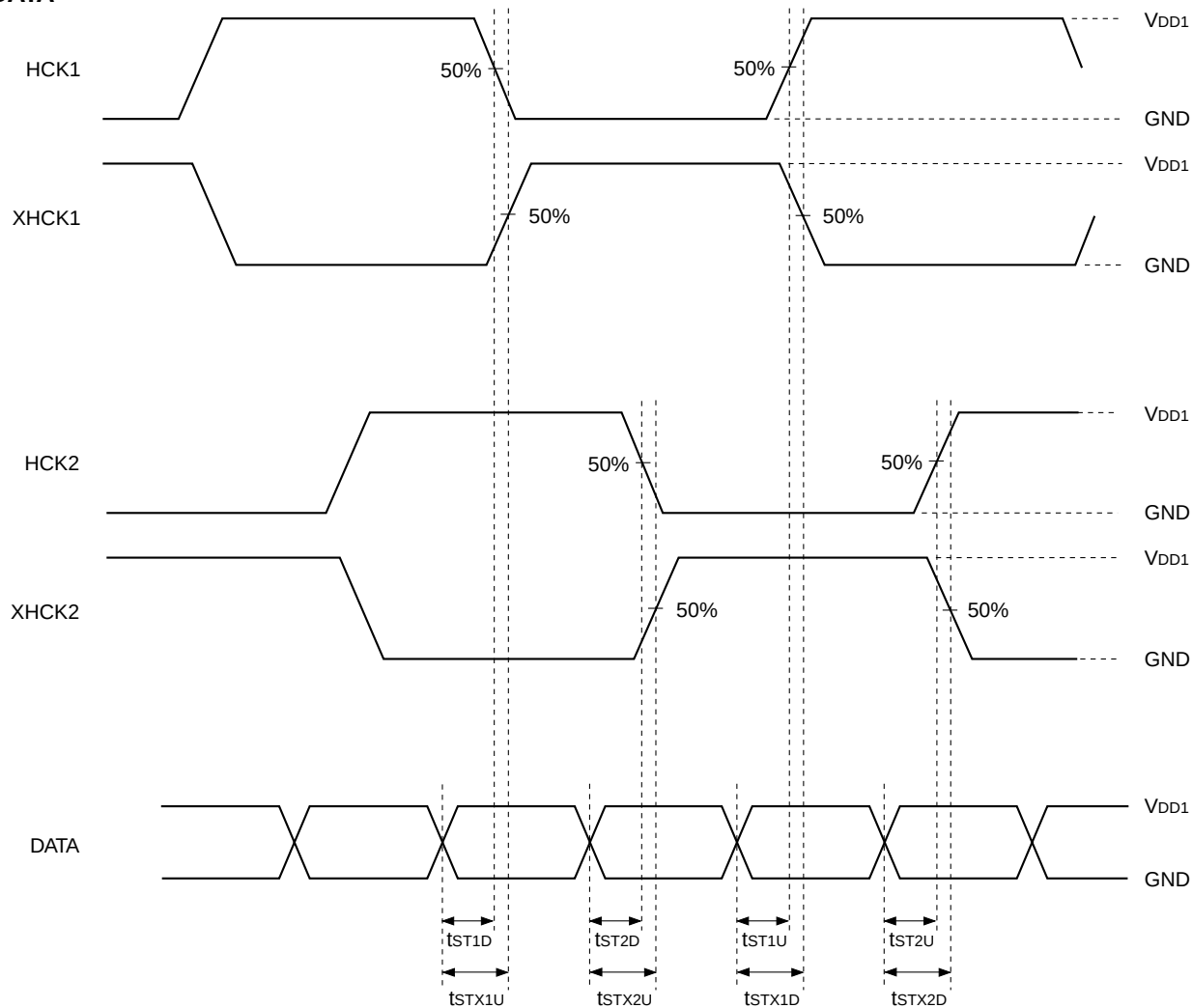
Horizontal System



Vertical System



DATA



PCI, PCO

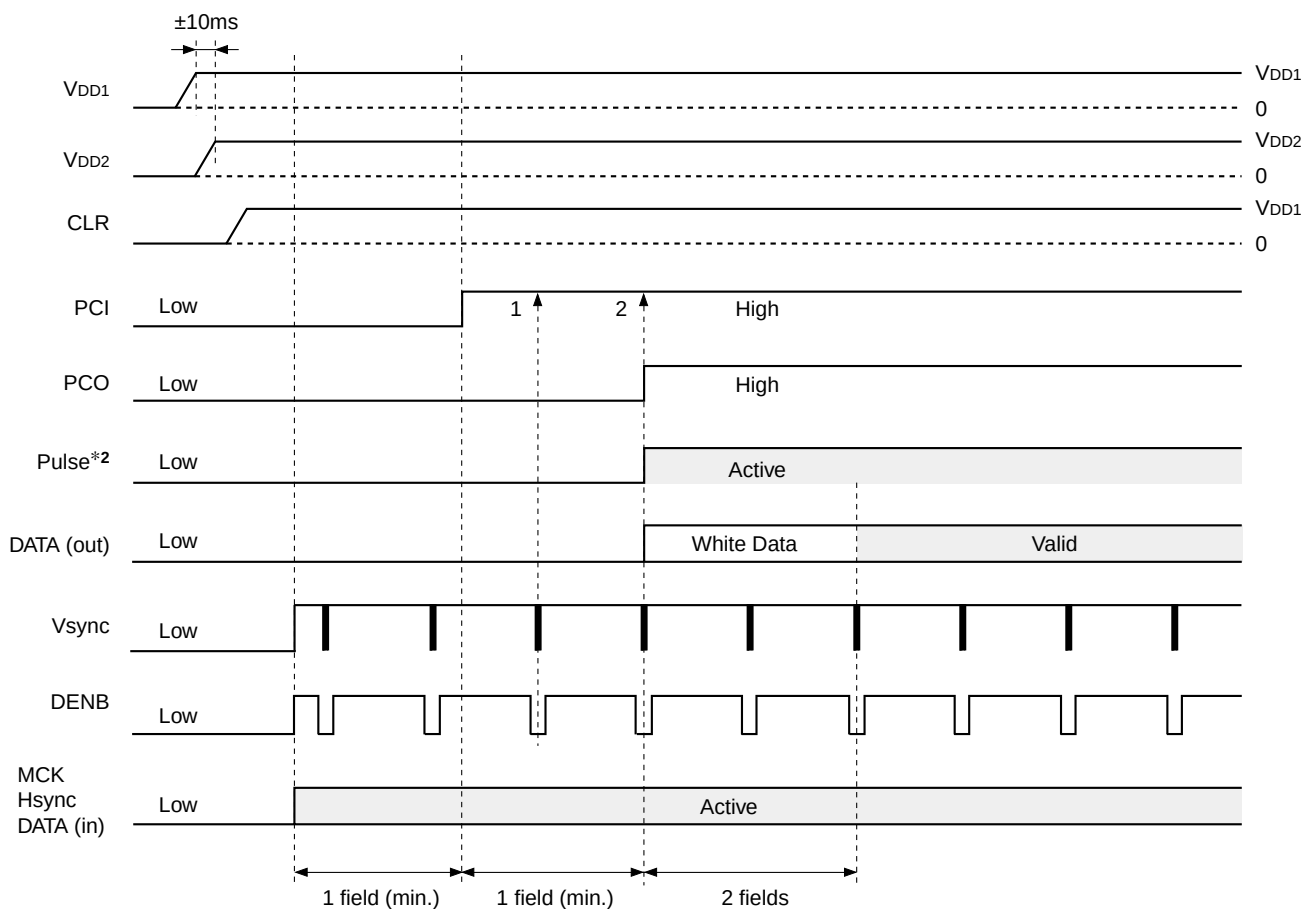
These pins control to turn power on/off of the ACX704AKM/BKM when the LCD is turned on/off. Connect PCO to DC-DC converter that can control power on/off of the ACX704AKM/BKM.

Power-on Sequence

- Raise and fall V_{DD1} and V_{DD2} simultaneously (within 10ms)
- Input the input signal*1 for 1 field (Min.), and then raise PCI.
- After PCI becomes high, latch is performed twice at Vsync. When both of them are high, PCO output is changed from low to high.

(Turn the power on of the ACX704AKM/BKM at this timing.)

Also, effective screen is displayed after two fields of entire white display from this timing.

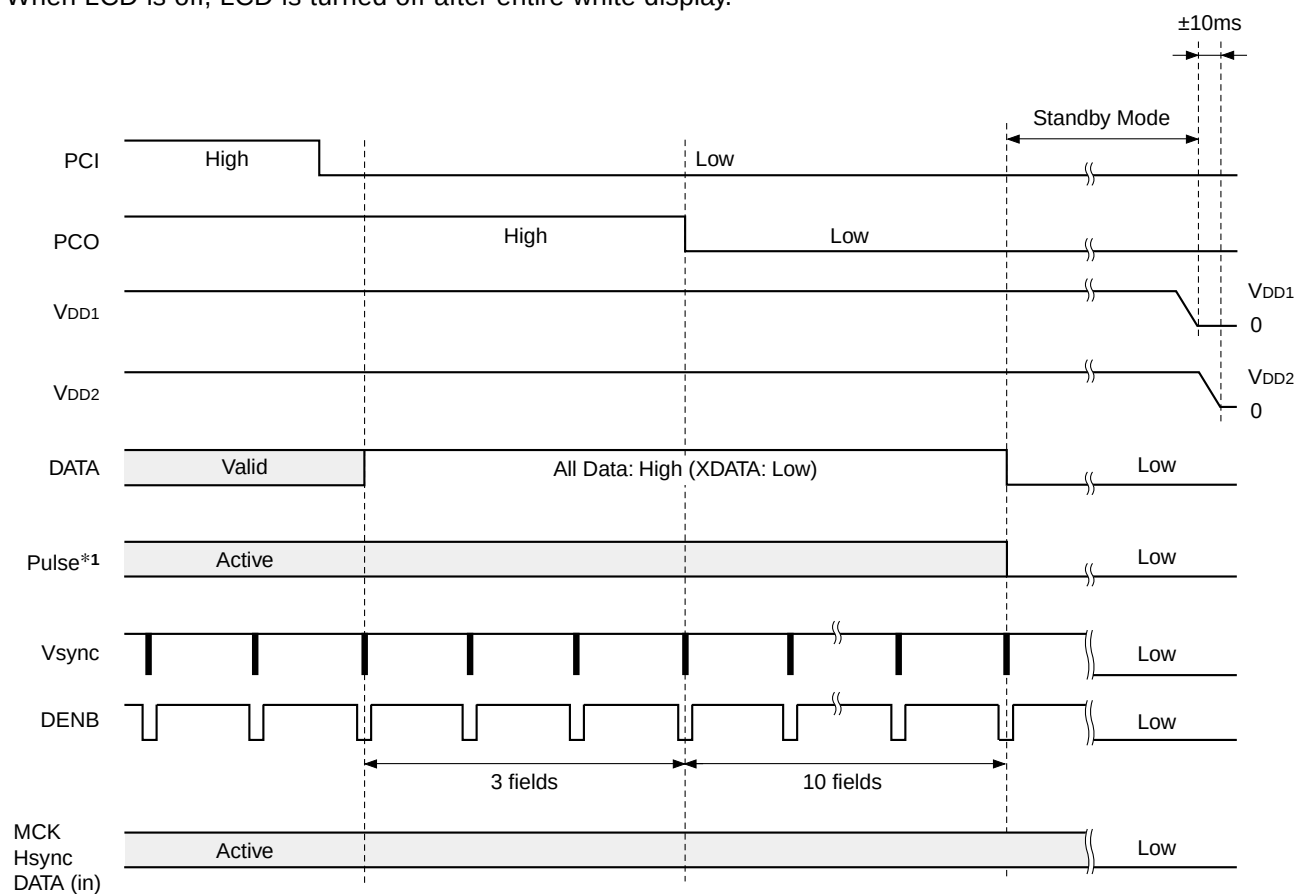


*1 Hsync, Vsync, DENB, MCK, DATA

*2 HST1, XHST1, HST2, XHST2, HCK1, XHCK1, HCK2, XHCK2, VST, XVST, VCK, XVCK, ENB, XENB, OE1, XOE1, OE2, XOE2, TESTO, (FRP)

Power-off Sequence (Standby)

- When LCD is off, LCD is turned off after entire white display.



*1 HST1, XHST1, HST2, XHST2, HCK1, XHCK1, HCK2, XHCK2, VST, XVST, VCK, XVCK, ENB, XENB, OE1, XOE1, OE2, XOE2, TESTO, (FRP)

SLIN

This is a selector switch for sync input signal mode.

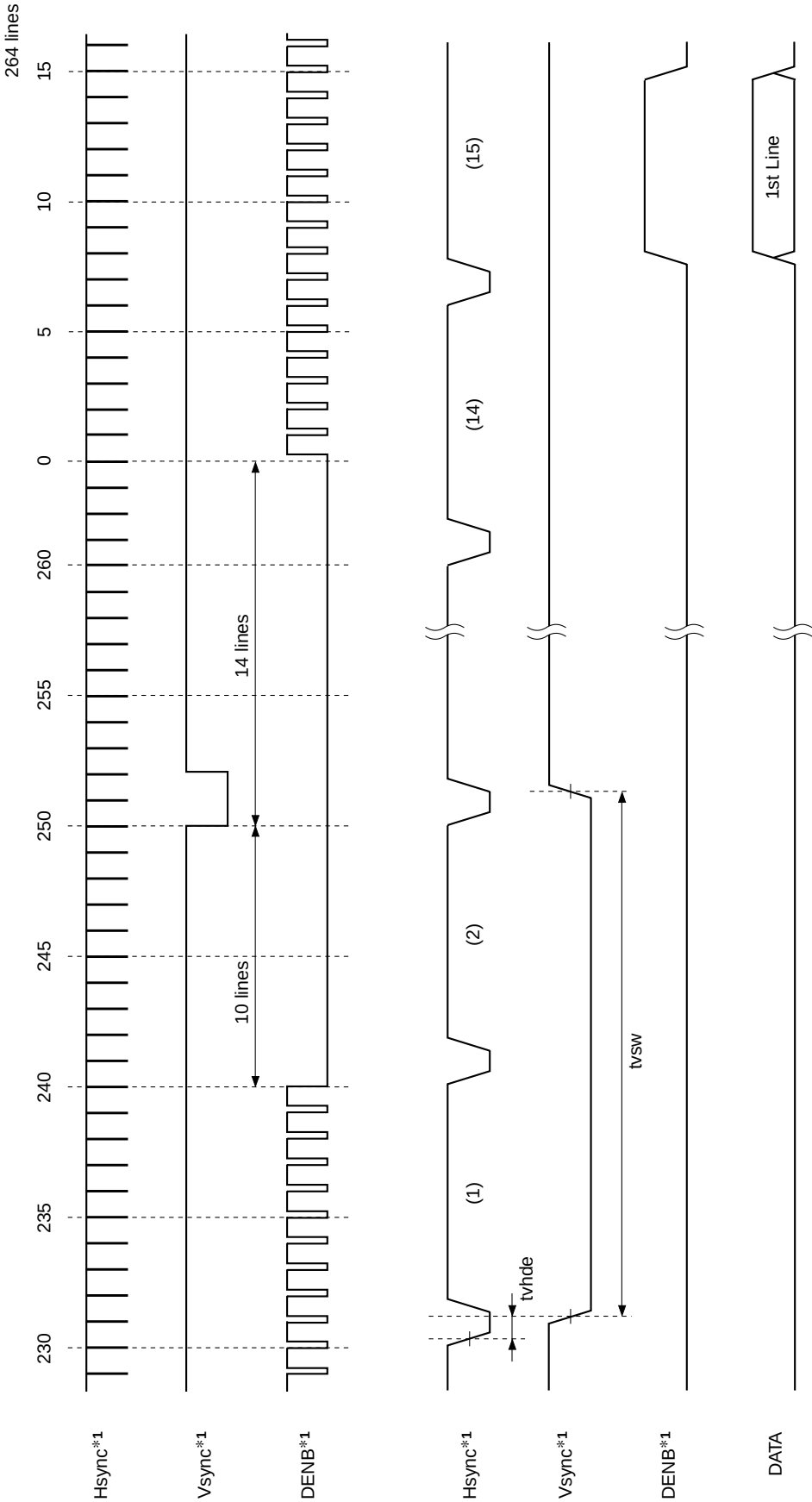
SLIN: Low → Hsync + Vsync Mode.

SLIN: High → DENB ONLY Mode. (Vsync is invalid.)

Input Signal AC Characteristics ($V_{DD1} = 3.0$ to $3.6V$, $T_a = -25$ to $+75^{\circ}C$)

Item	Symbol	Min.	Typ.	Max.
MCK frequency	f _{tch}	3MHz	5.58MHz	8MHz
MCK low, high pulse width	t _{ch} , t _{cl}	—	0.5t _{clk}	—
DATA setup time	t _{ds}	10ns	—	—
DATA hold time	t _{dh}	15ns	—	—
DENB setup time	t _{des}	10ns	—	—
DENB hold time	t _{deh}	15ns	—	—
Hsync setup time	t _{hss}	10ns	—	—
Hsync low pulse width	t _{hsw}	4t _{clk}	—	16t _{clk}

Vertical Direction Input Signal Timing Chart

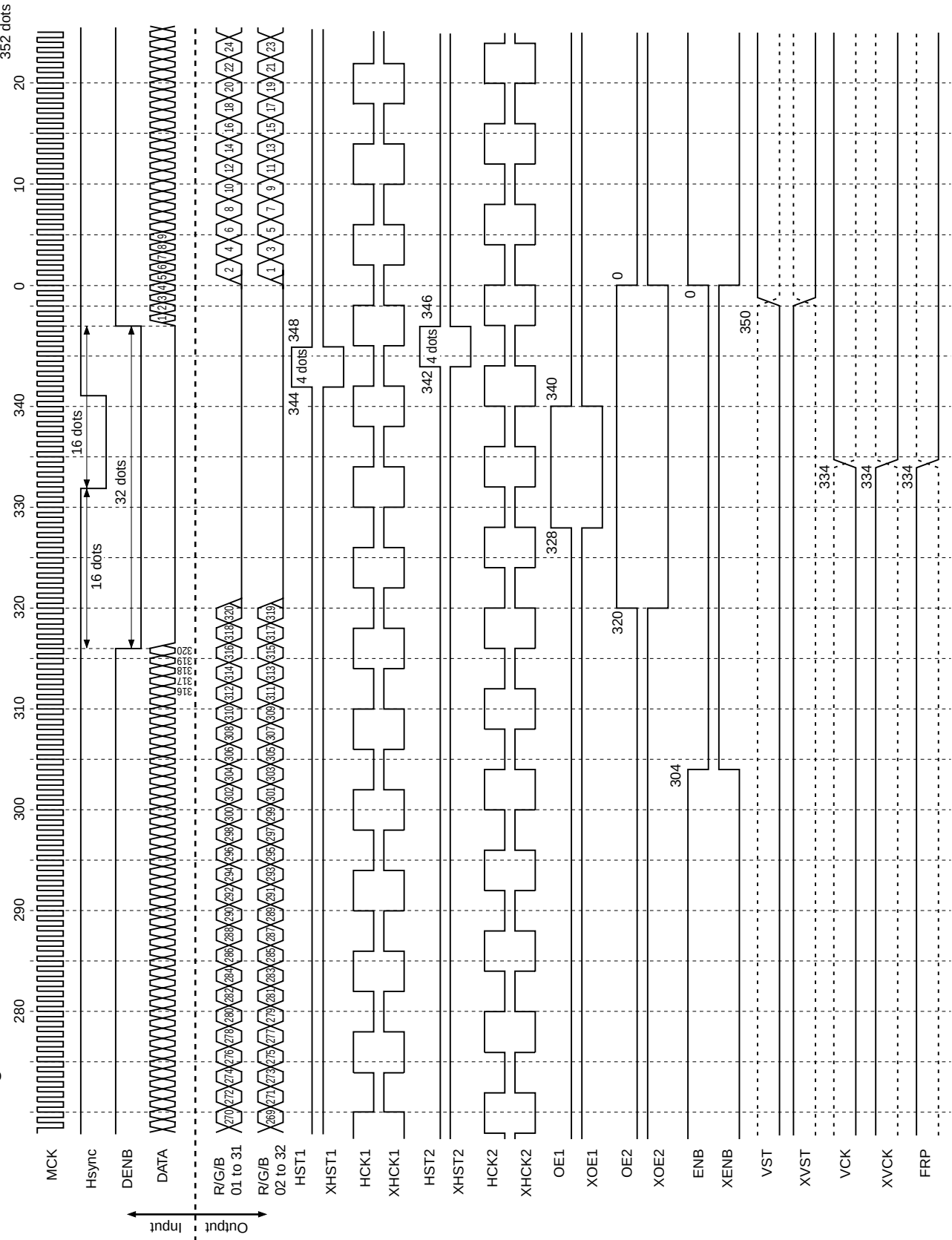


*1 Input either Hsync + Vsync or DENB as sync input signal.

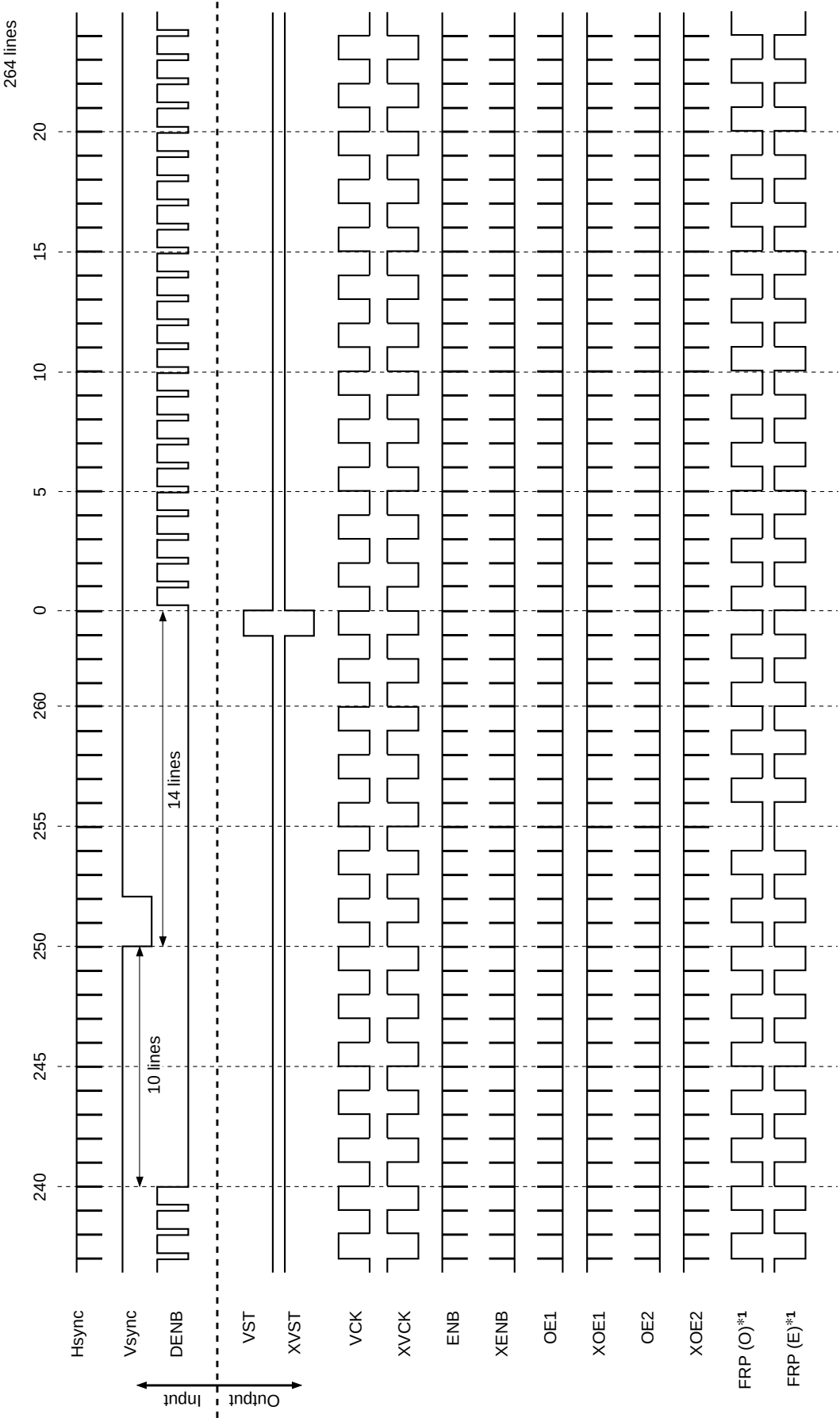
Input Signal AC Characteristics (V_{DD1} = 3.0 to 3.6V, T_a = -25 to +75°C)

Item	Symbol	Min.	Typ.	Max.
Hsync falling edge → Vsync falling edge	tvhde	3tclk	—	352tclk
Vsync low pulse width	tvsw	2 lines	—	14 lines

Horizontal Direction Timing Chart



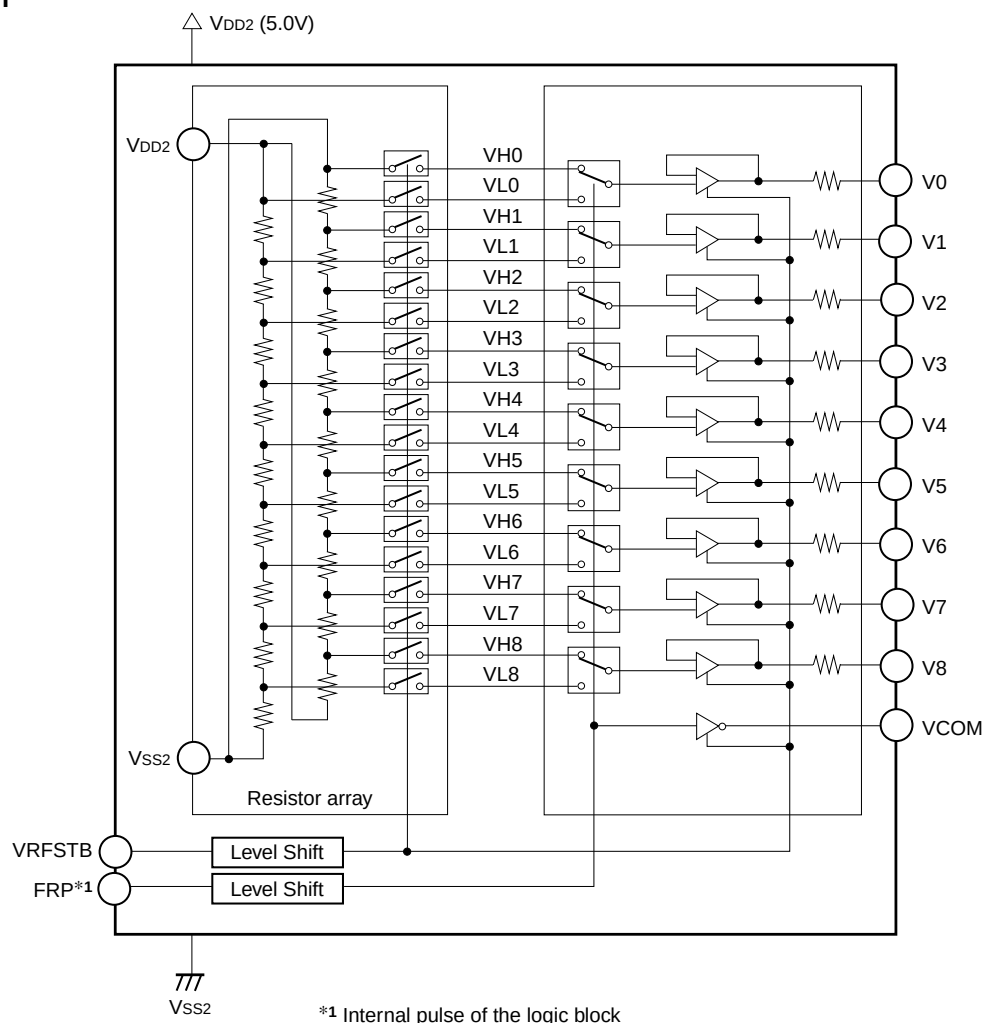
Vertical Direction Timing Chart



*1 FRP (O): FRP pulse at odd field. FRP (E): FRP pulse at even field.

Reference Voltage Driver Block

Block Diagram



Electrical Characteristics (Reference voltage driver block)

Resistor array output voltage

(V_{DD1} = 3.3V, V_{DD2} = 5.0V, T_a = 25°C)

Item	Min.	Typ.	Max.	Unit	Item	Min.	Typ.	Max.	Unit
VH0	—	4.800	—	V	VL0	—	0.200	—	V
VH1	—	3.900	—		VL1	—	1.100	—	
VH2	—	3.325	—		VL2	—	1.675	—	
VH3	—	2.950	—		VL3	—	2.050	—	
VH4	—	2.600	—		VL4	—	2.400	—	
VH5	—	2.250	—		VL5	—	2.750	—	
VH6	—	1.950	—		VL6	—	3.050	—	
VH7	—	1.500	—		VL7	—	3.500	—	
VH8	—	0.500	—		VL8	—	4.500	—	

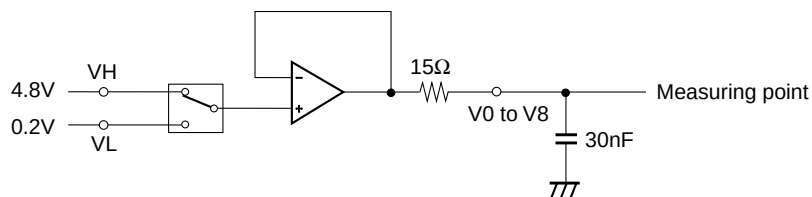
AC, DC Characteristics

(V_{DD1} = 3.3V, V_{DD2} = 5.0V, T_a = –25 to +75°C)

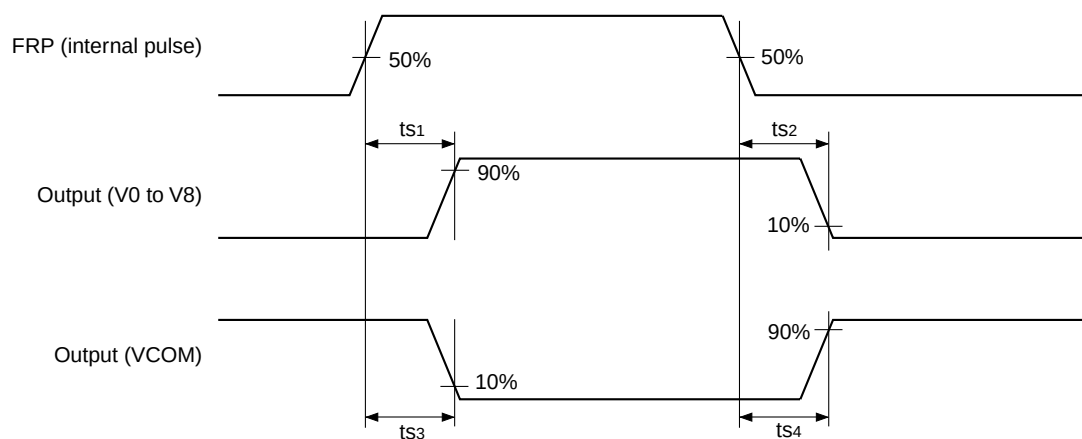
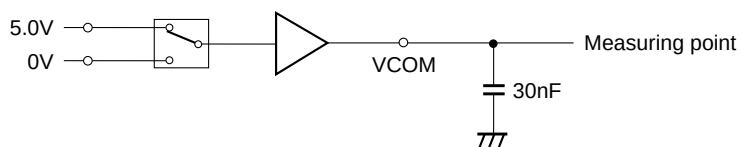
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD2}	—	4.7	5.0	5.3	V
Current consumption	I _{DD2}	Input voltage = 2.5V, During no load	—	3.4	6.0	mA
V _H , V _L input current high	I _{IH}	Input voltage = 4.8V	–0.15	—	0.15	μA
V _H , V _L input current low	I _{IL}	Input voltage = 0.2V	–0.15	—	0.15	μA
Voltage gain	A _V	Input voltage = 0.2 to 4.8V	0.985	—	—	V/V
Output voltage high	V _{OH}	I _{SOURCE} = 10mA	V _{DD2} – 1.0	—	—	V
Output voltage low	V _{OL}	I _{SINK} = 10mA	—	—	GND + 1.0	V
COM output voltage high	V _{COH}	I _{SOURCE} = 10mA	V _{DD2} – 0.1	—	—	V
COM output voltage low	V _{COL}	I _{SINK} = 10mA	—	—	GND + 0.1	V
Offset voltage	V _{OFF}	R _s = 10kΩ	—	—	20	mV
Load regulation	ΔV _O	Input voltage = 0.2 to 4.8V I _{SOURCE} = 10mA I _{SINK} = 10mA	—	±5	±10	mV
Output impedance	R _{IMP}	V _O to V ₈	—	15	—	Ω
Settling time 1	t _{s1}	Measurement circuit 1	—	—	10	μs
Settling time 2	t _{s2}	Measurement circuit 1	—	—	10	μs
Settling time 3	t _{s3}	Measurement circuit 2	—	—	6	μs
Settling time 4	t _{s4}	Measurement circuit 2	—	—	6	μs

Measurement Circuit

Measurement circuit 1



Measurement circuit 2



VRFSTB

This is a selector switch for reference voltage driver output on/off.

VRFSTB: Low → V0 to V8 and VCOM are GND level.

VRFSTB: High → V0 to V8 and VCOM are active.

The diagram illustrates the pin configuration and connections for the ACX704AKM/BKM chip. The chip has three main groups of pins: A1 through K2 on the left, A12 through L11 on the right, and M1 through M12 at the bottom. The connections are as follows:

- Left Side (A1-K2):**
 - A1: VRFSTB
 - B1: VL7
 - B2: VDD2
 - C1: V4
 - C2: VH7
 - C3: V6
 - D1: V3
 - D2: VDD2
 - D3: VSS2
 - D4: V5
 - E1: VH2
 - E2: V1
 - E3: VL2
 - E4: V2
 - F1: VL0
 - F2: VH0
 - F3: V0
 - F4: VSS2
 - G1: XOE2
 - G2: OE2
 - G3: XOE1
 - G4: OE1
 - H1: XHST2
 - H2: HST2
 - H3: XHST1
 - H4: HST1
 - J1: XHCK2
 - J2: HCK2
 - J3: XVCK
 - J4: VCK
 - K1: XHCK1
 - K2: HCK1
- Right Side (A12-L11):**
 - A12: TEST
 - B11: VSS1
 - A11: G02
 - D12: G12
 - C12: G22
 - B12: G32
 - E11: R02
 - E12: R12
 - F11: R22
 - F12: R32
 - E9: PCO
 - E10: SLIN
 - F9: CLR
 - F10: TESTO
 - G9: VSS1
 - G10: PCI
 - G11: Vsync
 - G12: Hsync/DENB
 - H9: R0
 - H10: R1
 - H11: R2
 - H12: R3
 - J9: G0
 - J10: G1
 - J11: G2
 - J12: G3
 - K9: B0
 - K10: B1
 - K11: B2
 - K12: B3
 - L12: MCK
 - L11: VDD1
- Bottom Side (M1-M12):**
 - M1: VDD1
 - M2: VSS1
 - L2: VST
 - L1: XVST
 - K4: ENB
 - K3: XENB
 - L3: XB01
 - M3: XB11
 - L4: XB21
 - M4: XB31
 - J5: XG01
 - K5: XG11
 - L5: XG21
 - M5: XG31
 - K6: XR01
 - L6: XR11
 - M6: XR21
 - J7: XR31
 - K7: VDD1
 - L7: B11
 - M7: B21
 - K8: B31
 - L8: G01
 - M8: G11
 - J8: G21
 - K8: G31
 - L9: R01
 - M9: R11
 - J9: R21
 - K9: R31
 - L10: M11
 - M10: M12
 - J10: TESTIP

Power supply connections include VDD1, VDD2, VSS1, and VSS2. The diagram also shows connections to other ACX704AKM/BKM chips and a DC-DC converter.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Unit: mm

Technical drawing of a 12x12 grid of circular features on a rectangular plate. The drawing includes dimensions for overall size (11.0), hole diameter (0.08), hole spacing (1.1), and hole diameter tolerance (0.08 ± 0.05). It also shows a detail of a single hole with a diameter of 0.20 and a tolerance of 0.20. The drawing is labeled with 'S' for surface finish and 'A' for material.

SONY CODE	TFBGA-128P-061
EIAJ CODE	P-TFBGA128-11x11-0.8
JEDEC CODE	_____

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	—————
TERMINAL MATERIAL	SOLDER
PACKAGE MASS	0.22g