SONY

CXD3611R

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD3611R is a timing generator IC which generates the timing pulses for performing progressive scan readout using the ICX414/415/424 CCD image sensors.

Features

- Base oscillation frequency
  24.545451MHz (ICX414, 424)/
  29.500000MHz (ICX415)
  (When in double speed drive mode:
  49.090902/59.000000MHz)
- Electronic shutter function
- Trigger shutter function
- Supports central scanning mode (two types)/ double speed drive mode
- Horizontal driver for CCD image sensor (However, uses external driver for double speed drive mode.)
- Vertical driver for CCD image sensor

Applications

Monitoring/image analysis

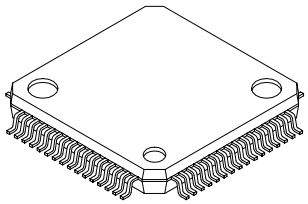
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

- ICX414 (Type 1/2, 330K pixels)
- ICX415 (Type 1/2, 460K pixels)
- ICX424 (Type 1/3, 330K pixels)

64 pin LQFP (Plastic)



Absolute Maximum Ratings

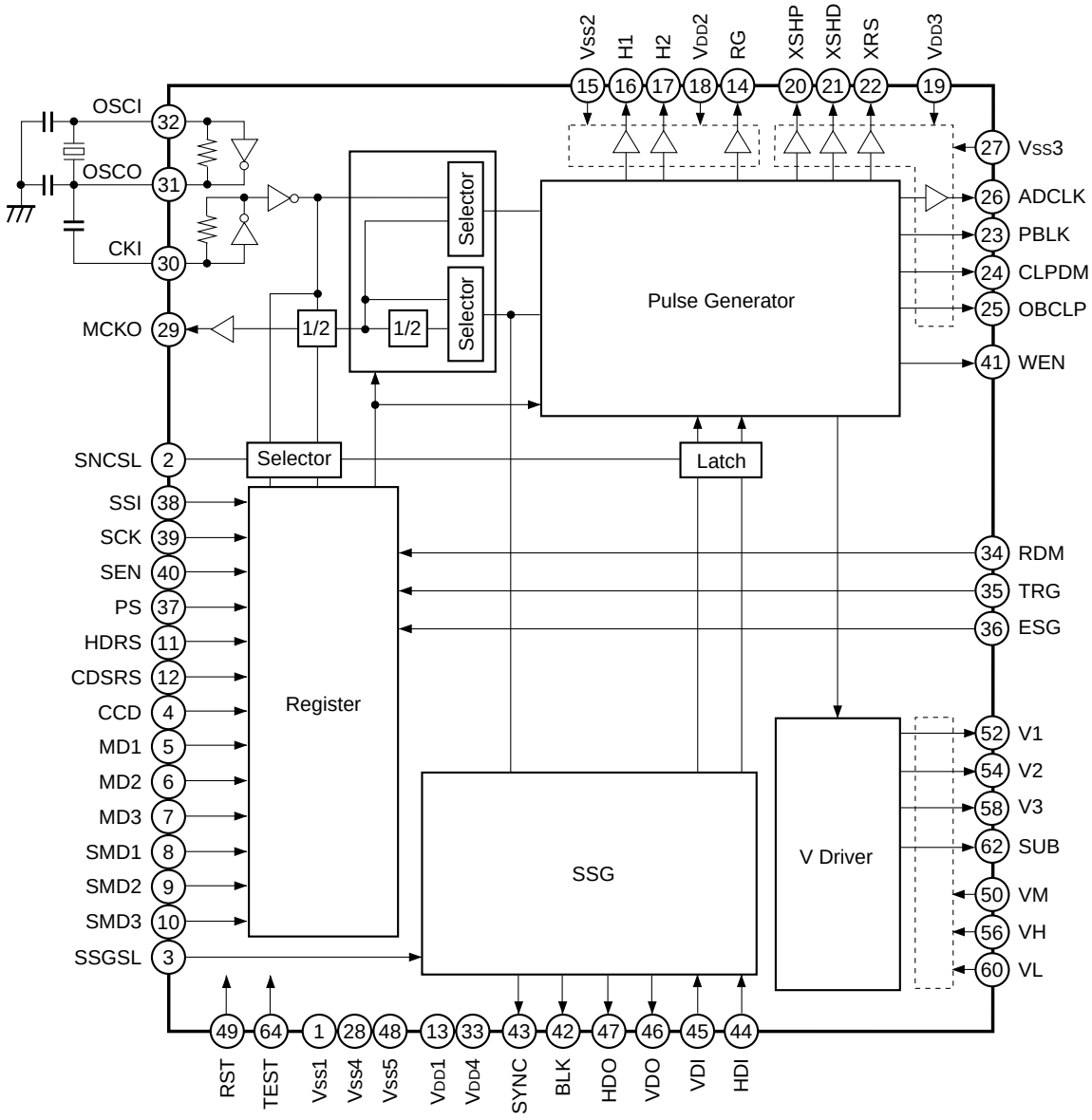
• Supply voltage	V_{DD}	Vss – 0.3 to +7.0	V
	VL	–10.0 to Vss	V
	VH	VL – 0.3 to +26.0	V
• Input voltage	V_I	Vss – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_{O1}	Vss – 0.3 to V_{DD} + 0.3	V
	V_{O2}	V_L – 0.3 to V_{SS} + 0.3	V
	V_{O3}	V_L – 0.3 to V_H + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}a, V_{DD}b	3.0 to 5.5	V
	V_{DD}c	3.0 to 3.6	V
	VM	0.0	V
	VH	14.5 to 15.5	V
	VL	–7.0 to –8.0	V
• Operating temperature			
	Topr	–20 to +75	°C

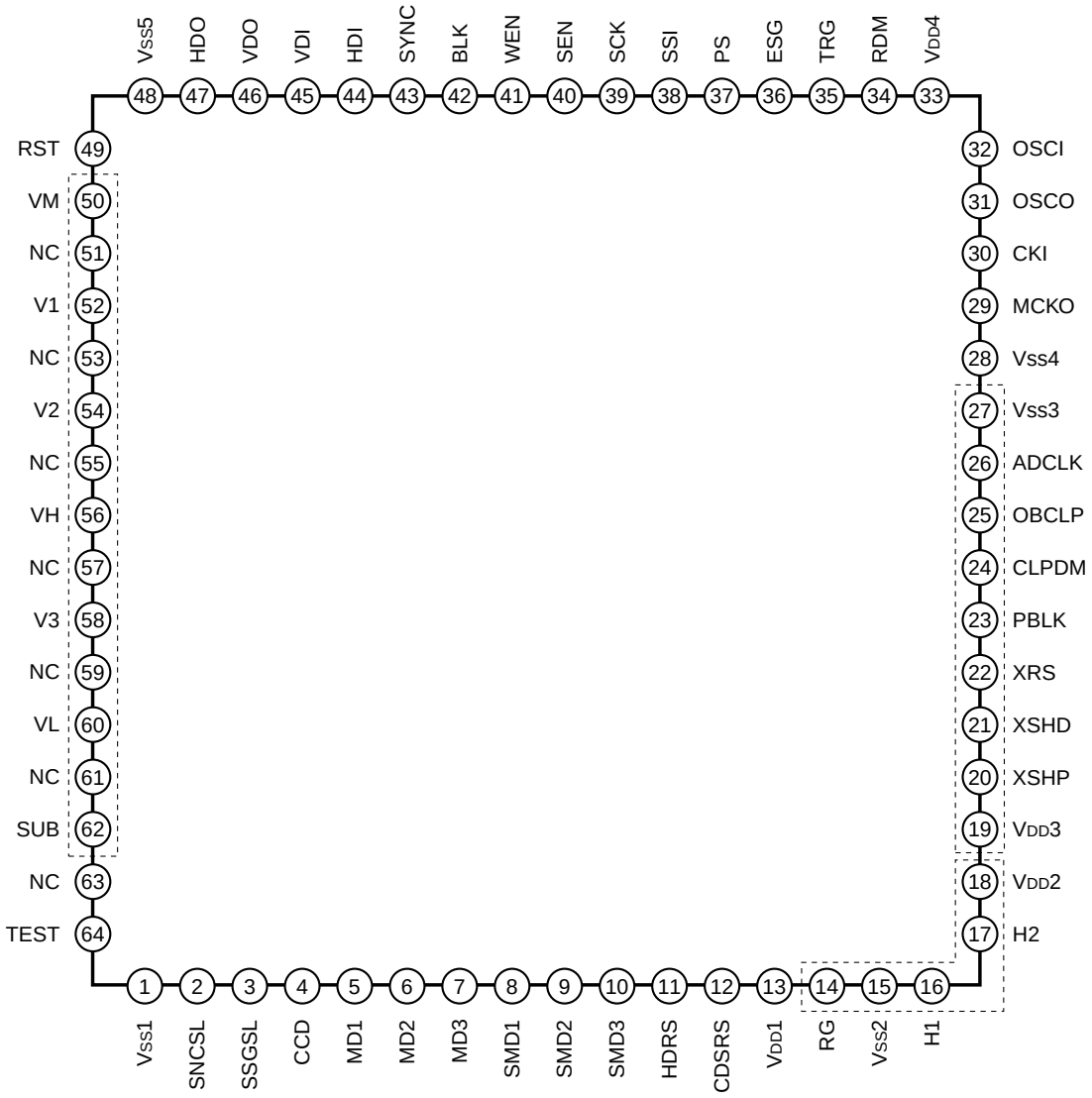
E02561-PS

Block Diagram



Notes) 1. CKI must always be input below amplitude V_{DD} with a sine wave.
2. The system block diagram above is an example using an oscillator.

Pin Configuration



* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{SS}1$	—	GND
2	SNCSL	I	Control input used to switch sync system High: CKI sync, Low: MCKO sync. With pull-down resistor
3	SSGSL	I	Pin used to switch external reset High: External sync has priority, Low: Internal sync has priority With pull-down resistor
4	CCD	I	Control input used to switch CCD High: ICX415, Low: ICX414/424 With pull-down resistor
5	MD1	I	Control input 1 used to switch drive mode See the section on parallel control With pull-down resistor
6	MD2	I	Control input 2 used to switch drive mode See the section on parallel control With pull-down resistor
7	MD3	I	Control input 3 used to switch drive mode See the section on parallel control With pull-down resistor
8	SMD1	I	Control input 1 used to switch exposure time See the section on parallel control With pull-down resistor
9	SMD2	I	Control input 2 used to switch exposure time See the section on parallel control With pull-down resistor
10	SMD3	I	Control input 3 used to switch exposure time See the section on parallel control With pull-down resistor
11	HDRS	I	Control input used to switch H system pulse polarity H1 and H2 are targeted (Default is positive polarity.) High: For external Dr, Low: For internal Dr With pull-down resistor
12	CDSRS	I	Control input used to switch CDS system pulse polarity XSHP, XSHD, XRS, OBCLP, CLPDM are targeted. High: Positive polarity, Low: Negative polarity With pull-down resistor
13	$V_{DD}1$	—	3.3V power supply. (Power supply for common logic block)
14	RG	O	CCD reset gate pulse output
15	$V_{SS}2$	—	GND
16	H1	O	CCD horizontal register clock output
17	H2	O	CCD horizontal register clock output
18	$V_{DD}2$	—	3.3V power supply. (Power supply for H1/H2/RG)
19	$V_{DD}3$	—	3.3V power supply. (Power supply for CDS)
20	XSHP	O	CCD precharge level sample-and-hold pulse output
21	XSHD	O	CCD data level sample-and-hold pulse output
22	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment
23	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning
24	CLPDM	O	CCD dummy signal clamp pulse output
25	OBCLP	O	CCD optical black signal clamp pulse output
26	ADCLK	O	Clock output for analog/digital conversion IC Logical phase can be adjusted using serial interface data.
27	$V_{SS}3$	—	GND

Pin No.	Symbol	I/O	Description
28	$V_{SS}4$	—	GND
29	MCKO	O	System clock output for signal processing IC
30	CKI	I	Inverter input
31	OSCO	O	Inverter output for oscillation; should be open or C grounded when not in use.
32	OSCI	I	Inverter input for oscillation; should be fixed to Low when not in use.
33	$V_{DD}4$	—	3.3V power supply. (Power supply for common logic block)
34	RDM	I	Trigger control, normally fixed to V_{DD}. See the section on trigger shutter function. With pull-up resistor
35	TRG	I	Trigger control, normally fixed to V_{DD}. See the section on trigger shutter function. With pull-up resistor
36	ESG	I	Readout pulse position control, normally fixed to V_{DD}. See the section on trigger shutter function. With pull-up resistor
37	PS	I	Control input used to switch serial and parallel High: Parallel, Low: Serial With pull-up resistor
38	SSI	I	Serial interface data input for internal mode settings. Schmitt trigger input
39	SCK	I	Serial interface clock input for internal mode settings. Schmitt trigger input
40	SEN	I	Serial interface strobe input for internal mode settings. Schmitt trigger input
41	WEN	O	Memory writing timing pulse output
42	BLK	O	Blank pulse output
43	SYNC	O	SYNC pulse output
44	HDI	I	Horizontal sync reset signal input With pull-up resistor
45	VDI	I	Vertical sync reset signal input With pull-up resistor
46	VDO	O	Vertical sync signal output
47	HDO	O	Horizontal sync signal output
48	$V_{SS}5$	—	GND
49	RST	I	Input pin for internal system reset Normally, apply reset during power-on. High: Normal operation, Low: Reset control Schmitt trigger input
50	VM	—	GND (Ground for vertical driver)
51	NC	—	No connection
52	VI	O	CCD vertical register clock output
53	NC	—	No connection
54	V2	O	CCD vertical register clock output
55	NC	—	No connection
56	VH	—	15.0V power supply. (Power supply for vertical driver)
57	NC	—	No connection
58	V3	O	CCD vertical register clock output
59	NC	—	No connection
60	VL	—	–7.5V power supply. (Power supply for vertical driver)

Pin No.	Symbol	I/O	Description
61	NC	—	No connection
62	SUB	O	CCD electronic shutter pulse output
63	NC	—	No connection
64	TEST	I	Pin for IC test, normally fixed GND. With pull-down resistor

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{DD}3$	$V_{DD}a$		3.0	3.3	5.5	V
Supply voltage 2	$V_{DD}2$	$V_{DD}b$		3.0	3.3	5.5	V
Supply voltage 3	$V_{DD}1$, $V_{DD}4$	$V_{DD}c$		3.0	3.3	3.6	V
Input voltage 1*1	RST, SSI, SCK, SEN	V_{t+}		0.8$V_{DD}c$			V
		V_{t-}				0.2$V_{DD}c$	V
Input voltage 2*2	SNCSL, SSGSL, TEST, CCD, MD1 to 3, SMD1 to 3, HDRS, CDSRS	V_{IH1}		0.7$V_{DD}c$			V
		V_{IL1}				0.3$V_{DD}c$	V
Input voltage 3*3	RDM, TRG, ESG, PS, VDI, HDI	V_{IH2}		0.7$V_{DD}c$			V
		V_{IL2}				0.3$V_{DD}c$	V
Output voltage 1	H1, H2	V_{OH2}	Feed current where I_{OH} = –14.0mA	$V_{DD}b$ – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 9.6mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	$V_{DD}b$ – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, PBLK, XRS, OBCLP, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	$V_{DD}a$ – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	MCKO	V_{OH5}	Feed current where I_{OH} = –3.3mA	$V_{DD}c$ – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 5	WEN, BLK, SYNC, VDO, HDO	V_{OH6}	Feed current where I_{OH} = –2.4mA	$V_{DD}c$ – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output current 1	V1, V2, V3	I_{OL}	V1, V2, V3 = –8.25V	10.0			mA
		I_{OM1}	V1, V2, V3 = –0.25V			–5.0	mA
		I_{OM2}	V2, V3 = 0.25V	5.0			mA
		I_{OH}	V2, V3 = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 These input pins are Schmitt trigger inputs.

*2 These input pins are with a pull-down resistor in the IC.

*3 These input pins are with a pull-up resistor in the IC.

Note) The table above indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DD}c/2$		V
Input voltage	OSCI	V_{IH}		$0.7V_{DD}c$			V
		V_{IL}				$0.3V_{DD}c$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –3.6mA	$V_{DD}c$ – 0.8			V
		V_{OL}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	$V_{IN} = V_{DD}c$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DD}c/2$		V
Input voltage		V_{IH}		$0.7V_{DD}c$			V
		V_{IL}				$0.3V_{DD}c$	V
Input amplitude		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

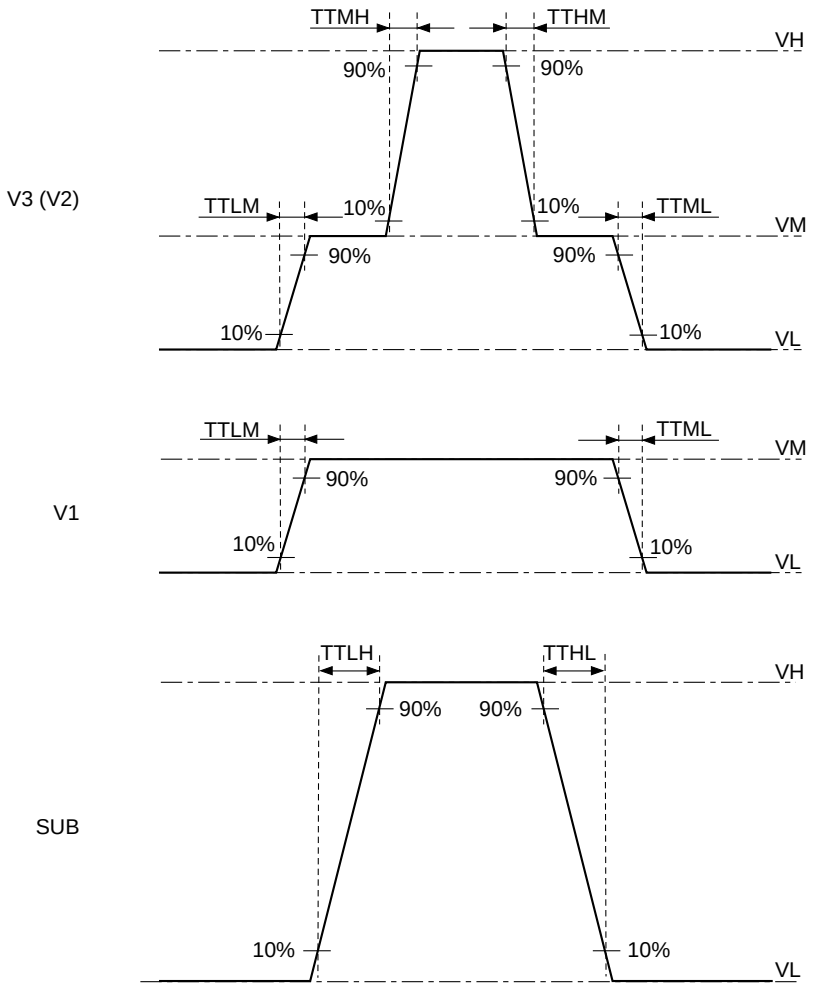
Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

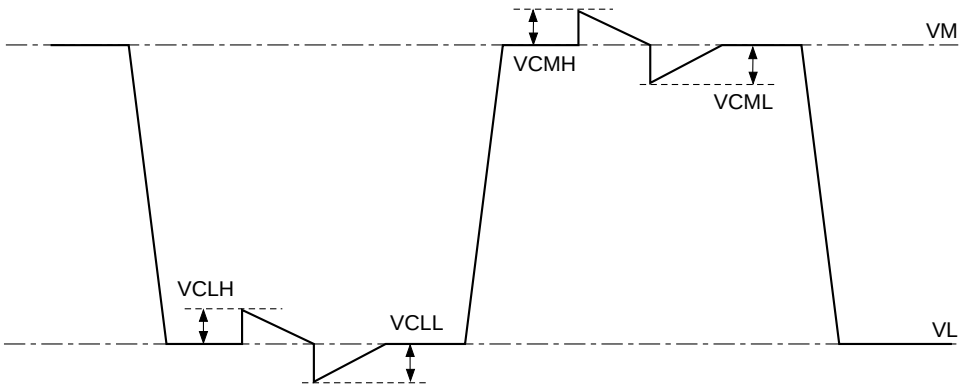
Notes)

1) The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2) For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3) To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

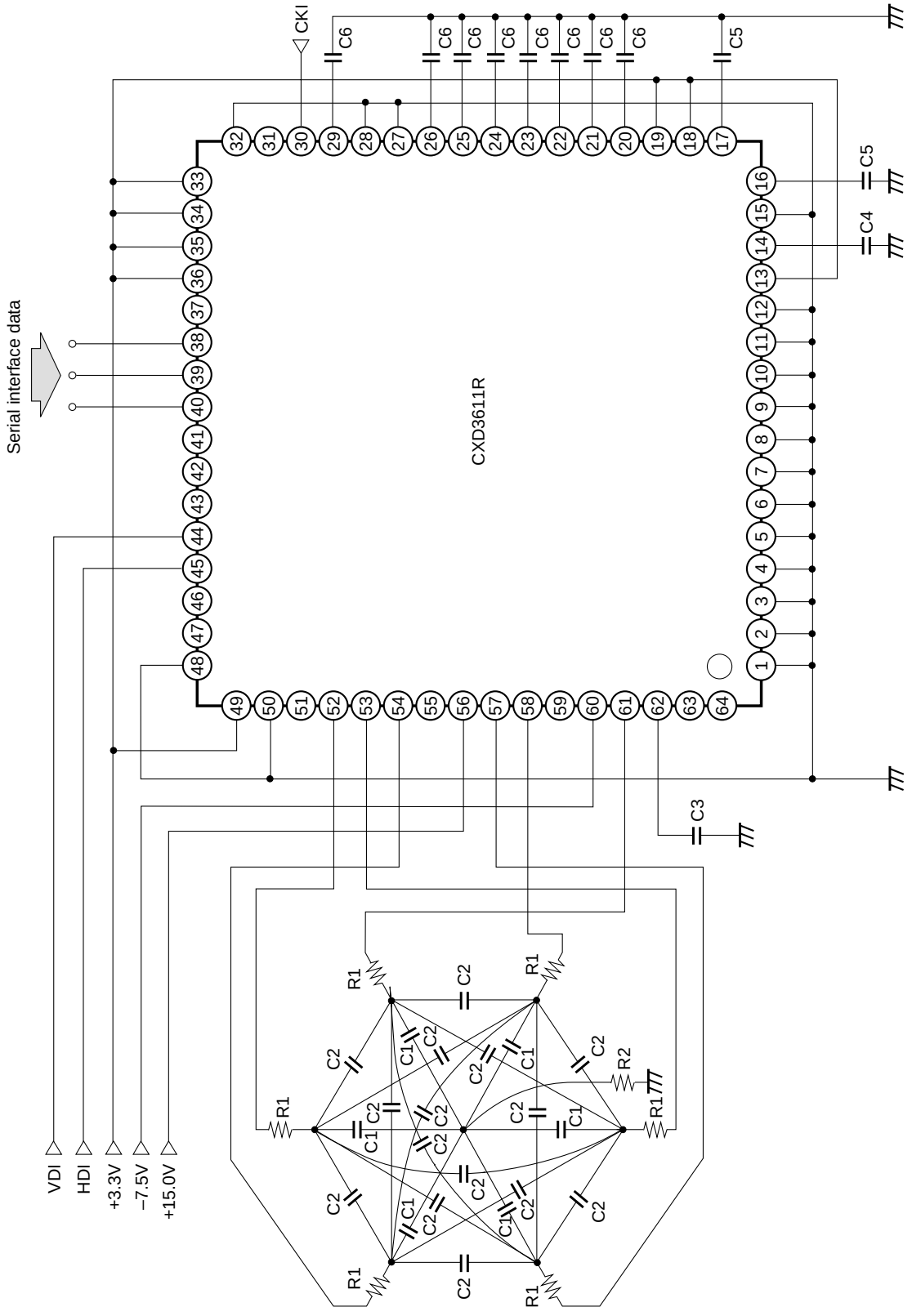
Switching Waveforms



Waveform Noise

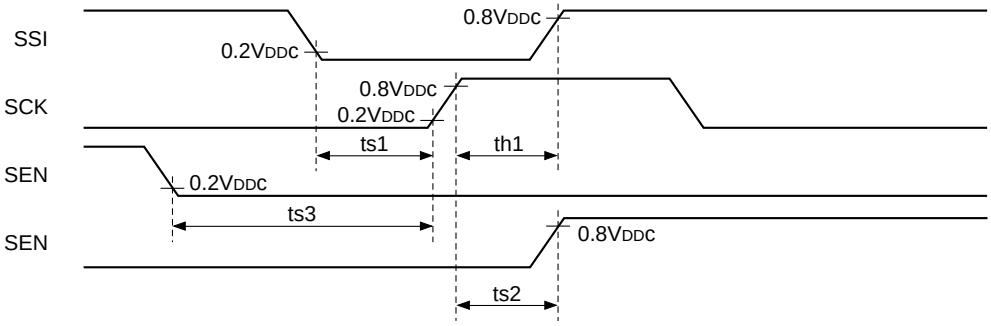


Measurement Circuit



AC Characteristics

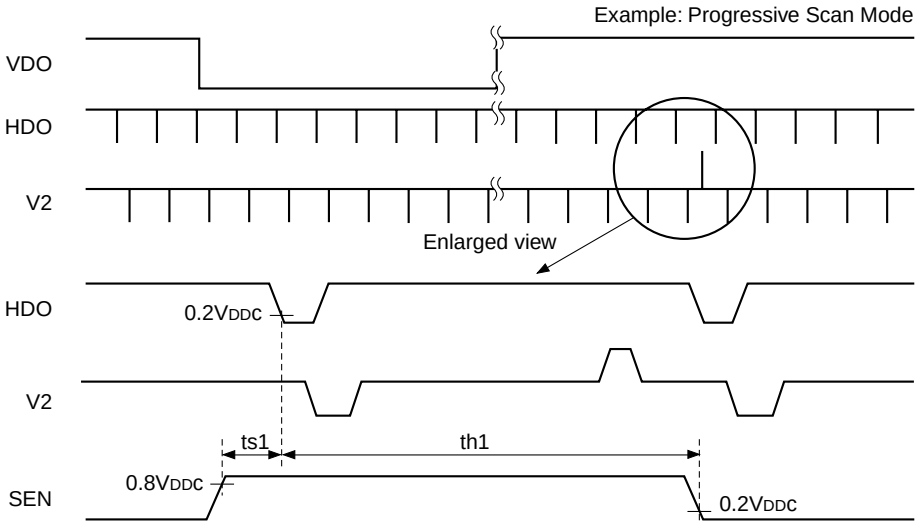
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SCK	20			ns
th1	SSI hold time, activated by the rising edge of SCK	20			ns
ts2	SCK setup time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SCK	20			ns

Serial interface clock internal loading characteristics



* Be sure to maintain a constantly high SEN logic level near the falling edge of the HDO in the horizontal period during which V2 and V3 values take the ternary value and during that horizontal period.

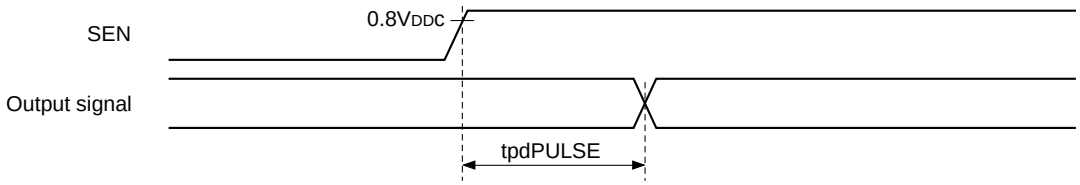
(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of HDO	0			ns
th1	SEN hold time, activated by the falling edge of HDO	32			µs

* Restrictions in the progressive scan mode when the ICX415 operating frequency is set to 29.5MHz.

Serial interface clock output variation characteristics

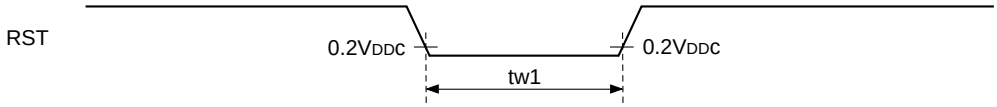
Normally, the serial interface data is loaded to the CXD3611R at the timing shown in the section "Serial interface clock internal loading characteristics". However, one exception to this is when the data such as CKMD is loaded to the CXD3611R and controlled at the rising edge of SEN. See "Description of Operation".



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		100	ns

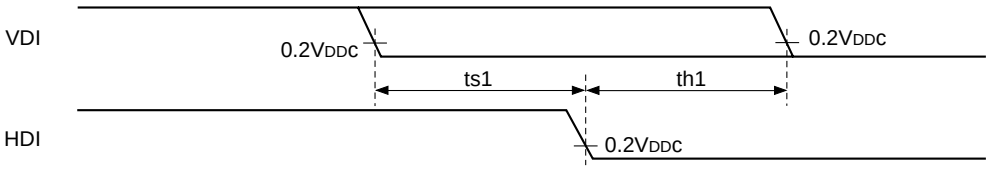
RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

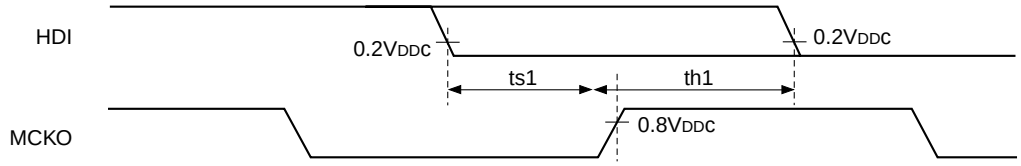
VDI and HDI phase characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VDI setup time, activated by the falling edge of HDI	0			ns
th1	VDI hold time, activated by the falling edge of HDI	0			ns

HDI loading characteristics

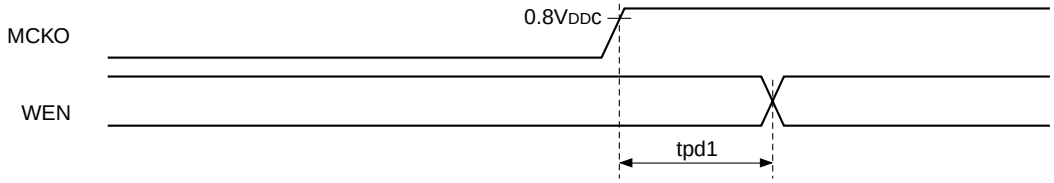


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{s1}	HDI setup time, activated by the rising edge of MCKO	16			ns
t_{h1}	HDI hold time, activated by the rising edge of MCKO	0			ns

Output variation characteristics



WEN load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{pd1}	Time until the above outputs change after the rise of MCKO	25		55	ns

Description of Operation

Pulses output from the CXD3611R are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on the following pages.

Pin Status Table

Pin No.	Symbol	CAM	RST	Pin No.	Symbol	CAM	RST	Pin No.	Symbol	CAM	RST
1	$V_{SS}1$	—		23	PBLK	ACT	H	45	VDI	ACT	ACT
2	SNCSL	ACT	ACT	24	CLPDM	ACT	H	46	VDO	ACT	H
3	SSGSL	ACT	ACT	25	OBCLP	ACT	H	47	HDO	ACT	H
4	CCD	ACT	ACT	26	ADCLK	ACT	ACT	48	$V_{SS}5$	—	
5	MD1	ACT	ACT	27	$V_{SS}3$	—		49	RST	ACT	L
6	MD2	ACT	ACT	28	$V_{SS}4$	—		50	VM	—	
7	MD3	ACT	ACT	29	MCKO	ACT	ACT	51	NC	—	
8	SMD1	ACT	ACT	30	CKI	ACT	ACT	52	V1	ACT	VL
9	SMD2	ACT	ACT	31	OSCO	ACT	ACT	53	NC	—	
10	SMD3	ACT	ACT	32	OSCI	ACT	ACT	54	V2	ACT	VM
11	HDRS	ACT	ACT	33	$V_{DD}4$	—		55	NC	—	
12	CDSRS	ACT	ACT	34	RDM	ACT	ACT	56	VH	—	
13	$V_{DD}1$	—		35	TRG	ACT	ACT	57	NC	—	
14	RG	ACT	ACT	36	ESG	ACT	ACT	58	V3	ACT	VL
15	$V_{SS}2$	—		37	PS	ACT	ACT	59	NC	—	
16	H1	ACT	ACT	38	SSI	ACT	DIS	60	VL	—	
17	H2	ACT	ACT	39	SCK	ACT	DIS	61	NC	—	
18	$V_{DD}2$	—		40	SEN	ACT	DIS	62	SUB	ACT	VL
19	$V_{DD}3$	—		41	WEN	ACT	L	63	NC	—	
20	XSHP	ACT	ACT	42	BLK	ACT	L	64	TEST	—	
21	XSHD	ACT	ACT	43	SYNC	ACT	L				
22	XRS	ACT	ACT	44	HDI	ACT	ACT				

Note) CAM means normal operation and RST means a state wherein control is applied by the RST pin (Pin 49).
ACT means that the circuit is operating, and DIS means that loading is stopped. L indicates a low output level, and H indicates a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin 56), VM (Pin 50) and VL (Pin 60), respectively, in the controlled status.

Parallel Interface Control

The CXD3611R has several pin control systems. Specifically, they are SNCSL (Pin 2), SSGSL (Pin 3), CCD (Pin 4), MD1 , MD2 , MD3 (Pins 5 to 7), SMD1 , SMD2 , SMD3 (Pins 8 to 10), HDRS (Pin 11), CDSRS (Pin 12), RDM (Pin 34), TRG (Pin 35), ESG (Pin 36), PS (Pin 37), HDI (Pin 44), VDI (Pin 45), and RST (Pin 49).

See "Pin Description" for details regarding: SNCSL , SSGSL , CCD , HDRS , CDSRS , PS , RST .

When parallel control is selected in the PS pin (Pin 37), the control indicated below takes priority over the serial control, described later. Note that (double) indicates that the base oscillation frequency ratio is doubled and it has entered a low speed drive. When a double speed drive is entered, it means that drive at a normal speed can be used.

Also, a single field 1 means only the ODD sided field is repeated so half of the 0.5H is applied to that V frequency. Single field 2 means only the ODD sided field simultaneously, but has 1H units for that V frequency.

MD2/MD1		Low/Low	Low/High	High/Low	High/High
MD3	Low	Progressive scan	Central scan 1	Single field 1	Interlace
	High	Progressive scan (Double)	Central scan 2	Single field 2	Interlace (Double)

* See the section relating to serial interface control and drive mode, describe later, for details.

SMD3	SMD2	SMD1	ICX414/424		ICX415		Unit
			Progressive scan	Interlace	Progressive scan	Interlace	
Low	Low	Low	No SUB 000h	No SUB 000h	No SUB 000h	No SUB 000h	—
Low	Low	High	1/100 16Fh	1/100 068h	1/120 1FEh	1/120 0B5h	s
Low	High	Low	1/250 1CDh	1/250 0C7h	1/250 232h	1/250 0F9h	s
Low	High	High	1/500 1EDh	1/500 0E6h	1/500 251h	1/500 118h	s
High	Low	Low	1/1000 1FCh	1/1000 0F6h	1/1000 260h	1/1000 128h	s
High	Low	High	1/2000 204h	1/2000 0FEh	1/2000 268h	1/2000 130h	s
High	High	Low	1/4000 208h	1/4000 102h	1/4000 26Ch	1/4000 134h	s
High	High	High	All SUB 20Dh	All SUB 106h	All SUB 270h	All SUB 138h	—

* Uses progressive scan mode and interlace mode as standards.
Central scan mode and single field mode are not strictly combined.

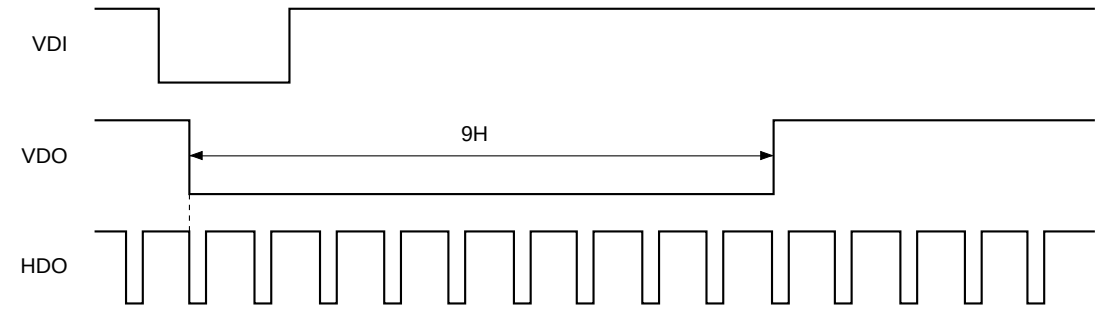
TRG , RDM , ESG use the trigger shutter function. The trigger shutter function relates to serial control and the electronic shutter function, and as such is described later.

The functions for HDI and VDI are switched by SSGSL .
VDI is received as V-reset when the internal SSG priority is set to (SSGSL = L). However, basically, VDI / HDI are fixed at high so substantially, it is an internal SSG drive.
VDO is V-Reset by VD1 , when the external sync priority is set to (SSGSL = H). This IC simply repeats idle transfers of V when a 1V operation is cut and a longer cycle is applied. Also, H-Reset occurs for HDO by HDI .
Note that for external sync priority, operations without a VDI / HDI reset input are not guaranteed.

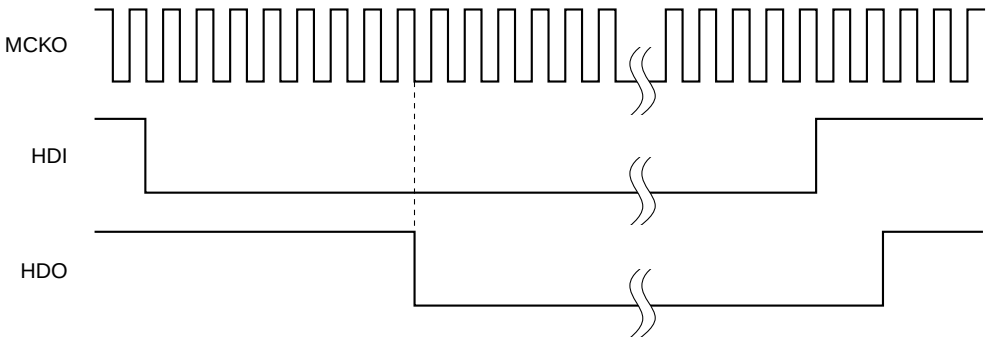
In the interlace system mode, when a falling edge of the VDI input from an external source is detected, it determines whether it is ODD or EVEN. If ODD, a V-Reset is applied on the falling edge of the HDO and the midway of the HDO if EVEN, so that the VDO falls. VDI requires a pulse width of over 2H.

Also, in all, an H-Reset is applied when a falling edge of an HDI reset signal is detected and HDO falls with the falling edge after 9MCKO. The minimum reset pulse width of the HDI is 10MCKO.

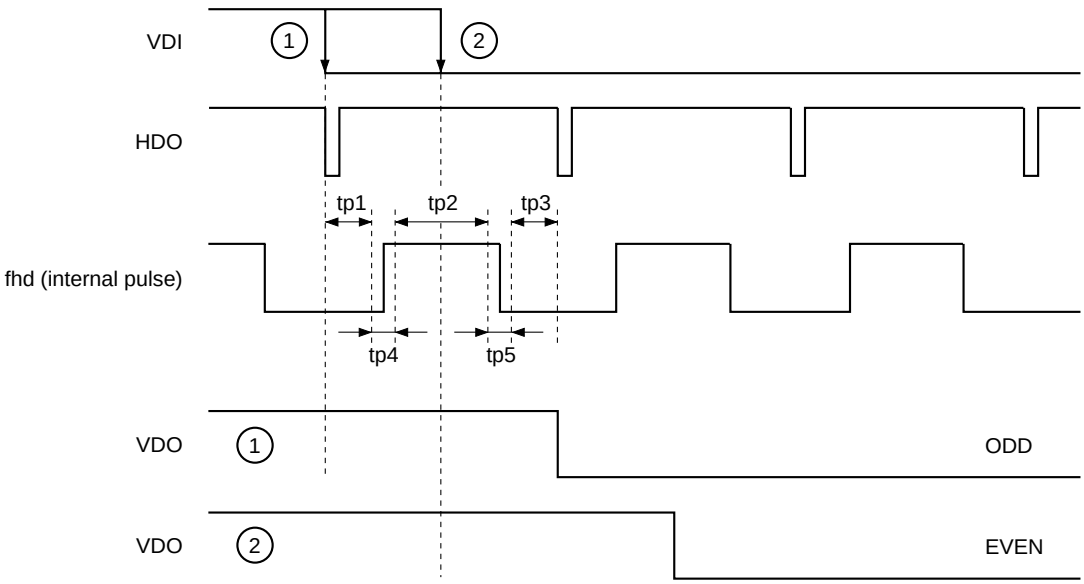
V-Reset



H-Reset



Field Identification (When VDI is input in the interlace system mode)

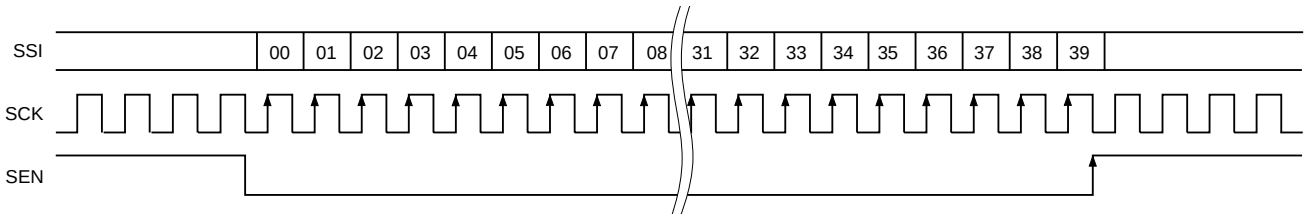


Symbol	Definition	ICX414/424 (ck)	ICX415 (ck)
tp1	Region to reset to ODD	273	329
tp2	Region to reset to EVEN	384	465
tp3	Region to reset to ODD	—	—
tp4	Prohibited region	4	4
tp5	Prohibited region	4	4

* There are no particular standards because HDO periods can be any value according to the HDI reset.
* Clock unit is MCKO.

Serial Interface Control

The CXD3611R can be controlled by the serial interface data transmitted in the format below, for controls other than those that are applied by MD1 , MD2 , MD3 (Pins 5 to 7) and SMD1 , SMD2 , SMD3 (Pins 8 to 10) when serial control or parallel control is selected in the PS (Pin 37).
Serial interface data latches with the rising edge of the SEN for each 1 category and reflects taking in at the falling edge of the HDO in the readout field. The readout field indicates horizontal period during which V2 and V3 values take the ternary value.



Note that there are three main categories in serial interface data. Specifically, they are: CXD3611R drive control data (control data), electronic shutter data (shutter data) and trigger shutter data (trigger data).
The following describes each in detail.

Control Data

Data	Name	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08, D09	CTG	Category switching	00 → CTL		0 0
D10, D11	—	—	—	—	0 0
D12 to D14	MODE	Drive mode switching	See the section on drive mode		All 0
D15	CKMD	Base oscillation frequency division switching*1	2 frequency division	4 frequency division	0
D16 to D19	—	—	—	—	All 0
D20, D21	PTOB	OBCLP waveform pattern switching	See the section on OBCLP waveform patterns		1 0
D22, D23	LDAD	ADCLK logic phase switching	See the section on ADCLK logic phase		1 0
D24	FGOB	Vertical direction width OBCLP generation switching*2	ON	OFF	0
D25	RGRS	RG pulse inversion switching	Posotive polarity	Negative polarity	0
D26 to D39	—	—	—	—	All 0

*1 See the section on drive mode

*2 See the section on wide OBCLP generation

Shutter Data

Data	Name	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08, D09	CTG	Category switching	01 → SHT		0 0
D10, D11	—	—	—	—	0
D12	SMD	Electronic shutter mode switching*1	OFF	ON	0
D13	HTSG	HTSG control switching*1	OFF	ON	0
D14 to D23	SVT	Electronic shutter vertical period specification	See the section on electronic shutter		All 0
D24 to D33	SHT	Electronic shutter horizontal period specification	See the section on electronic shutter		All 0
D34 to D39	—	—	—	—	All 0

*1 See the section on electronic shutter

Trigger Data

Data	Name	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08, D09	CTG	Category switching	10 → TRIG		0 0
D10 to D23	—	—	—	—	All 0
D24 to D33	TSG	Trigger shutter horizontal period specification	See the section on trigger shutter		All 0
D34	—	—	—	—	0
D35	TFINT	TSINT function switching*1	OFF	ON	0
D36 to D39	TSINT	Trigger shutter fine adjustment specification	See the section on trigger shutter		All 0

*1 See the section on trigger shutter

Detailed Description of Each Data

Shared data: D08 to D09 CTG [Category]

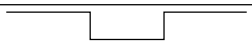
Of the data provided to the CXD3611R by the serial interface, the CXD3611R loads D10 and subsequent data to each data register as shown in the table below according to the combination of D08 and D09 .

D09	D08	Description of operation
0	0	Loading to control data register
0	1	Loading to shutter data register
1	0	Loading to trigger data register
1	1	Test mode

Note that the CXD3611R can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D20 to D21 PTOB [OBCLP waveform pattern]

This indicates the OBCLP waveform pattern. The default is "Normal". See the timing chart for details regarding decode values.

D21	D20	Waveform pattern	ICX414/424	ICX415
0	0	 (Normal)	11 to 31	11 to 36
0	1	 (Shifted forward)	9 to 29	9 to 34
1	0	 (Shifted rearward)	13 to 33	14 to 39
1	1	 (Wide)	9 to 33	9 to 39

Control data: D24 FGOB [Vertical direction wide OBCLP generation]

This controls wide OBCLP generation during the vertical OPB period. When this function is turned ON, D20 and D21 PTOB specification is disabled for the output. See the Timing Charts for the actual operation. The default is "ON".

D24	Description of operation
0	Vertical direction wide OBCLP generation ON
1	Vertical direction wide OBCLP generation OFF

Control data: D22 to D23 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is "90°" relative to MCKO.

D23	D22	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: [Drive mode]

CXD3611R realizes various drive modes using the control data D12 to D14 MODE and CCD pins (Pin 4). The following gives detailed descriptions. First, the basic drive modes are shown below. This uses of the control data MODE D12 and D13 .

D13	D12	Description of operation
0	0	Progressive scan mode (default)
0	1	Central scan mode
1	0	Single field mode
1	1	Interlace mode

The progressive scan mode is a drive mode that reads out all of the line data of the CCD image sensor.
The central scan mode is a drive mode that uses the progressive scan mode as a base to read out the central image in a high frame rate.
The interlace mode is a drive mode for outputting according to TV standards.
The single field mode is a drive mode for reading only single field of the aforementioned interlace mode.
Base on these, it uses MODE D14 to realize the following variations.

D13/D12		0/0	0/1	1/0	1/1
D14	0	Progressive Scan	Central scan 1	Single field 1	Interlace
	1	Single field 3	Central scan 2	Single field 2	Single field 4

If D14 is allotted while D12 and D13 are in the central scan mode, it behaves in the following manner. When D14 is "0", it drives in the pattern called central scan mode 1. When D14 is "1" it drives in the pattern called central scan mode 2.
Other patterns are variations of the single field mode. To describe the items of the table, single field 1 drives by repeating the ODD side of the interlace mode. Single field 3 drives by repeating the EVEN side of the interlace mode. Single field 2 repeats the ODD side of the interlace mode, but if an NTSC standard CCD is used, it enters a pattern to drive cutting the field applying 262.5H into HD units of 262H. Single field 4, in the same way, enters a pattern to drive the EVEN side of the interlace mode in 262H units. However, these last two modes are actually controls for the internal SSG, so when using an external sync, this function is not guaranteed.
Depending on the pin control CCD, it switches to the ICX414/424 for NTSC (EIA) standard systems and to ICX415 for PAL (CCIR) standard systems. See the timing chart for details regarding either drive mode.
Finally, as for the double-speed mode, it switches according to the D15 CKMD, but when realizing this drive mode, set the base oscillation frequency to two times the normal speed. By switching using the parameters above, normal and double speeds can be dually used. To switch this parameter with the base oscillation frequency at its normal state, operation is in 1/2 speed drive mode, but the CCD operates outside of its guarantee.

Control data/shutter data: [Electronic shutter]

The CXD3611R realizes various electronic shutter functions by using shutter data D12 SMD, D13 HTSG, D14 to D23 SVT, and D24 to D33 SHT.

These functions are described in detail below.

First, the various modes are shown below. These modes are switched using shutter data D12 SMD.

D12	Description of operation
0	Electronic shutter stopped mode
1	Electronic shutter mode

The electronic shutter data is expressed as shown in the table below using D24 to D35 SHT as an example.

MSB									LSB
D33	D32	D31	D30	D29	D28	D27	D26	D25	D24
0	1	1	1	0	0	0	0	1	1
↓			↓				↓		
1			C				3		

→ Expressed as IC3h .

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[Electronic shutter mode]

During this mode, the shutter data items have the following meanings.

Name	Data	Description
SVT	Shutter: D14 to D23	Number of vertical periods specification (000h ≤ SVT ≤ 3FFh)
SHT	Shutter: D24 to D33	Number of horizontal periods specification (000h ≤ SHT ≤ 3FFh)

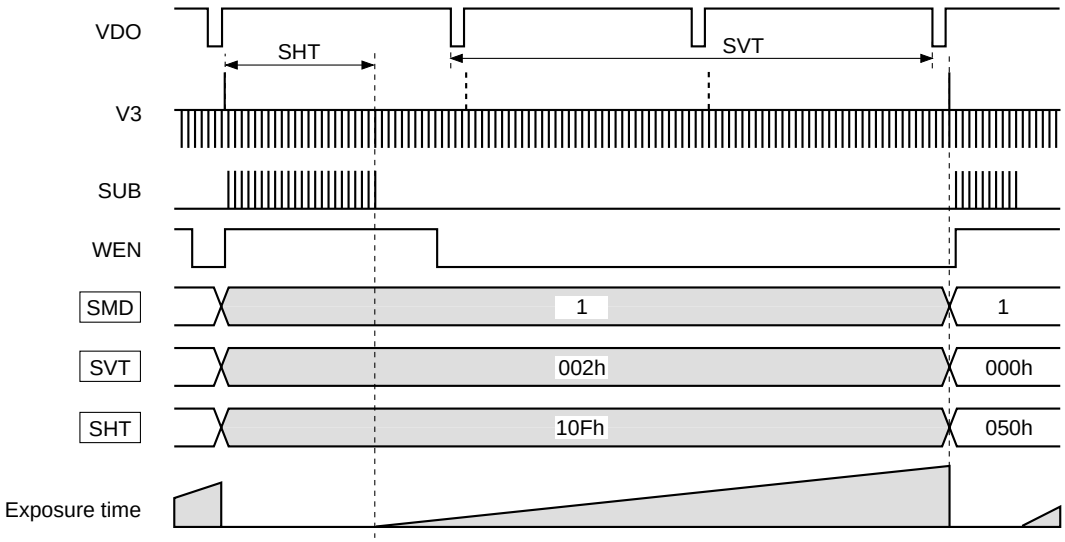
Note) The bit data definition area is assured in terms of the CXD3611R functions, and does not assure the CCD characteristics.

The period during which SVT and SHT are specified together is the shutter speed. The exposure time calculation formula is shown below. In actual operation, the precise exposure time is calculated from the operating frequency, VD and HD periods, decoding value during the horizontal period, and other factors.

(Exposure time) = SVT × (1V period) + {(number of HD per 1V) – (SHT + 1)} × (1H period)
+ (the distance from SUB falling edge of the readout period to the SG falling edge)

Concretely, when specifying high-speed shutter, SVT is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVT is set to "001h" or higher, the serial interface data is not loaded until this period is finished.

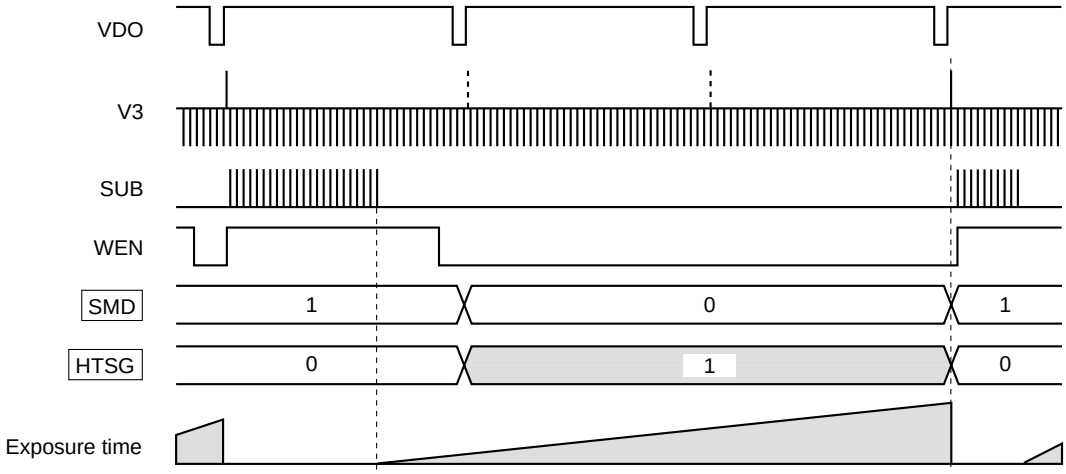
The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHT can be considered as (number of SUB pulses – 1). Also, the readout period is the normal horizontal period during which V2 and V3 values take the ternary value and SG indicates the readout pulse for the third value.



[HTSG control mode]

This mode controls the V2, V3 ternary values output (readout pulse block) using D13 HTSG.
However, when D12 SMD is in the electronic shutter mode, note that this operation is not guaranteed.

D13	Description of operation
0	Readout pulse (SG) normal operation
1	HTSG control mode

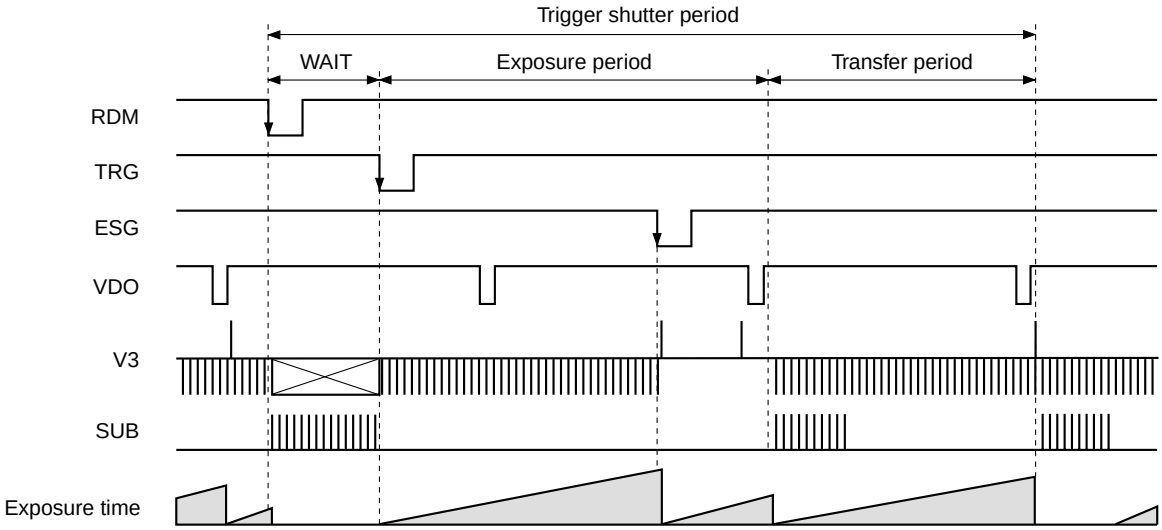


Trigger data: [Trigger shutter]

The CXD3611R realizes trigger shutter functions by using trigger data D24 TSG, D35 TFINT and D36 to D39 TSINT and RDM (Pin 34), TRG (Pin 35) and ESG (Pin 36).

These functions are described in detail below.

First, the basic sequences of the trigger shutter function are shown below.



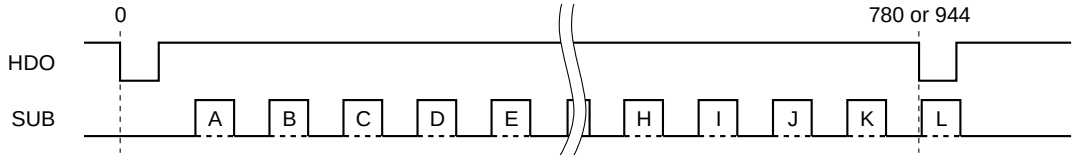
Initially, it enters a WAIT period from a horizontal period immediately following the falling edge of the RDM to begin high speed sweeping. At this time, SUB also generates horizontal periods simultaneously.

Next, immediately following the falling edge of TRG, it enters the exposure period from the horizontal period. High speed sweeping that had been generated up to that point is stopped whereat normal transfers begin. Simultaneously, SUB also ceases. The final SUB pulse specified is generated immediately following the falling edge of TRG. At this time, the settings of D36 to D39 TSINT are reflected enabling fine adjustments of the ultra-high speed shutter exposure time. However, only when D35 TFINT is set to ON, this function enables the internal counter and allows its use. See the table below for details regarding the adjustment data.

Next, immediately following the falling edge of the ESG, a readout pulse is generated in the horizontal period to set the exposure time. Then, data transfer occurs in sync to the next VD period, but normal transfers stop up to that point. Also, the readout pulse position can be specified using serial control. The positions counted as 0, 1, 2, ... from the horizontal period immediately following the falling edge of TRG, while the ESG is fixed to a high state, are specified using D24 to D33 TSG. However, parallel control has priority, so when executed from serial to parallel, it is possible to output the readout pulse twice in the same exposure time. However, operations in this situation are not guaranteed, so be careful of the sequences.

Note that it is presumed that the drive mode specified in the transfer period is either the progressive scan mode or the central scan mode systems. If the drive mode is set to something else, operations are not guaranteed. Furthermore, be aware that readout pulse outputs will be aborted. Normal SUB output is accepted from the transfer period. Also, this IC will not respond even if only TRG is applied. Always combine a sequence that uses RDM and TRG as a set. In other words, when omitting the high speed sweeping, RDM and TRG should be applied simultaneously.

[Trigger shutter fine adjustment data]



[For ICX414/424]

Position	D39	D38	D37	D36	Ascending position	Descending position
A	0	0	0	0	72*1	95*1
B	0	0	0	1	137	160
C	0	0	1	0	202	225
D	0	0	1	1	267	290
E	0	1	0	0	332	355
F	0	1	0	1	397	420
G	0	1	1	0	462	485
H	0	1	1	1	527	550
I	1	0	0	0	592	615
J	1	0	0	1	657	680
K	1	0	1	0	722	745
L	1	0	1	1	7*2	30*2
—	Remainder is invalid				—	—

[For ICX415]

Position	D39	D38	D37	D36	Ascending position	Descending position
A	0	0	0	0	99*1	122*1
B	0	0	0	1	177	200
C	0	0	1	0	255	278
D	0	0	1	1	333	356
E	0	1	0	0	411	434
F	0	1	0	1	489	512
G	0	1	1	0	567	590
H	0	1	1	1	645	668
I	1	0	0	0	723	746
J	1	0	0	1	801	824
K	1	0	1	0	879	902
L	1	0	1	1	13*3	36*3
—	Remainder is invalid				—	—

Note) Position data represents the counted values from the falling edge of the HRO to the rising edge of the MCKO.

*1 Default timings for each drive mode.

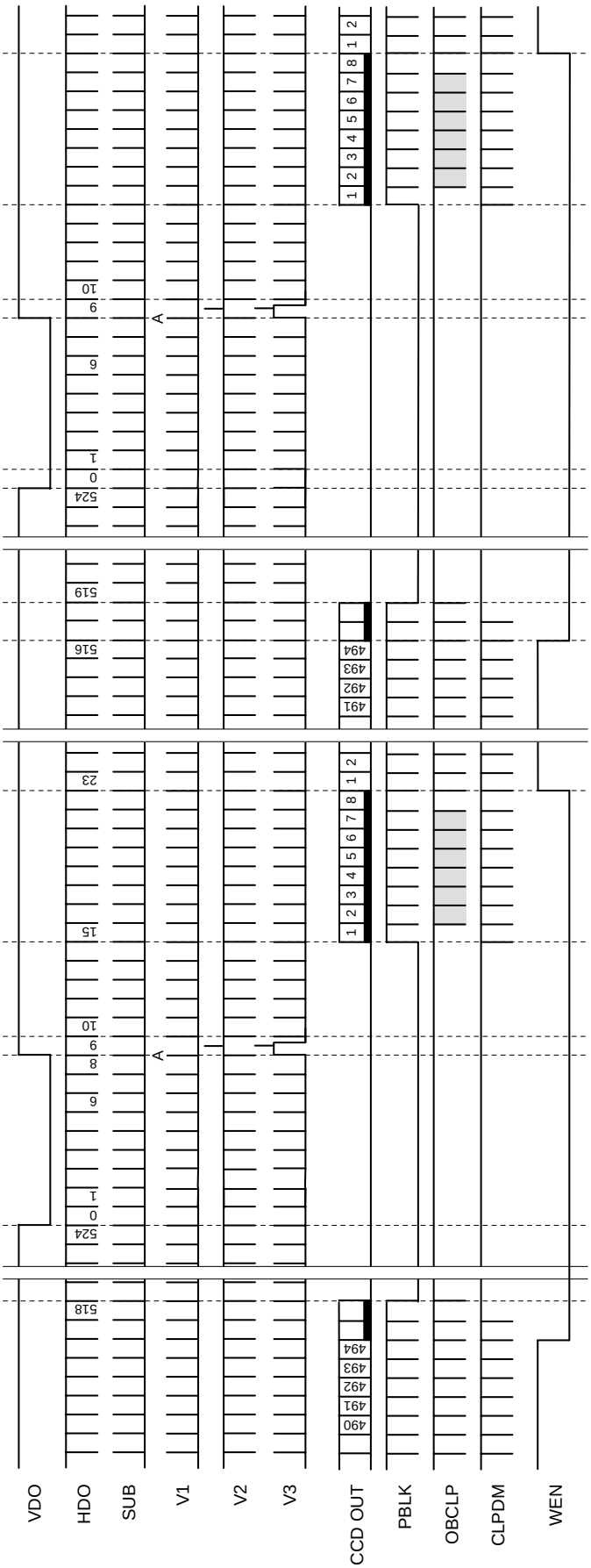
*2 This timing has a variable point in the 780ck cycle HDO.

*3 This timing has a variable point in the 944ck cycle HDO.

Chart-1 Vertical Direction Timing Chart

MODE
Progressive Scan Mode (Non-interlace)

Applicable CCD image sensor
• ICX414/424



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VR in this chart is described in 525H (1H: 780ck) units.

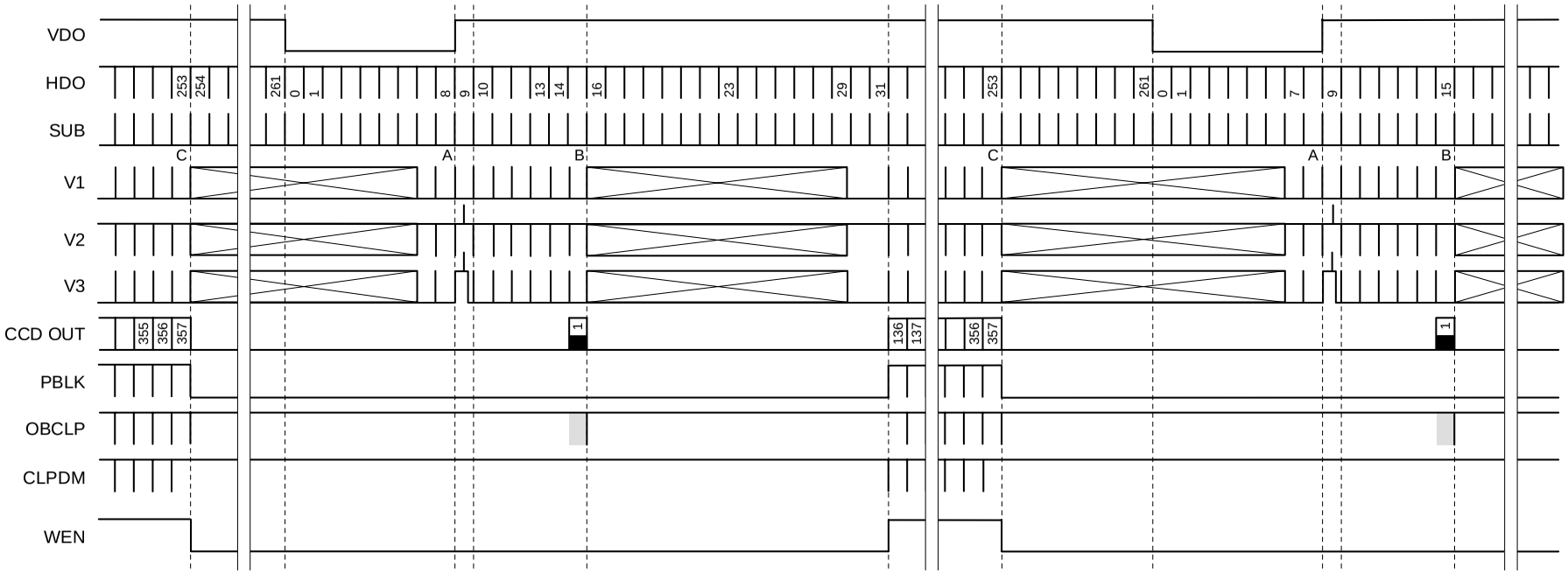
Chart-2 Vertical Direction Timing Chart

MODE

Central Scan 1 Mode

Applicable CCD image sensor

• ICX414/424



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 262H (1H: 780ck) units.
* Valid line count in this drive mode: 222 lines

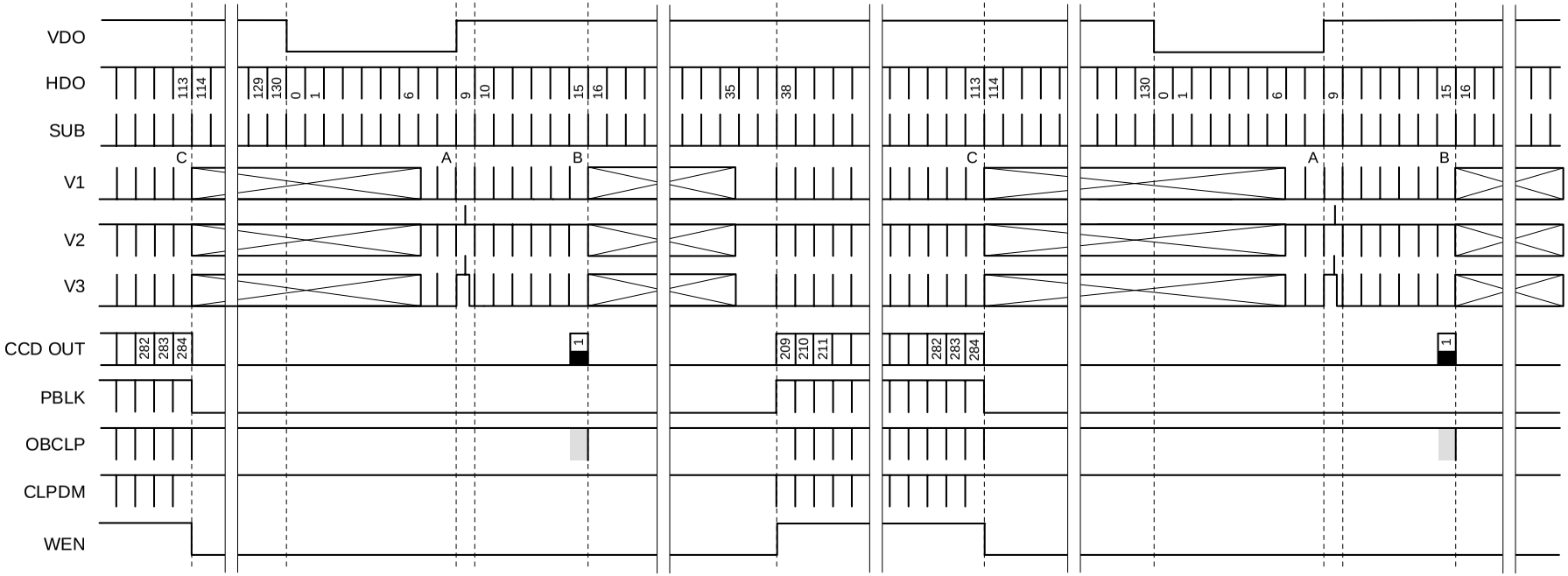
Chart-3 Vertical Direction Timing Chart

MODE

Central Scan 2 Mode

Applicable CCD image sensor

• ICX414/424

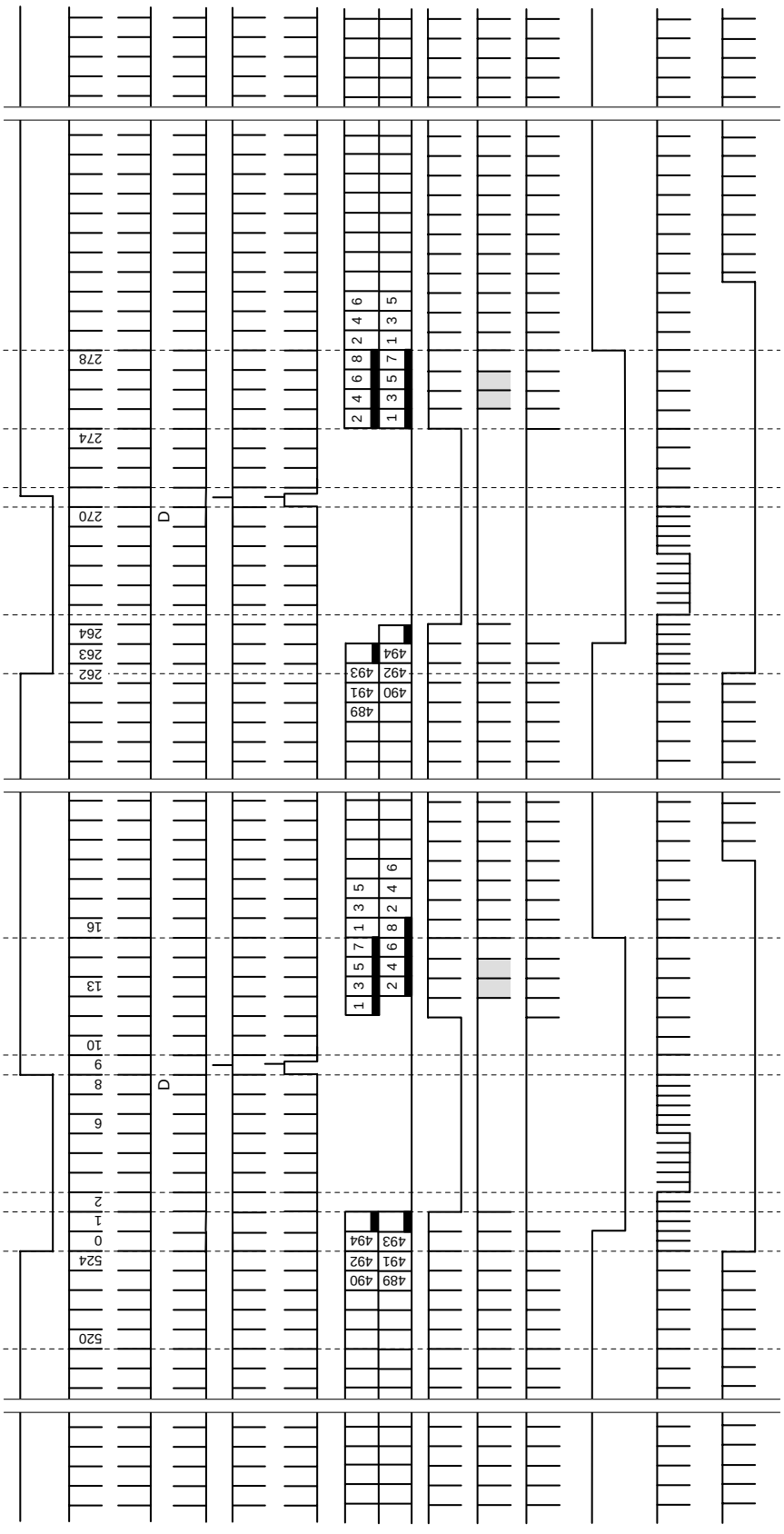


* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 131H (1H: 780ck) units.
* Valid line count in this drive mode: 76 lines

Chart-4 Vertical Direction Timing Chart

MODE
Pixel Add Mode (Interlace)

Applicable CCD image sensor
• ICX414/424



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 262H (1H: 780ck) units.

Chart-5 Horizontal Direction Timing Chart

MODE
Progressive Scan Mode

Applicable CCD image sensor
• ICX414/424

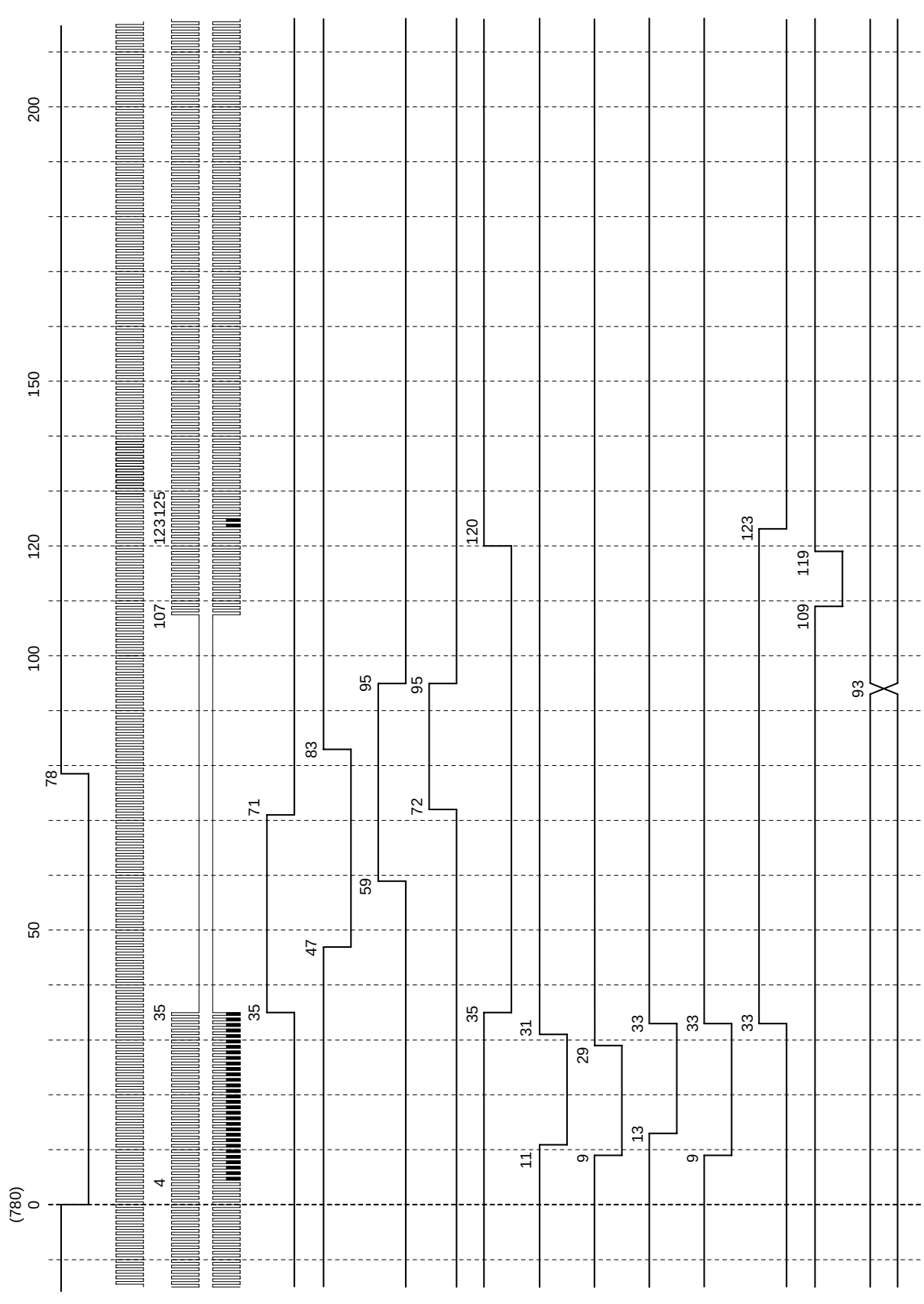
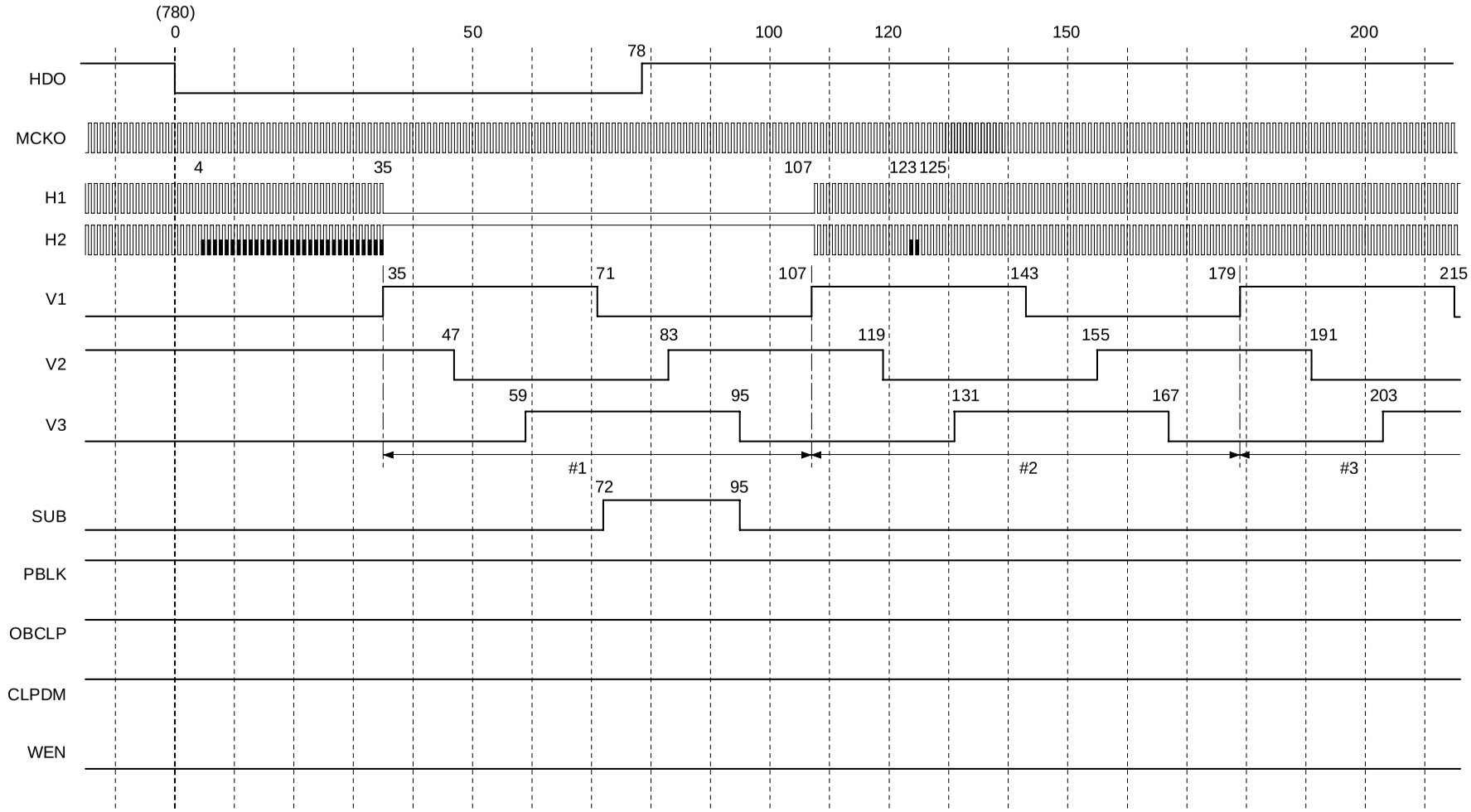


Chart-6 **Horizontal Direction Timing Chart**
(Frame shift: B)
(High speed sweeping: C)

MODE
Central Scan 1 Mode, Central Scan 2 Mode

Applicable CCD image sensor
• ICX414/424



	Frame Shift	High Speed Sweep
Central Scan 1	#142 (14H)	#167 (16H)
Central Scan 2	#215 (20H)	#255 (24H)

Chart-7 Horizontal Direction Timing Chart

MODE
Pixel Add Mode (Interlace Mode)

Applicable CCD image sensor
• ICX414/424

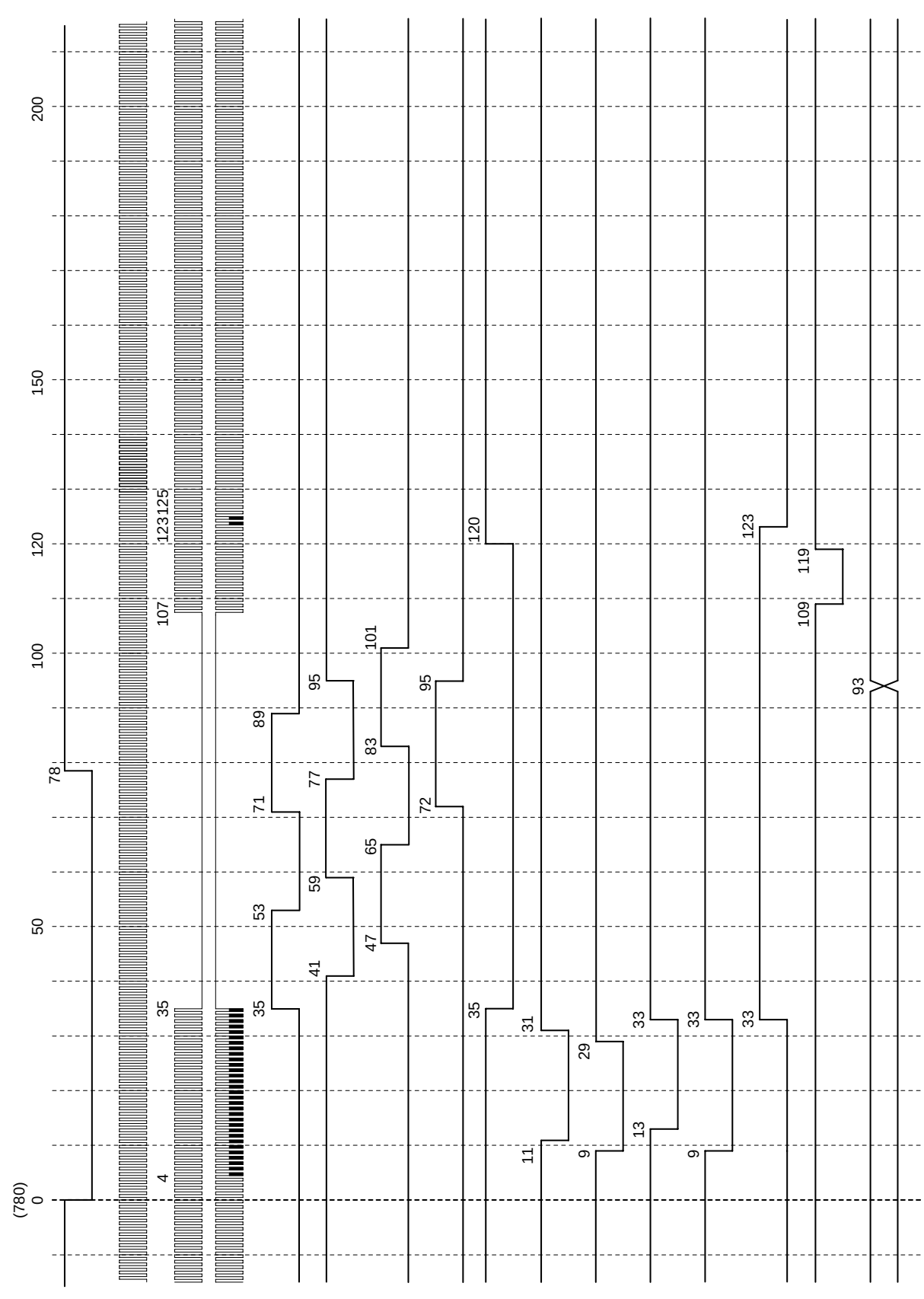


Chart-8 Horizontal Direction Timing Chart (Readout: A)

MODE
Progressive Scan Mode

Applicable CCD image sensor
• ICX414/424

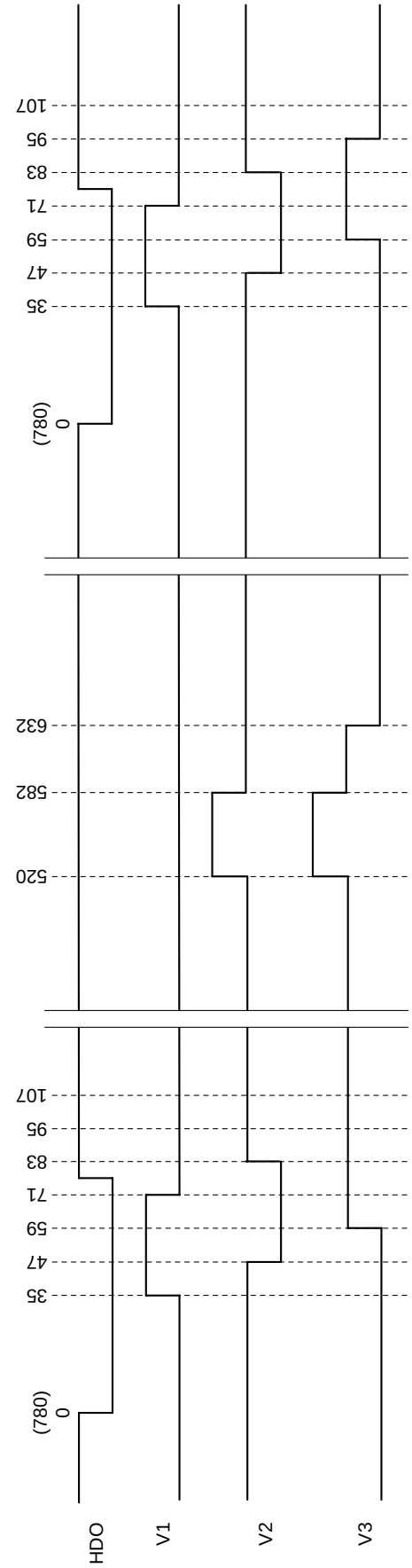


Chart-9 Horizontal Direction Timing Chart

Applicable CCD image sensor
• ICX414/424

MODE
Pixel Add Mode (Interlace)

Readout: D

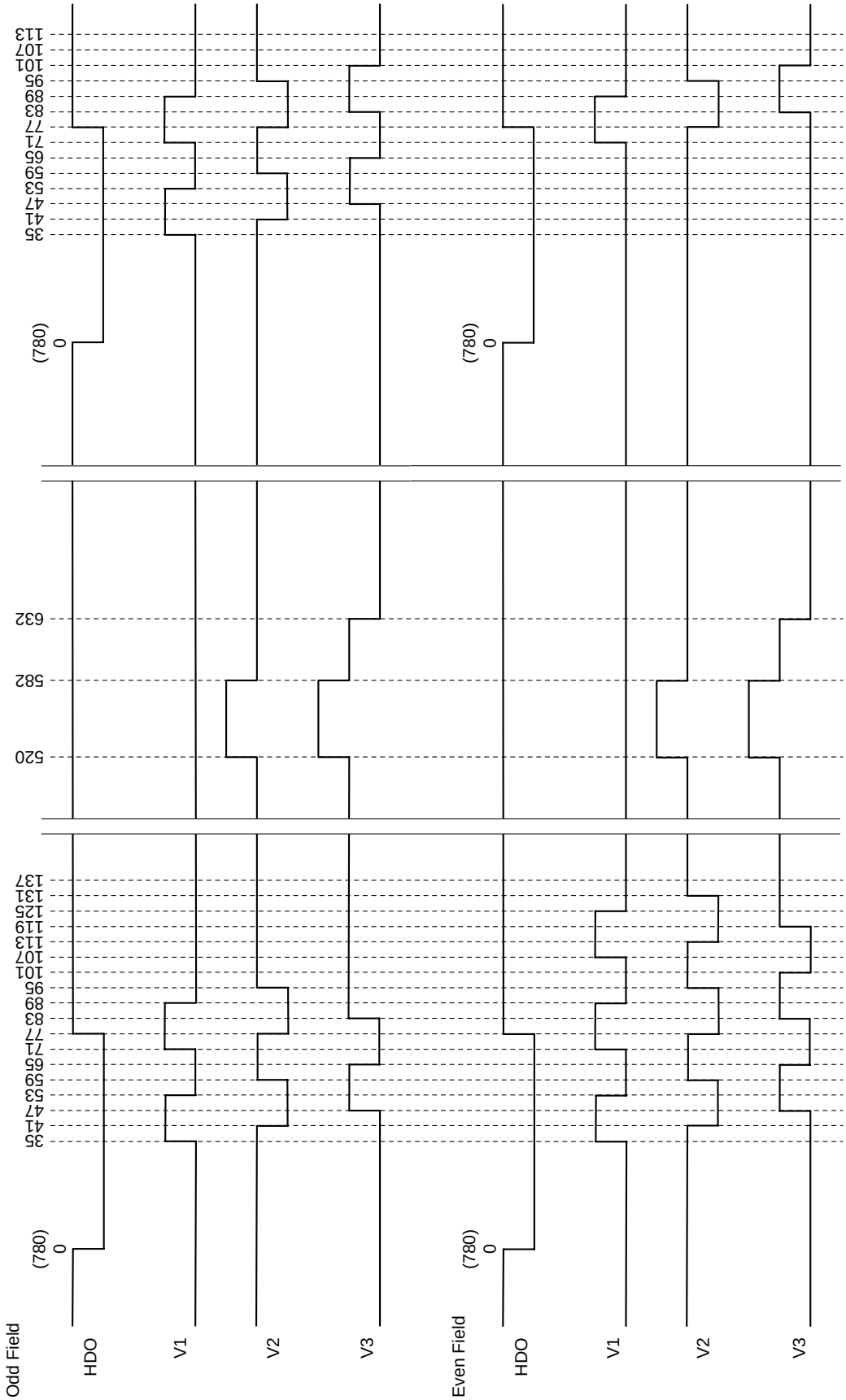
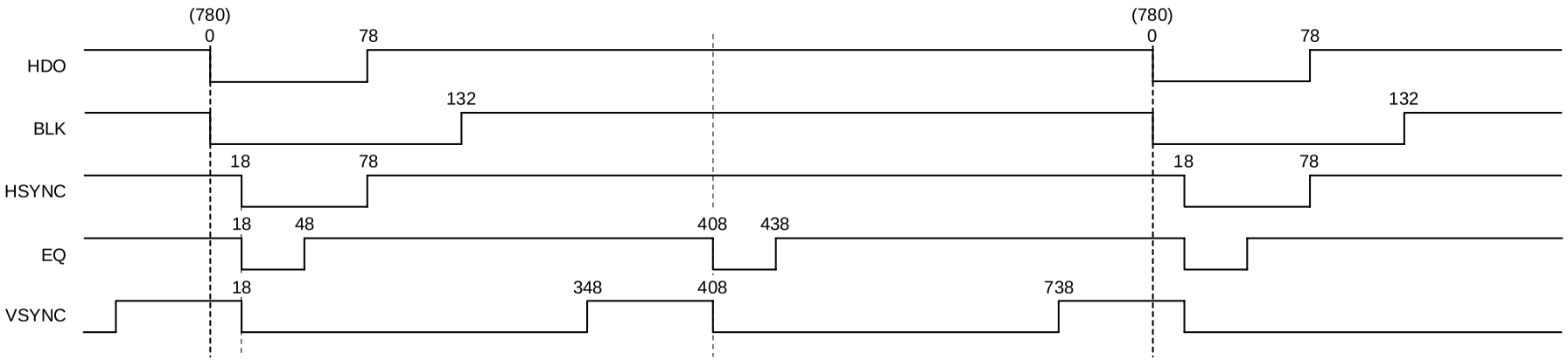


Chart-10 **Horizontal Direction Timing Chart (SSG Pulse)**

MODE
Pixel Add Mode (Interlace)

Applicable CCD image sensor
• ICX414/424



* HSYNC, EQ and VSYNC are combined and output from the SYNC pin. They are not individual pulses output externally.

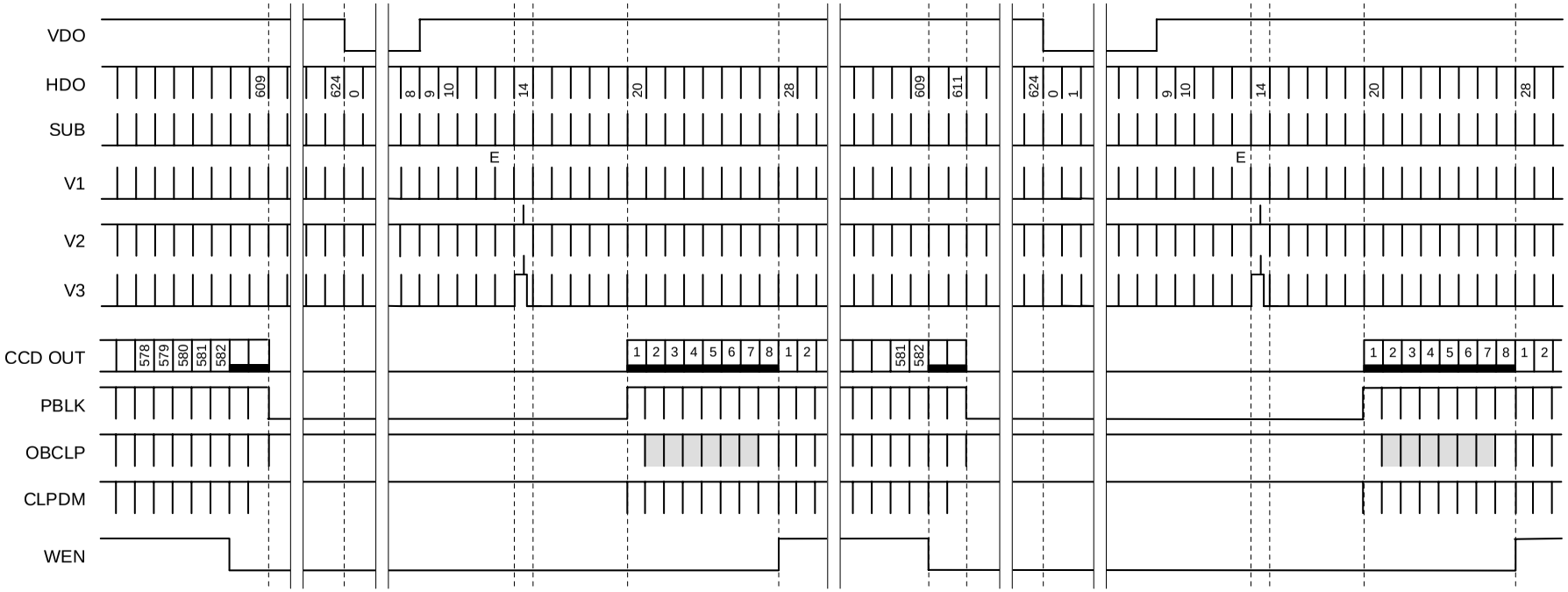
Chart-11 Vertical Direction Timing Chart

MODE

Progressive Scan Mode (Non-Interlace)

Applicable CCD image sensor

• ICX415



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 625H (1H: 944ck) units.

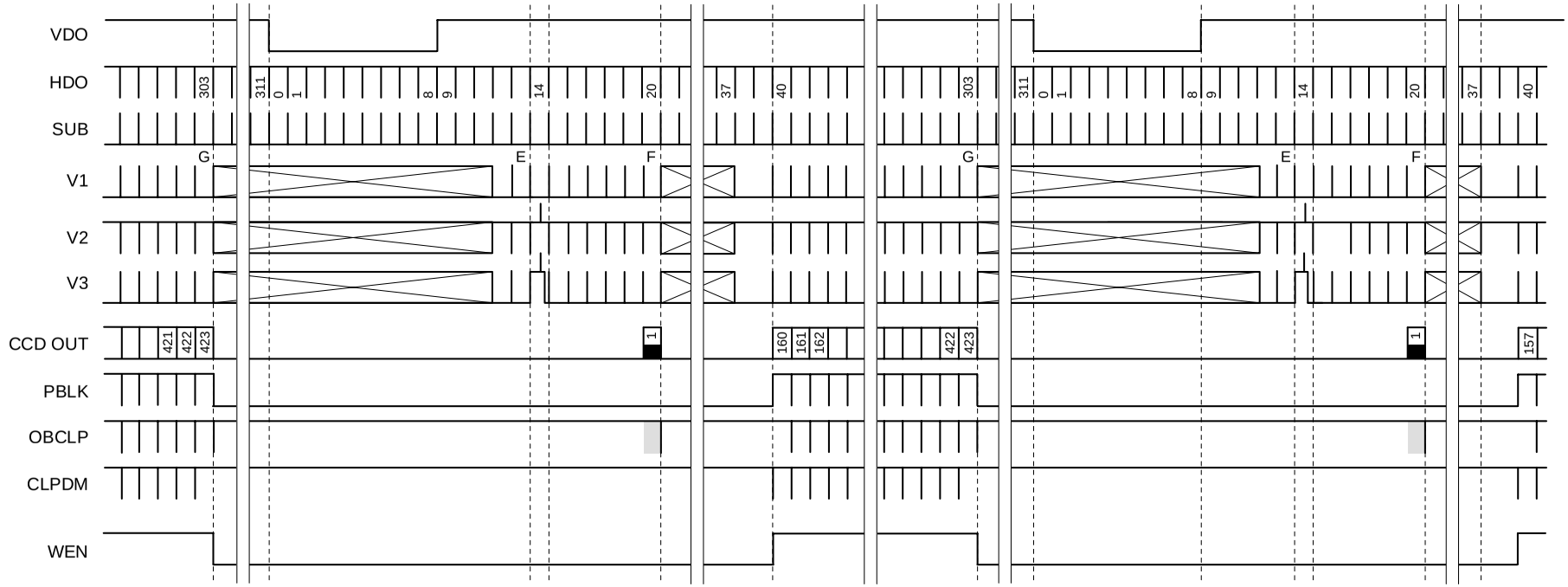
Chart-12 Vertical Direction Timing Chart

MODE

Central Scan 1 Mode

Applicable CCD image sensor

• ICX415

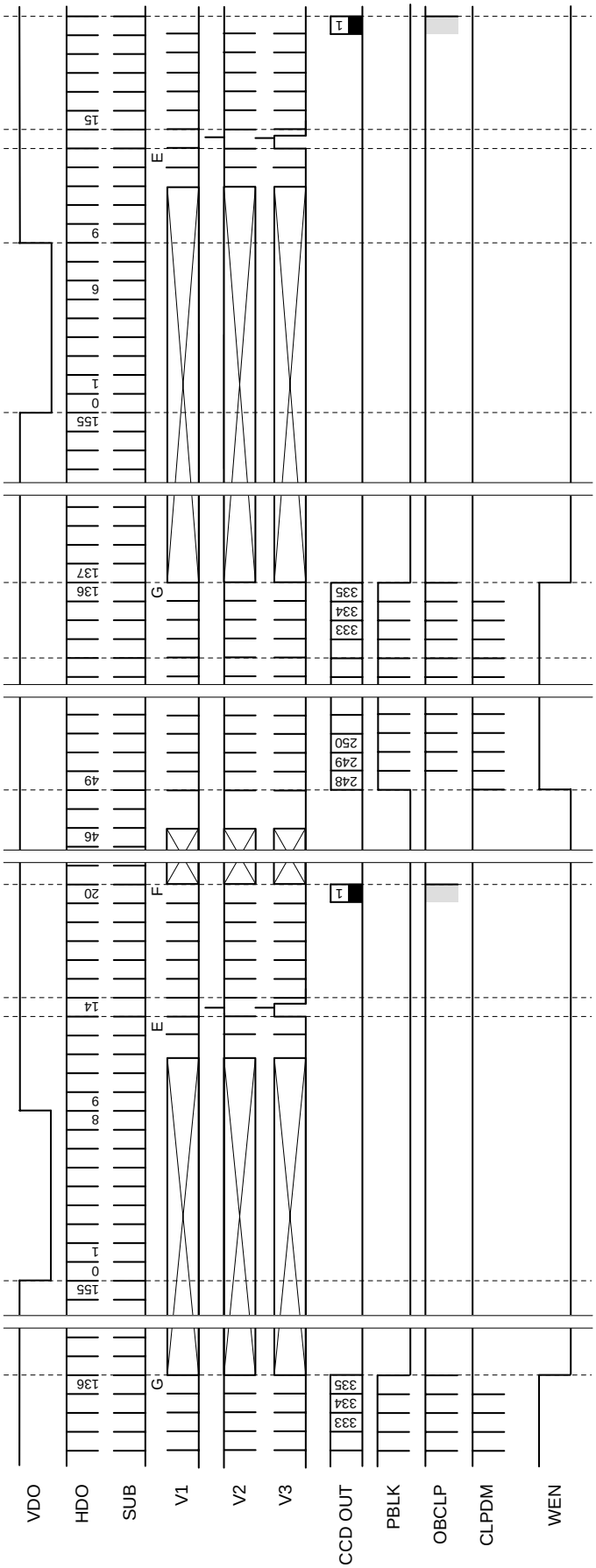


* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 312H (1H: 944ck) units.
* Valid line count in this drive mode: 264 lines

Chart-13 Vertical Direction Timing Chart

Applicable CCD image sensor
• ICX415

MODE
Central Scan 2 Mode



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 156H (1H: 944ck) units.
* Valid line count in this drive mode: 88 lines

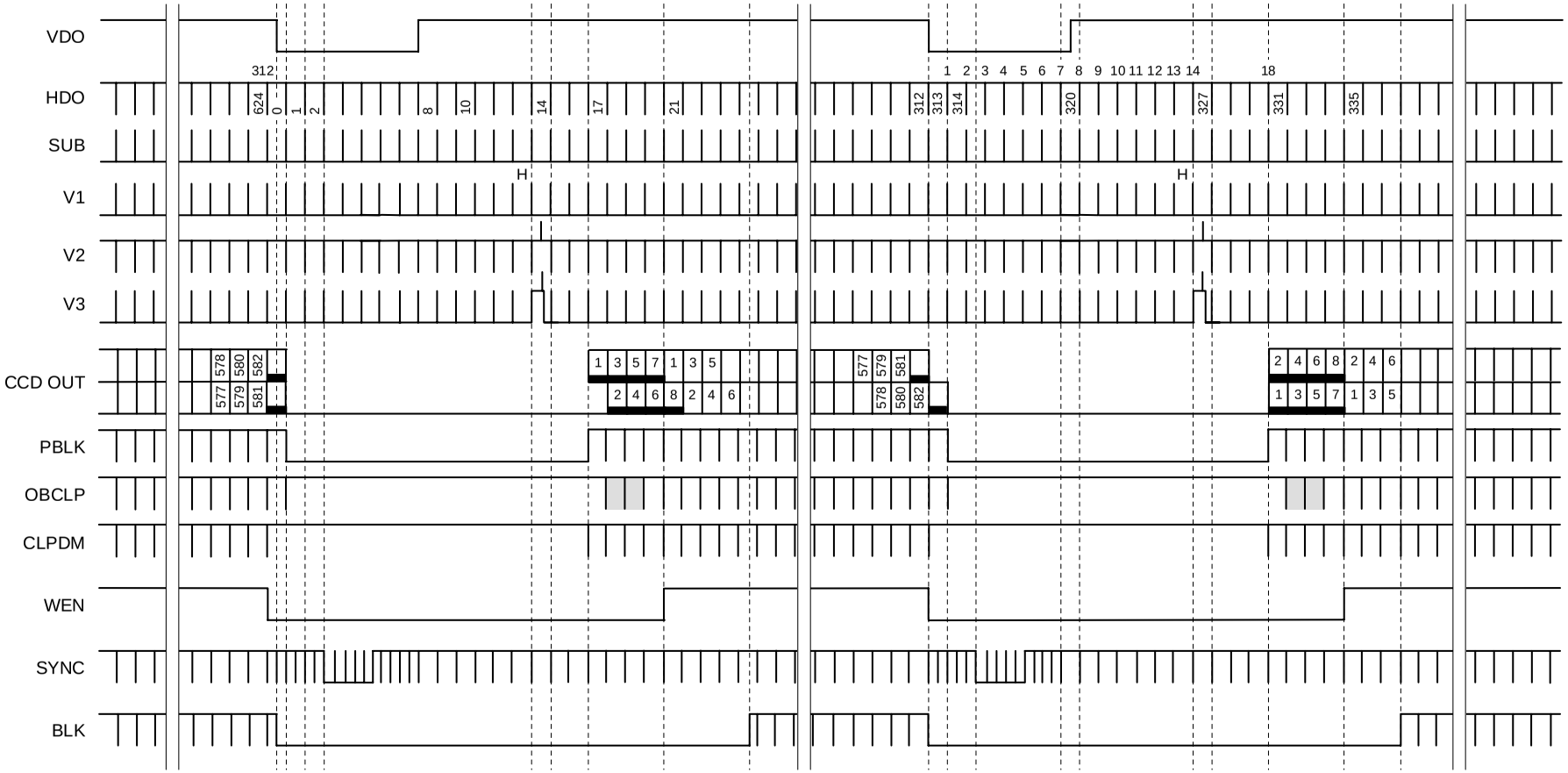
Chart-14 Vertical Direction Timing Chart

MODE

Pixel Add Mode (Interlace)

Applicable CCD image sensor

• ICX415



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* VDO in this chart is described in 3125H (1H: 944ck) units.

Chart-15 Horizontal Direction Timing Chart

MODE
Progressive Scan Mode

Applicable CCD image sensor
• ICX415

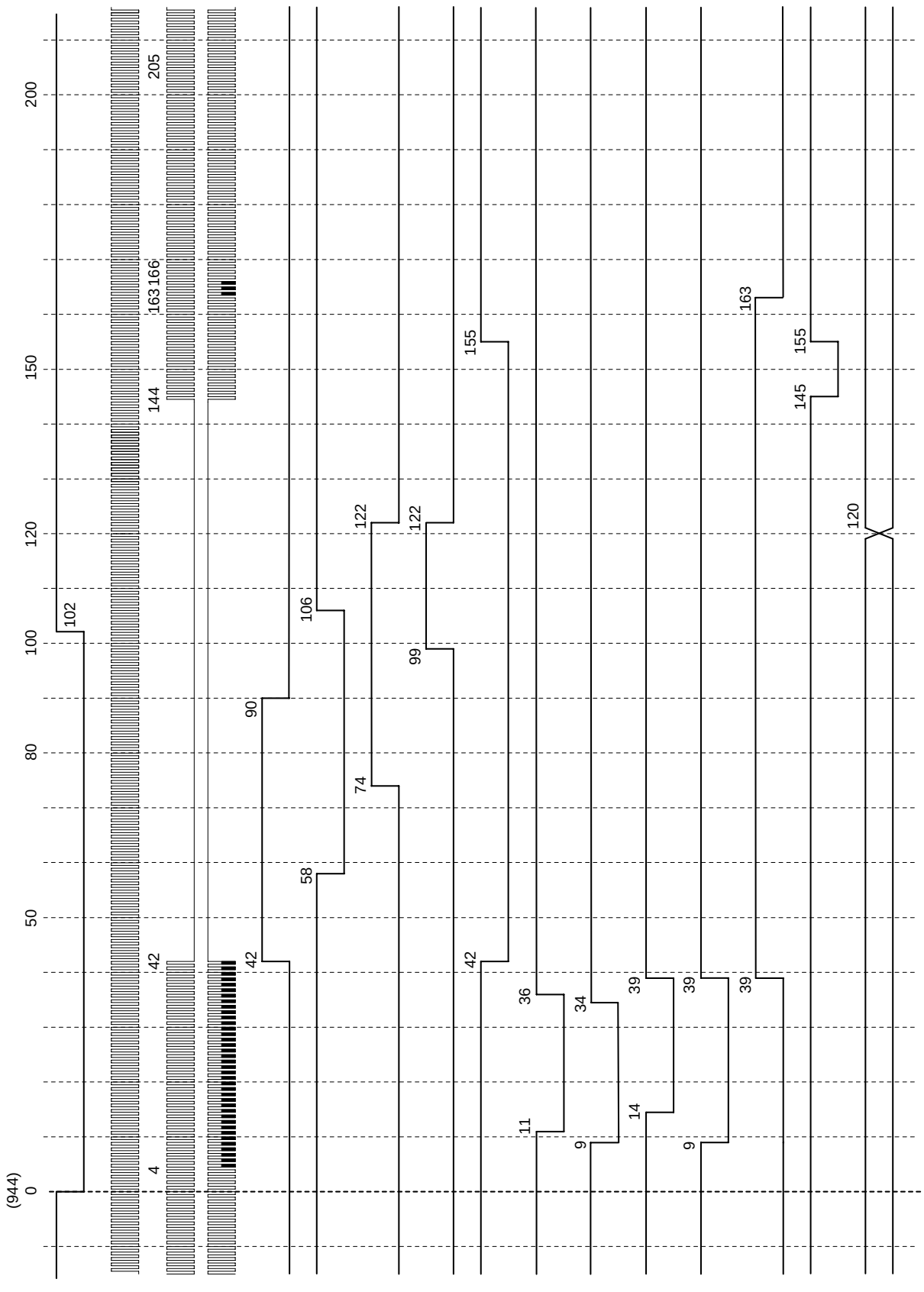
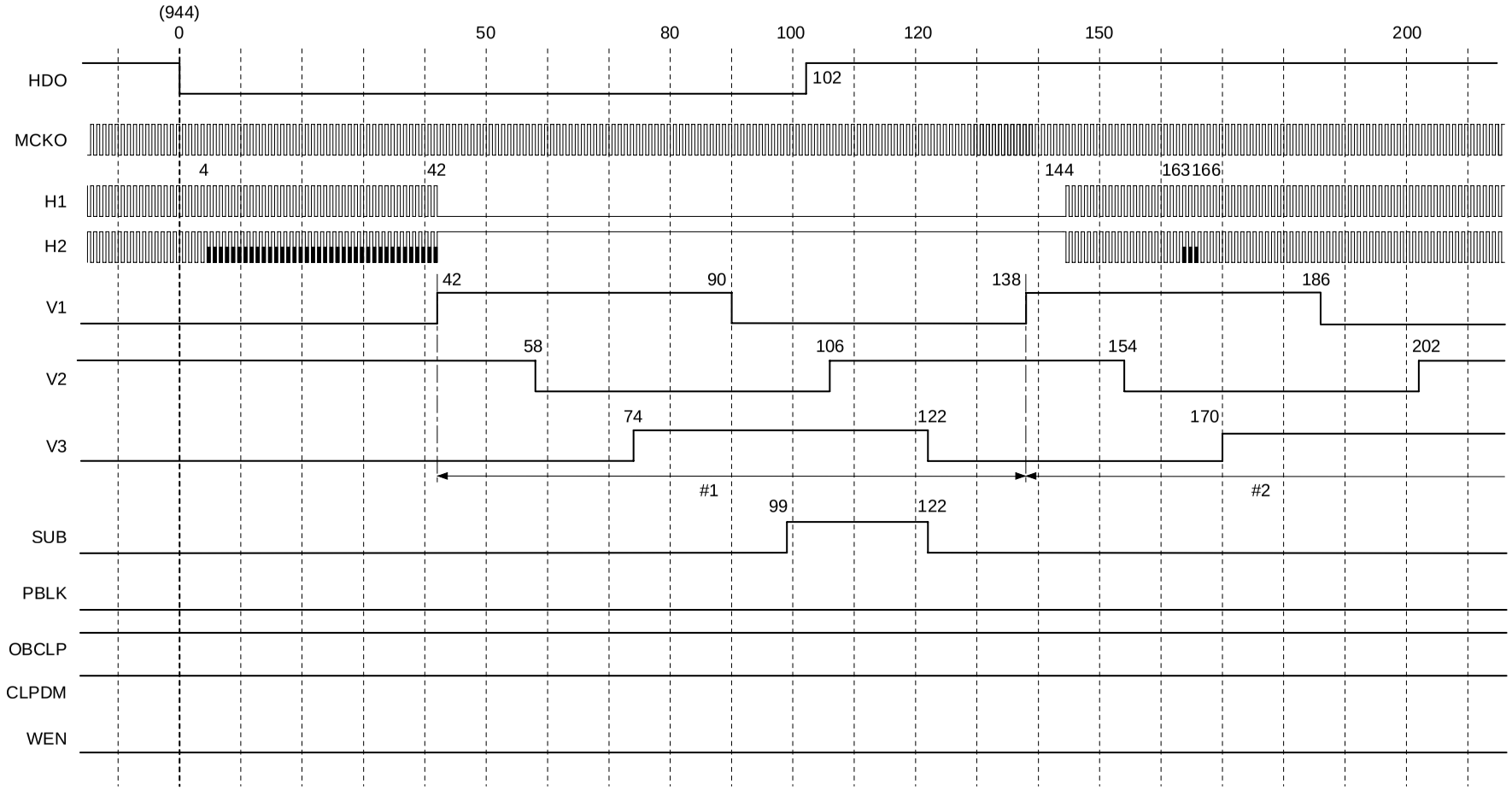


Chart-16 **Horizontal Direction Timing Chart**
(Frame shift: F)
(High speed sweeping: G)

MODE
Central Scan 1 Mode, Central Scan 2 Mode

Applicable CCD image sensor
• ICX415



	Frame Shift	High speed Sweep
Central Scan 1	#166 (17H)	#197 (20H)
Central Scan 2	#254 (26H)	#299 (31H)

Chart-17 Horizontal Direction Timing Chart

MODE
Pixel Add Mode (Interlace)

Applicable CCD image sensor
• ICX415

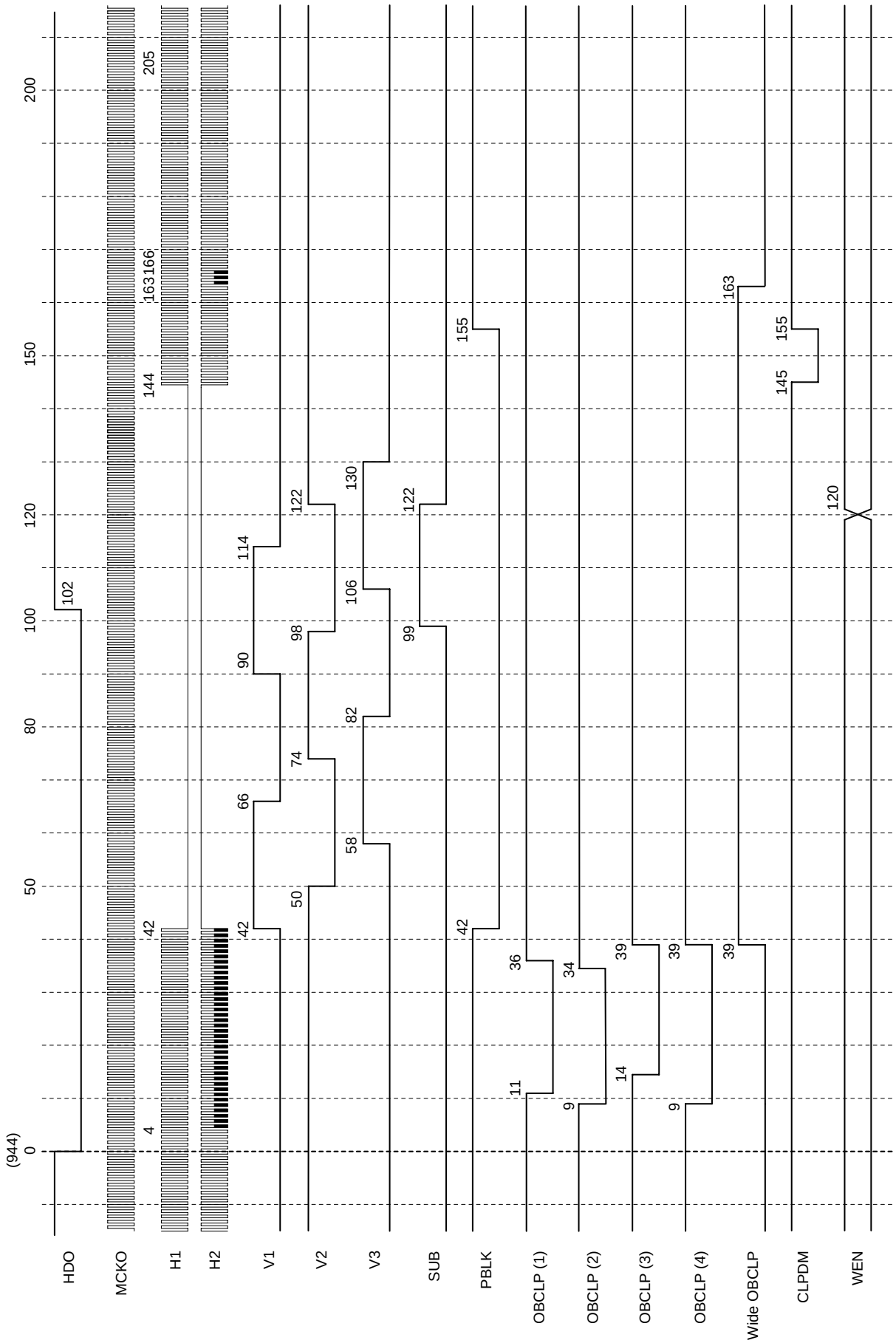


Chart-18 Horizontal Direction Timing Chart (Readout: E)

MODE
Progressive Scan Mode

Applicable CCD image sensor
• ICX415

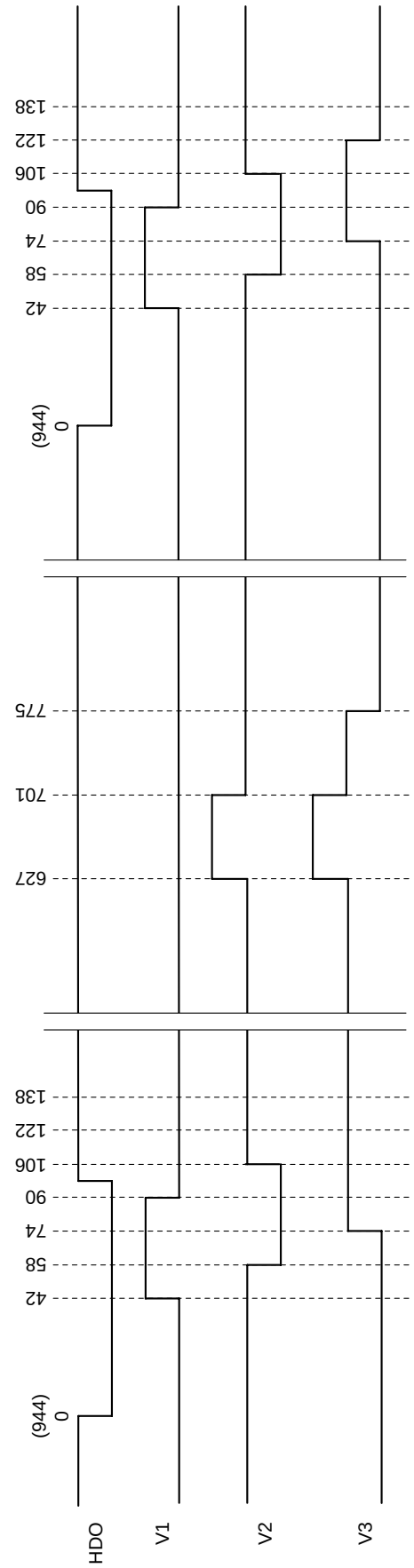


Chart-19 Horizontal Direction Timing Chart
(Readout: H)

Applicable CCD image sensor
• ICX415

MODE
Pixel Add Mode (Interlace)

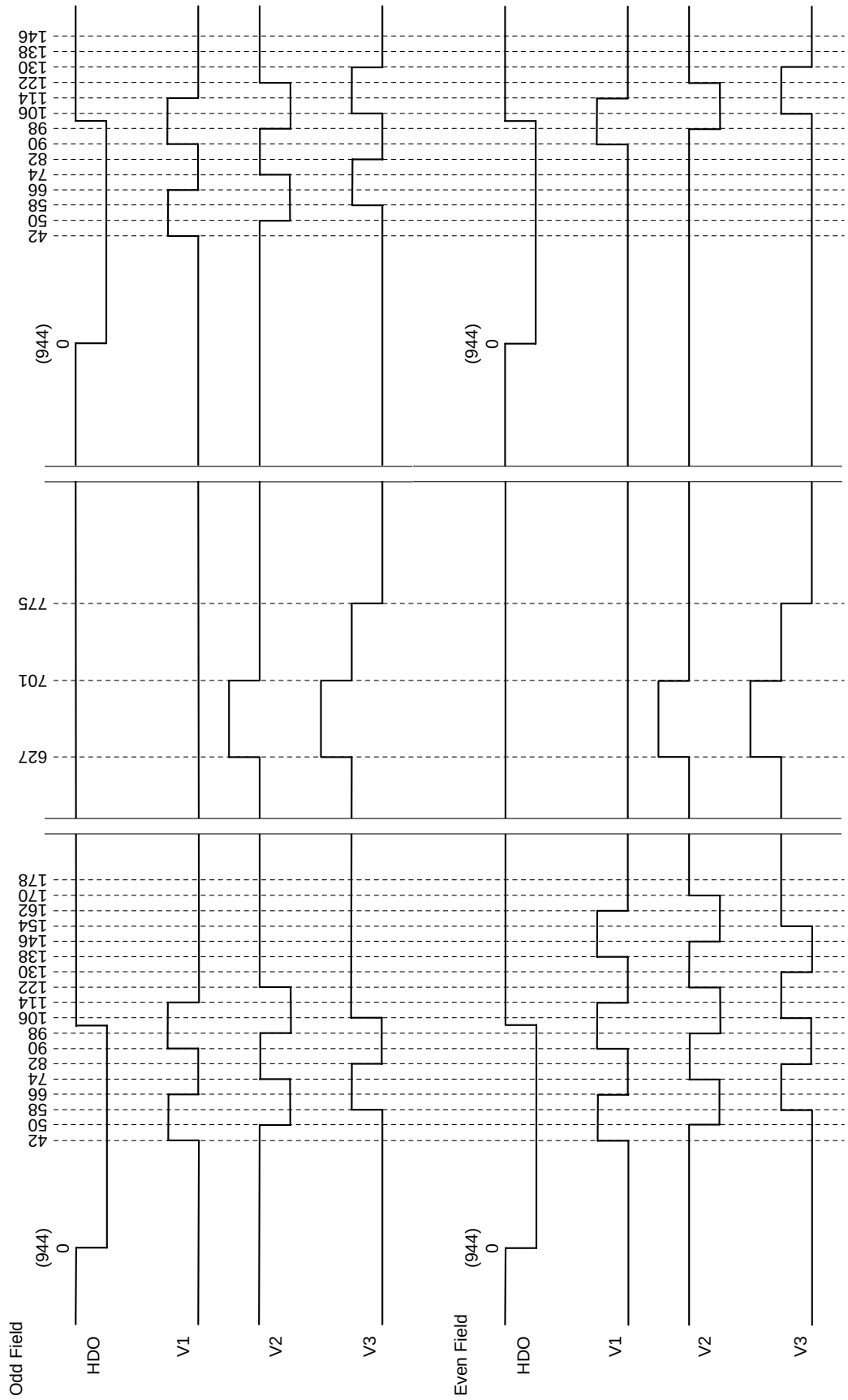
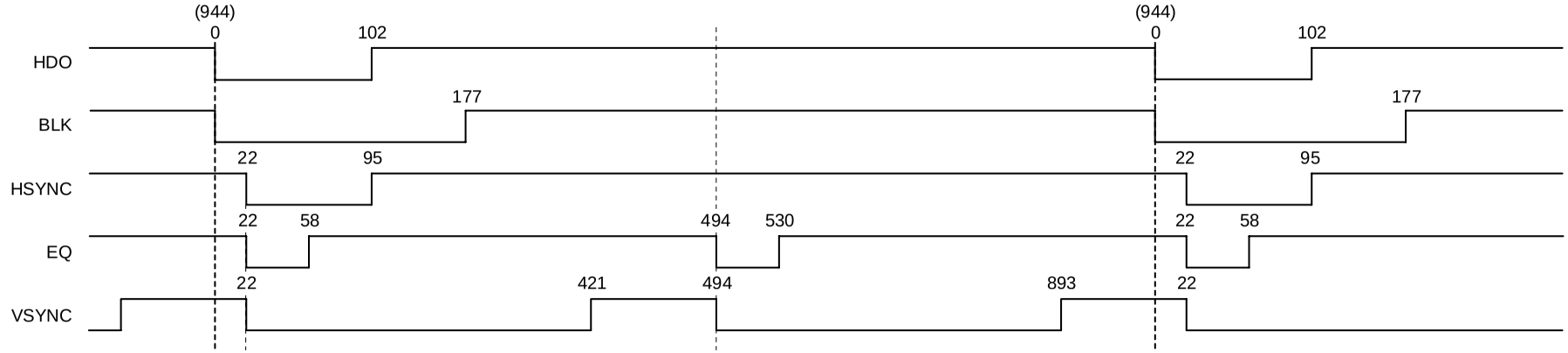


Chart-20 **Horizontal Direction Timing Chart (SSG Pulse)**

MODE
Pixel Add Mode (Interlace)

Applicable CCD image sensor
• ICX415



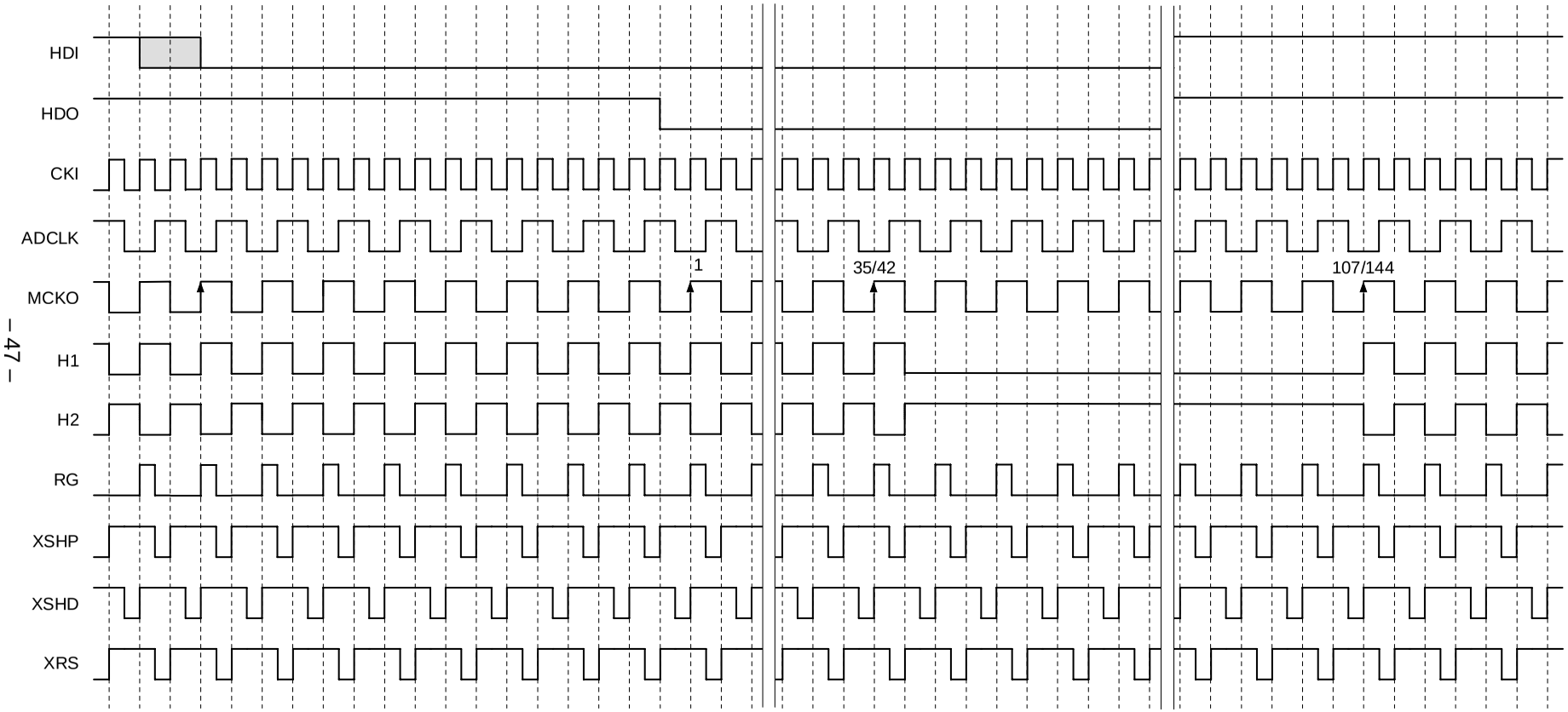
* HSYNC, EQ and VSYNC are combined and output from the SYNC pin. They are not individual pulses output externally.

Chart-21 High-Speed Phase Timing Chart

MODE

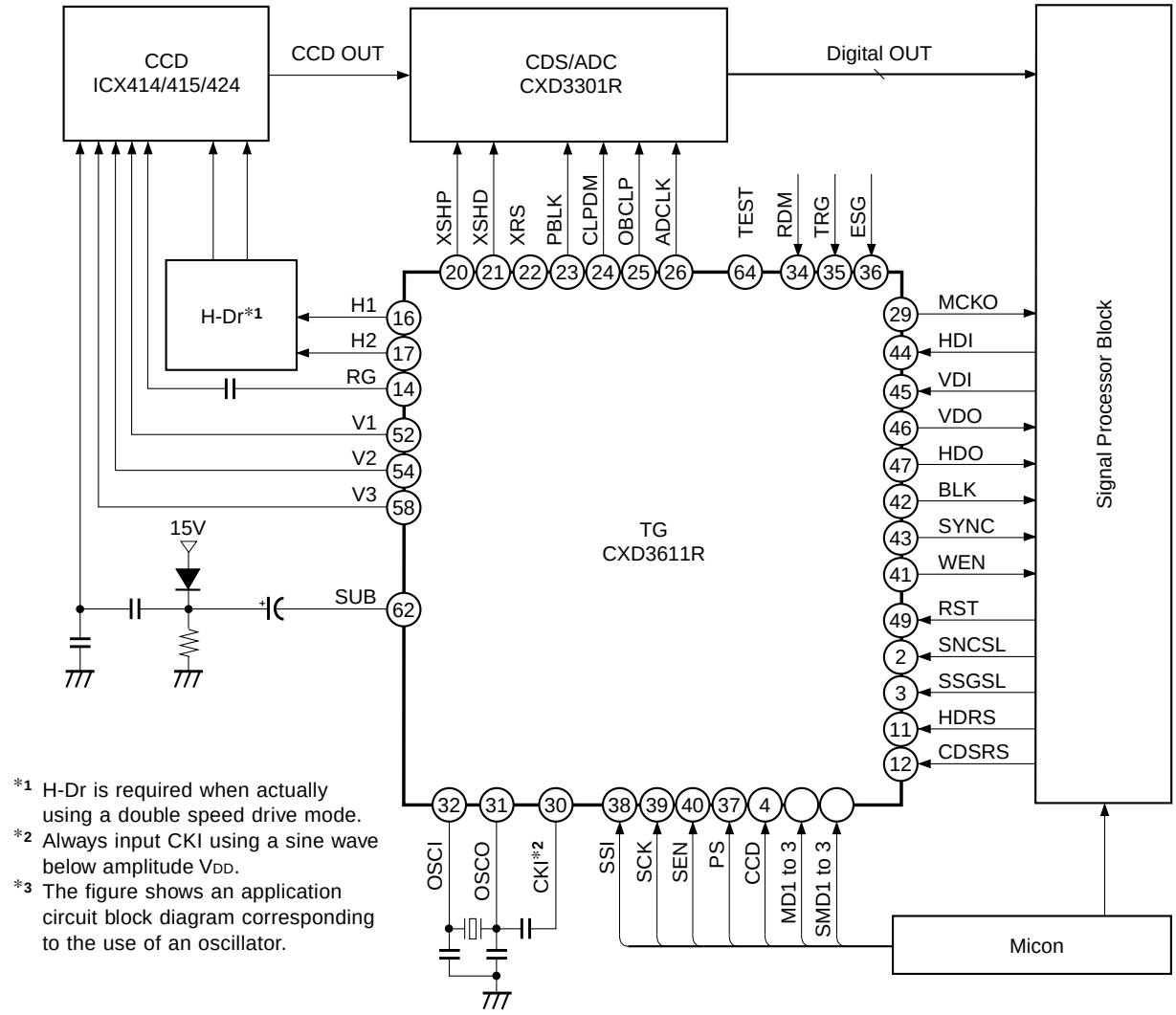
Applicable CCD image sensor

• ICX414/424/415



* HDO indicates the logical positional relationship when an H-Reset is applied to CXD3611R by HDI. The actual output requires a delay.
* The phase relationship of each pulse shows the logical position relationship. For the actual output, a delay is added to each pulse.
* The logical ADCLK can be specified by the serial interface data.
* Pin settings are in default.

Application Circuit Block Diagram

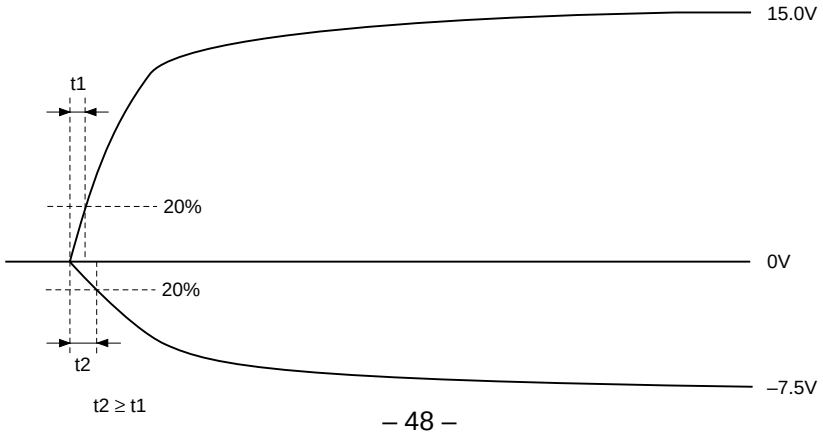


*1 H-Dr is required when actually using a double speed drive mode.
*2 Always input CKI using a sine wave below amplitude V_{DD}.
*3 The figure shows an application circuit block diagram corresponding to the use of an oscillator.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

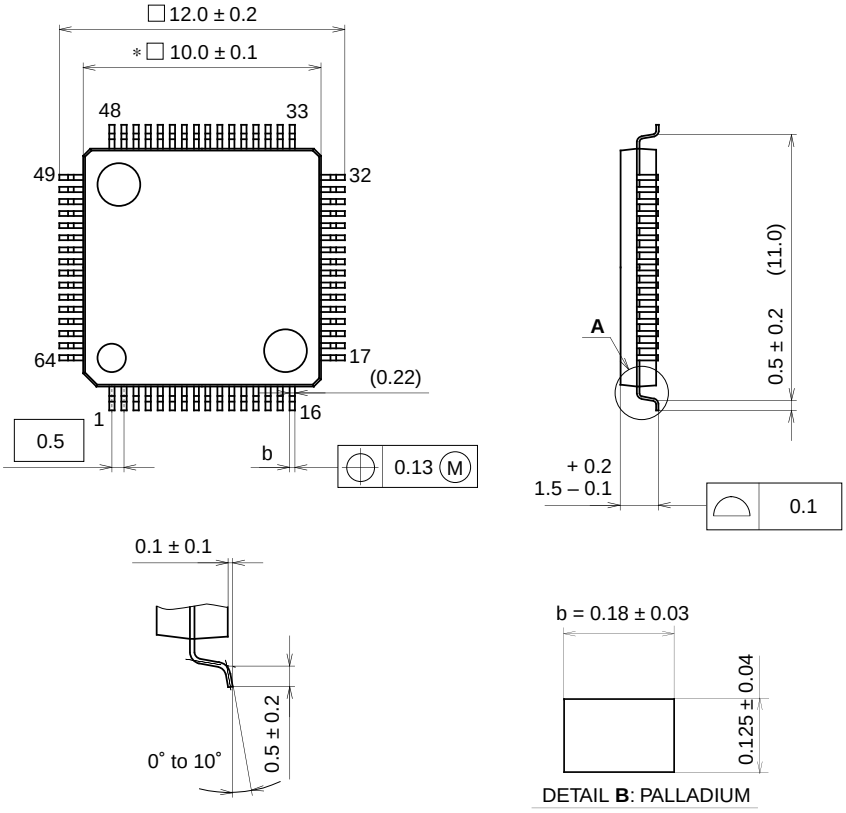
Notes on Power-on

Of the three –7.5V, +15.0V, +3.3V power supplies, be sure to start up the –7.5V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	P-LQFP64-10x10-0.5
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g