SONY

CXG1015N

Power Amplifier/Antenna Switch for PHS

Description

The CXG1015N is a power amplifier/antenna switch MMIC for PHS. This is designed using the Sony's GaAs J-FET process and operates at a single positive power supply.

Features

- Single positive power supply 3.0 V
- Output power 20.2 dBm
  (Antenna switch transfer output pin power)
- Low current consumption 160 mA
  (Output power of 20.2 dBm)
- High power gain 39 dB Typ.
  (Output power of 20.2 dBm)
- Low insertion loss 0.5 dB Typ.
- Small mold package 20-pin SSOP
  (Pin interval of 0.5 mm pitch)

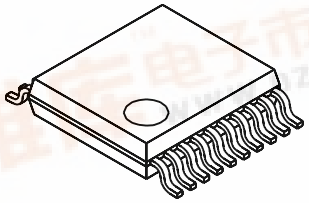
Structure

GaAs J-FET MMIC

Applications

- Power amplifiers for PHS
- Antenna switches for PHS

20 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	Vgs0	1.5	V
• Drain current	I_{DD}	550	mA
• Power dissipation	P_D	3	W
• Channel temperature	Tch	150	°C
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Electrical Characteristics

Power Amplifier + Antenna Switch Transfer Block

V_{DD}=3.0 V, V_{CTL}=2.0 V, f=1.90 GHz (Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
* Current consumption	I_{DD}		160		mA
* Gate voltage adjustment value	$V_{GG}2$	0	0.25	0.7	V
Output power (Power Amplifier + Antenna Switch Transfer Block)	P_{OUT}	20.2			dBm
* Power gain	G_P	35.5	39	42	dB
* Adjacent channel leak power ratio (600 kHz±100 kHz)	ACPR600		–59	–54	dBc

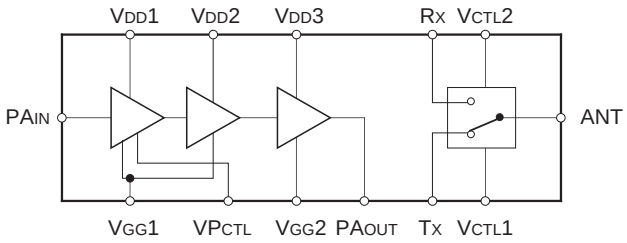
* Values where $V_{GG}1$ and $V_{GG}2$ are adjusted so that I_{DD} becomes 160 mA when the power amplifier output pin and the antenna switch transfer input pin are connected on the Sony's recommended evaluation board and the output power on the antenna switch transfer output pin is 20.2 dBm.

Antenna Switch Receive Block

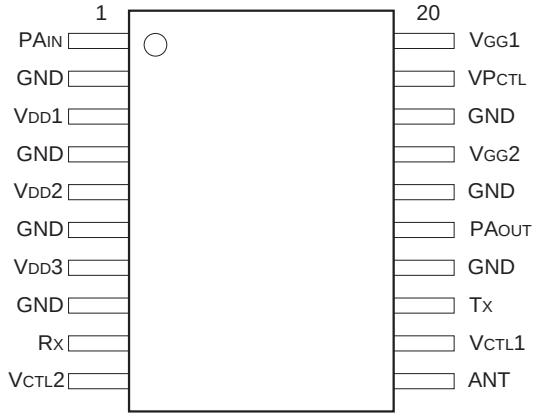
V_{CTL}(L)=0 V, V_{CTL}(H)=3.0 V (Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Insertion loss	IL		0.5	0.8	dB
Isolation	ISO	20	24		dB
Control pin current	I_{CTL}		40	100	µA

Block Diagram



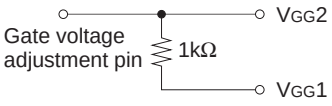
Pin Configuration



Antenna Switch Operation

VCTL1=3 V	ANT-TX	ON
VCTL2=0 V	ANT-RX	OFF
VCTL1=0 V	ANT-TX	OFF
VCTL2=3 V	ANT-RX	ON

Gate Bias Circuit of Power Amplifier Block



Recommended Current Adjustment Method

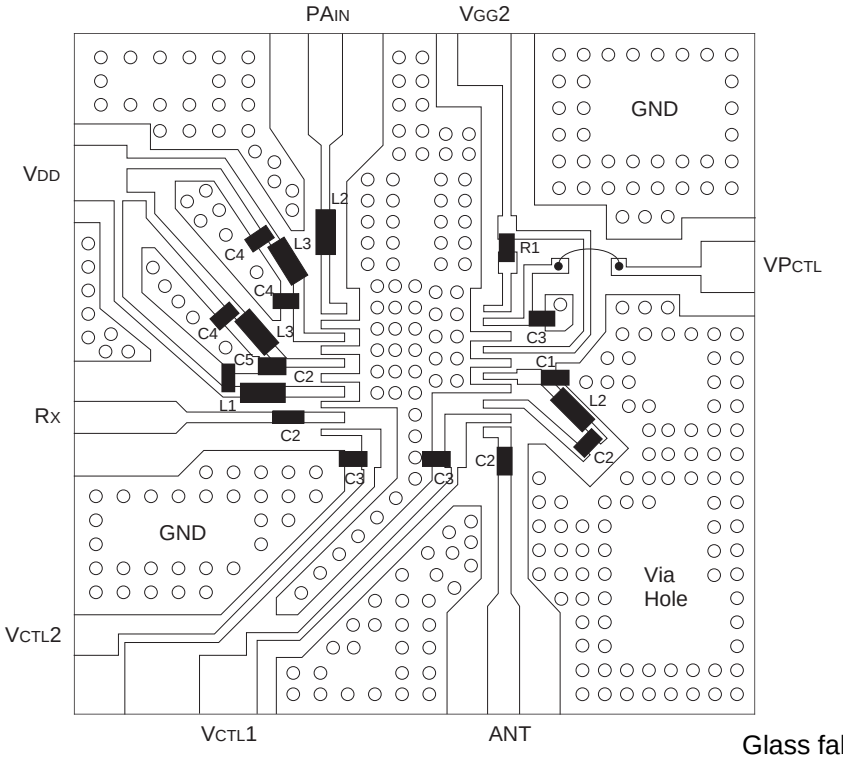
(1) VGG2/PIN separate adjustment

(VGG2 adjustment 1)	(PIN adjustment 1)	(VGG2 adjustment 2)	(PIN adjustment 2)
When the RF input (PIN) off, the current consumption (IDD) is adjusted to 160 mA.	The output power (POUT) is adjusted to 20.2 dBm.	The current consumption (IDD) is finely adjusted to 160 mA.	The output power (POUT) is finely adjusted to 20.2 dBm.
Variation of IDD and POUT due to adjustment	IDD=160±20 mA POUT=20.2 dBm	IDD=160 mA POUT=20.2±0.2 dBm	IDD=160±5 mA POUT=20.2 dBm

(2) Simple adjustment

(IDD read)	(VGG2 setting)	(PIN adjustment)
When the RF input (PIN) is off, the gate voltage (VGG2) is set to 0.4 V and IDD is read.	The formula* where VGG2=f (IDD: VGG2=0.4 V) is used to set VGG2.	The output power (POUT) is adjusted to 20.2 dBm.
	* e.g. VGG2=a-b × IDD	IDD=160±5 mA POUT=20.2 dBm

Recommended Evaluation Circuit



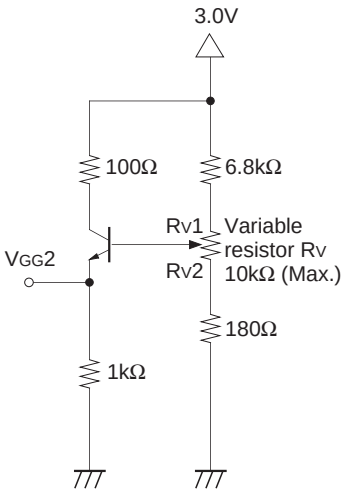
R1=1kΩ

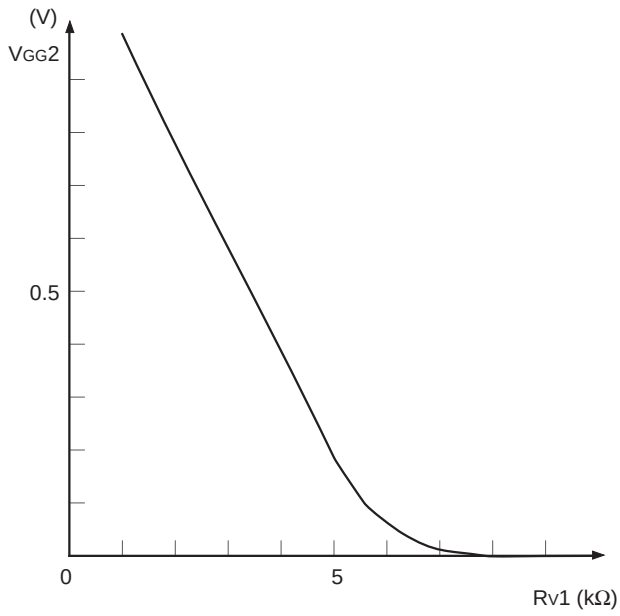
L1=1.8nH
L2=2.2nH
L3=18nH

C1=1pF
C2=30pF
C3=100pF
C4=1nF
C5=10nF

Glass fabric-base epoxy board
GND for the overall back side
Dimension : 25 mm × 25 mm
Thickness : 0.2 mm

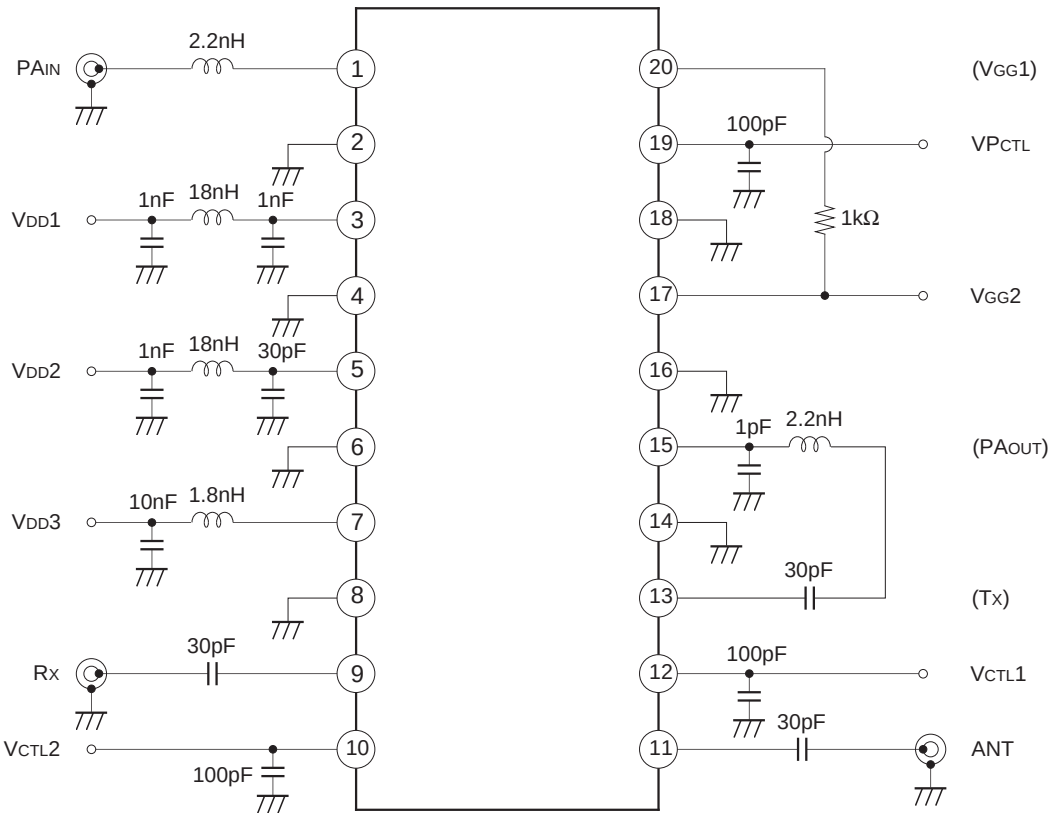
Recommended Gate Bias Circuit and Circuit Characteristics





Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

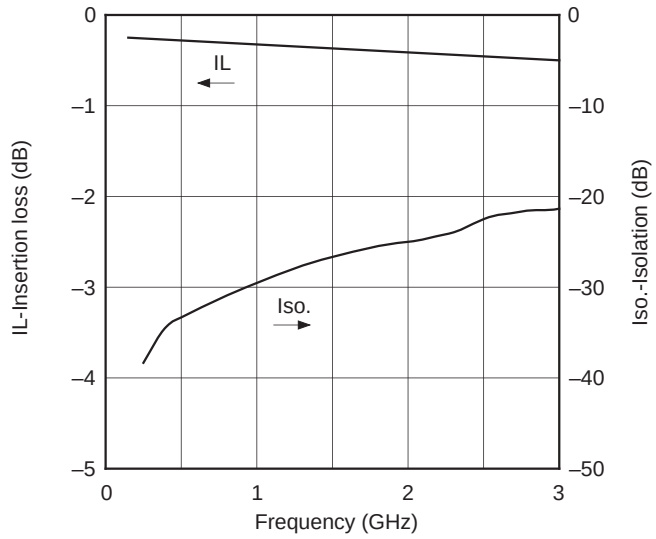
Recommended External Circuit



Example of Representative Characteristics (Ta=25 °C)

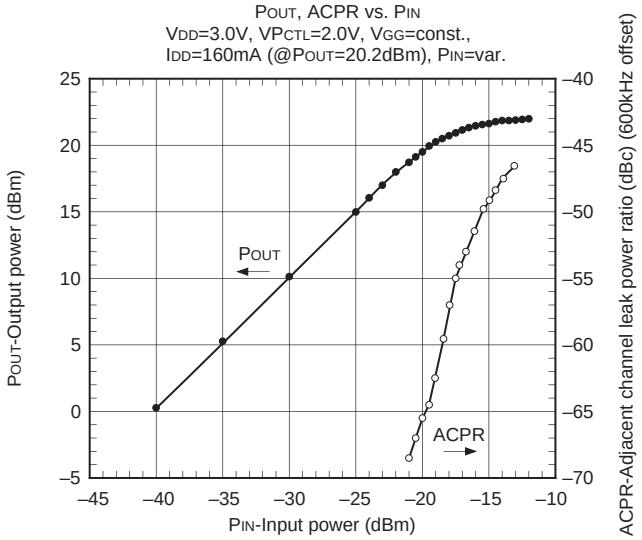
Antenna Switch Receive Block

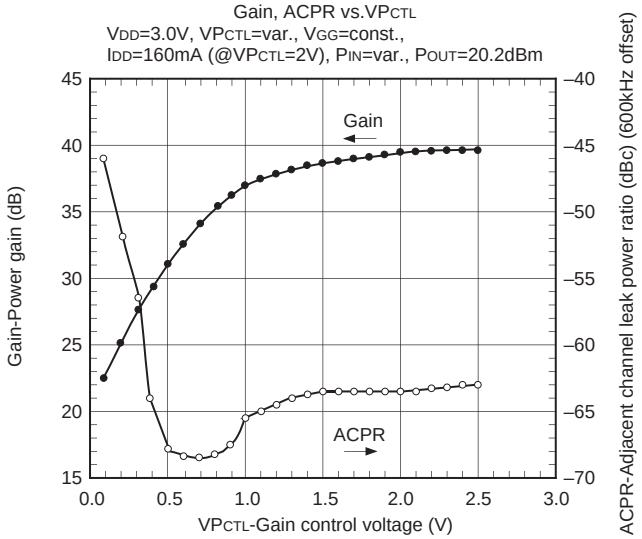
IL, Iso. vs. Freq.

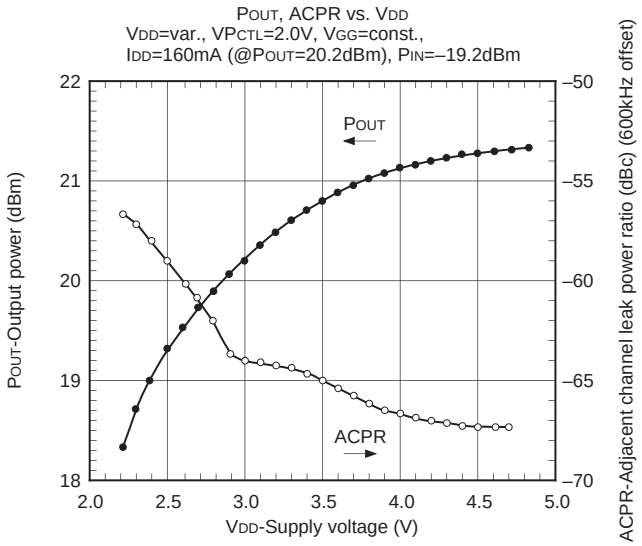


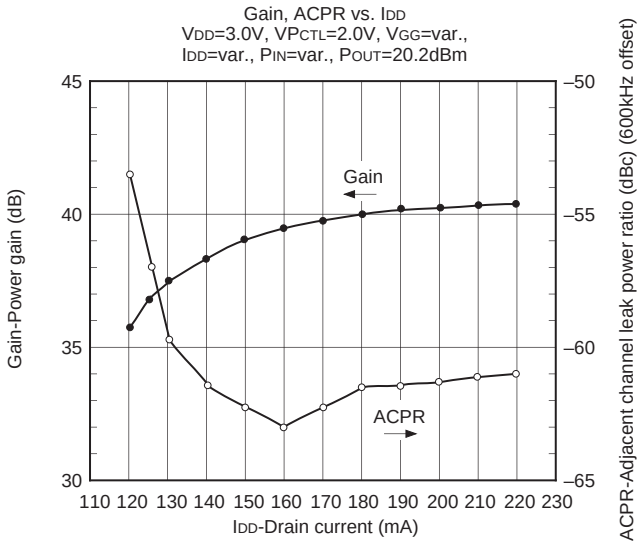
Example of Representative Characteristics

Power Amplifier + Antenna Switch Transfer Block



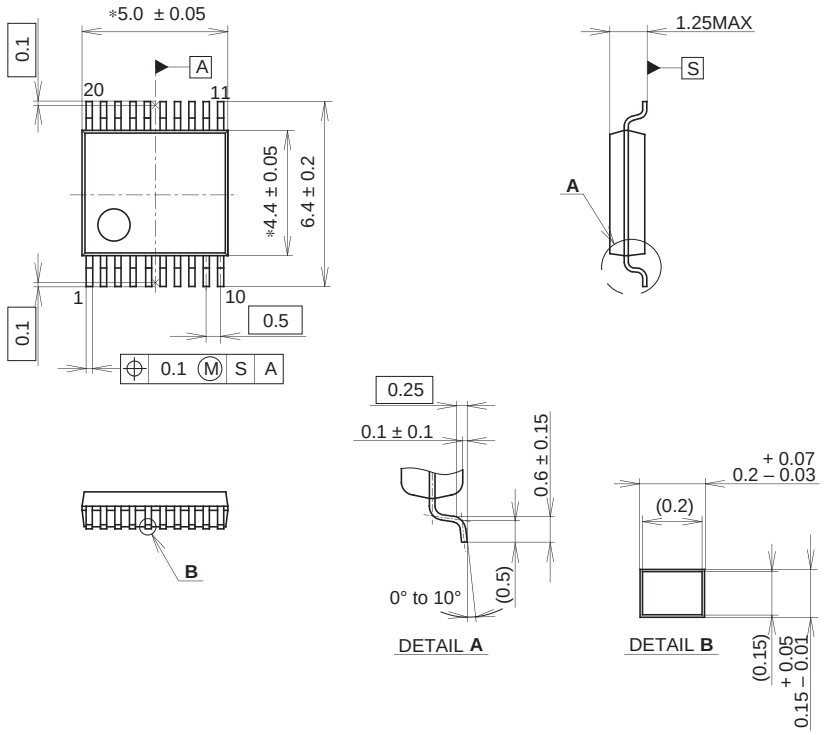






Package Outline Unit : mm

20PIN SSOP(PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L03
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g