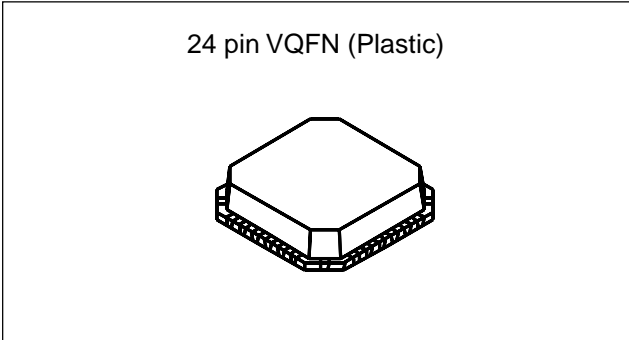


High Power 5 × 4 Antenna Switch MMIC with Integrated Control Logic for PDC Dual Phone

Description

The CXG1127ER is a high power antenna switch MMIC for PDC 800MHz and 1.5GHz dual phone. The CXG1127ER is suited to connect 2Tx/3Rx to one of 4 antennas. The CXG1127ER has on-chip logic circuit for operation with 5 CMOS inputs. The Sony's GaAs J-FET process is used for low insertion loss and low voltage operation.



Features

- Low insertion loss: 0.45dB @900MHz, 0.55dB @1.5GHz
- High linearity: Harmonic < - 65dBc
- CMOS compatible input control
- Small package: 24-pin VQFN (4.0mm × 4.0mm)

Applications

5 × 4 antenna switch for digital cellular such as PDC handsets

Structure

GaAs J-FET MMIC

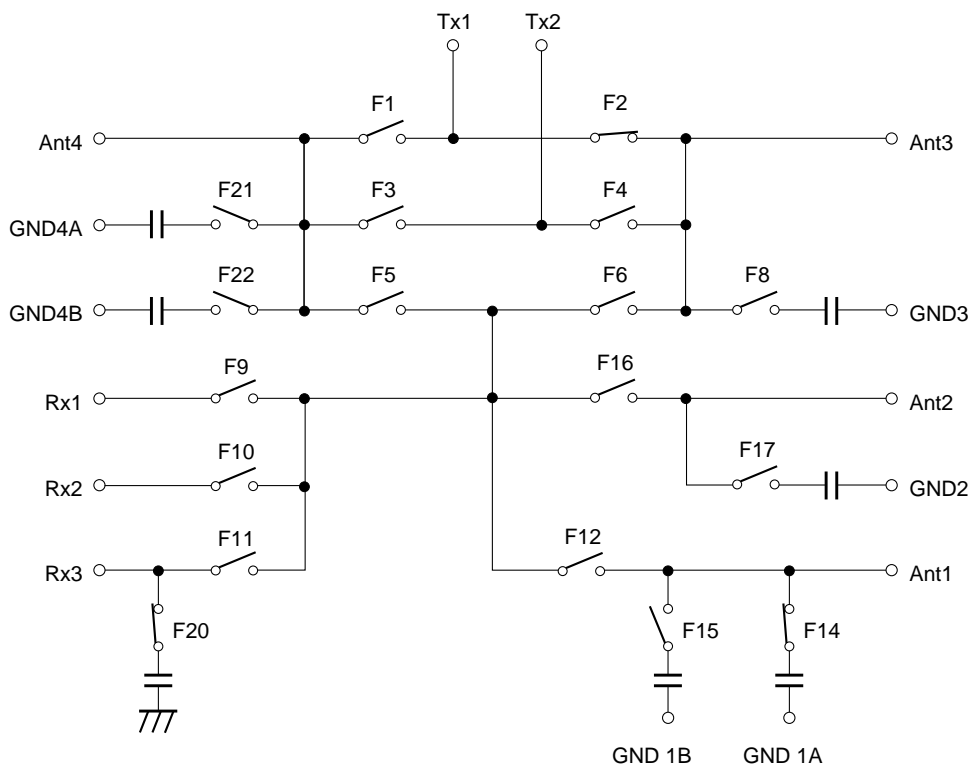
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V _{DD}	7	V
• Control voltage	V _{DD}	5	V
• Operating temperature	T _{opr}	-35 to +85	°C
• Storage temperature	T _{stg}	-65 to +150	°C

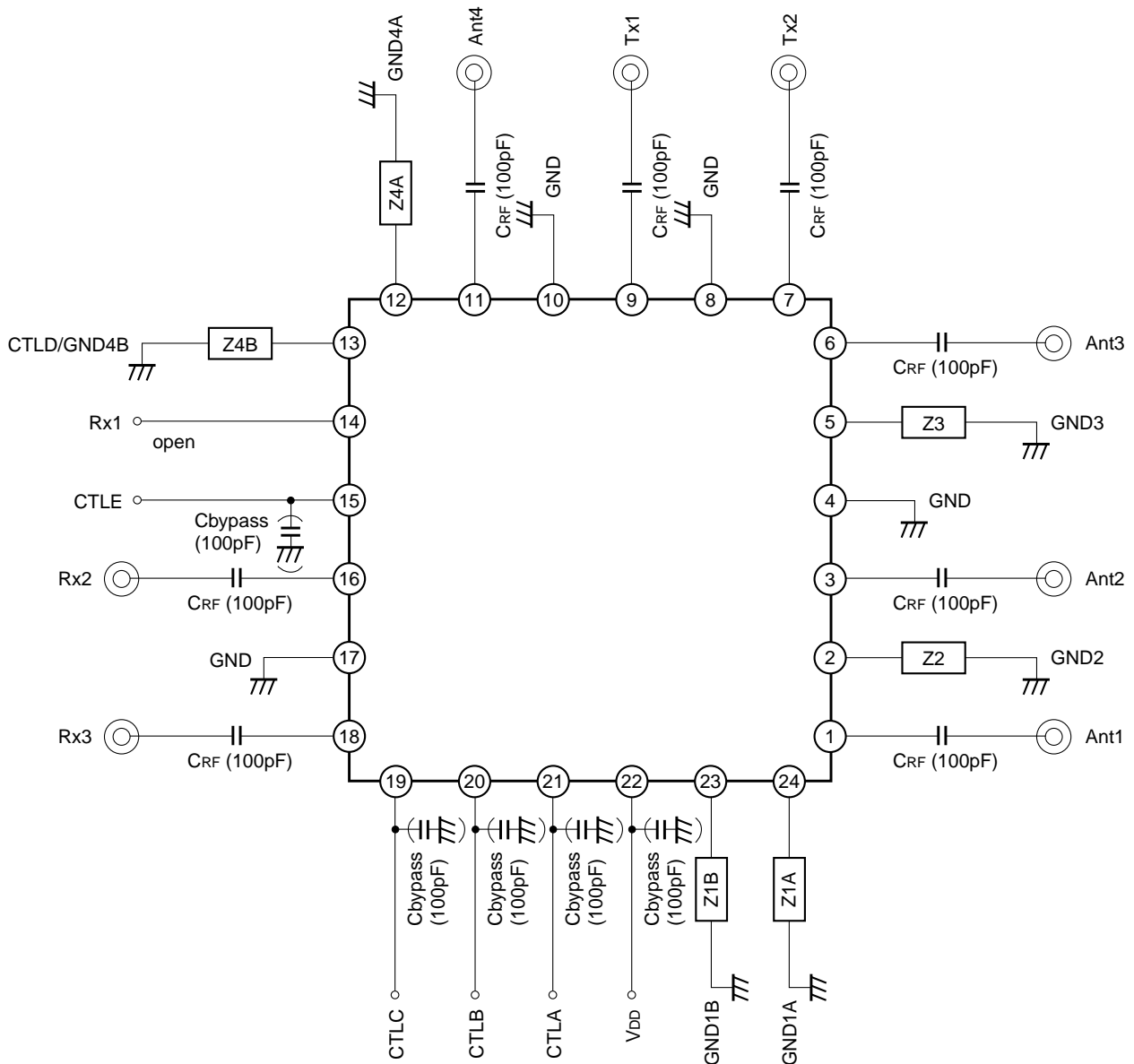
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Block Diagram



Pin Configuration/Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF de-coupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

In the case that Rx1 is not used, the processing of the pin is as follows:

- Rx1 is recommended to be open.
- CTLD/GNG4B should be grounded as a DC.

Truth Table

A: Rx/Tx

B: main/diversity

C: External/antenna

D: 800MHz digital/800MHz analog

E: 800MHz/1.5GHz

State	On Pass	A	B	C	D	E	F1	F2	F3	F4	F5	F6	F8	F9	F10	F11	F12	F14	F15	F16	F17	F20	F21	F22
1	Tx1 – Ant3	H	—	L	—	L	L	H	H	L	L	L	L	L	L	L	L	H	L	L	H	H	H	L
2	Tx1 – Ant4	H	—	H	—	L	H	L	L	H	L	L	H	L	L	L	L	H	L	L	H	H	L	L
3	Tx2 – Ant3	H	—	L	—	H	H	L	L	H	L	L	L	L	L	L	L	L	H	L	H	H	L	H
4	Tx2 – Ant4	H	—	H	—	H	L	H	H	L	L	L	H	L	L	L	L	L	H	L	H	H	L	L
5	Rx1 – Ant3	L	L	L	H	L	H	L	H	L	L	H	L	H	L	L	L	H	L	L	H	H	H	L
6	Rx2 – Ant3	L	L	L	L	L	H	L	H	L	L	H	L	L	H	L	L	H	L	L	H	H	H	L
7	Rx3 – Ant3	L	L	L	—	H	H	L	H	L	L	H	L	L	L	H	L	L	H	L	H	L	L	H
8	Rx1 – Ant4	L	L	H	H	L	L	H	L	H	H	L	H	H	L	L	L	H	L	L	H	H	L	L
9	Rx2 – Ant4	L	L	H	L	L	L	H	L	H	H	L	H	L	H	L	L	H	L	L	H	H	L	L
10	Rx3 – Ant4	L	L	H	—	H	L	H	L	H	H	L	H	L	L	H	L	L	H	L	H	L	L	L
11	Rx1 – Ant2	L	H	L	H	L	L	L	L	L	L	L	H	H	L	L	L	H	L	H	L	H	H	L
12	Rx2 – Ant2	L	H	L	L	L	L	L	L	L	L	L	H	L	H	L	L	H	L	H	L	H	H	L
13	Rx3 – Ant2	L	H	L	—	H	L	L	L	L	L	L	H	L	L	H	L	L	H	H	L	L	L	H
14	Rx1 – Ant1	L	H	H	H	L	L	L	L	L	L	L	H	H	L	L	H	L	L	L	H	H	H	L
15	Rx2 – Ant1	L	H	H	L	L	L	L	L	L	L	L	H	L	H	L	H	L	L	L	H	H	H	L
16	Rx3 – Ant1	L	H	H	—	H	L	L	L	L	L	L	H	L	L	H	H	L	L	L	H	L	L	H

DC Bias Condition

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
V _{DD}	2.4	3.0	3.3	V
V _{ctl} (H)	2.0	3.0	3.3	V
V _{ctl} (L)	0		0.4	V

Electrical Characteristics

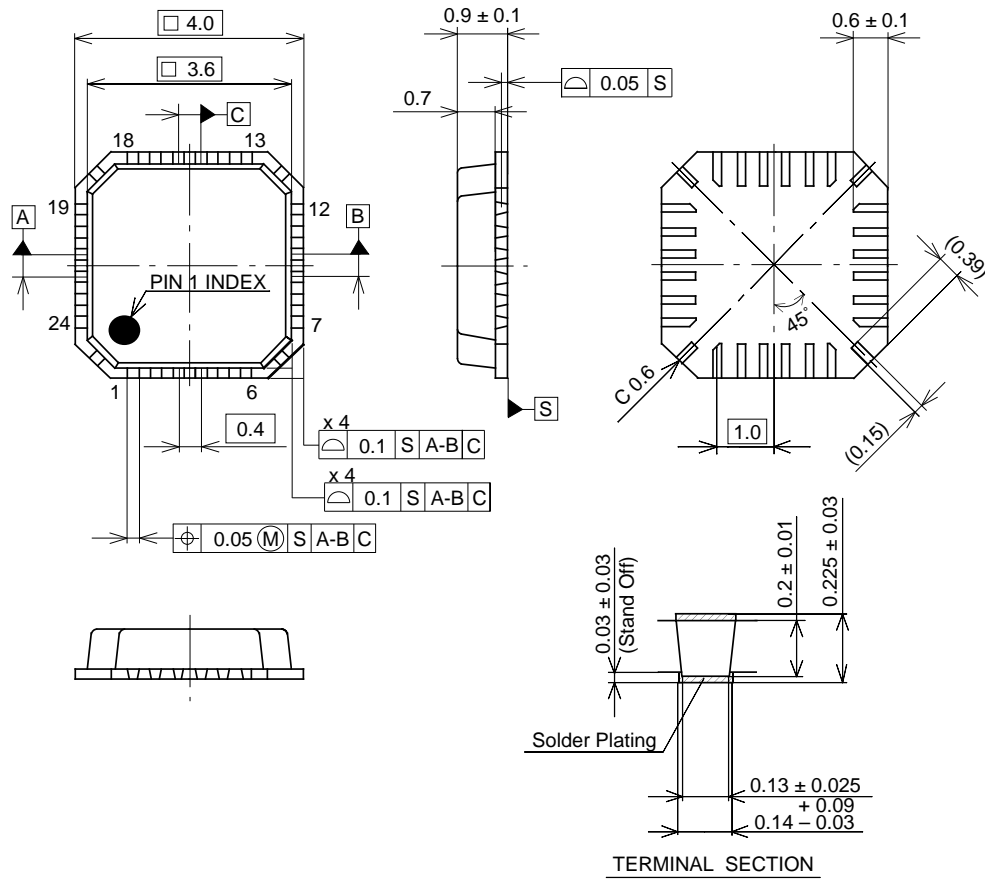
(Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx1 – Ant3	*1	—	0.45	0.75	dB
		Tx1 – Ant4	*1	—	0.45	0.75	dB
		Tx2 – Ant3	*2	—	0.55	0.85	dB
		Tx2 – Ant4	*2	—	0.55	0.85	dB
		Rx2 – Ant3	*3	—	0.85	1.15	dB
		Rx2 – Ant4	*3	—	0.90	1.20	dB
		Rx2 – Ant2	*3	—	0.65	0.95	dB
		Rx2 – Ant1	*3	—	0.65	0.95	dB
		Rx3 – Ant3	*4	—	1.10	1.40	dB
		Rx3 – Ant4	*4	—	1.15	1.45	dB
		Rx3 – Ant2	*4	—	0.80	1.10	dB
		Rx3 – Ant1	*4	—	0.80	1.10	dB
Harmonics	2fo	Tx1 – Ant3	*5	—	-75	-60	dBc
		Tx1 – Ant4	*5	—	-75	-60	dBc
		Tx2 – Ant3	*6	—	-75	-60	dBc
		Tx2 – Ant4	*6	—	-75	-60	dBc
	3fo	Tx1 – Ant3	*5	—	-70	-60	dBc
		Tx1 – Ant4	*5	—	-70	-60	dBc
		Tx2 – Ant3	*6	—	-70	-60	dBc
		Tx2 – Ant4	*6	—	-70	-60	dBc
ACP	±50kHz	Tx1 – Ant3	*5	—	-67	-57	dBc
		Tx1 – Ant4	*5	—	-67	-57	dBc
		Tx2 – Ant3	*6	—	-67	-57	dBc
		Tx2 – Ant4	*6	—	-67	-57	dBc
	±100kHz	Tx1 – Ant3	*5	—	-73	-65	dBc
		Tx1 – Ant4	*5	—	-73	-65	dBc
		Tx2 – Ant3	*6	—	-73	-65	dBc
		Tx2 – Ant4	*6	—	-73	-65	dBc
P1dB	P1dB	Tx1 – Ant3	V _{DD} = 3V	33	34	—	dBm
		Tx1 – Ant4	V _{DD} = 3V	33	34	—	dBm
		Tx2 – Ant3	V _{DD} = 3V	33	34	—	dBm
		Tx2 – Ant4	V _{DD} = 3V	33	34	—	dBm
Switching speed	TSW			—	2	—	μs
Bias current	I _{DD}		V _{DD} = 3.0V	—	0.8	1.2	mA
Control current	I _{ctl}		V _{ctl} (H) = 3V	—	30	70	μA

-
- *1 Pin = 29.5dBm, 0/3V control, $V_{DD} = 3.0V$, 889MHz to 960MHz
 - *2 Pin = 29.5dBm, 0/3V control, $V_{DD} = 3.0V$, 1,439MHz to 1,443MHz
 - *3 Pin = 10dBm, 0/3V control, $V_{DD} = 3.0V$, 810MHz to 885MHz
 - *4 Pin = 10dBm, 0/3V control, $V_{DD} = 3.0V$, 1,487MHz to 1,491MHz
 - *5 $\pi/4$ -shifted DQPSK, Pin = 29.5dBm, 0/3V control, $V_{DD} = 3.0V$, 889MHz to 960MHz,
ACP ($\pm 50kHz$) < -70dBc, ACP ($\pm 100kHz$) < -75dBc, 2nd harmonics < -75dBc, 3rd harmonics < -75dBc
 - *6 $\pi/4$ -shifted DQPSK, Pin = 29.5dBm, 0/3V control, $V_{DD} = 3.0V$, 1,439MHz to 1,443MHz,
ACP ($\pm 50kHz$) < -70dBc, ACP ($\pm 100kHz$) < -75dBc, 2nd harmonics < -75dBc, 3rd harmonics < -75dBc
- * Rx1 is open for all conditions.

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-03
EIAJ CODE	_____
JEDEC CODE	_____

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm