

**SONY**

# CXK582000TM/YM/M -85LL/10LL

## 262144-word × 8-bit High Speed CMOS Static RAM *Preliminary*

### Description

The CXK582000TM/YM/M is a high speed CMOS static RAM organized as 262144-words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption and high speed and board package line-up.

The CXK582000TM/YM/M is a suitable RAM for portable equipment with battery back up.

### Features

- Fast access time (Access time)
  - 85LL 85ns (Max.)
  - 10LL 100ns (Max.)
- Low standby current 40μA (Max.)
- Low data retention current 24μA (Max.)
- Single +5V supply: 4.5V to 5.5V.
- Low voltage data retention : 2.0V (Min.)
- Broad package line-up

CXK582000TM/YM	8mm × 20mm 32 pin TSOP Package
CXK582000M	525mil 32 pin SOP Package

### Function

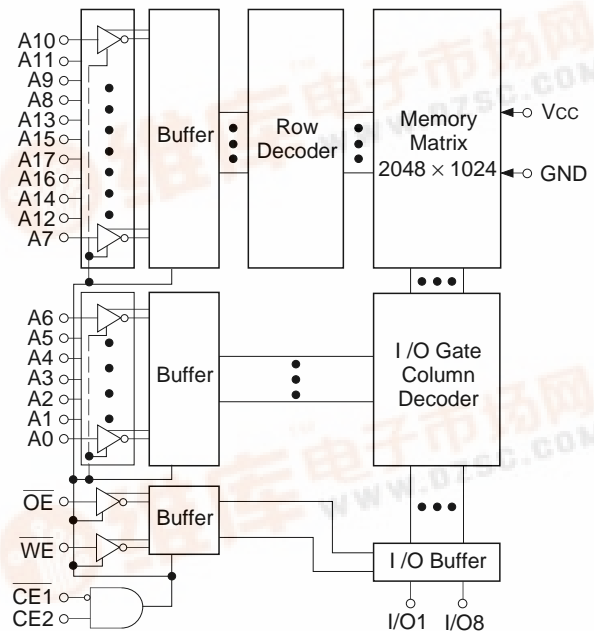
262144 word x 8 bit static RAM

### Structure

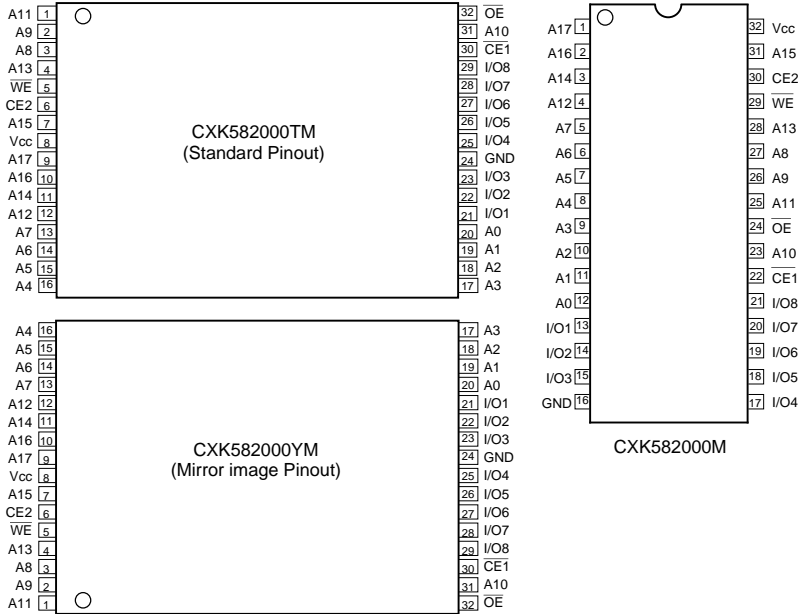
Silicon gate CMOS IC



### Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$ , $\overline{CE2}$	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\* V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	ISB1, ISB2
×	L	×	×	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	×	L	Write	Data in	Icc1, Icc2, Icc3

×: "H" or "L"

**DC Recommended Operating Conditions** (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

**• DC Characteristics**

(V<sub>CC</sub> = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE1} = V_{IL}$ , $\overline{CE2} = V_{IH}$ V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA	—	7	15	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100% I <sub>OUT</sub> = 0mA	-85LLX	—	45	80	mA
			-10LLX	—	40	70	
	I <sub>CC3</sub>	Cycle time 1μs duty = 100% I <sub>OUT</sub> = 0mA $\overline{CE1} \leq 0.2V$ $\overline{CE2} \geq V_{CC} - 0.2V$ V <sub>IL</sub> ≤ 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	—	12	24	mA	
Standby current	I <sub>SB1</sub>	$\overline{CE2} \leq 0.2V$ or $\left\{ \begin{array}{l} \overline{CE1} \geq V_{CC} - 0.2V \\ \overline{CE2} \geq V_{CC} - 0.2V \end{array} \right.$	0 to +70°C	—	—	40	μA
			0 to +40°C	—	—	8	
			+25°C	—	1.4	4	
	I <sub>SB2</sub>	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$	—	0.6	3	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.0mA	—	—	0.4	V	

\* V<sub>CC</sub> = 5V, Ta = 25°C

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

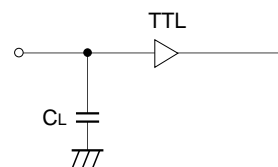
Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	7	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	8	pF

**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

• **AC test conditions** (V<sub>CC</sub> = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V <sub>IH</sub> = 2.2V
Input pulse low level	V <sub>IL</sub> = 0.8V
Input rise time	t <sub>r</sub> = 5ns
Input fall time	t <sub>f</sub> = 5ns
Input and output reference level	1.5V
Output load conditions	C <sub>L</sub> * = 100pF, 1TTL



\* C<sub>L</sub> includes scope and jig capacitances.

• Read cycle ( $\overline{WE} = "H"$ )

(Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	85	—	100	ns
Chip enable access time ( $\overline{CE1}$ )	t <sub>CO1</sub>	—	85	—	100	ns
Chip enable access time (CE2)	t <sub>CO2</sub>	—	85	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	45	—	50	ns
Output hold from address change	t <sub>OH</sub>	15	—	15	—	ns
Chip enable to output in low Z ( $\overline{CE1}$ , CE2)	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE1}$ , CE2)	t <sub>HZ1</sub> , t <sub>HZ2</sub> *	—	25	—	35	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	—	25	—	35	ns

\* t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

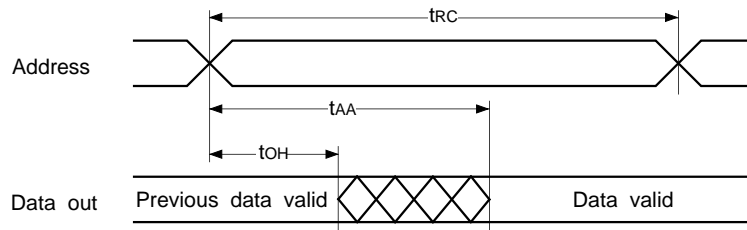
(Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	65	—	70	—	ns
Chip enable to end of write	t <sub>CW</sub>	65	—	70	—	ns
Data to write time overlap	t <sub>DW</sub>	35	—	45	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	5	—	5	—	ns
Write recovery time ( $\overline{CE1}$ , CE2)	t <sub>WR1</sub>	5	—	5	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	—	25	—	30	ns

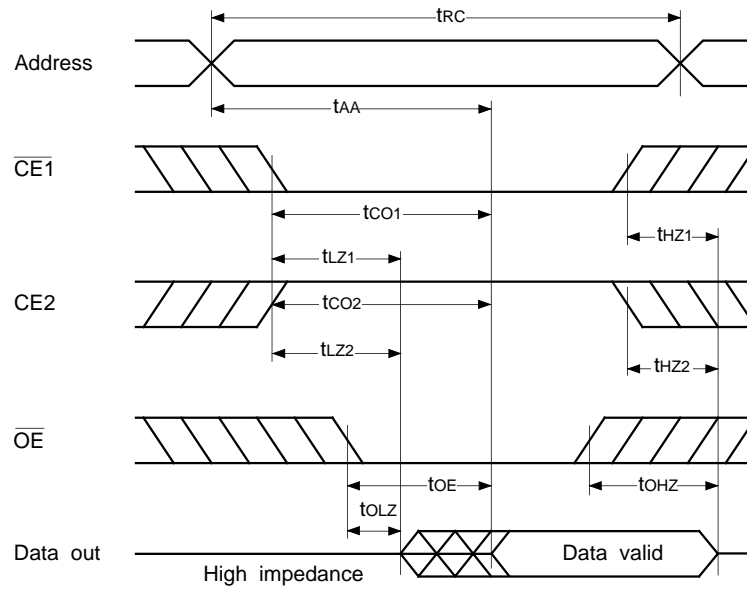
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

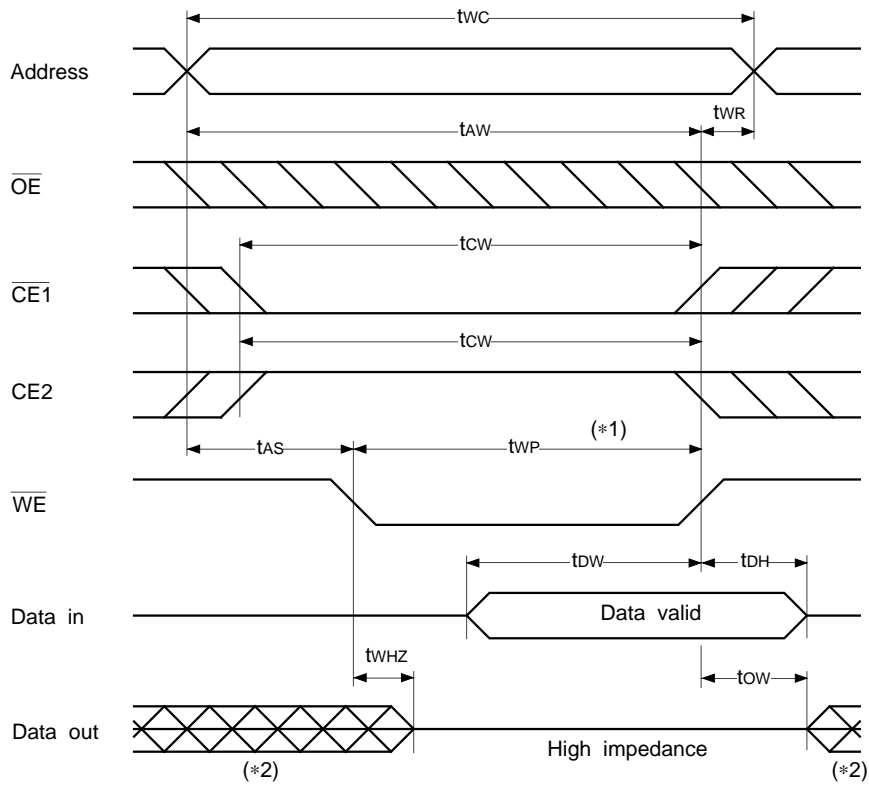
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



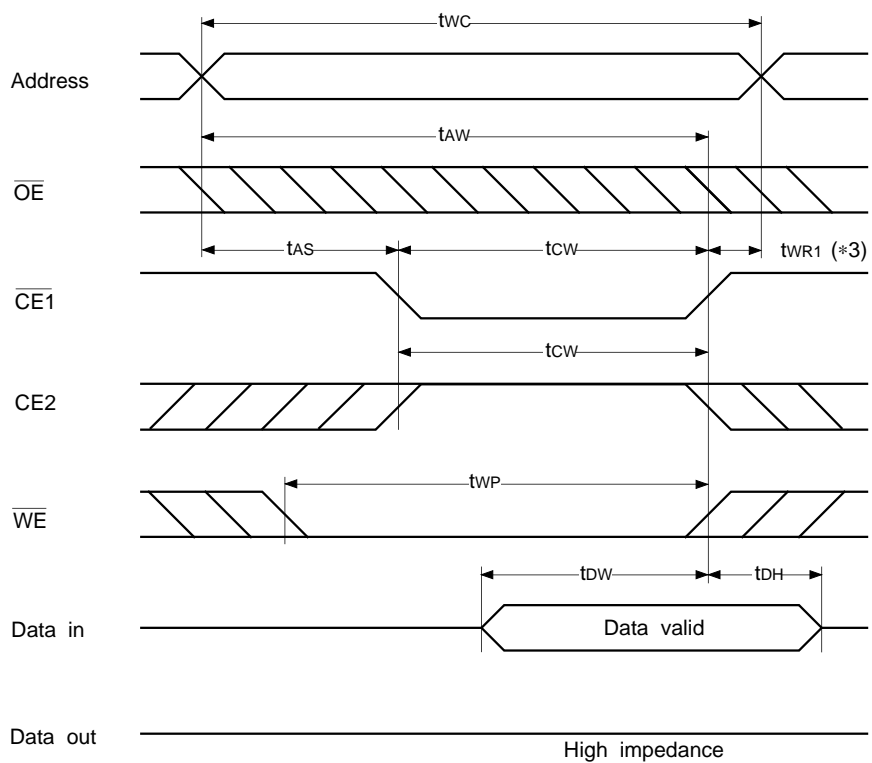
- Read cycle (2) :  $\overline{WE} = V_{IH}$



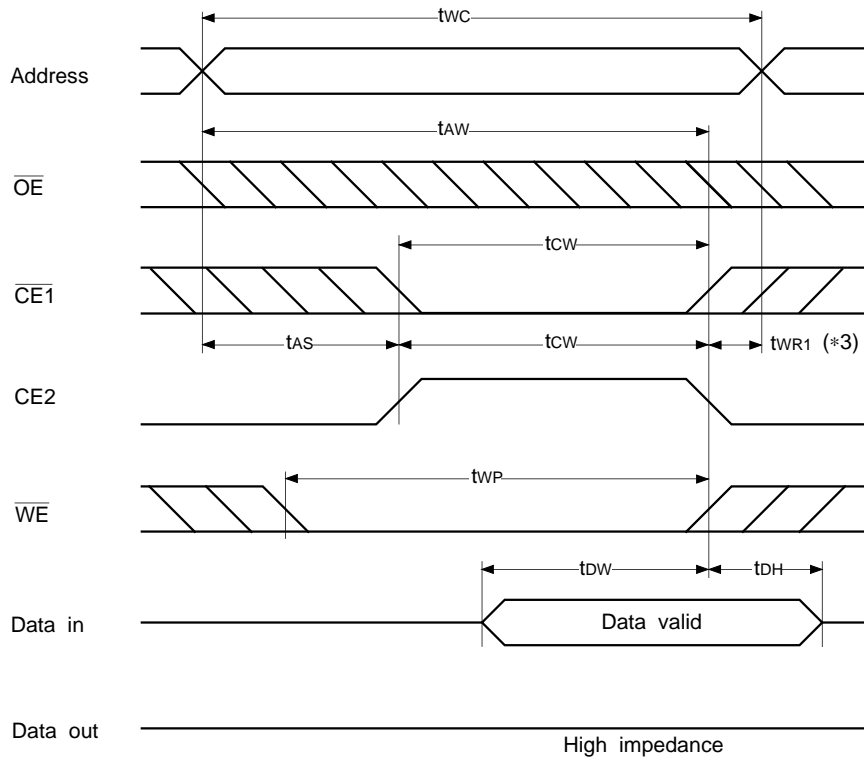
• Write cycle (1) :  $\overline{\text{WE}}$  control



• Write cycle (2) :  $\overline{\text{CE1}}$  control



• Write cycle (3) : CE2 control

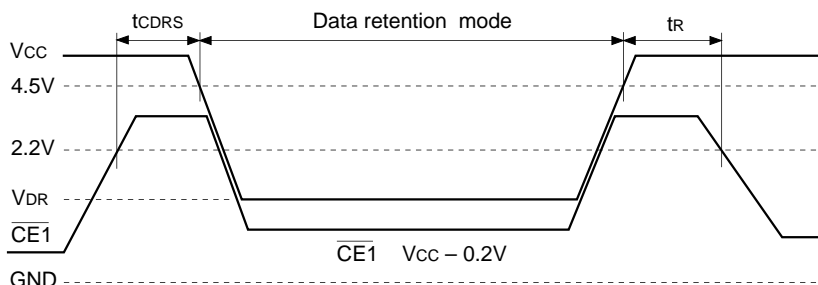


- \*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and  $\overline{CE2}$  is at high simultaneously.
- \*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- \*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of  $\overline{CE2}$ , whichever comes earlier, until the end of the write cycle.

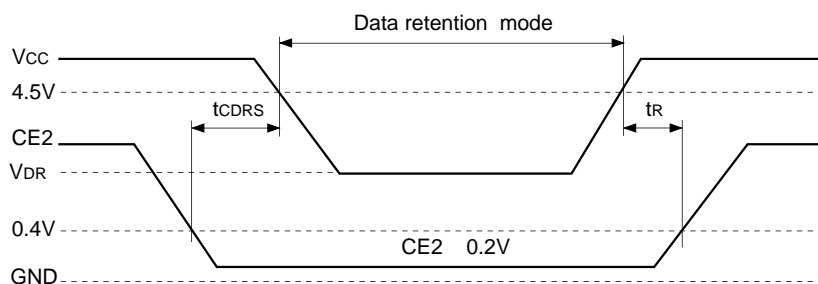


**Data retention waveform**

- Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)



- Low supply voltage data retention waveform (2) (CE2 control)



**Data Retention Characteristics**

(Ta = 0 to +70°C)

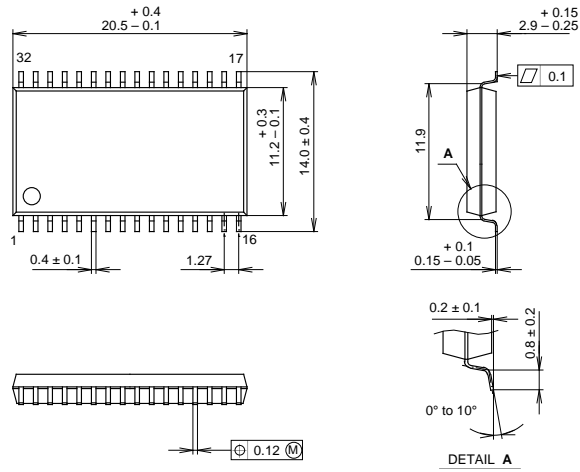
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	VDR	*	2.0	—	5.5	V	
Data retention current	ICCDR1	VCC = 3.0V*1	0 to +70°C	—	—	24	μA
			0 to +40°C	—	—	4.8	
			+25°C	—	0.8	2.4	
	ICCDR2	VCC = 2.0 to 5.5V*	—	1.4	40	μA	
Data retention setup time	tCDRS	Chip disable to data retention mode	0	—	—	ns	
Recovery time	tr		5	—	—	ms	

\*  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  (CE2 control)



CXK582000M

32PIN SOP (PLASTIC) 525mil



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	+SOP032-P-0525-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____