SONY

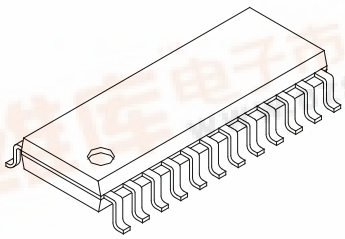
CXL1511M

CCD Delay Line for PAL

Description

The CXL1511M is an IC developed for use in conjunction with Y/C signal processing ICs for PAL. This CCD delay line provides the comb filter output for eliminating the chrominance signal cross talk and 1H delay output for luminance signals.

24 pin SOP (Plastic)



Features

- Single power supply (5V)
- Built-in triplex progression PLL circuit
- Comb filter characteristics selectable
- Delay time for 1H delay output selectable
- Built-in peripheral circuits
- Positive phase signal input, positive phase signal output

Functions

- Comb filter output
- 1H delay output for luminance signal
- Clock driver
- Autobias circuit
- Input clamp circuit (for luminance signals)
- Center bias circuit (for chrominance signals)
- Sample-and-hold circuit
- Triplex progression PLL circuit
- Luminance signal delay time/comb filter characteristics selection circuit
- Clock buffer output circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Voltage (Ta = 25°C)

V_{DD} 5V ± 5%

Structure

CMOS-CCD

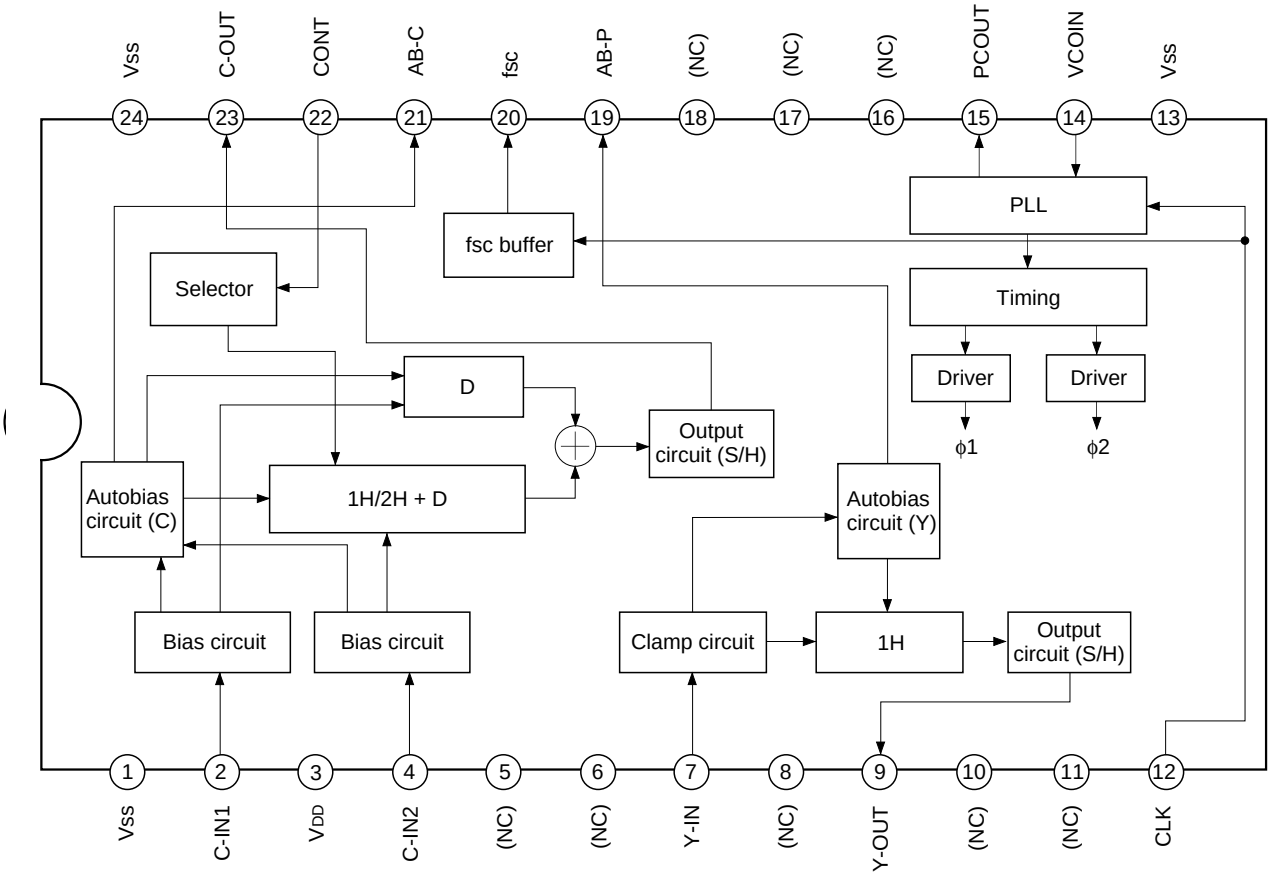
Recommended Clock Conditions (Ta = 25°C)

- Input clock amplitude V_{CLK} 0.3Vp-p to 1.0Vp-p (0.5Vp-p Typ.)
- Clock frequency f_{CLK} 4.433619MHz
- Input clock waveform sine wave

Input Signal Amplitude

Vsig 350mVp-p (Typ.), 575mVp-p (Max.)

Block Diagram and Pin Configuration (Top View)



SOP 24pin

Pin No.	Symbol	I/O	Description
1	V_{SS}	—	GND
2	C-IN1	I	Chrominance signal input 1
3	V_{DD}	—	Power supply
4	C-IN2	I	Chrominance signal input 2
5	(NC)	—	—
6	(NC)	—	—
7	Y-IN	I	Luminance signal input
8	(NC)	—	—
9	Y-OUT	O	Luminance signal output
10	(NC)	—	—
11	(NC)	—	—
12	CLK	I	Clock input
13	V_{SS}	—	GND
14	VCOIN	I	VCO input
15	PCOUT	O	Phase comparator output
16	(NC)	—	—
17	(NC)	—	—
18	(NC)	—	—
19	AB-P	O	Autobias output (P)
20	fsc	O	fsc buffer output
21	AB-C	O	Autobias output (C)
22	CONT	I	Control input
23	C-OUT	O	Chrominance signal output
24	V_{SS}	—	GND

Description of Functions

The CXL1511M enables the chrominance comb filter characteristics and luminance signal delay time to be selected in the control input state.

CONT	Mode (typical example)	Chrominance comb filter chracteristics	Luminance signal delay time (number of CCD bits)
L	PAL/GBI	2H (1702.5bit)	1H (848.5bit)
H	4.43NTSC	1H (844.5bit)	1H (842.5bit)

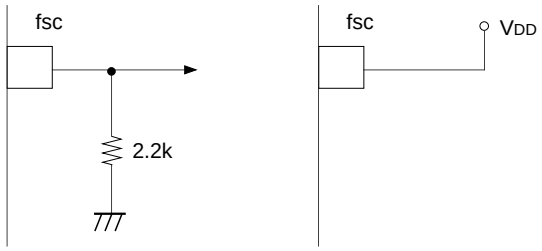
CONT Input Level

L/H	Min.	Typ.	Max.	Unit
L	—	0	0.5	V
H	2.0	5.0	6.0	

- **fsc Output Pin**

  The buffer output of the clock input from the CLK pin is provided at the fsc output pin. Since a pull-up resistor is contained inside the IC, the supply voltage is produced during open, and the output is stopped. Connect a 2.2kΩ pull-down resistor when the fsc output is to be used.

<When in use> <When not in use>



Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 4.433619MHz, V_{CLK} = 500mVp-p sine wave)

See electrical Characteristics Measurement Circuit

Item	Symbol	Measurement condition	SW condition								Min.	Typ.	Max.	Unit	NOTE
			1	2	3	4	5	6	7	8					
Supply current	IDD1	—	b	b	b	a	a	a	—	—		35	50	mA	1
	IDD2		b	b	b	a	b	a	—	—					

Chrominance Signal Characteristics (No signals input to Y-IN)

Item	Symbol	Measurement condition	SW condition							Min.	Typ.	Max.	Unit	NOTE
			1	2	3	4	5	6	7					
Low frequency gain	GLC1	(See Note 2)	a	a	b	a	—	a	b	–2	0	2	dB	2
	GLC2		a	a	b	a	—	a	b					
Frequency response	FC1	(See Note 3)	a	a	b	a	—	a	b	–2.7	–1.7	0	dB	3
	FC2		a	a	b	a	—	a	b					
Linearity	LIC1	(See Note 4)	a	a	b	a	—	a	b	–0.3	0	0.3	dB	4
	LIC2		a	a	b	a	—	a	b					
Comb depth min. gain	CCD1	(See Note 5)	a	a	b	a	—	a	b		–40	–25	dB	5
	CCD2		a	a	b	a	—	a	b					
SN ratio	SNC1	50% white video signal	a	a	b	a	—	a	d	52	56		dB	6
	SNC2		a	a	b	a	—	a	d					
Coupling level	CPC1	(See Note 7)	b	b	b	a	—	a	b		10	50	mVrms	7
	CPC2		b	b	b	a	—	a	b					
Delay time	DC	(See Note 8)	a	b	b	—	—	a	a	—	260	—	ns	8

<Luminance Signal Characteristics> (No signals input to C-IN1, C-IN2)

Item	Symbol	Measurement condition	SW condition							Min.	Typ.	Max.	Unit	NOTE
			1	2	3	4	5	6	7					
Low frequency gain	GLY1	(See Note 2)	b	b	a	—	b	b	b	–2	0	2	dB	2
	GLY2		b	b	a	—	a	b	b					
Frequency response	FY1	(See Note 3)	b	b	a	—	b	b	b	–2.7	–1.7	0	dB	3
	FY2		b	b	a	—	b	b	b					
Differential gain	DGY1	5-step staircase wave	b	b	a	—	a	b	c	0	3	5	%	9
	DGY2		b	b	a	—	a	b	c					
Differential Phase	DPY1	5-step staircase wave	b	b	a	—	a	b	c	0	3	5	deg	9
	DPY2		b	b	a	—	a	b	c					
Linearity	LNY1	(See Note 10)	b	b	a	—	a	b	a	35	40	43	%	10
	LNY2		b	b	a	—	a	b	a					
SN ratio	SNY1	50% white video signal	b	b	a	—	b	b	d	52	56		dB	6
	SNY2		b	b	a	—	b	b	d					
Coupling level	CPY1	(See Note 7)	b	b	b	—	b	b	b		10	50	mVrms	7
	CPY2		b	b	b	—	b	b	b					

Note

1. This is the IC's supply current value when no signals are input.

2. This is the C-OUT and Y-OUT pin output gain when 500mVp-p sine waves are input to C-IN1, C-IN2 and Y-IN.

   (Example of calculation)

   $$GLC1 = 20 \log \frac{\text{C-OUT pin output voltage (mVp-p)}}{\text{500 (mVp-p)}} \text{ [dB]}$$

   Input signal frequency
   - GLC1 (2H) : 203.126kHz
   - GLC2 (1H) : 204.750kHz
   - GLY1, GLY2 : 200kHz

3. This indicates the difference in the C-OUT and Y-OUT pin output gain when 200mVp-p low- and high-frequency sine waves are input to C-IN1, C-IN2 and Y-IN. Set the input bias (Vbias) to 2.0V when measuring the luminance signal characteristics (GLY1, GLY2, GHY1, GHY2).

   (Example of calculation)

   $$FC1 = 20 \log \frac{\text{C-OUT pin output voltage (high frequency) (mVp-p)}}{\text{C-OUT pin output voltage (low frequency) (mVp-p)}} \text{ [dB]}$$

   Input signal frequency (low frequency) → see Note 2
   Input signal frequency (high frequency)
   - Chrominance signal (2H) : 4.429712MHz
   - Chrominance signal (1H) : 4.425744MHz
   - Luminance system : 4.43MHz

4. Calculate with the gain applying when 200mVp-p and 500mVp-p sine waves (see Note 2 for the frequencies) are input to C-IN1 and C-IN2.

   (Example of calculation)

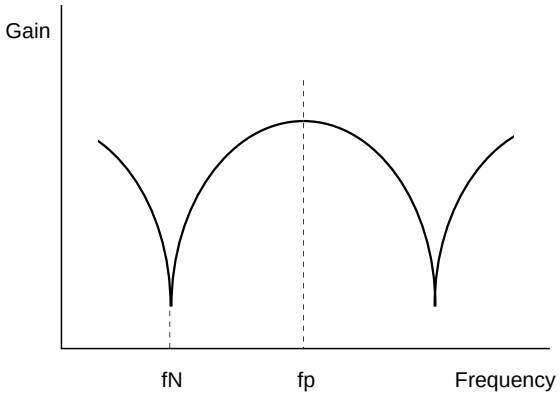
   $$LIC1 = 20 \log \left(\frac{\dfrac{\text{Output voltage with 500mVp-p input (mVp-p)}}{\text{500mVp-p}}}{\dfrac{\text{Output voltage with 200mVp-p input (mVp-p)}}{\text{200mVp-p}}} \right) \text{ [dB]}$$

5. Measure the difference of the C-OUT output gain when 500mVp-p sine waves have been input to C-IN1 and C-IN2 at the following frequencies.

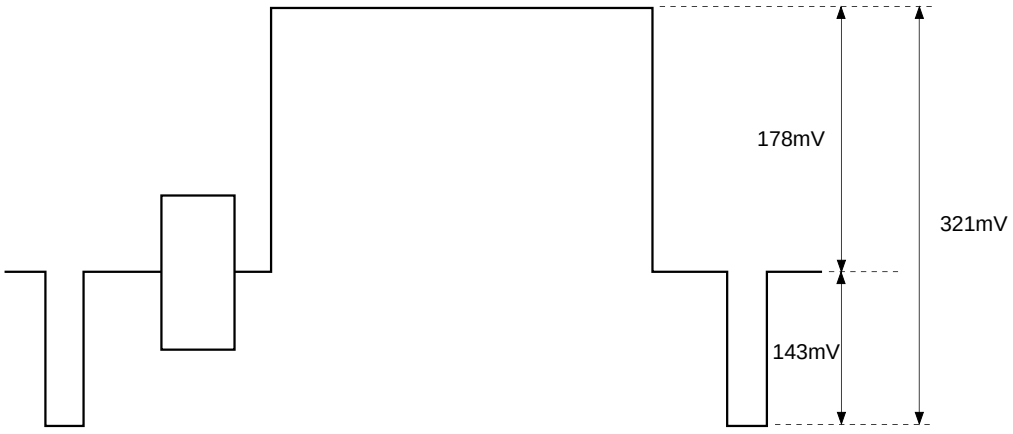
   Input signal frequency

	fp	fN
CCD1	4.429712MHz	4.425806MHz
CCD2	4.425744MHz	4.417869MHz

   The frequency response for the outputs at fp and fN are shown in the figure below.



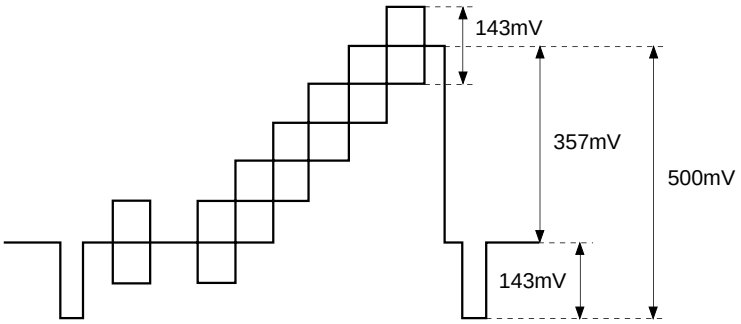
6. Using the BPF 100kHz to 5MHz in the Sub Carrier Trap mode, measure the SN ratio on the video noise meter when the 50% white video signal shown in the figure below is input.



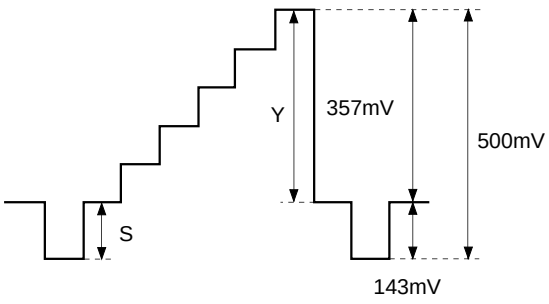
7. Measure the internal clock component (3fsc: 13.300856MHz component) when no signals are input.

8. Measure the delay time of the C-OUT output when the C-IN1 signal is input.

9. On the vector scope, measure the differential gain and differential phase when the 5-step staircase wave shown in the figure below is input.



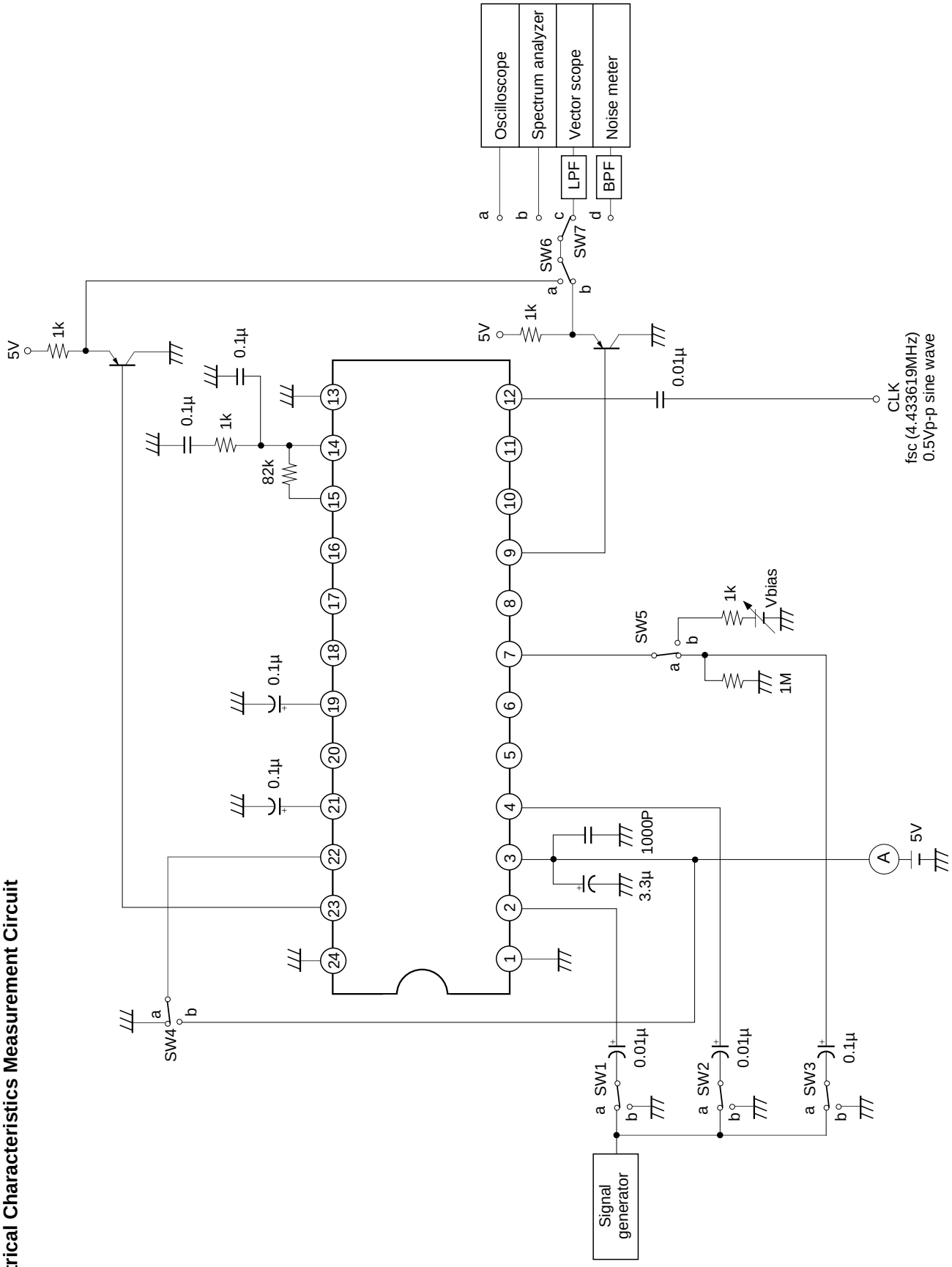
10. Input the 5-step staircase wave only for the luminance signal shown in the figure below, and measure the Y-OUT luminance level (Y) and SYNC level (S).



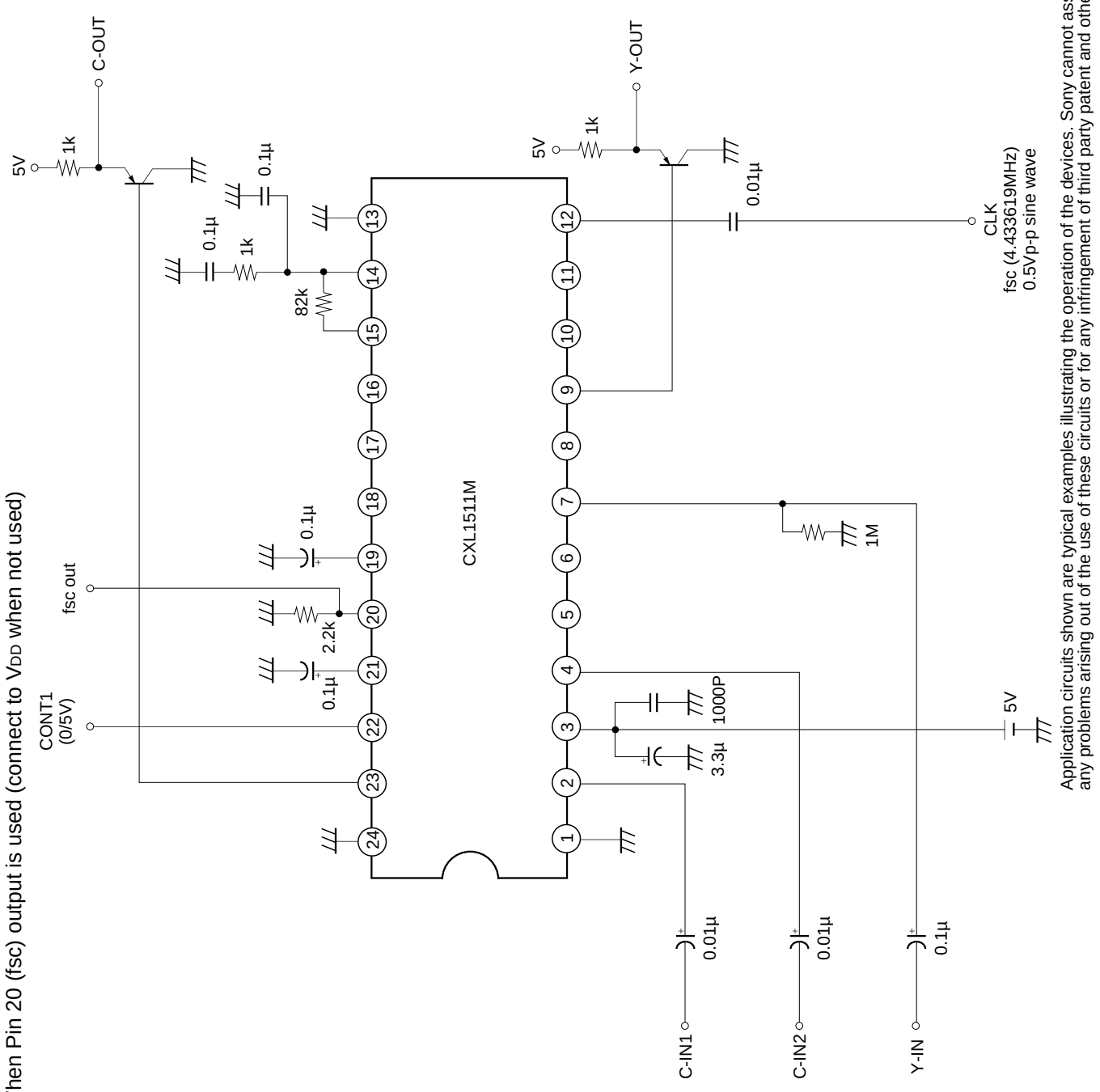
(Example of calculation)

$$LNY1 = \frac{S\ (mV)}{Y\ (mV)} \times 100$$

Electrical Characteristics Measurement Circuit



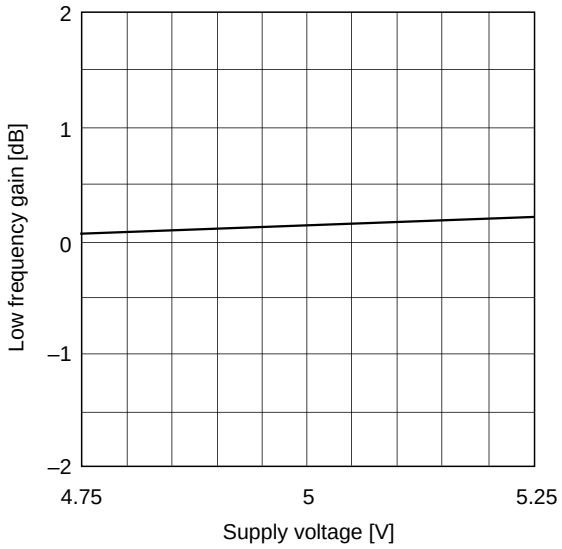
Application Circuit When Pin 20 (fsc) output is used (connect to V_{DD} when not used)



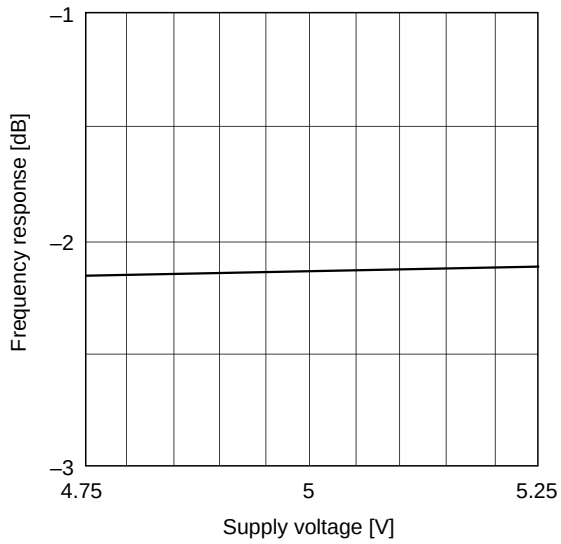
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

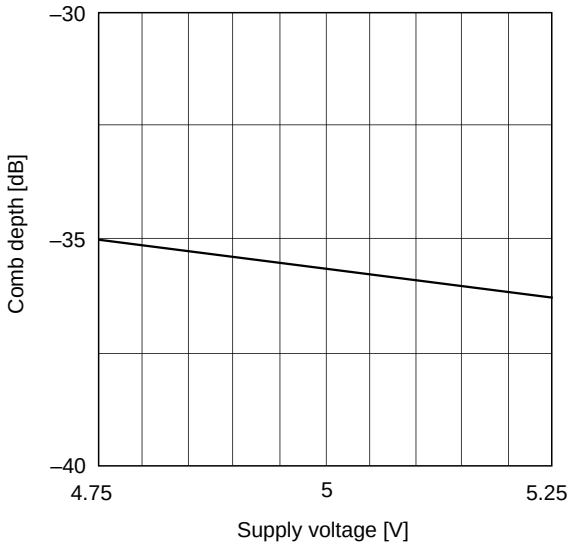
Low frequency gain vs. Supply voltage



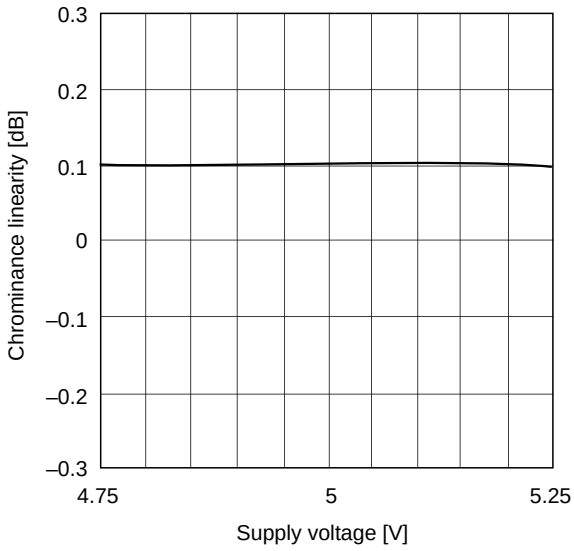
Frequency response vs. Supply voltage



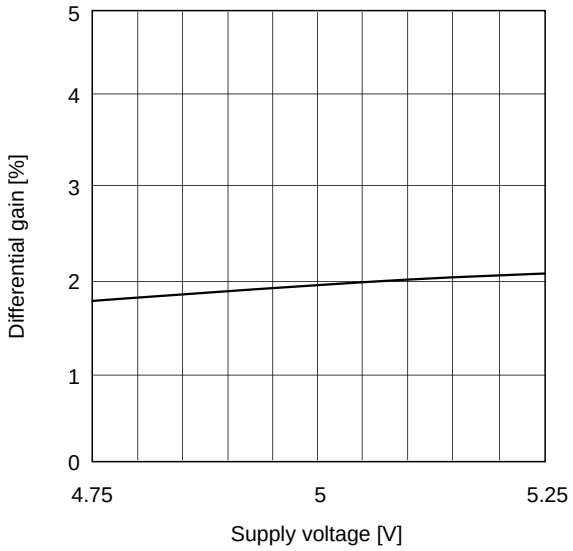
Comb depth vs. Supply voltage



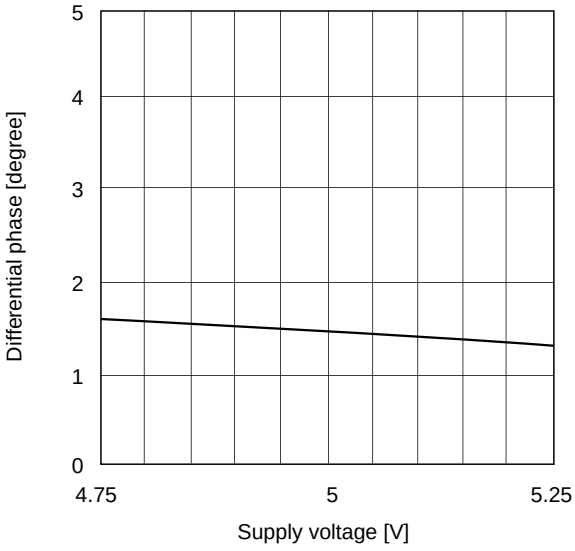
Chrominance linearity vs. Supply voltage



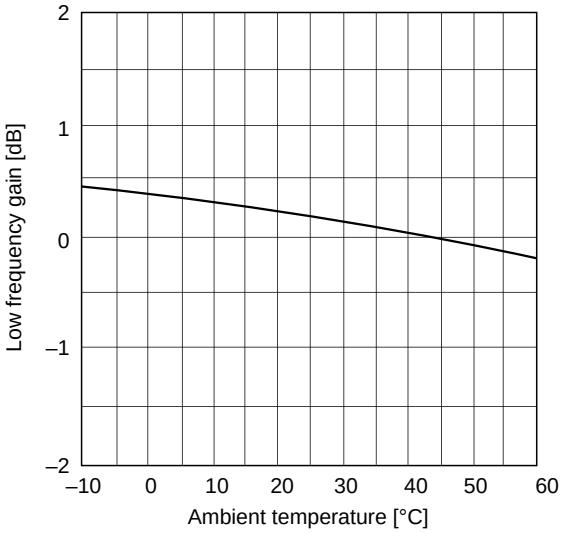
Differential gain vs. Supply voltage



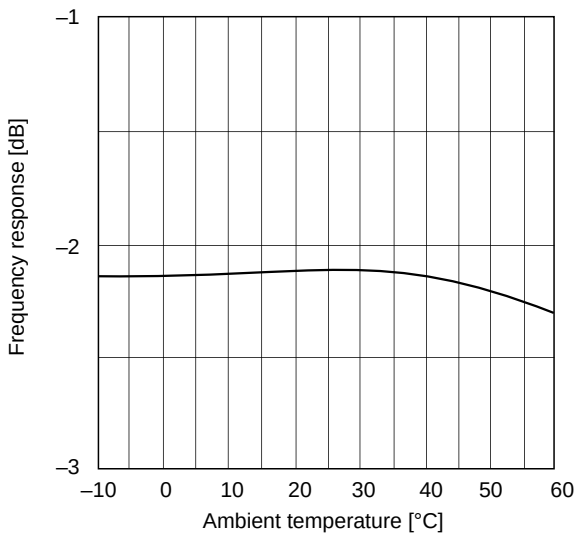
Differential phase vs. Supply voltage



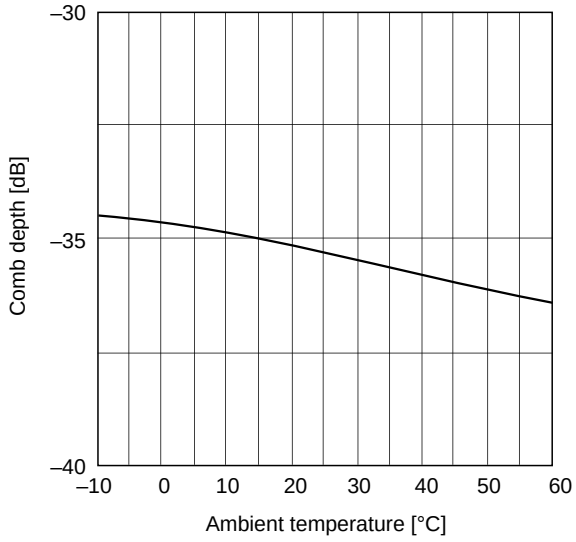
Low frequency gain vs. Ambient temperature



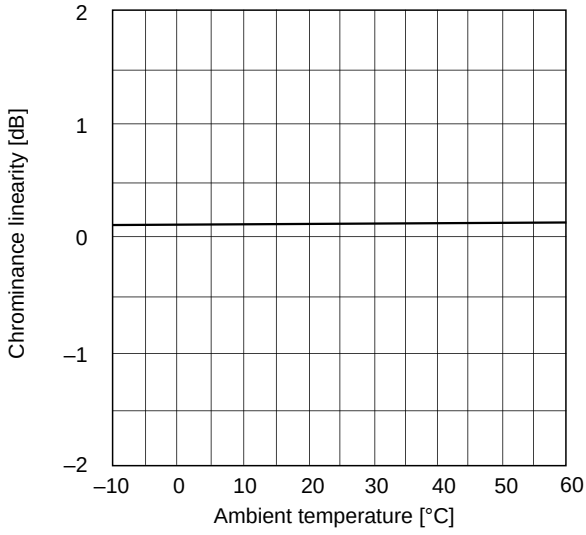
Frequency response vs. Ambient temperature



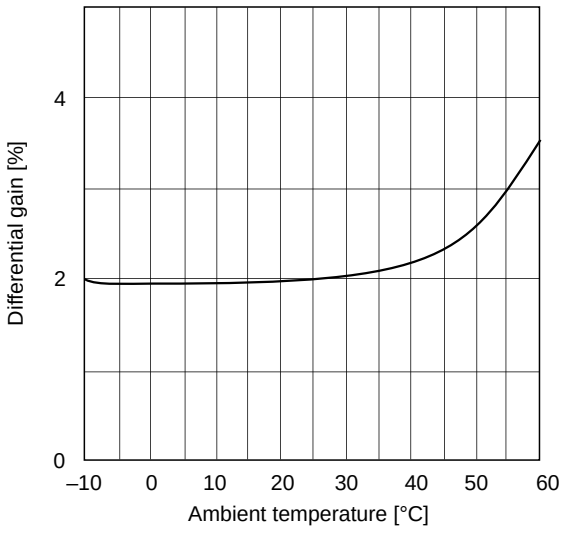
Comb depth vs. Ambient temperature



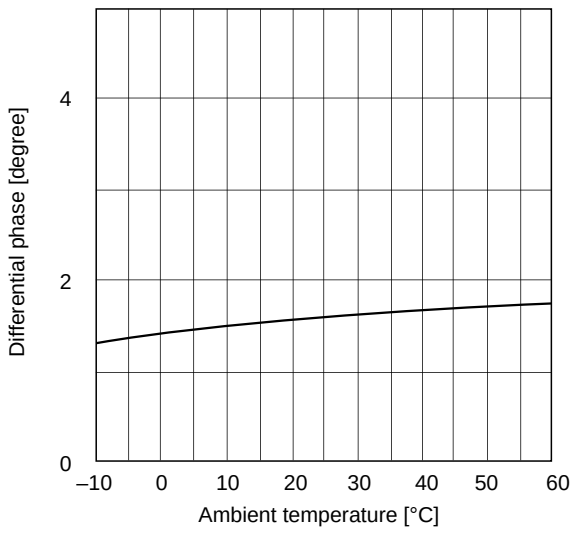
Chrominance linearity vs. Ambient temperature



Differential gain vs. Ambient temperature

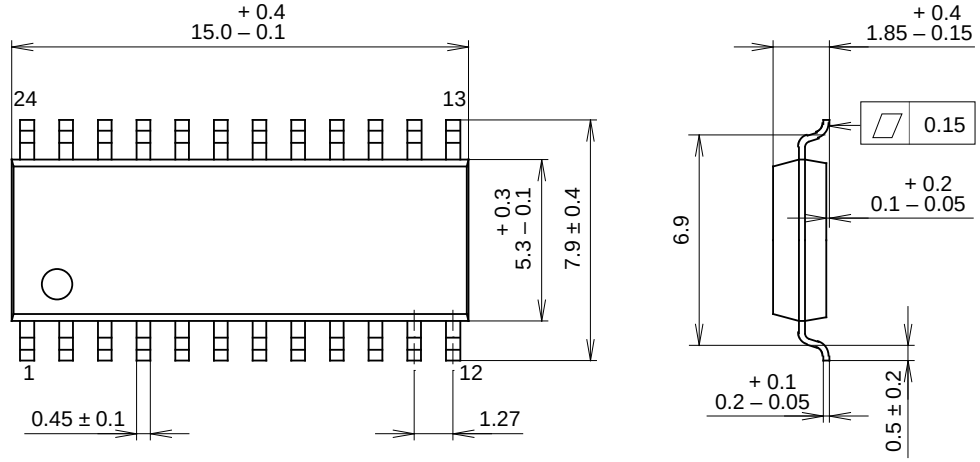


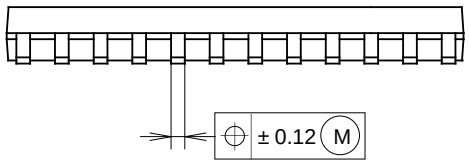
Differential phase vs. Ambient temperature



Package Outline Unit: mm

24PIN SOP (PLASTIC)





SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g