SONY

CXL5502M/N/P

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5502M/N/P are CMOS-CCD delay line ICs that provide 1H delay time for NTSC signals including the external low-pass filter.

The ICs contain a PLL circuit (quadruple progression).

Features

- Single power supply (5V)
- Low power consumption 95mW (Typ.)
- Built-in peripheral circuits
- Clamp level of I/O signal can be selected
- Built-in quadruple PLL circuit

Functions

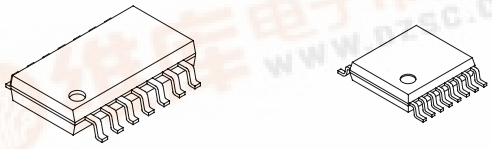
- 905-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit
- PLL circuit (quadruple progression)

Structure

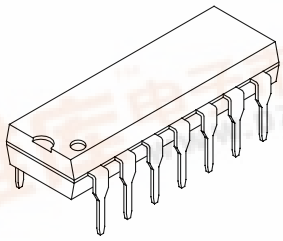
CMOS-CCD

CXL5502M
14 pin SOP (Plastic)

CXL5502N
16 pin SSOP (Plastic)



CXL5502P
14 pin DIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5502M	400	mW
	CXL5502N	260	mW
	CXL5502P	800	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0 (0.5Vp-p typ.)	Vp-p
• Clock frequency	f_{CLK}	3.579545	MHz
• Input clock waveform	Sine wave		

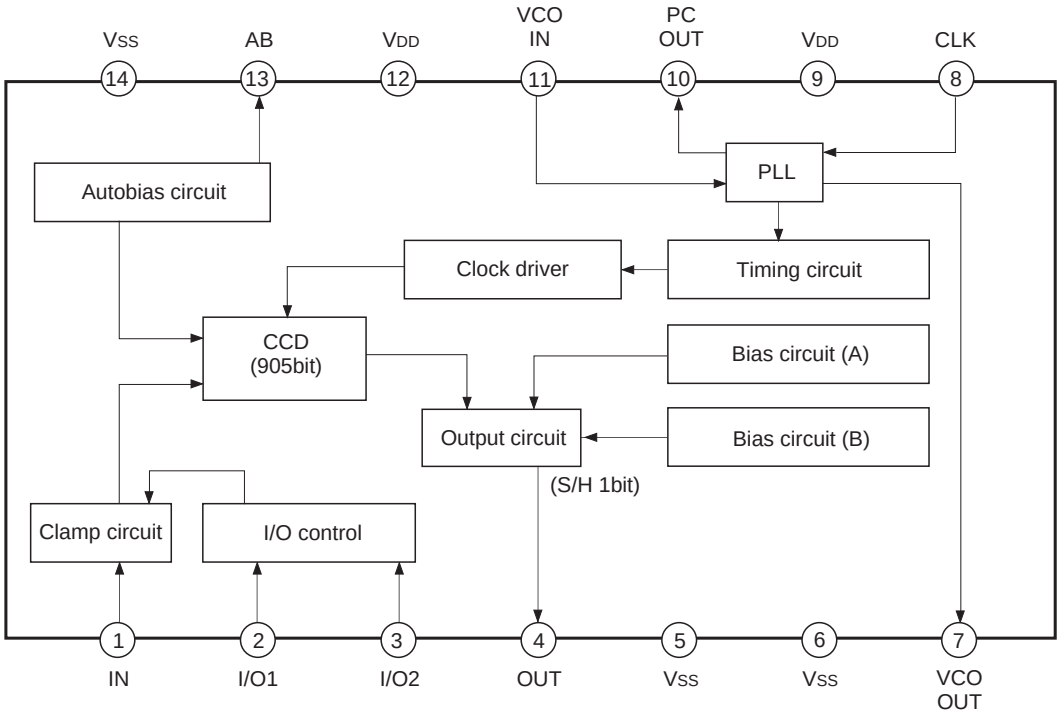
Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 572mVp-p (Max.)
(at internal clamp condition)

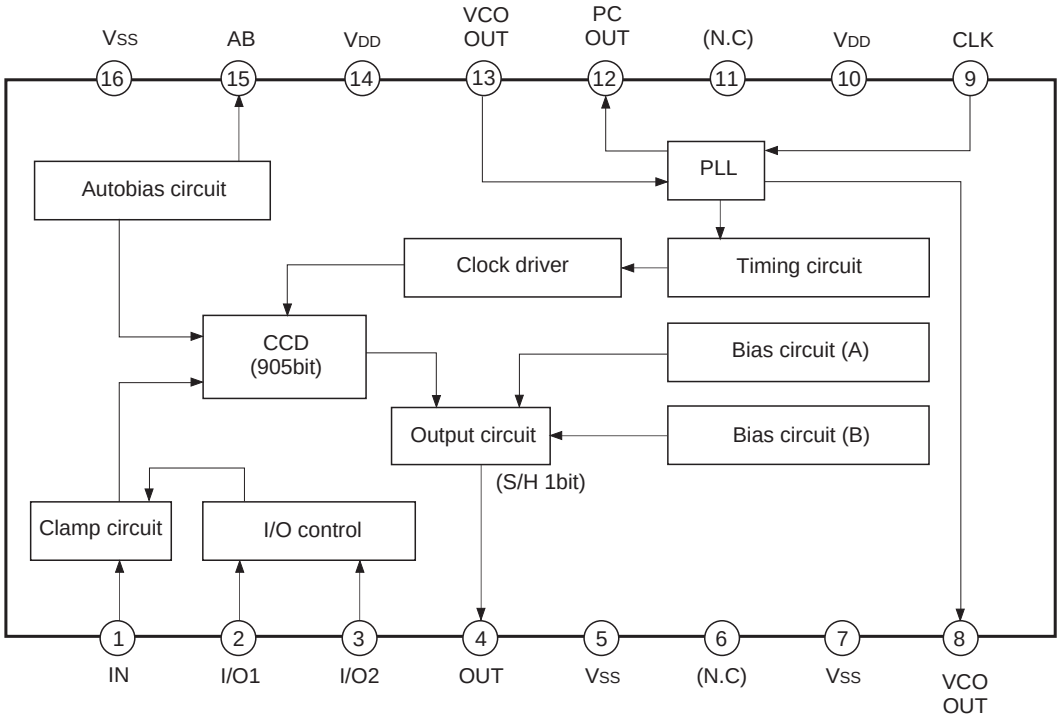
E89930E79-PS

Block Diagram and Pin Configuration (Top View)

CXL5502M/P



CXL5502N



Pin Description

CXL5502M/P

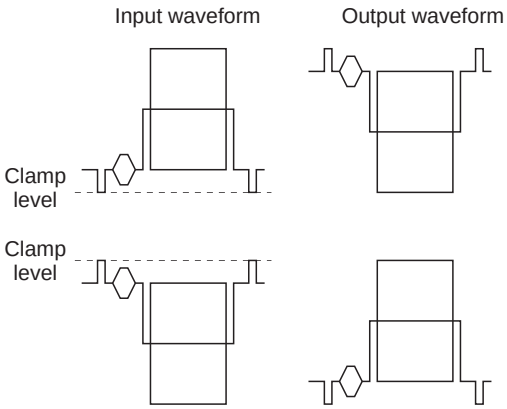
Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O1	I	I/O control 1	
3	I/O2	I	I/O control 2	
4	OUT	O	Signal output	40 to 500Ω
5	V_{SS}	—	GND	
6	V_{SS}	—	GND	
7	VCO OUT	O	VCO output	
8	CLK	I	Clock input	> 100kΩ
9	V_{DD}	—	Power supply (5V)	
10	PC OUT	O	Phase comparator output	
11	VCO IN	I	VCO input	
12	V_{DD}	—	Power supply (5V)	
13	AB	O	Autobias DC output	600 to 200kΩ
14	V_{SS}	—	GND (SUB)	

CXL5502N

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O1	I	I/O contorl 1	
3	I/O2	I	I/O contorl 2	
4	OUT	O	Signal output	40 to 500Ω
5	V_{SS}	—	GND	
6	(N.C)	—	—	
7	V_{SS}	—	GND	
8	VCO OUT	O	VCO output	
9	CLK	I	Clock input	> 100kΩ
10	V_{DD}	—	Power supply (5V)	
11	(N.C)	—	—	
12	PC OUT	O	Phase comparator output	
13	VCO IN	I	VCO input	
14	V_{DD}	—	Power supply (5V)	
15	AB	O	Autobias DC output	600 to 200kΩ
16	V_{SS}	—	GND (SUB)	

Description of Function

In the CXL5502M/N/P, the condition of I/O control pins (Pins 2 and 3) control the input signal clamp condition and the mode of the output signal with relation to its input signal.
There are 2 modes for the I/O signal.



(1) PN mode
(Low level clamp/reverse phase output mode)

(2) NP mode
(High level clamp/positive phase output mode)

I/O Control Pin

(1) I/O1 (Pin 2)
Control of the I/O signal condition
DC open ..... Input signal is low level clamped and the output signal is inverted in relation to the input signal. As the pin is biased to 2.5V by means of the resistance inside the IC, a decoupling capacitor of around 1000pF is necessary.
GND ..... Input signal is high level clamped and the output signal turns into an inverted signal.

(2) I/O2 (Pin 3)
Control of the input signal clamp condition
0V ..... Internal clamp condition
5V ..... Non internal clamp condition
Center biased to approx. 2.1V by means of the IC internal resistance (several 10kΩ).
Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.

Electrical Characteristics (Ta = 25°C, V_{DD} = 5V, f_{CLK} = 3.579545MHz, V_{CLK} = 500mVp-p, Sine wave)

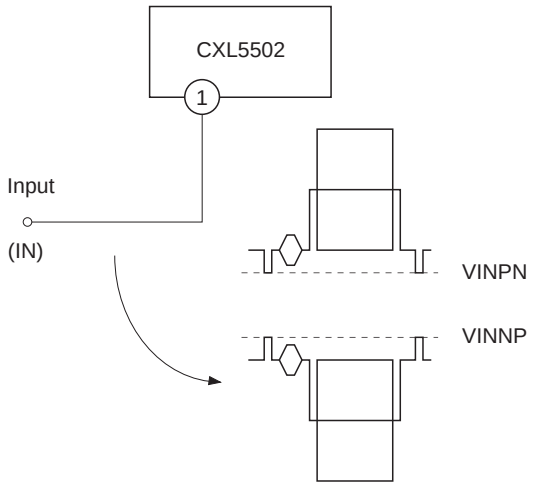
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition							Bias condition Vbias1 (V) (Note 1)	Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	6	7						
Supply current	IDDPN	—	—	c	b	b	b	a	—	—	10	19	28	mA	2
	IDDNP					a	a								
Low frequency gain	GLPN	200kHz, 500mVp-p, sine wave	a	a	b	b	b	a	b	—	–2	0	2	dB	3
	GLNP					a	a								
Frequency response	fPN	200kHz ⟷ 3.57MHz, 150mVp-p, sine wave	b ⇕ c	a	a	b	b	b	b	2.1	–2	–1	0	dB	4
	fNP					a	a								
Differential gain	DGPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	%	5
	DGNP			b		a	a								
Differential phase	DPPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	degree	5
	DPNP			b		a	a								
S/H pulse coupling	CPPN	No signal input	—	c	a	b	b	b	a	VINPN + 0.5	—	—	350	mVp-p	6
	CPNP					a	a			VINNP					
S/N ratio	SNPN	50% white video signal (See Note 7)	e	a	b	b	b	a	d	—	52	56	—	dB	7
	SNNP			b		a	a								

Notes

(1) VINPN and VINNP are defined as follows.

VINPN and VINNP are the input signal clamp levels of PN and NP modes clamping the video signal sync tip level.



Testing of VINPN and VINNP is executed with a voltmeter under the following SW conditions.

Item	SW condition							Test point
	1	2	3	4	5	6	7	
VINPN	—	c	b	b	b	a	—	V1
VINNP	—	c	b	a	a	a	—	

(2) This is the IC supply current value during clock and signal input.

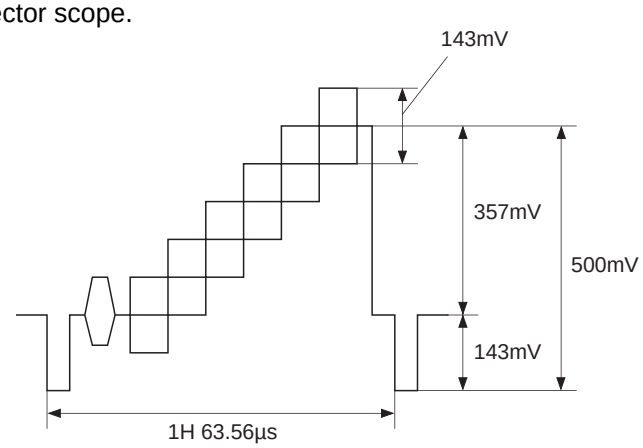
(3) GLPN, GLNP are output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.
(Example of calculation)

$$GLPN = 20 \log \frac{\text{OUT pin output voltage (PN mode) [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

(4) Indicates the dissipation at 3.57MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 3.57MHz sine wave is fed to same, calculation is made according to the following formula. The input part bias is tested at 2.1V.
(Example of calculation)

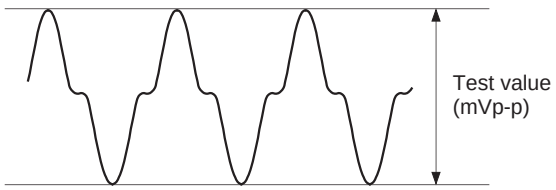
$$fPN = 20 \log \frac{\text{OUT pin otuput voltage (PN mode, 3.57MHz) [mVp-p]}}{\text{OUT pin output voltage (PN mode, 200kHz) [mVp-p]}} \text{ [dB]}$$

(5) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the figure below is input are tested at the vector scope.

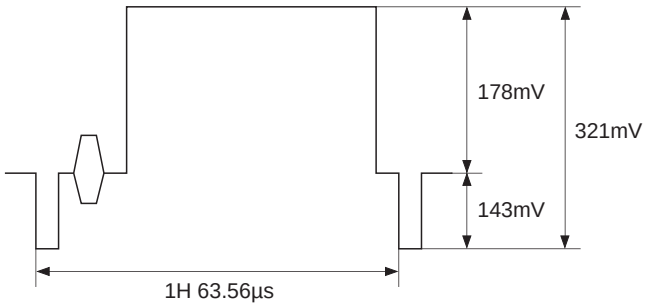


Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

(6) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at VINPN + 0.5V and VINNP for PN and NP modes respectively.



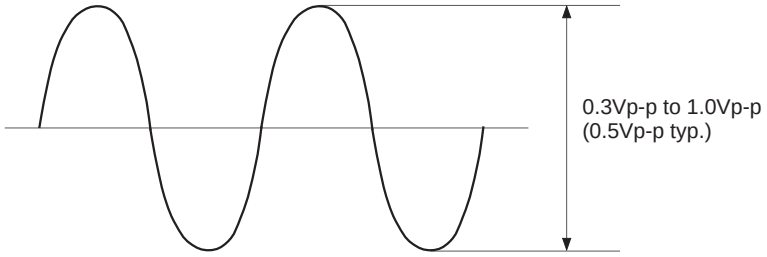
(7) S/N ratio during a 50% white video signal input shown in figure below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



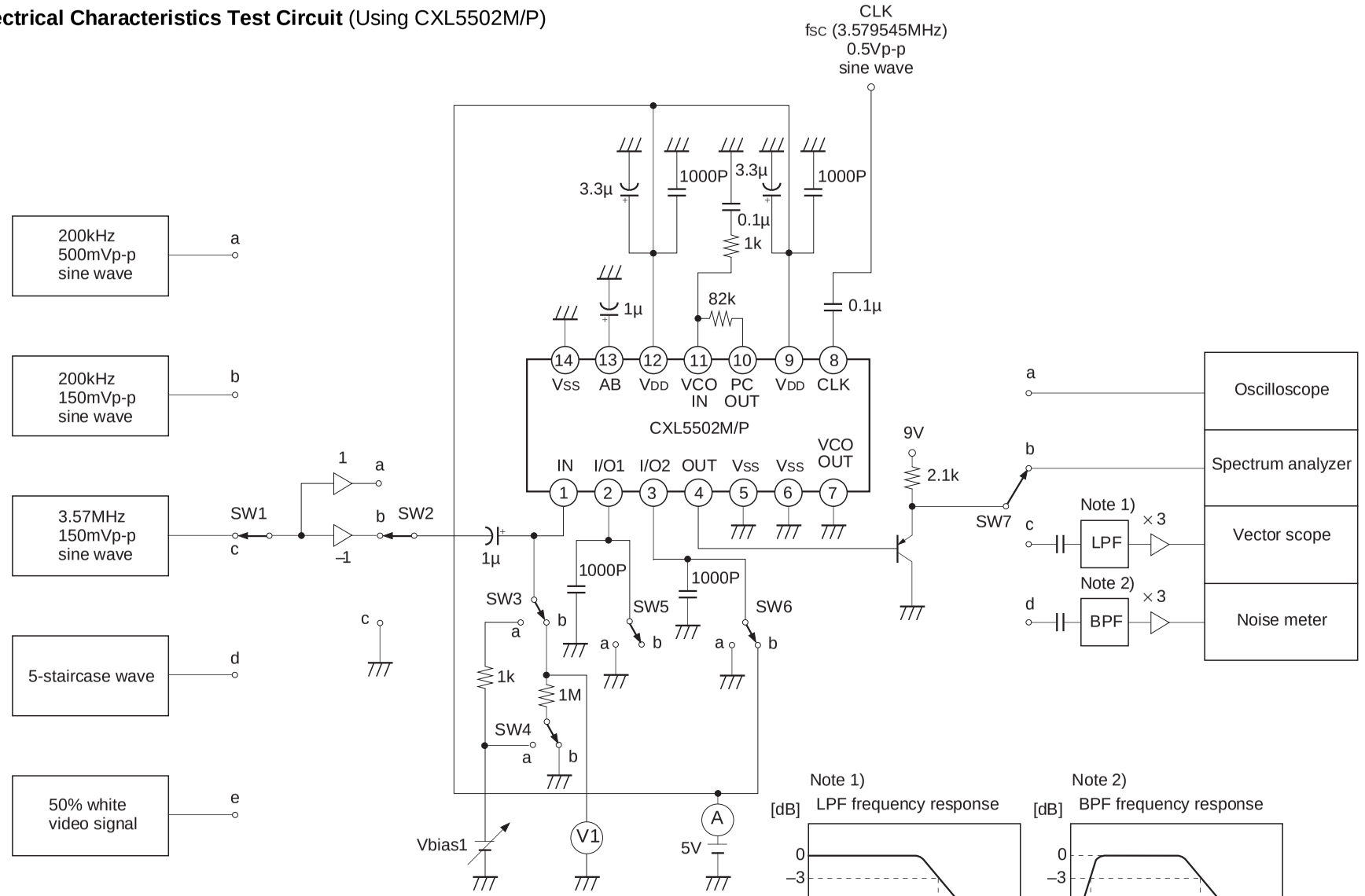
Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

Clock

fsc (3.579545MHz) sine wave



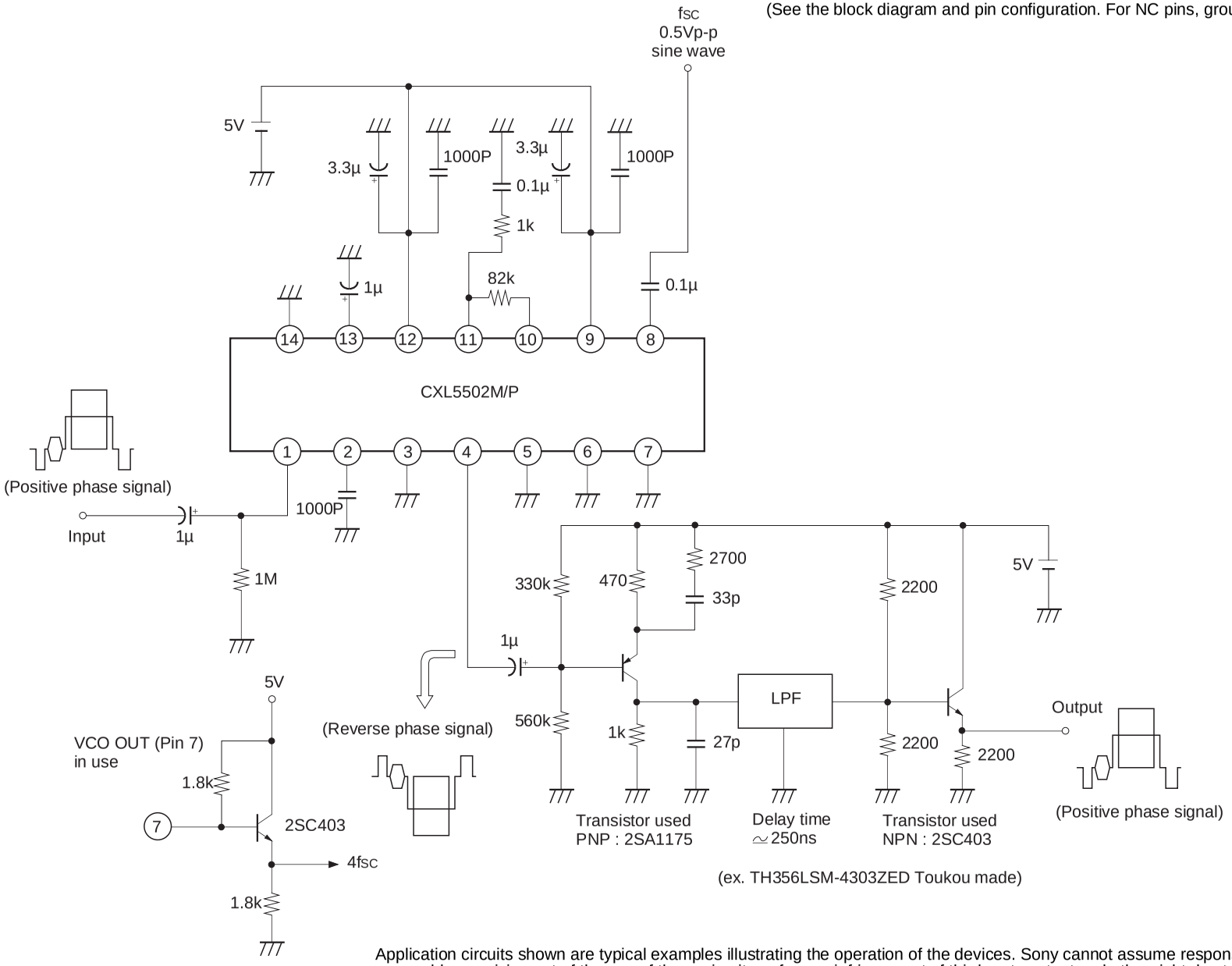
Electrical Characteristics Test Circuit (Using CXL5502M/P)



* When using CXL5502N, change the connection terminal only.
(See the block diagram and pin configuration. For NC pins, ground them.)

Application Circuit (Using CXL5502M/P)

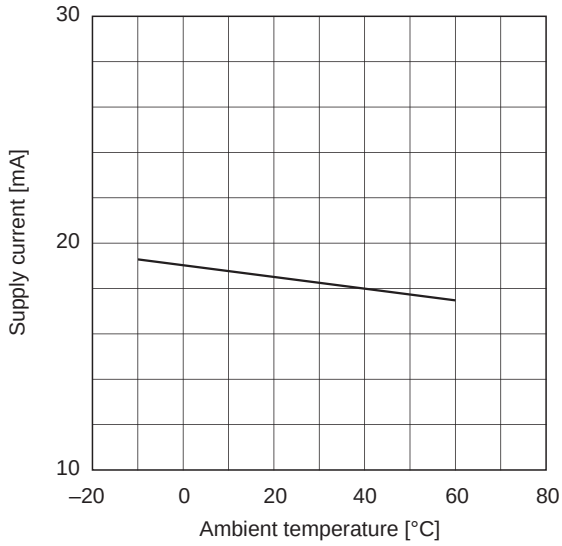
* When using CXL5502N, change the connection terminal only.
(See the block diagram and pin configuration. For NC pins, ground them.)



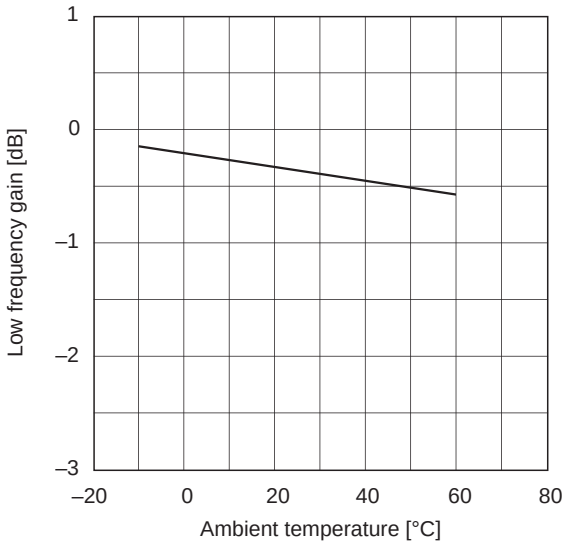
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

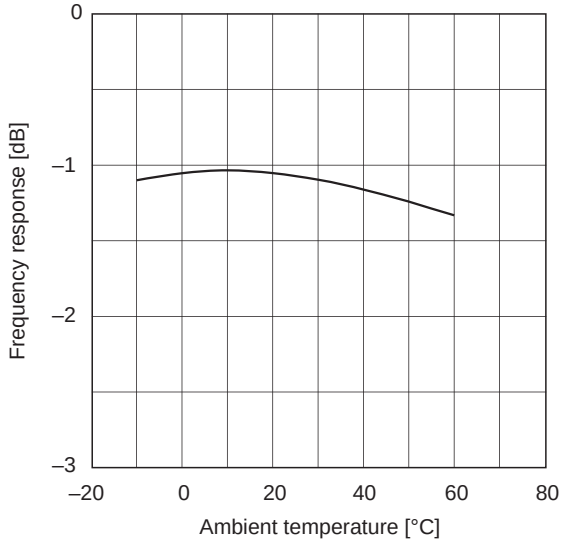
Supply current vs. Ambient temperature



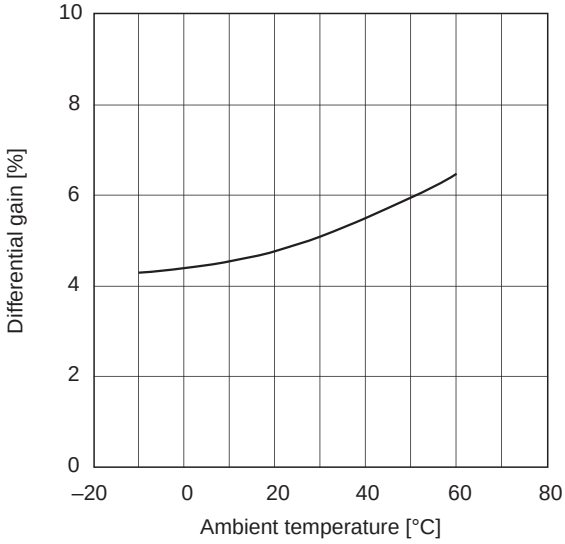
Low frequency gain vs. Ambient temperature



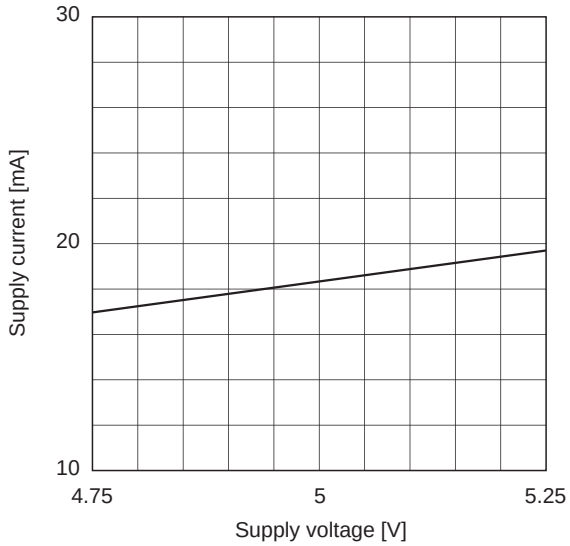
Frequency response vs. Ambient temperature



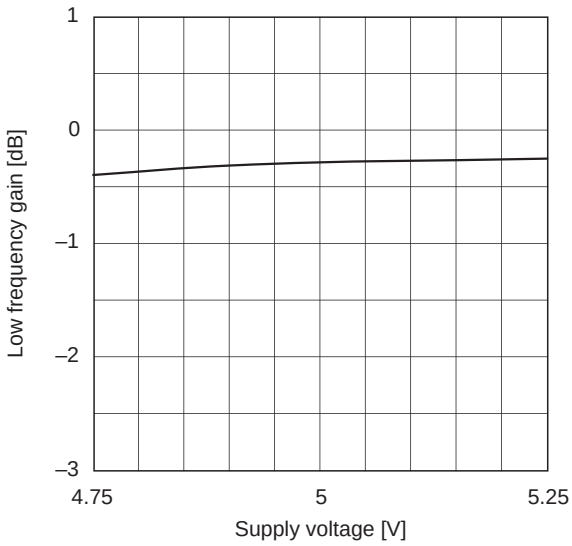
Differential gain vs. Ambient temperature



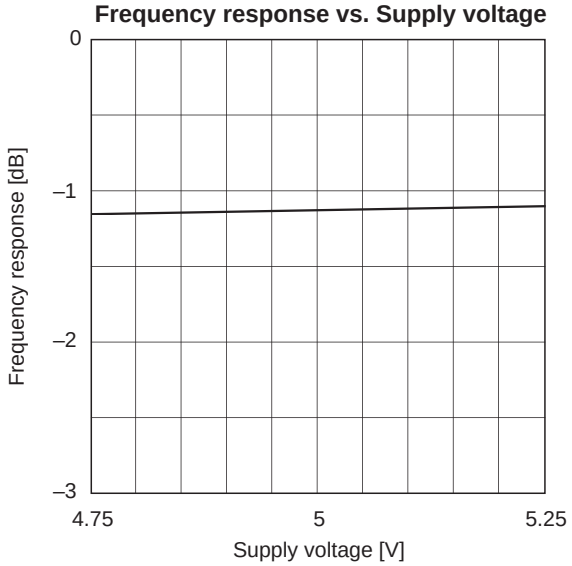
Supply current vs. Supply voltage



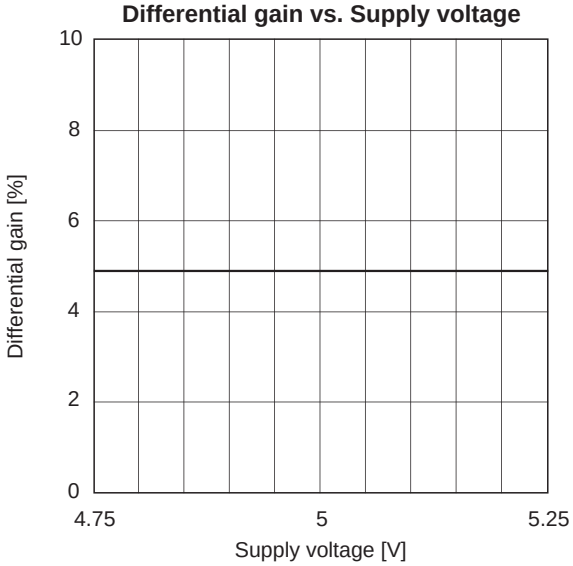
Low frequency gain vs. Supply voltage



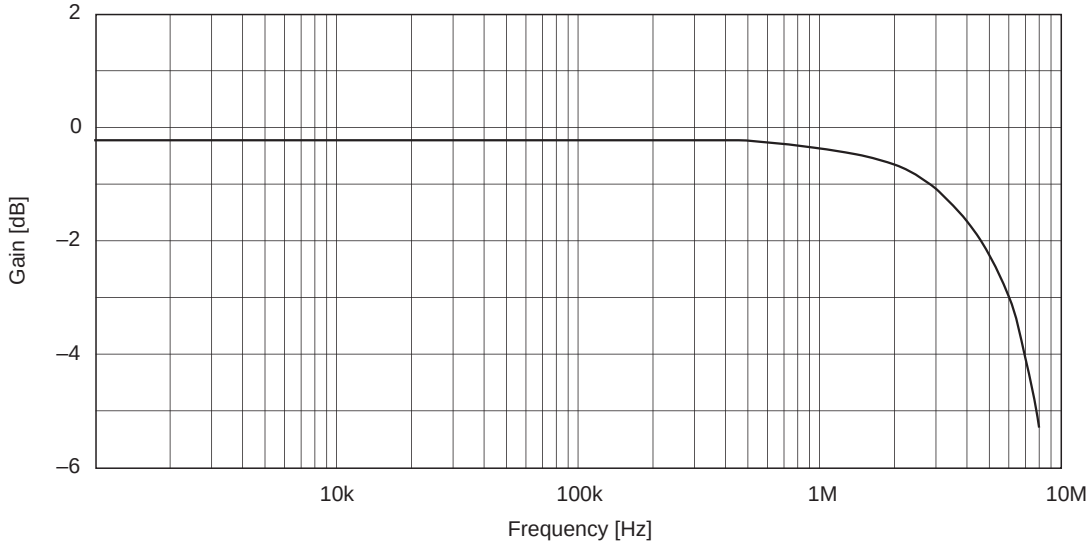
Frequency response vs. Supply voltage



Differential gain vs. Supply voltage



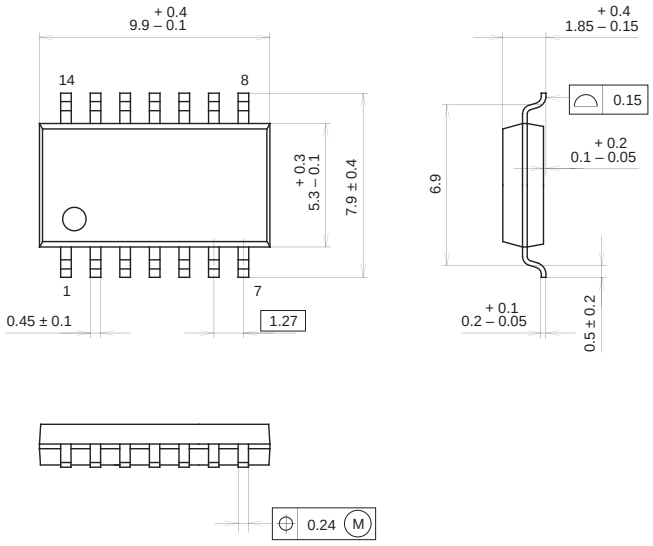
Frequency response



Package Outline Unit: mm

CXL5502M

14PIN SOP (PLASTIC)

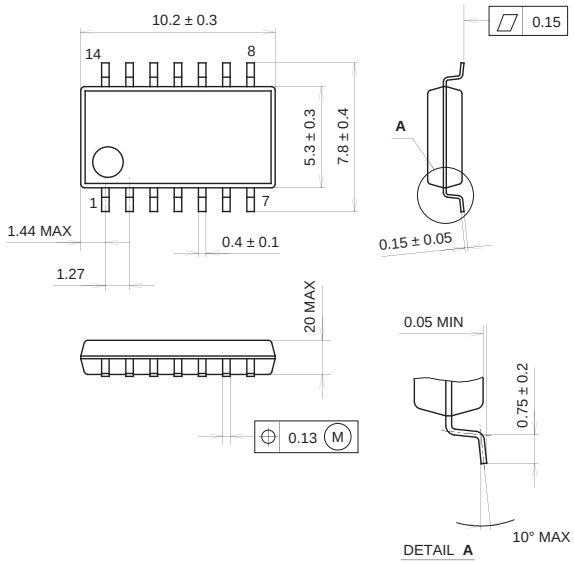


PACKAGE STRUCTURE

SONY CODE	SOP-14P-L01
EIAJ CODE	SOP014-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

14PIN SOP (Plastic) 300mil



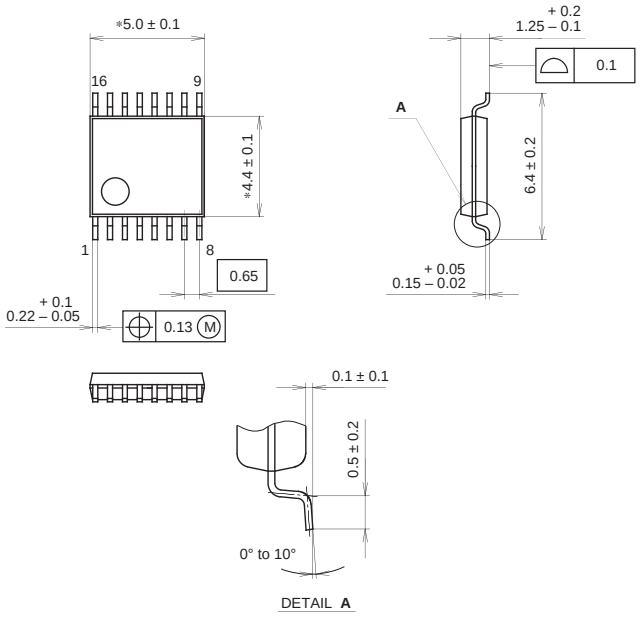
PACKAGE STRUCTURE

SONY CODE	SOP-14P-L121
EIAJ CODE	*SOP014-P-0300-AX
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXL5502N

16PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

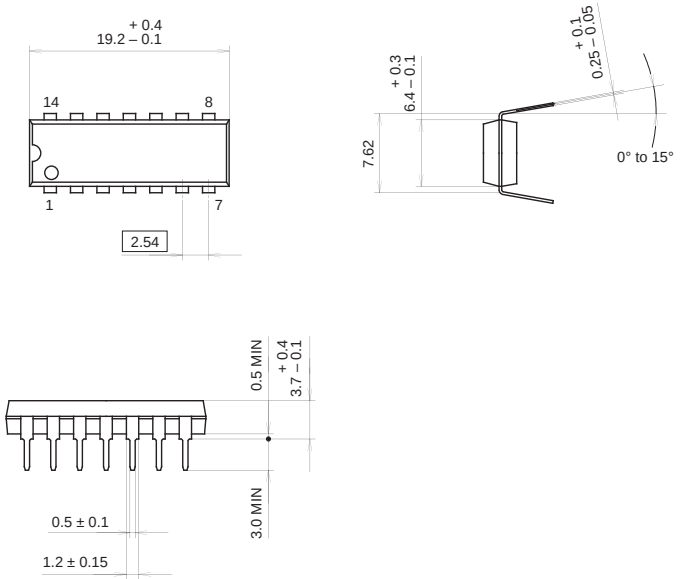
SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

CXL5502P

14PIN DIP (PLASTIC)



SONY CODE	DIP-14P-01
EIAJ CODE	DIP014-P-0300
JEDEC CODE	Similar to MO-001-AH

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.9g