

SONY

CXP5084/5086

CMOS 4-bit Single Chip Microcomputer

Description

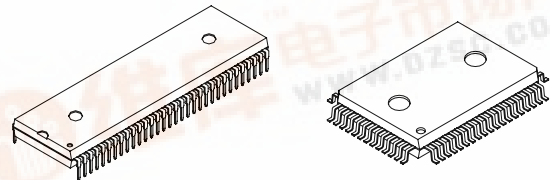
The CXP5084/5086 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function and a liquid crystal displayer (LCD) controller/driver. They are integrated into a single chip with the standby function etc. which are to be operated at low power consumption.

Features

- Instruction cycle 3.8μs/4.19MHz
1.9μs/4.19MHz
(High speed version)
- ROM capacity 4096 × 8 bits (CXP5084)
6144 × 8 bits (CXP5086)
- RAM capacity 400 × 4 bits
(Including stack, display area)
- 32 general purpose I/O ports
- LCD controller/driver (Direct drive possible)
 - Optional specification of 24, 20 or 16 segment outputs
 - 1/2, 1/3, 1/4 duty selectable through program
 - 1/3 bias
- 2 external interruption input pins
- 8-bit/4-bit variable serial I/O
- 8-bit timer, 8-bit timer/event counter and 18-bit time base timer are independently controllable
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 types of power down modes: sleep and stop
- Power on reset circuit (Mask option)
- Available option of either crystal oscillation or CR oscillation (mask option) types for the oscillation circuit
- 64-pin plastic SDIP/QFP available
- Piggyback package (CXP5080) available

64 pin SDIP (Plastic)

64 pin QFP (Plastic)

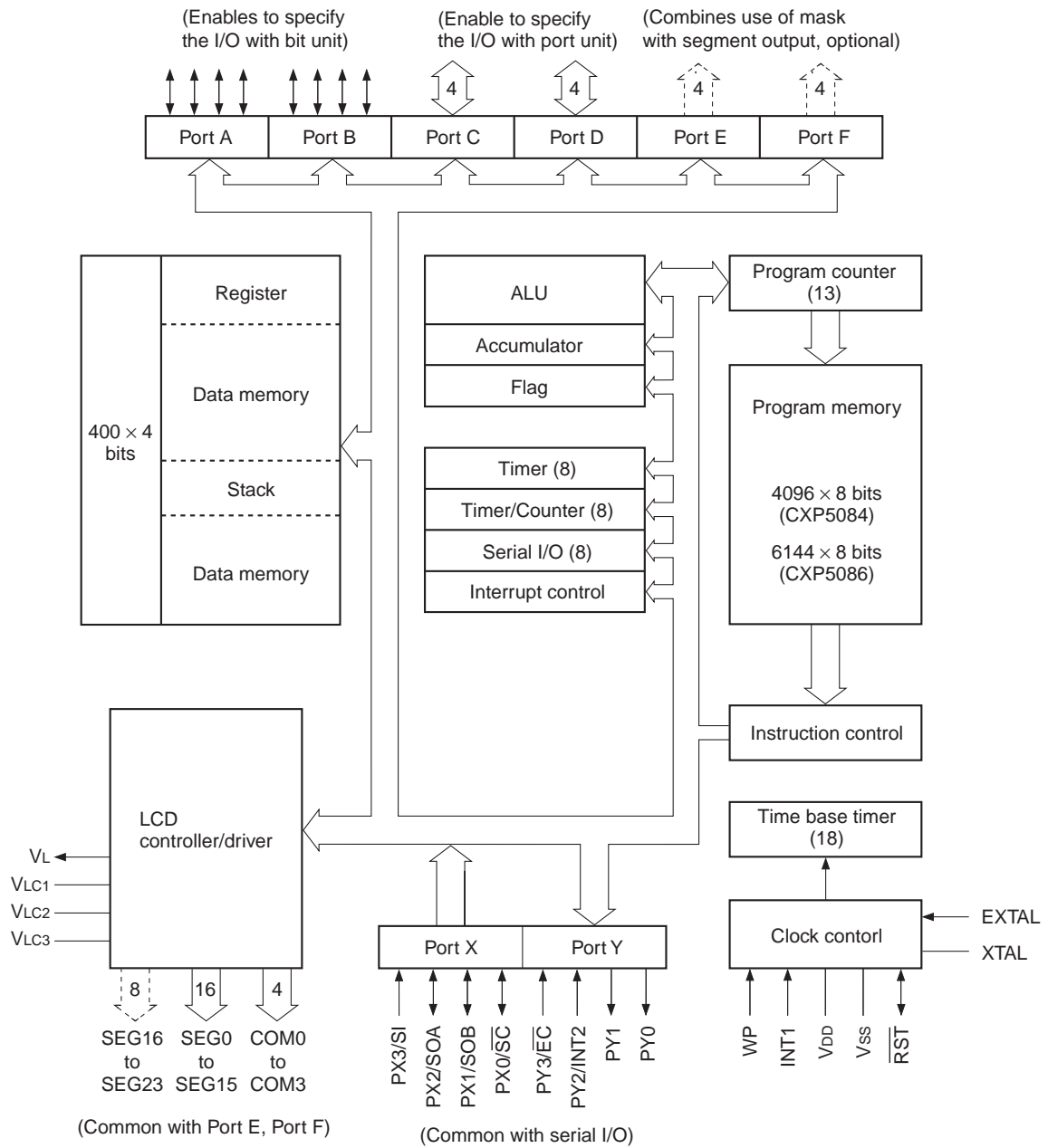


Structure

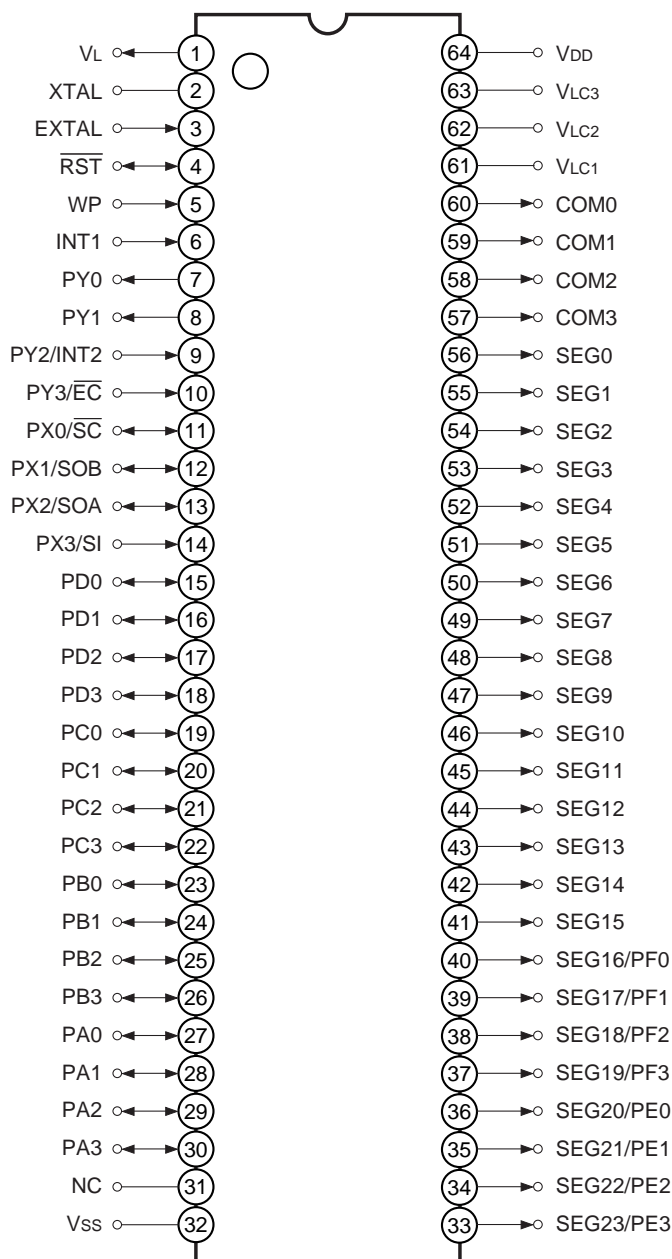
Silicon gate CMOS IC

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Block Diagram

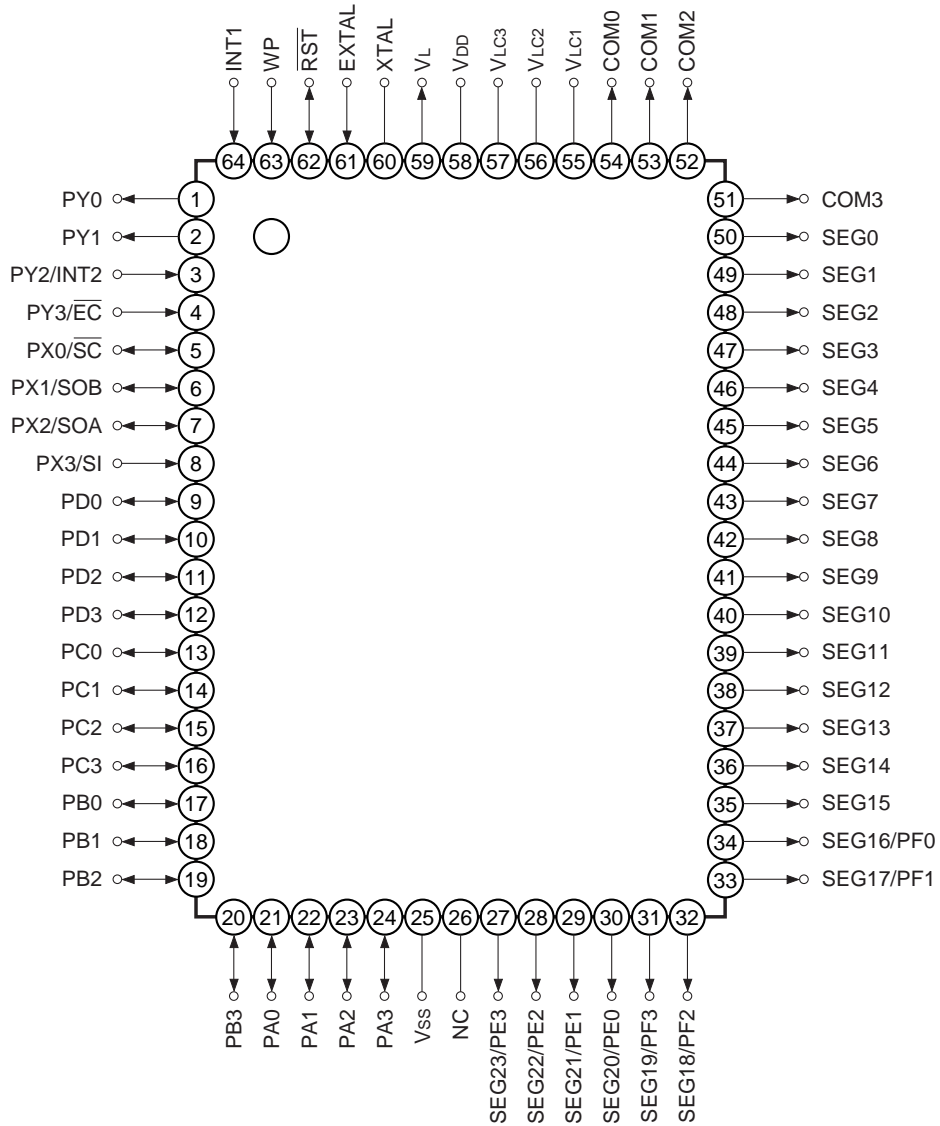


Pin Assignment 1 (Top View) 64-pin SDIP Package



Note) Do not make any connection to NC pin.

Pin Assignment 2 (Top View) 64-pin QFP Package



Note) Do not make any connection to NC pin.

Absolute Maximum Ratings

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Power supply voltage	V _{DD}	-0.3 to +7.0	V	
LCD bias voltage	V _{LC1} , V _{LC2} , V _{LC3}	-0.3 to +7.0* ¹	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
High level output current	I _{OH}	-5	mA	General purpose port* ² : per pin
High level total output current	∑I _{OH}	-50	mA	Entire pin total
Low level output current	I _{OL}	15	mA	General purpose port* ² : per pin
Low level total output current	∑I _{OL}	50	mA	Entire pin total
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _d	1000	mW	SDIP
		600	mW	QFP

*¹ V_{LC1}, V_{LC2}, V_{LC3}, V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*² The PE and PF are specified when PA to PD, PX0 to PX2, PY0, PY1 and mask option are selected as the port.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed data hold operation range during stop
LCD bias voltage	V _{LC1} , V _{LC2} , V _{LC3}	V _{SS}	V _{DD}	V	Liquid crystal power supply voltage* ¹
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ²
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin* ³
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ²
	V _{ILEX}	-0.3	0.4	V	EXTAL pin* ³
Operating temperature	T _{opr}	-20	+75	°C	

*¹ The optimum value is determined by the characteristics of the liquid crystal display element used.

*² They are the respective pins of INT1, WP, PX0, PX3, PY2, PY3 and \overline{RST} .

*³ Specified only during external clock input.

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PF*1, PX0 to PX2, PY0, PY1, VL (VOL only) RST (VOL only)	VDD = 4.5V, IOH = -0.5mA*2	4.0			V
			VDD = 4.5V, IOH = -1.0mA*2	3.5			V
			VDD = 4.5V, IOH = -10µA*3	4.0			V
			VDD = 4.5V, IOH = -200µA*3	2.4			V
Low level output voltage	VOL		VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
Input current	I _{IH}	EXTAL*4	VDD = 5.5V, VIH = 5.5V	0.5		40	µA
	I _{I_{LE}}			-0.5		-40	µA
	I _{I_{LR}}	RST*5	VDD = 5.5V, VIL = 0.4V	-1.5		-400	µA
	I _{I_L}	PA to PF*6, PX0 to PX2*6, PX3*8, PY0*7, PY1*7, PY2*8, PY3*8, INT1*8, WP*8, RST*5				-2.0	mA
High impedance I/O leakage current	I _{I_Z}		VDD = 5.5V VI = 0, 5.5V			±10	µA
Common output impedance	R _{COM}	COM0 to COM3	VDD = 5V VLC1 = 3.75V		3	5	kΩ
Segment output impedance	R _{SEG}	SEG0 to SEG15 SEG16 to SEG23*1	VLC2 = 2.5V VLC3 = 1.25V		5	15	kΩ
Current power supply	I _{DD}	VDD	VDD = 5.5V During external clock 1MHz operation Entire output pins open		1.3 (2)*9	4 (6)*9	mA
	I _{DDSP}			Sleep mode	0.4 (0.5)*9	1.2 (2)*9	mA
	I _{DD_S}			Stop mode		10	µA
Input capacitance	C _{IN}	VLC1 to VLC3, COM0 to COM3, SEG0 to SEG15, SEG16 to SEG23*1, Other pins than VDD, Vss	Clock 1MHz 0V for no measured pins		10	20	pF

*1 PE to PF show when the combined pins are selected as the port, and SEG16 to SEG23 show when the combined pins are selected as the segment output.

*2 It is when the respective pins of PA to PF and PX0 to PX2 select the 3-state output circuit, and PY0 and PY1 are when the inverter output circuit is selected.

*3 It is when the respective pins of PA to PF, PX0 to PX2, PY0 and PY1 select the pull-up resistance.

*4 It is when the crystal or ceramic oscillation circuit is selected.

*5 The RST pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

*6 The respective pins of PA to PF and PX0 to PX2 specify the input current when the pull-up resistance is selected, and specify the leakage current when in the port state during the 3-state output circuit or standby is selected at high impedance.

*7 The respective pins of PY0 and PY1 specify the input current when the pull-up resistance is selected, and specify the leakage current when the port state during standby is selected at high impedance.

*8 The respective pins of PX3, PY2, PY3, INT1 and WP only specify the leakage current.

*9 The value in parentheses shows the specification of the current power supply of the high speed version.

AC characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1., Fig. 2.	1	5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1., Fig. 2.*1 External clock drive	90		ns
System clock input rising and falling times	t_{CR} t_{CF}	EXTAL	Fig. 1., Fig. 2.*1 External clock drive		200	ns
Event count clock input pulse width	t_{EL} t_{EH}	\overline{EC}	Fig. 3.	$t_{sys}^{*2} + 0.05$		μs
Event count clock input rising and falling times	t_{ER} t_{EF}	\overline{EC}	Fig. 3.		20	ms

*1 The external clock in Fig. 2. is specified only when the option is selected for crystal or ceramic oscillation.

*2 In the standard version, $t_{sys} = 16/f_c$

In the high speed version, $t_{sys} = 8/f_c$

Note) When adjusting the frequency accurately, there may be cases in which they differ from Fig. 2.

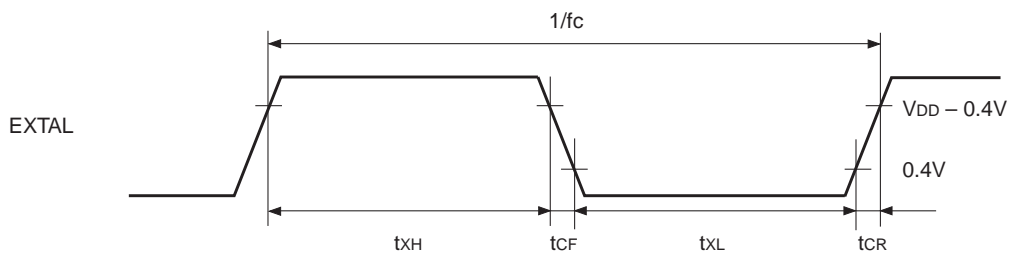


Fig. 1. Clock timing

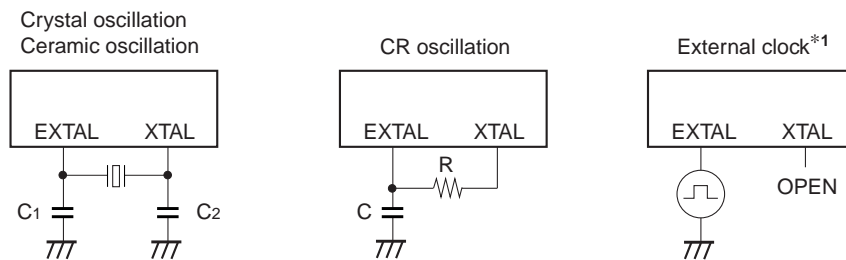


Fig. 2. Clock applying condition

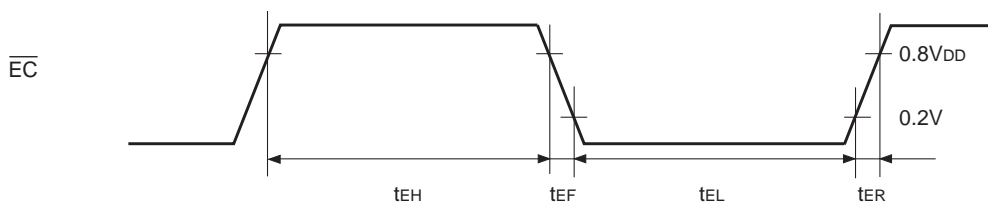


Fig. 3. Event count clock timing

(2) Serial transfer

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock (\overline{SC}) cycle time	t_{KCY}	\overline{SC}	Input mode	$t_{sys}/4 + 1.42$		μs
			Output mode	t_{sys}		μs
Serial transfer clock (\overline{SC}) high and low level widths	t_{KH} t_{KL}	\overline{SC}	Input mode	$t_{sys}/8 + 0.7$		μs
			Output mode*1	$t_{sys}/2 - 0.1$		μs
			Output mode*2	$t_{sys}/2 - 1.6$		μs
Serial data input setup time (against $\overline{SC} \uparrow$)	t_{SIK}	SI	\overline{SC} input mode	0.1		μs
			\overline{SC} output mode	0.2		μs
Serial data input hold time (against $\overline{SC} \uparrow$)	t_{KSI}	SI	\overline{SC} input mode	$t_{sys}/8 + 0.5$		μs
			\overline{SC} output mode	0.1		μs
High data*3 output delay time from the \overline{SC} falling time	t_{KSOA}	SOA			$t_{sys}/8 + 0.5$	μs
	t_{KSOB}	SOB				
High data*4 output delay time from the \overline{SC} falling time	t_{KSOA}	SOA			$t_{sys}/8 + 1.6$	μs
	t_{KSOB}	SOB				
Low data output delay time from the \overline{SC} falling time	t_{KSOA}	SOA			$t_{sys}/8 + 0.5$	μs
	t_{KSOB}	SOB				

*1 It is specified when \overline{SC} pin is selected to the 3-state output by the mask option.

*2 It is specified when \overline{SC} pin is selected to the pull-up resistance by the mask option. As the t_{sys} receives restriction by this item, take notice that it limits the upper limit of the system clock frequency f_c .

*3 It is specified when SOA and PX1/SOB pins are selected to the 3-state output by the mask option.

*4 It is specified when SOA and PX1/SOB pins are selected to the pull-up resistance by the mask option.

Note 1) In the standard version, $t_{sys} = 16/f_c$

In the high speed version, $t_{sys} = 8/f_c$

Note 2) The load of data output delay time is 50pF + 1TTL.

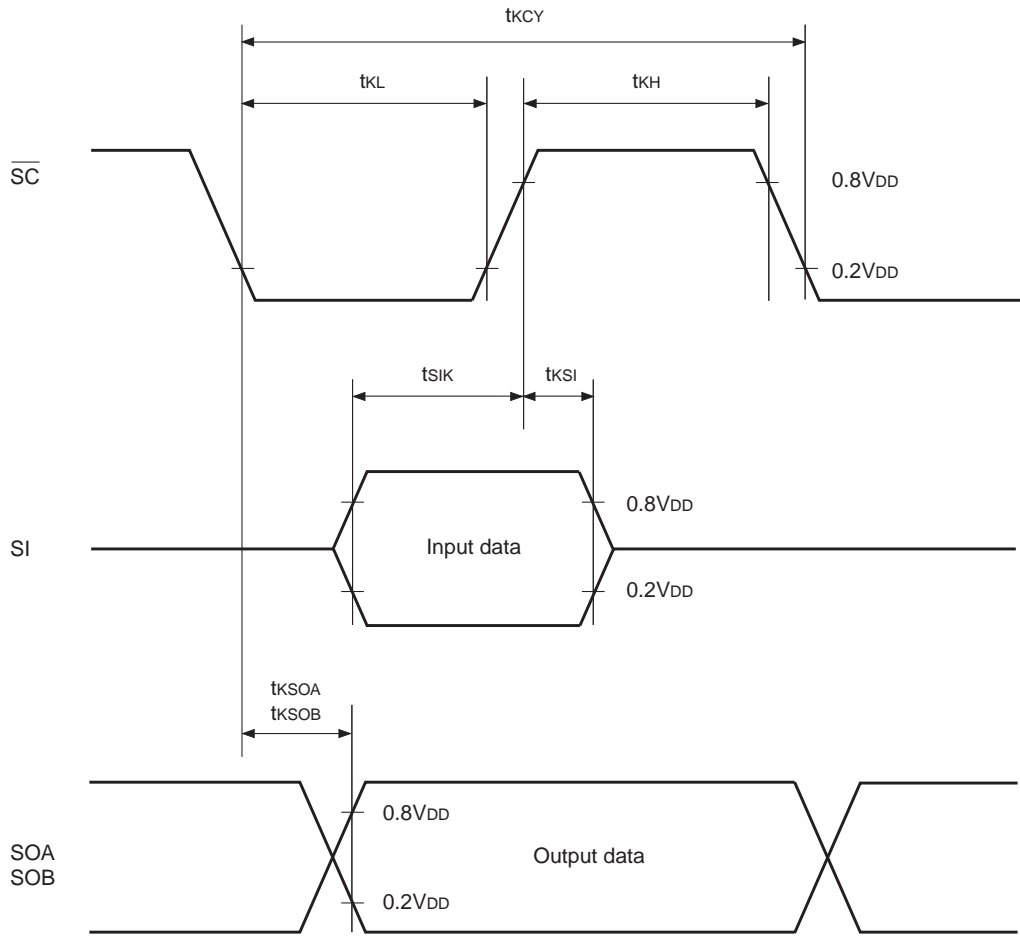


Fig. 4. Serial transfer timing

(3) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{I1H} , t_{I1L}	INT1	During edge detection mode	$t_{sys} + 0.05$		μs
	t_{I2H} , t_{I2L}	INT2		$t_{sys} + 0.05$		μs
Reset input low level width	t_{RSL}	\overline{RST}		$2t_{sys}$		μs
Wake-up input high level width	t_{WPH}	WP	Stop mode	500		ns
			Sleep mode	$t_{sys} + 0.05$		μs

Note) In the standard version, $t_{sys} = 16/f_c$
 In the high speed version, $t_{sys} = 8/f_c$

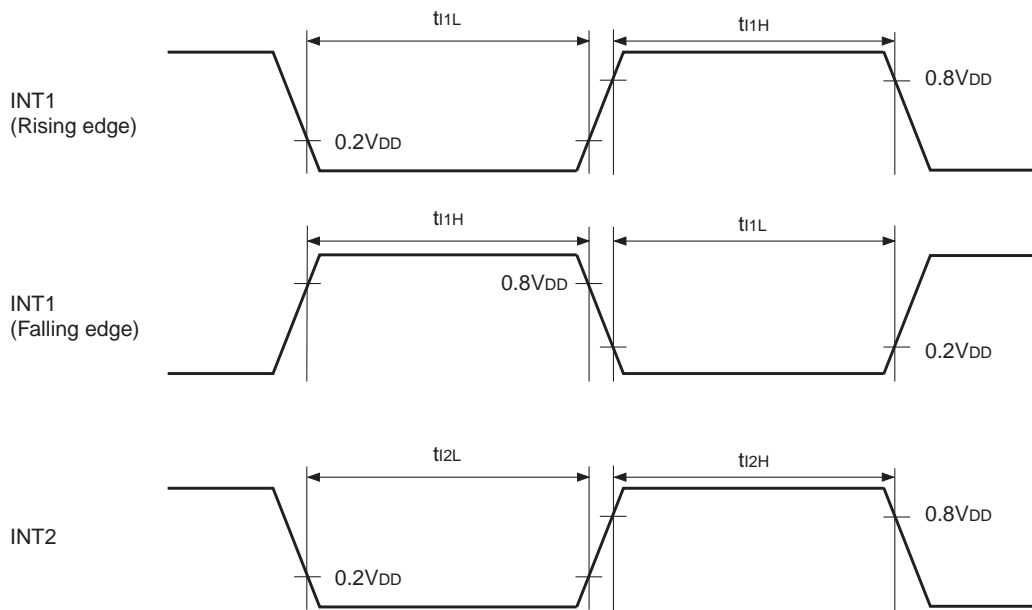


Fig. 5. Interruption input timing

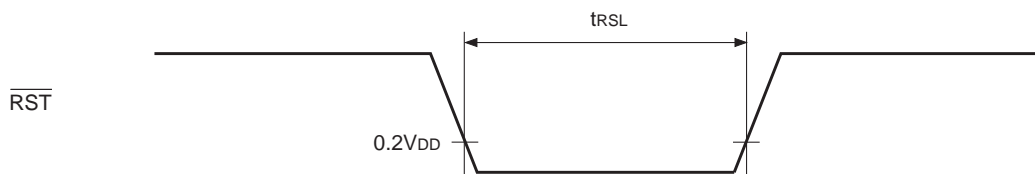


Fig. 6. Reset input timing

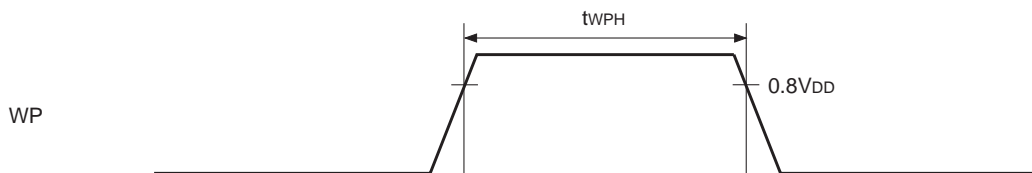


Fig. 7. Wake-up input timing

Power on reset*

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t _R	V _{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t _{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



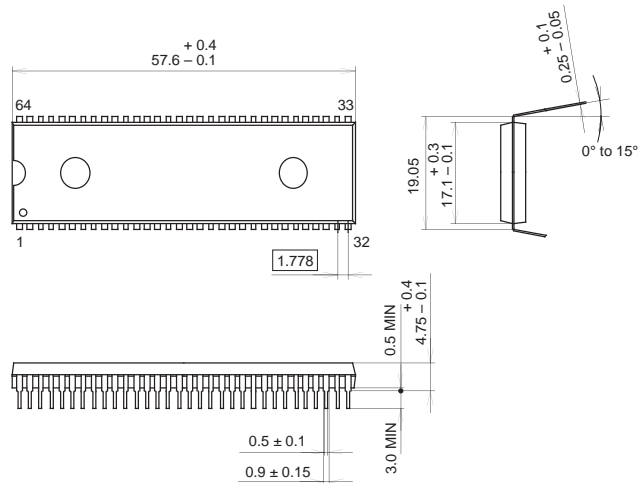
Raise the power supply smoothly.

Fig. 8. Power on reset

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

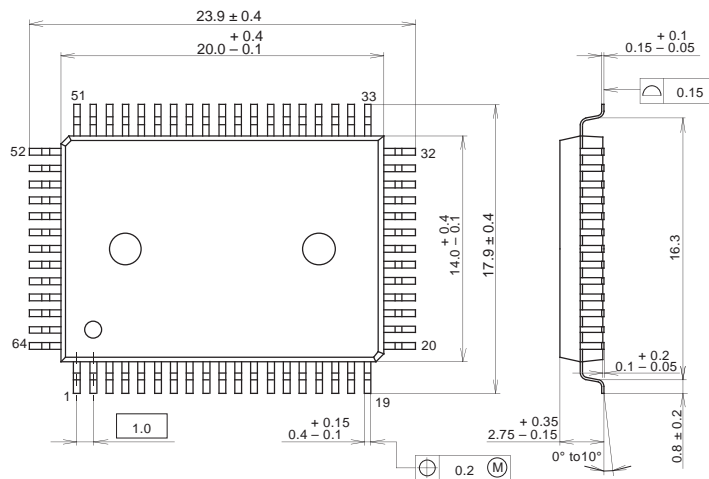


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g