SONY

CXP740056/740096/740010

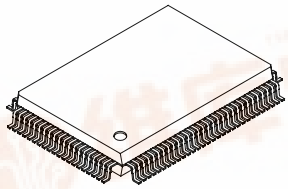
CMOS 8-bit Single Chip Microcomputer

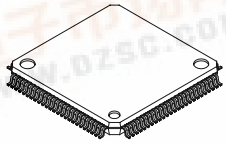
Description

The CXP740056/740096/740010 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, remote control receive circuit, PWM output, and the like besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP740056/740096/740010 also provides the sleep/stop functions that enables lower power consumption.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)





Structure

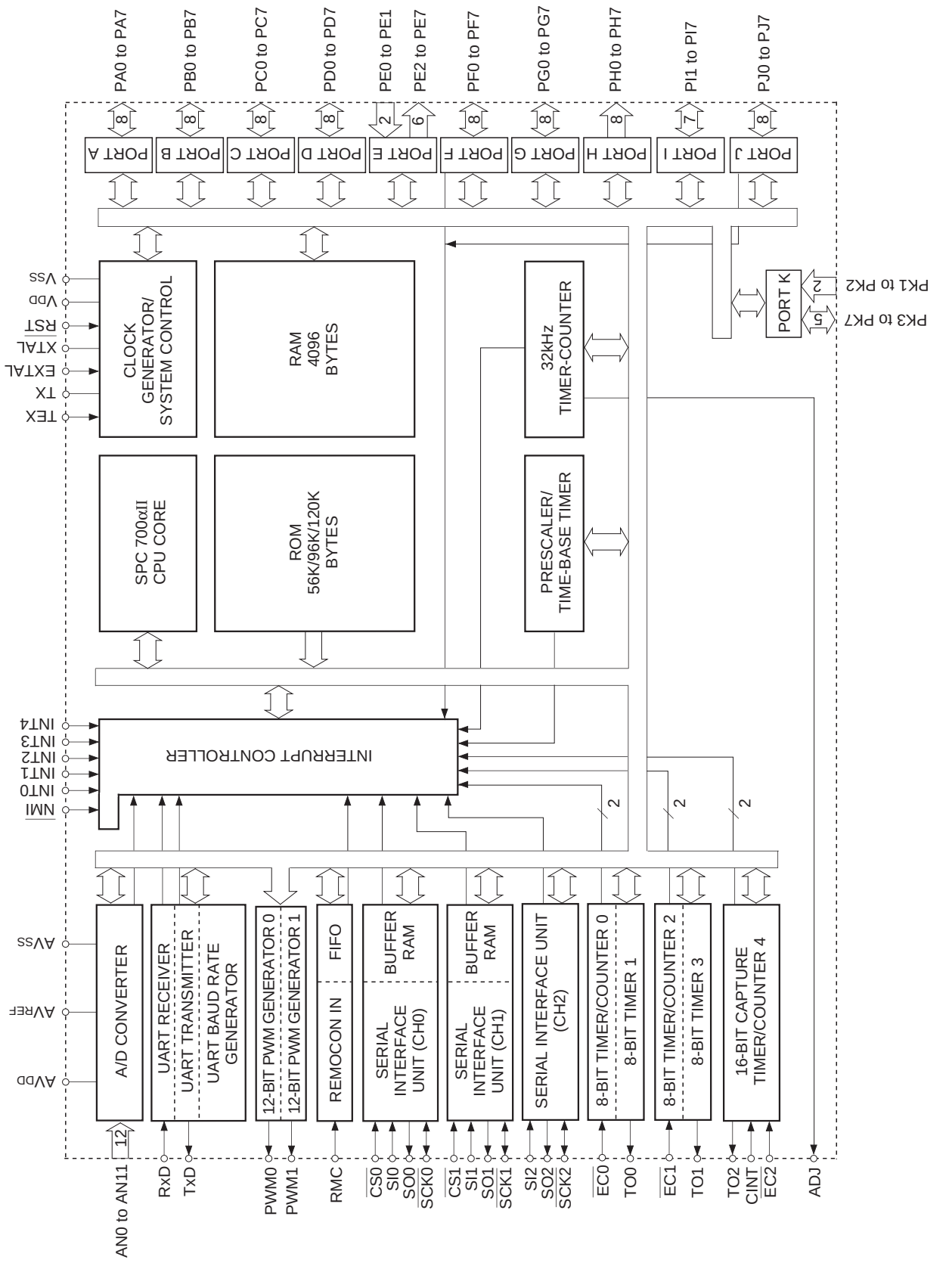
Silicon gate CMOS IC

Features

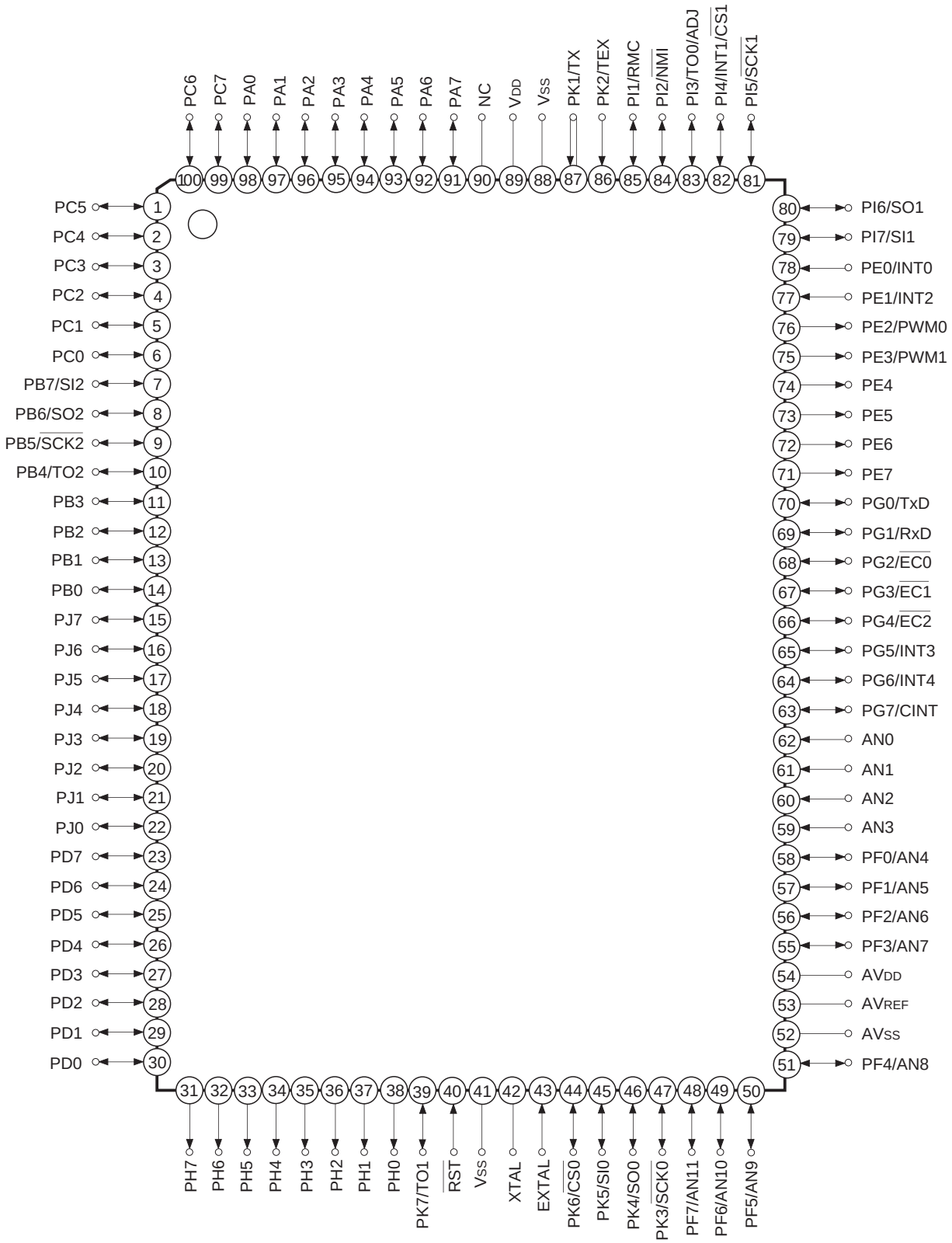
- A wide instruction set (211 instructions) which covers various types of data.
  — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
  167ns at 24MHz operation (4.5 to 5.5V)
  333ns at 12MHz operation (2.7 to 5.5V)
  122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
  56K bytes (CXP740056)
  96K bytes (CXP740096)
  120K bytes (CXP740010)
- Incorporated RAM capacity
  4096 bytes
- Peripheral functions
  — A/D converter
  8 bits, 8 channels, successive approximation method
  (Conversion time 10.3µs at 24MHz)
  — Serial interface
  Srart-stop synchronization (UART), 1 channel
  Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 2 channels
  8-bit clock syncronization (MSB/LSB first selectable), 1 channel
  — Timer
  8-bit timer 2 channels, 8-bit timer/counter 2 channels,
  19-bit time-base timer, 16-bit capture timer/counter
  32kHz timer/counter
  — Remote control receive circuit
  Noise elimination circuit
  8-bit pulse measuring counter, 6-stage FIFO
  — PWM output
  12 bits, 2 channels
- Interruption
  22 factors, 15 vectors, multi-interruption possible
- Standby mode
  Sleep/stop
- Package
  100-pin plastic QFP/LQFP
- Piggy/evaluation chip
  CXP740000

E98406-PS

Block Diagram



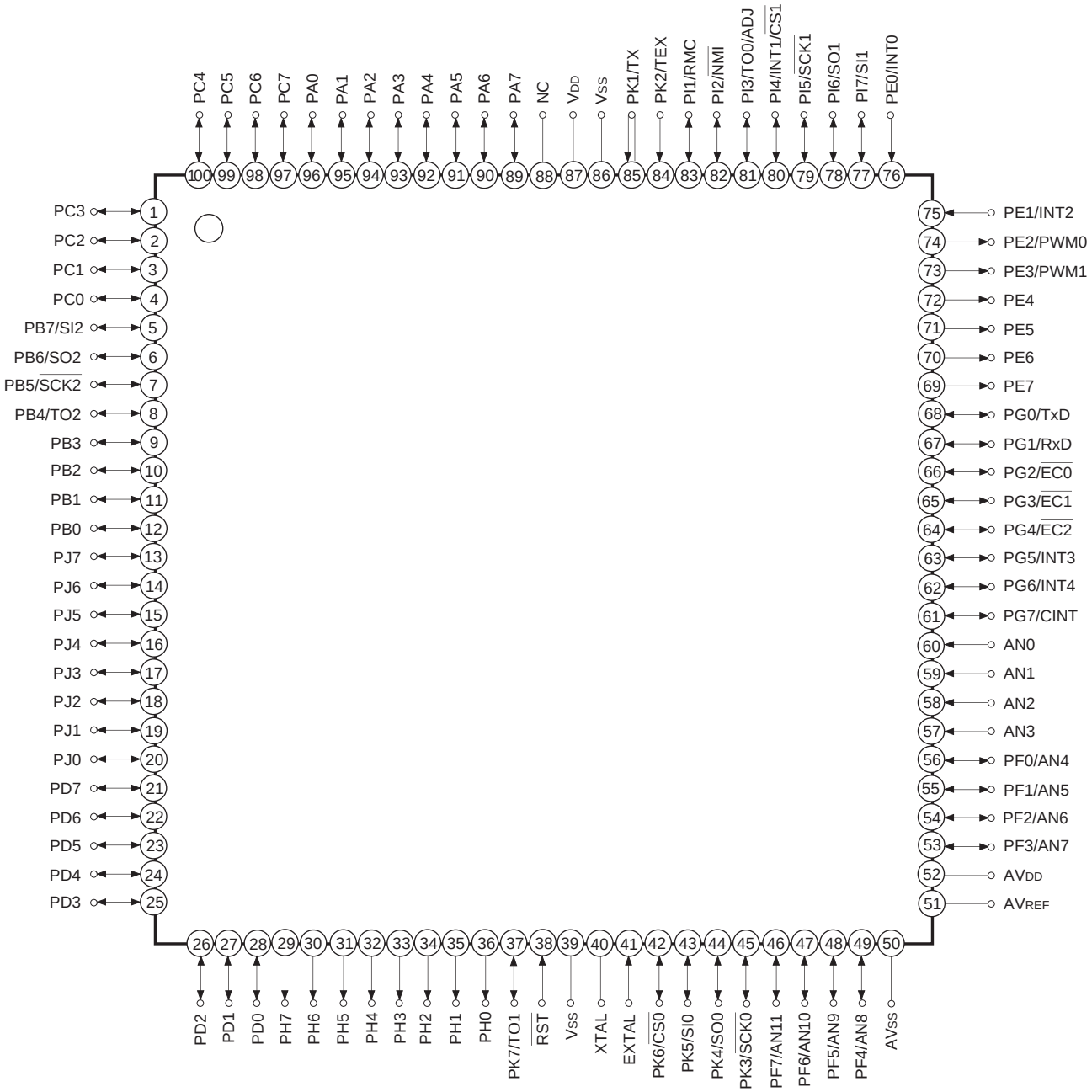
Pin Assignment (Top View) 100-pin QFP package



Note) 1. NC (Pin 90) is left open.

2. VSS (Pins 41 and 88) are both connected to GND.

Pin Assignment (Top View) 100-pin LQFP package



Note) 1. NC (Pin 88) is left open.

2. VSS (Pins 39 and 86) are both connected to GND.

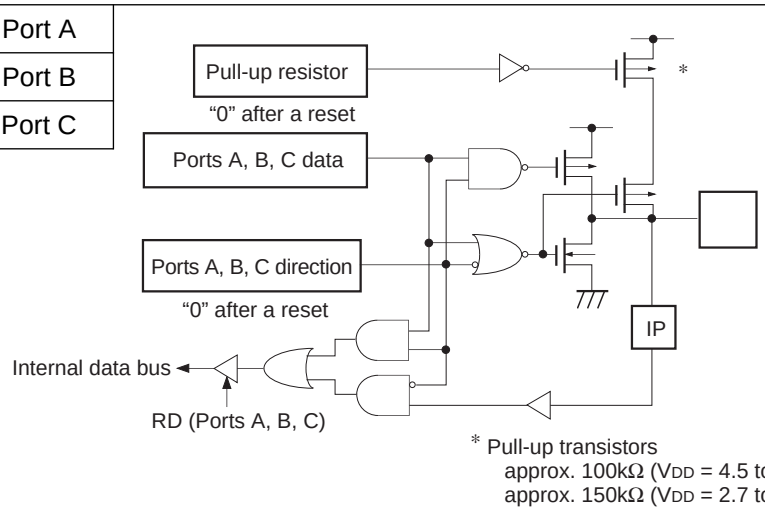
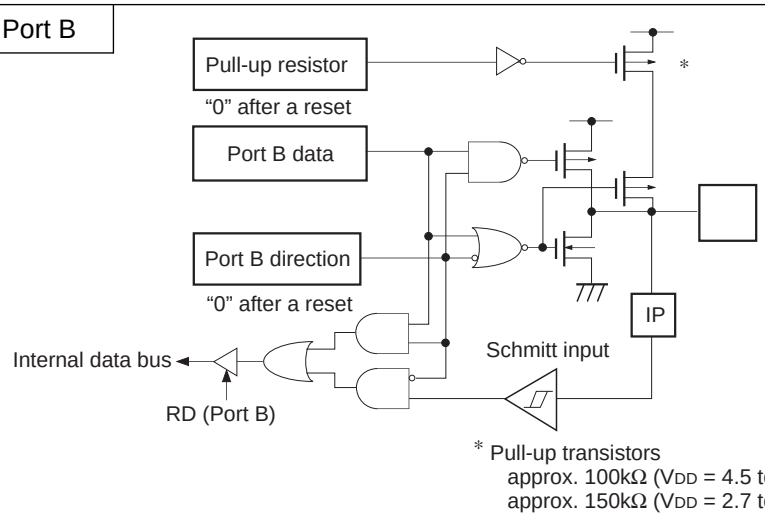
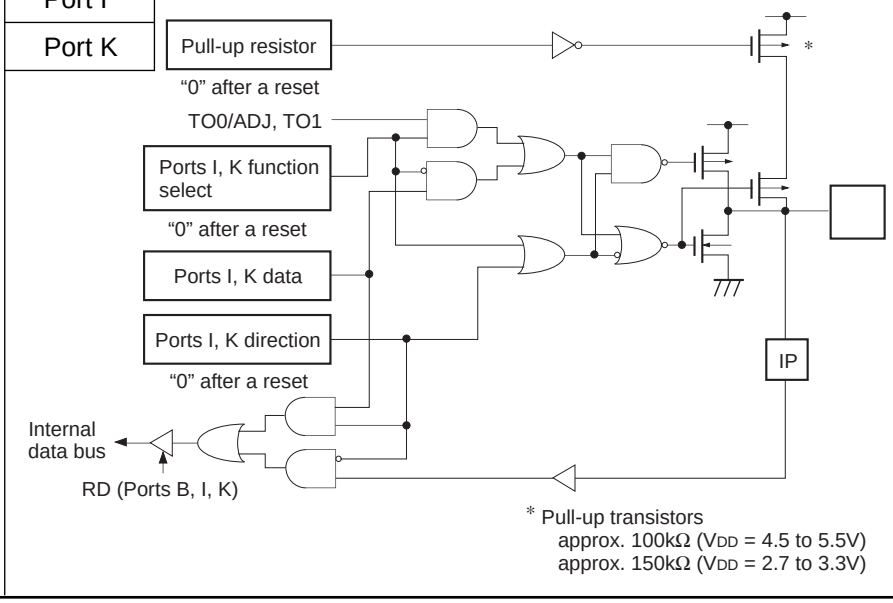
Pin Description

Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PB0 to PB3	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PB4/TO2	I/O/Output		16-bit timer/counter rectangular wave output.
PB5/$\overline{\text{SCK2}}$	I/O/I/O		Serial clock I/O (CH2).
PB6/SO2	I/O/Output		Serial data output (CH2).
PB7/SI2	I/O/Input		Serial data input (CH2).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PE0/INT0	Input/Input	(Port E) 8-bit port. Lower 2 bits are for input; upper 6 bits are for output. (8 pins)	External interrupt inputs. (2 pins)
PE1/INT1	Input/Input		
PE2/PWM0	Output/Output		12-bit PWM outputs. (2 pins)
PE3/PWM1	Output/Output		
PE4 to PE7	Output		
PF0/AN4 to PF7/AN11	I/O	(Port F) 8-bit I/O port. PF4 to PF7 can be set in a unit of single bits as standby release inputs. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (8 pins)

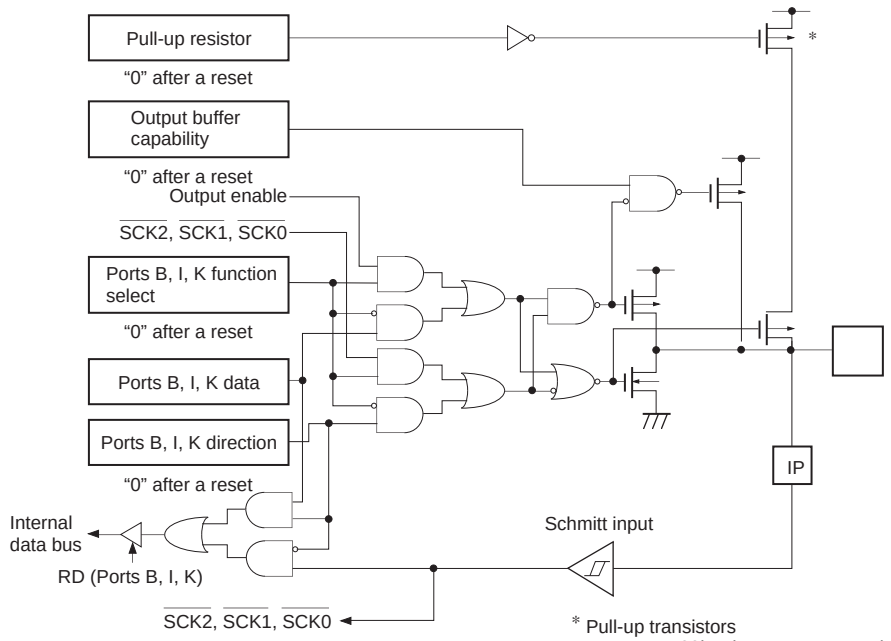
Symbol	I/O	Description	
PG0/TxD	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	UART transmission data output.
PG1/RxD	I/O/Input		UART reception data input.
PG2/$\overline{EC0}$	I/O/Input		External event input for 8-bit timer/counter 0.
PG3/$\overline{EC1}$	I/O/Input		External event input for 8-bit timer/counter 2.
PG4/$\overline{EC2}$	I/O/Input		External event input for 16-bit timer/counter.
PG5/INT3	I/O/Input		External interrupt inputs. (2 pins)
PG6/INT4	I/O/Input		
PG7/CINT	I/O/Input		External capture input to 16-bit timer/counter.
PH0 to PH7	Output	(Port H) 8-bit I/O port. Operated as N-ch open drain output for medium voltage drive (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Remote control receiver circuit input.
PI2/$\overline{NMI}$	I/O/Input		Non-maskable interrupt input.
PI3/TO0/ ADJ	I/O/Output/ Output		Output for the 8-bit timer/counter 1 rectanguler waves and 32-kHz oscillation frequency demultiplication.
PI4/INT1/ $\overline{CS1}$	I/O/Input/ Input		External interrupt input. / Chip select input for serial interface (CH1).
PI5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PI6/SO1	I/O/Output		Serial data output (CH1).
PI7/SI1	I/O/Input		Serial data input (CH1).
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. I/O can be set in a unit of single bits. Standby release input can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PK1/TX	Input	(Port K) 7-bit port. lower 2 bits are for input; upper 5 bits are for I/O. I/O can be set in a unit of single bits. For PK3 to PK7, incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Crystal connectors for 32-kHz timer/counter clock oscillation circuit. For usage as event count, connect clock oscillation source to TEX, and leave TX open.
PK2/TEX	Input/Input		
PK3/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PK4/SO0	I/O/Output		Serial data output (CH0).
PK5/SI0	I/O/Input		Serial data input (CH0).
PK6/$\overline{CS0}$	I/O/Input		Chip select input for serial inteface (CH0).
PK7/TO1	I/O/Output		8-bit timer/counter 3 rectangular wave output.

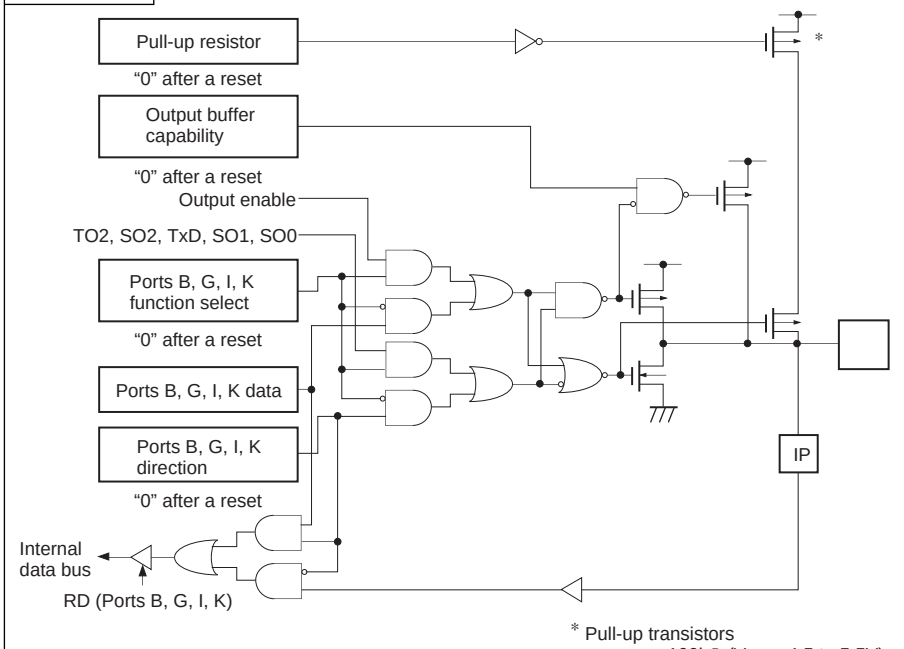
Symbol	I/O	Description
AN0 to AN3	Input	Analog inputs to A/D converter. (4 pins)
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL pin and input a reversed phase clock to XTAL pin.
XTAL		
$\overline{RST}$	Input	System reset; active at Low level.
NC		Not connected. Leave this pin open for normal operation.
AV_{DD}		Positive power supply of A/D converter.
AV_{REF}	Input	Reference voltage input of A/D converter.
AV_{SS}		GND of A/D converter.
V_{DD}		Positive power supply.
V_{SS}		GND. Connect both V_{SS} pins to GND.

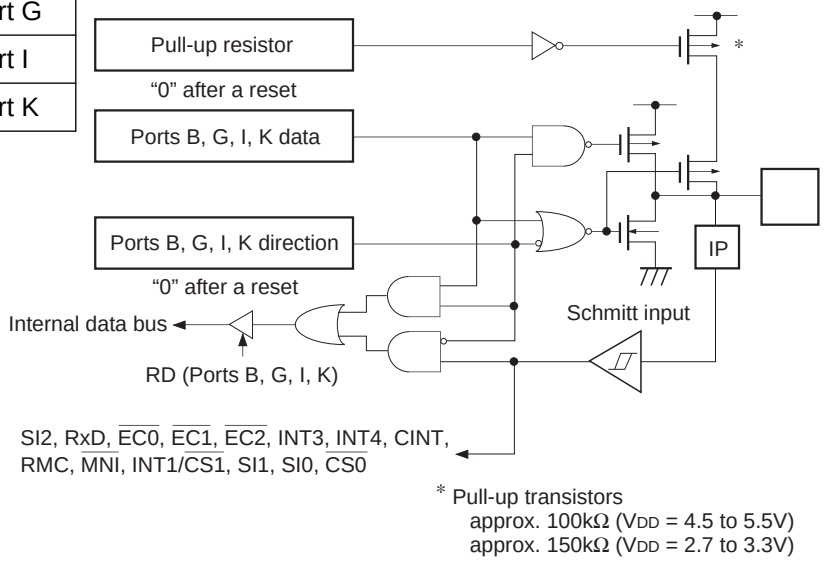
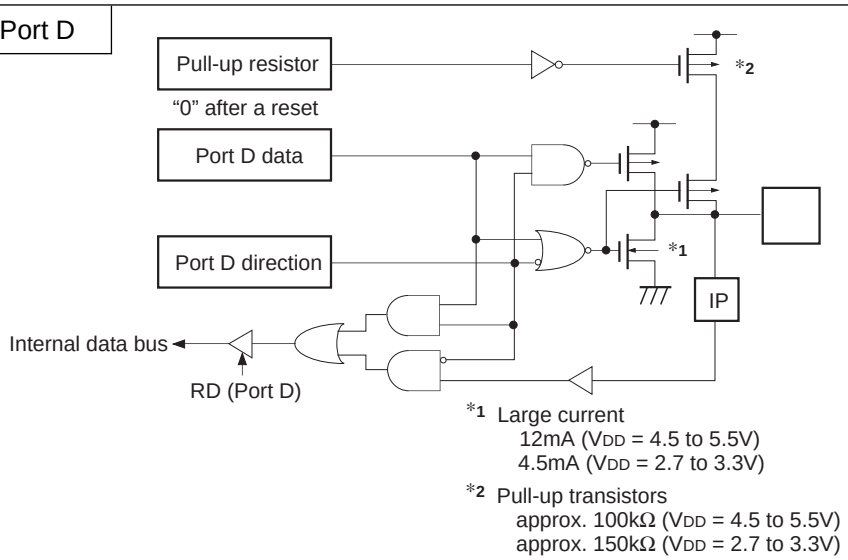
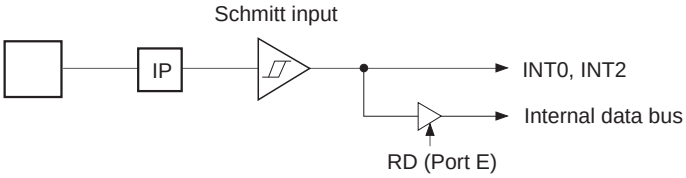
I/O Circuit Format for Pins

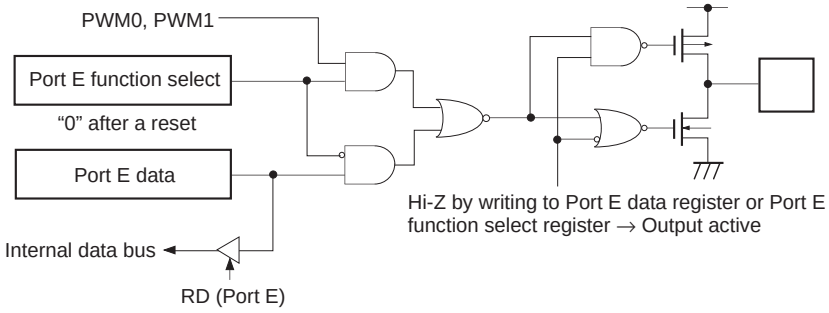
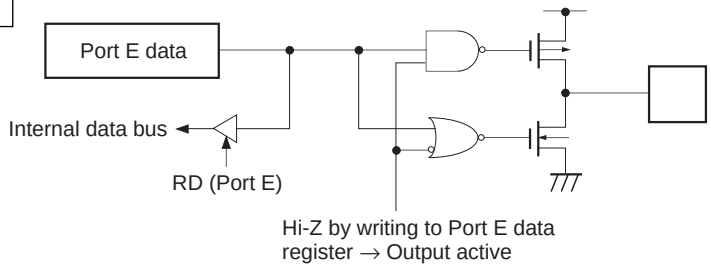
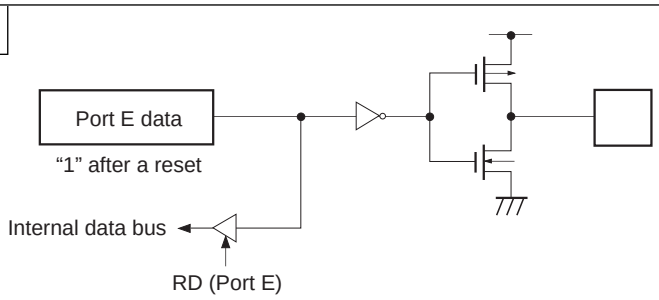
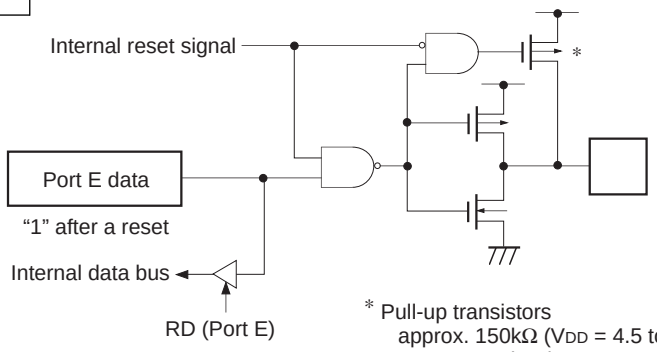
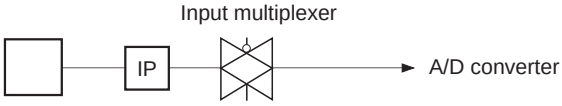
Pin	Circuit format	After a reset
PA0 to PA7 PB0 PB2 PC0 to PC7 18 pins	Port A Port B Port C 	Hi-Z
PB1 PB3 2 pins	Port B 	Hi-Z
PB4/TO2 PI3/TO0/ADJ PK7/TO1 3 pins	Port I Port K 	Hi-Z

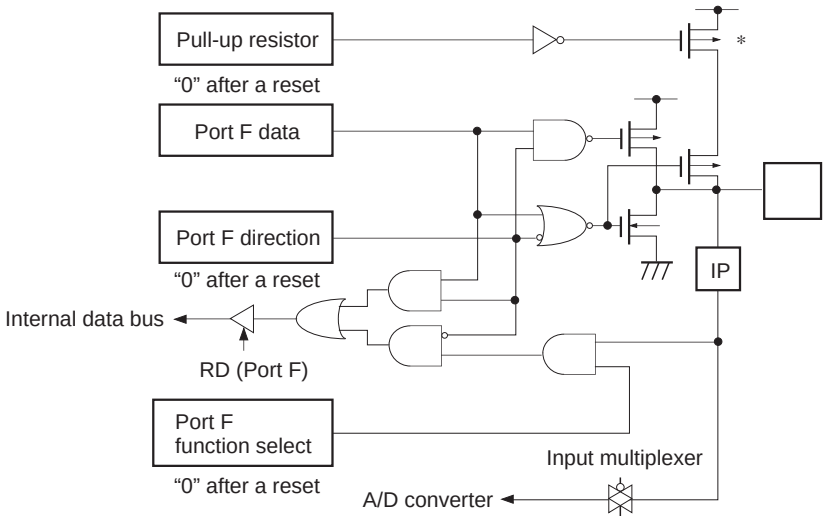
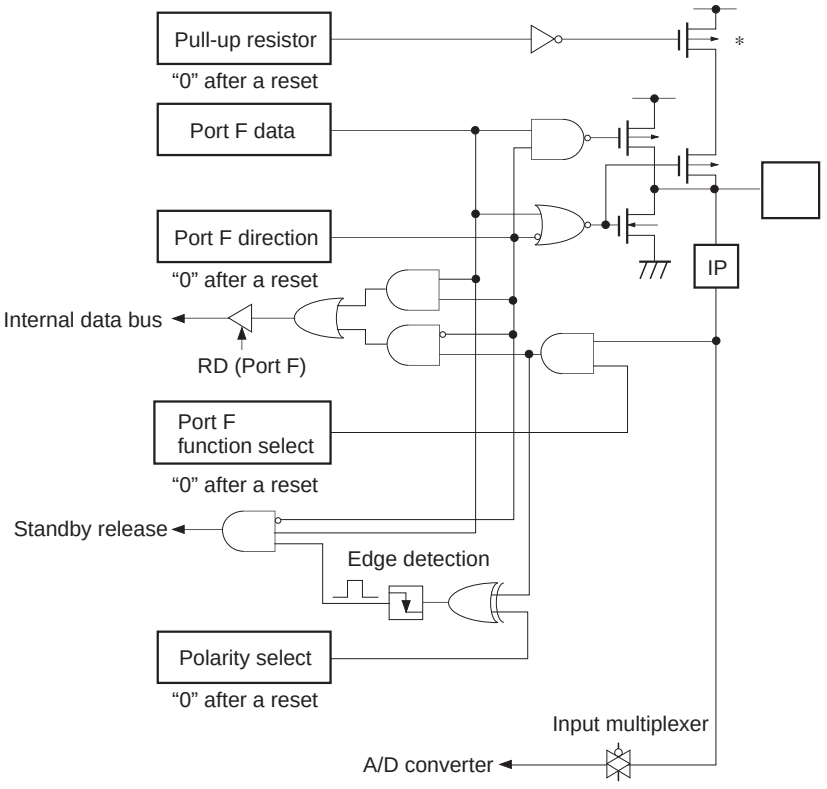
Pin	Circuit format	After a reset
PB5/$\overline{SCK2}$ PI5/$\overline{SCK1}$ PK3/$\overline{SCK0}$ 3 pins	Port B Port I Port K	Hi-Z
PB6/SO2 PG0/TxD PI6/SO1 PK4/SO0 4 pins	Port B Port G Port I Port K	Hi-Z

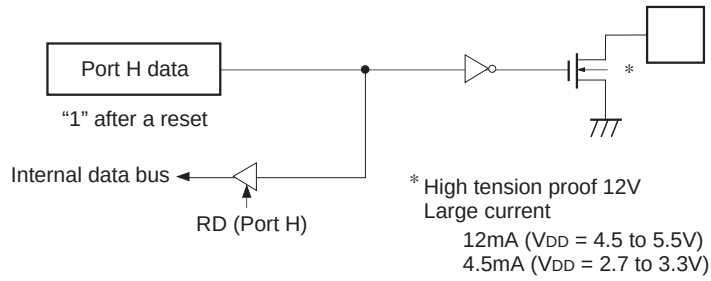
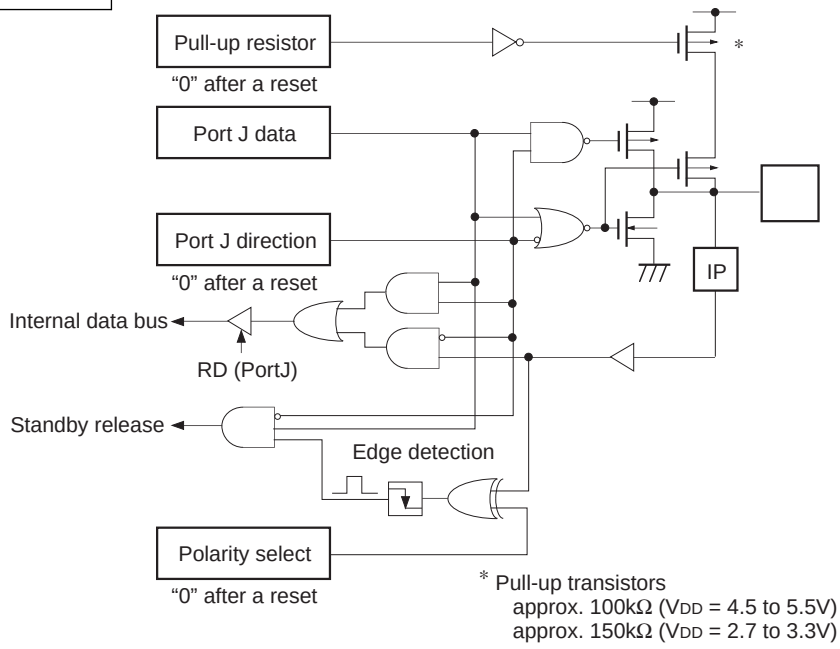
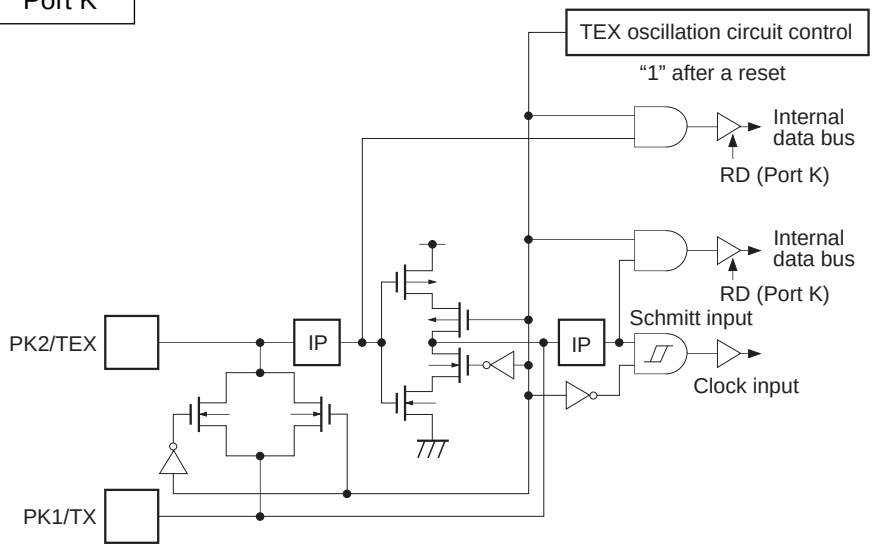


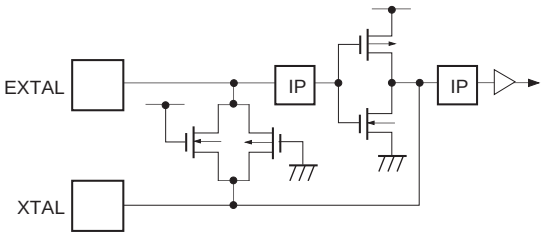
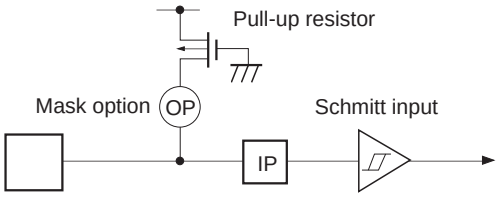


Pin	Circuit format	After a reset
PB7/SI2 PG1/RxD PG2/$\overline{EC0}$ PG3/$\overline{EC1}$ PG4/EC2 PG5/INT3 PG6/INT4 PG7/CINT PI1/RMC PI2/$\overline{NMI}$ PI4/INT1/$\overline{CS1}$ PI7/SI1 PK5/SI0 PK6/$\overline{CS0}$ 14 pins	Port B Port G Port I Port K 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z
PE0/INT0 PE1/INT2 2 pins	Port E 	Hi-Z

Pin	Circuit format	After a reset
PE2/PWM0 PE3/PWM1 2 pins	Port E 	Hi-Z
PE4 PE5 2 pins	Port E 	Hi-Z
PE6 1 pin	Port E 	High level
PE7 1 pin	Port E 	("H" level "H"level at ON resistance of pull-up transistor during a reset.)
AN0 to AN3 4 pins		Hi-Z

Pin	Circuit format	After a reset
PF0/AN4 to PF3/AN7 4 pins	Port F  * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F  * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z

Pin	Circuit format	After a reset
PH0 to PH7 8 pins	Port H  	Hi-Z
PJ0 to PJ7 8 pins	Port J  	Hi-Z
PK1/TX PK2/TEX 2 pins	Port K  	Oscillation stop port input

Pin	Circuit format	After a reset
EXTAL XTAL 2 pins	 • Diagram shows circuit configuration during oscillation. • When program stops the oscillation, the feedback registor disconnects, and XTAL is driven at "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin		"L" level (during a reset)

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
	AV_{REF}	AV_{SS} to +7.0	V	
Input voltagte	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	All pins excluding large current outputs (value per pin)
	I_{OLC}	20	mA	Large current outputs (value per pin) *3
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package
		380		LQFP package

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 The large current output pins are Port D and H (PD, PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = 24MHz or less	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock.
		2.7	5.5	V	fc = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode	
		2.7	5.5	V	Guaranteed operation range for TEX	
		2.5	5.5	V	Guaranteed data hold operation range during stop mode	
Analog voltage	AV_{DD}	2.7	5.5	V	*1	
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2, *6	
		0.8V_{DD}	V_{DD}	V	*2, *7	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*3	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4, *6, TEX pin*5, *6	
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL pin*4, *7, TEX pin*5, *7	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *6	
		0	0.2V_{DD}	V	*2, *7	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*3	
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4, *6, TEX pin*5, *6	
		–0.3	0.2	V	EXTAL pin*4, *7, TEX pin*5, *7	
Operating temperature	Topr	–20	+75	°C		

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 Normal input port (PA, PB0, PB2, PB4, PB6, PC, PD, PF, PG0, PI3, PI6, PJ, PK1, PK2, PK4, PK7)

*3 $\overline{RST}$, PB1, PB3, PB5/$\overline{SCK2}$, PB7/SI2, PE0/INT0, PE1/INT2, PG1/RxD, PG2/$\overline{EC0}$, PG3/$\overline{EC1}$, PG4/$\overline{EC2}$, PG5/INT3, PG6/INT4, PG7/CINT, PI1/RMC, PI2/$\overline{NMI}$, PI4/INT1/$\overline{CS1}$, PI5/$\overline{SCK1}$, PI7/SI1, PK3/$\overline{SCK0}$, PK5/SI0, PK6/$\overline{CS0}$

*4 Specifies only when the external clock is input.

*5 Specifies only when the external event count is input.

*6 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*7 This case applies to the range of 2.7 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
		PB5, PB6*1, PG0*1, PI5, PI6*1, PK3, PK4*1	V_{DD} = 4.5V, I_{OH} = –1.0mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –2.4mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PD*3, PF to PG*3, PI to PK*3				–45	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}	PA to PD*3, PF to PG*3, PI to PK*3, PE, AN0 to AN3 $\overline{RST}$*2	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr off state)	L_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I_{DD1}	V_{DD}	24MHz crystal oscillation ($C_1 = C_2 = 15pF$) $V_{DD} = 5V \pm 0.5V$		27	47	mA
	I_{DDS1}		Sleep mode $V_{DD} = 5V \pm 0.5V$		1.0	5.0	mA
	I_{DD2}		32kHz crystal oscillation ($C_1 = C_2 = 47pF$) $V_{DD} = 3V \pm 0.3V$		30	75	µA
	I_{DDS2}		Sleep mode $V_{DD} = 3V \pm 0.3V$		12	40	µA
	I_{DDS3}		Stop mode (Termination of EXTAL and TEX pins crystal oscillation) $V_{DD} = 5V \pm 0.5V$			10	µA
Input capacity	C_{IN}	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0= "1, 1, 1, 1, 1") are ON.

*2 $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

*4 When all pins are open.

Electrical Characteristics

DC Characteristics (V_{DD} = 2.7 to 3.3V) (Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	V_{DD} = 2.7V, I_{OH} = –0.12mA	2.5			V
			V_{DD} = 2.7V, I_{OH} = –0.45mA	2.1			V
		PB5, PB6*1, PG0*1, PI5, PI6*1, PK3, PK4*1	V_{DD} = 2.7V, I_{OH} = –0.24mA	2.5			V
			V_{DD} = 2.7V, I_{OH} = –0.9mA	2.1			V
Low level output voltage	V_{OL}	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	V_{DD} = 2.7V, I_{OL} = 1.0mA			0.25	V
			V_{DD} = 2.7V, I_{OL} = 1.4mA			0.4	V
		PD, PH	V_{DD} = 2.7V, I_{OL} = 4.5mA			0.9	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.3V, V_{IH} = 3.3V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.3V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.3V, V_{IL} = 3.3V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.3V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 3.3V, V_{IL} = 0.3V	–0.9		–200	µA
	I_{IL}	PA to PD*3, PF to PG*3, PI to PK*3				–20	µA
			V_{DD} = 3.3V, V_{IL} = 2.7V	–1.0			µA
I/O leakage current	I_{IZ}	PA to PD*3, PF to PG*3, PI to PK*3, PE, AN0 to AN3, $\overline{RST}$*2	V_{DD} = 3.3V V_I = 0, 3.3V			±10	µA
Open drain output leakage current (N-ch Tr off state)	L_{LOH}	PH	V_{DD} = 3.3V V_{OH} = 12V			50	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I_{DD1}	V_{DD}	12MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 3.0V ± 0.3V*3		8	20	mA
	I_{DDS1}		Sleep mode V_{DD} = 3.0V ± 0.3V		0.3	1.5	mA
	I_{DDS3}		Stop mode (Termination of EXTAL and TEX pins crystal oscillation) V_{DD} = 3.0V ± 0.3V			10	µA
Input capacity	C_{IN}	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0 = "1, 1, 1, 1, 1") are ON.

*2 $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

*4 When all pins are open.

AC Characteristics

(1) Clock timing (Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1		24	MHz
				1		12	
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	28			ns
			External clock drive	37.5			
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise time, fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 000FEh).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

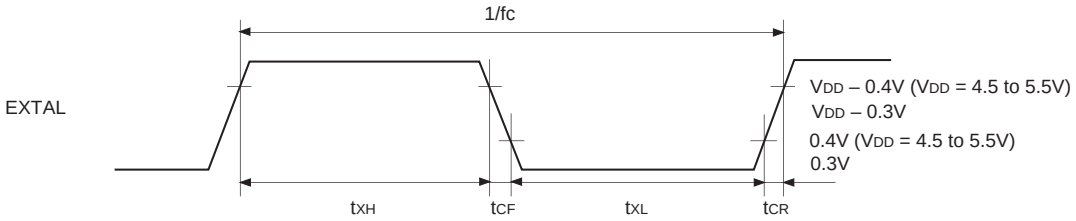


Fig. 1. Clock timing

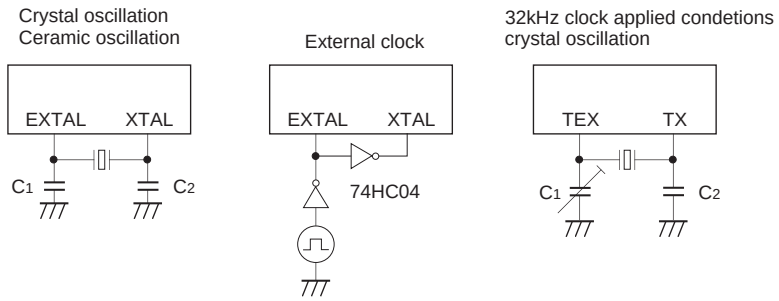


Fig. 2. Clock applied conditions

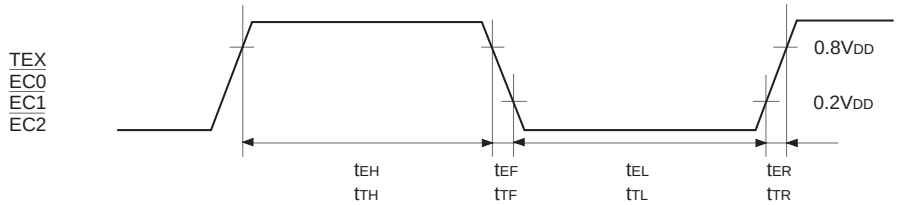


Fig. 3. Event count clock timing

(2) Serial transfer (CH0, CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS}\uparrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0 SO1	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0 SI1	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0 SI1	$\overline{SCK}$ input mode	2tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Note 4) This case applies that Port I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "0, 0, 0, 0") is OFF.

Serial transfer (CH0, CH1) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 250	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		1.5tsys + 250	ns
$\overline{CS}\uparrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0 SO1	Chip select transfer mode		1.5tsys + 250	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0 SI1	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0 SI1	$\overline{SCK}$ input mode	2tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Note 4) This case applies that Port G/I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "1, 1, 1, 1") is ON.

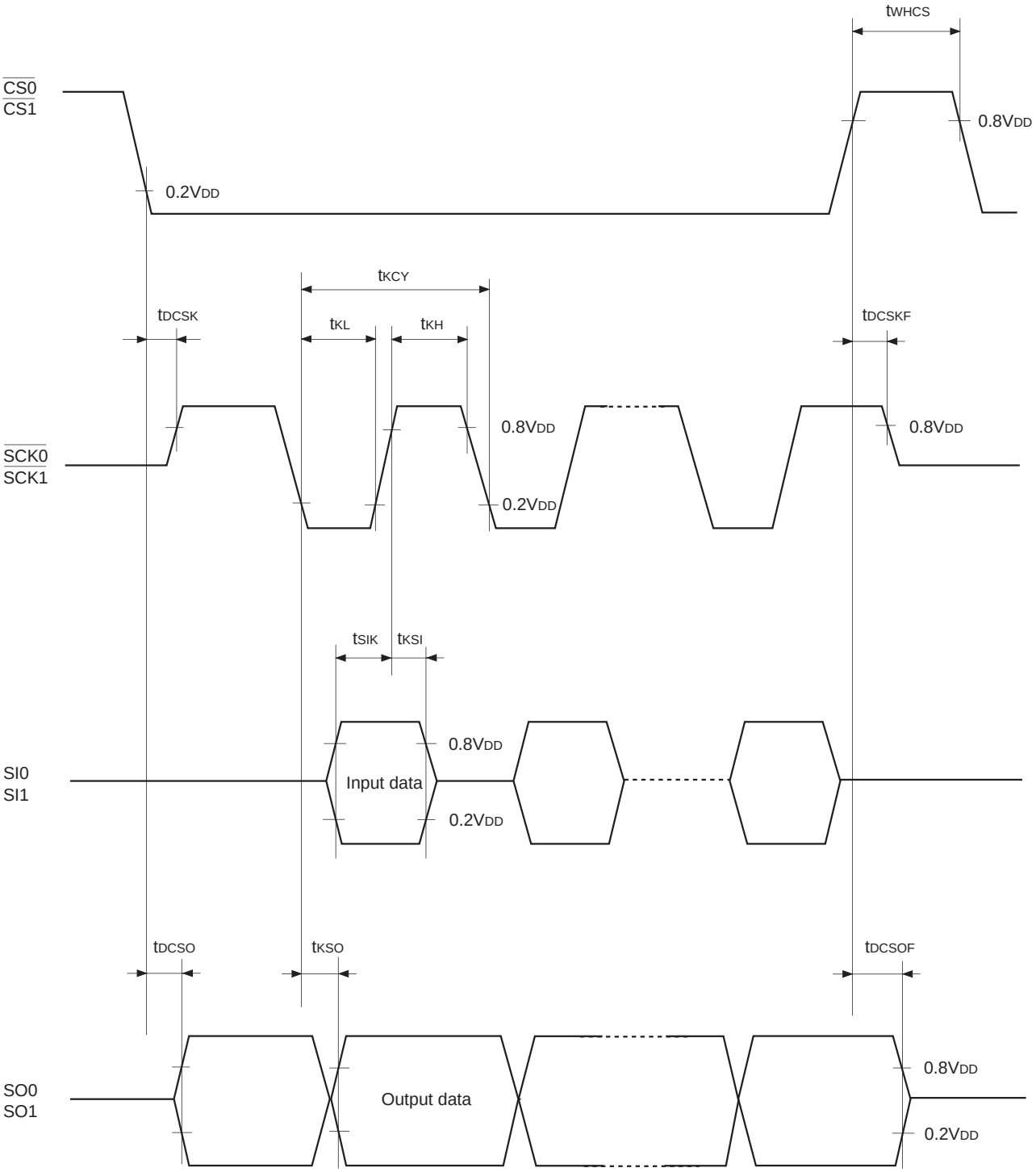


Fig. 4. Serial transfer CH0, CH1 timing

Serial transfer (CH2) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK2}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK2}$	Input mode	400		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI2	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow \rightarrow$ SO delay time	t_{KSO}	SO2	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK2}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{SCK2}$ output mode and SO2 output delay time is 50pF+1TTL.

Note 4) This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = “0, 0”) is OFF.

Serial transfer (CH2) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK2}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK2}$	Input mode	400		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI2	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow \rightarrow$ SO delay time	t_{KSO}	SO2	$\overline{SCK}$ input mode		250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK2}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{SCK2}$ output mode and SO2 output delay time is 50pF.

Note 4) This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = “1, 1”) is ON.

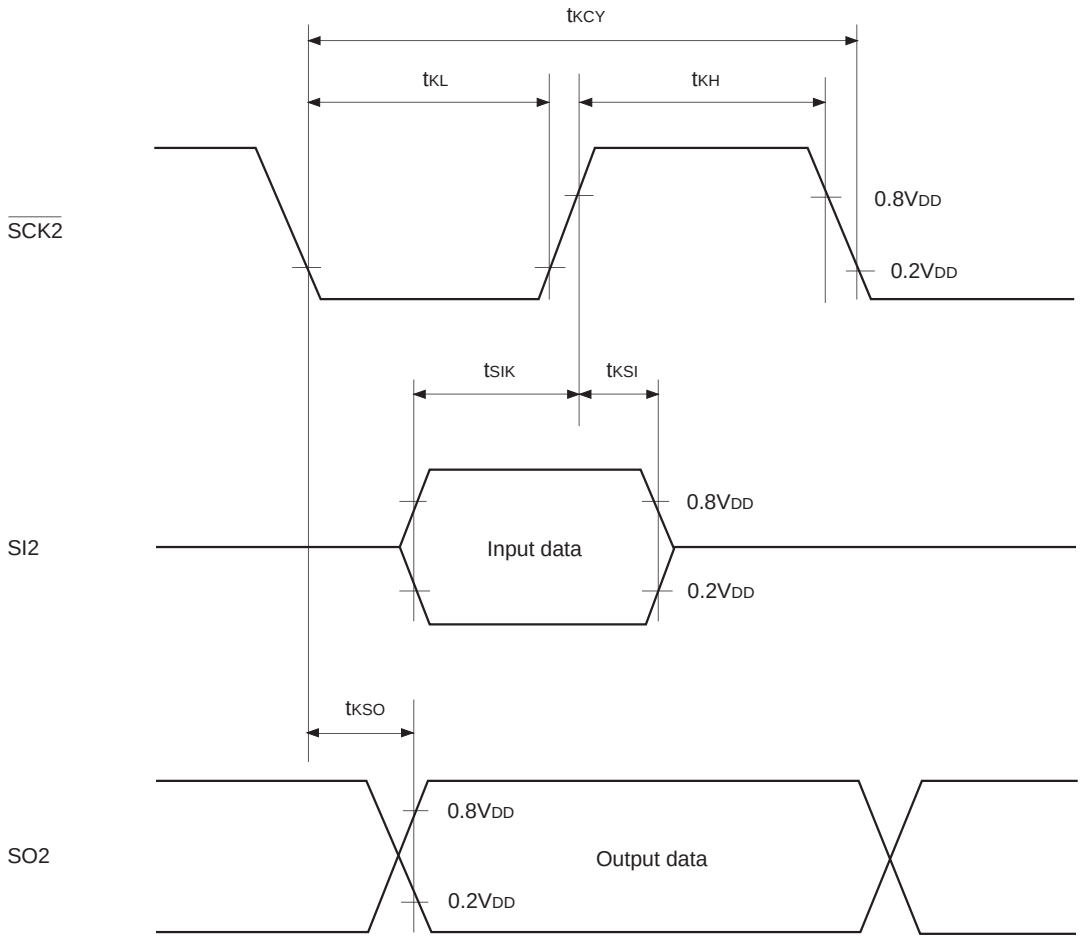


Fig. 5. Serial transfer CH2 timing

(3) A/D converter characteristics

(Ta = –20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity errror			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±2	LSB
Absolute error						±3	LSB
Conversion time	t_{CONV}			31/f_{ADC}*3, *4			µs
Sampling time	t_{SAMP}			10/f_{ADC}*3, *4			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} – 0.5			V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	µA

(Ta = –20 to +75°C, V_{DD} = AV_{DD} = 2.7 to 3.3V, AV_{REF} = 2.7 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity errror			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 3.0V V_{SS} = AV_{SS} = 0V			±2	LSB
Absolute error						±3	LSB
Conversion time	t_{CONV}			31/f_{ADC}*3, *4			µs
Sampling time	t_{SAMP}			10/f_{ADC}*3, *4			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 2.7 to 3.3V	AV_{DD} – 0.3			V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.4	0.7	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	µA

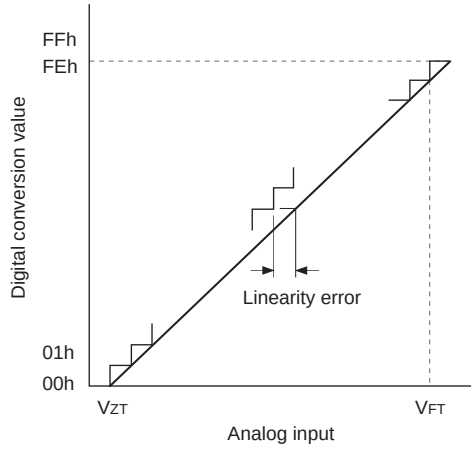


Fig. 6. Definition of A/D converter terms

*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 000F9h).

PS3 selected f_{ADC} = fc/4

PS4 selected f_{ADC} = fc/8

However, when PS3 is selected, fc is 12MHz or less.

*4 Sub clock operated t_{CONV} = 34/f_{TEX}

t_{SAMP} = 10/f_{TEX}

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

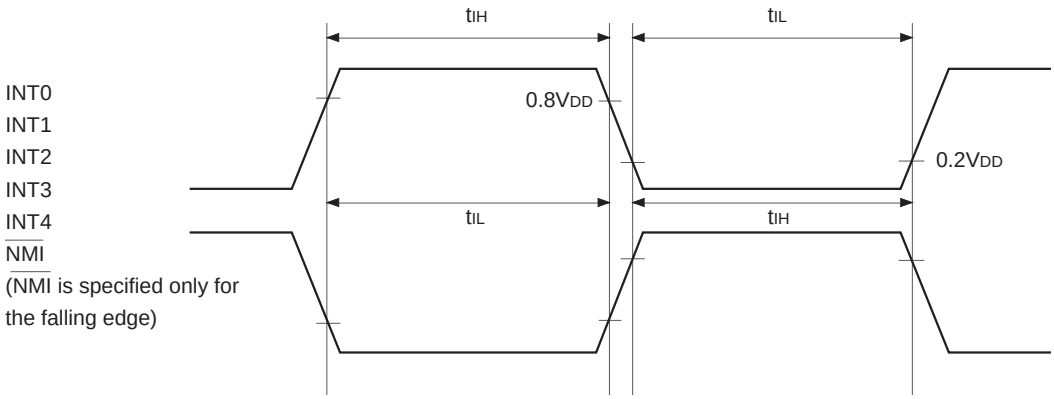


Fig. 7. Interruption input timing

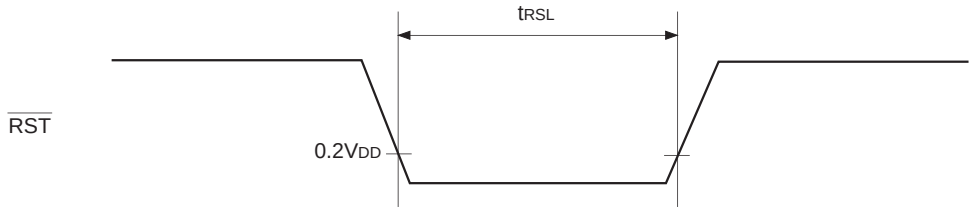
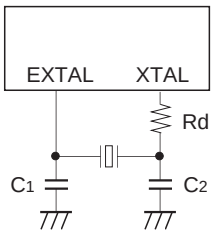


Fig. 8. $\overline{RST}$ input timing

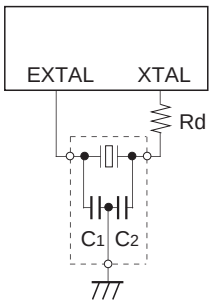
Appendix

Fig. 9. Recommended oscillation circuit

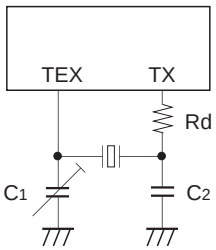
(i) Main clock



(ii) Main clock



(iii) Sub clock



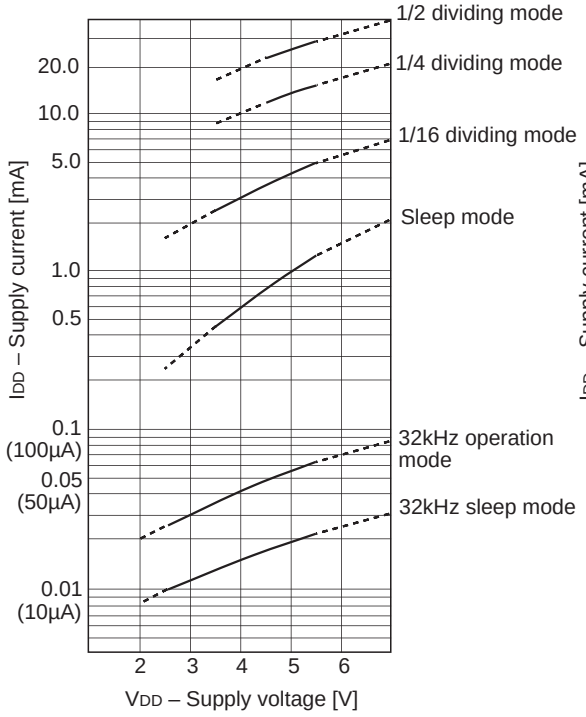
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0 *1	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5			
	CST10.0MTW*	10.0	30	30		(ii)	
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330 *1	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0 *1		
		12.0	5	5			
		16.0	Open	Open			
	P3	32.768kHz	30	33	120k	(iii)	
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	C_L = 12.5pF

* Indicates types with on-chip grounding capacitor (C1, C2).

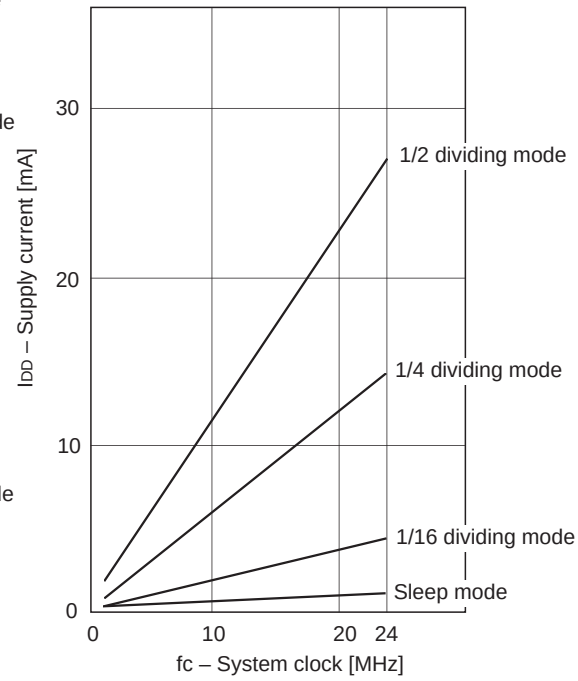
*1 XTAL series resistor (Rd = 500Ω or less) is hard to affect noise by ESD.

Characteristics Curve

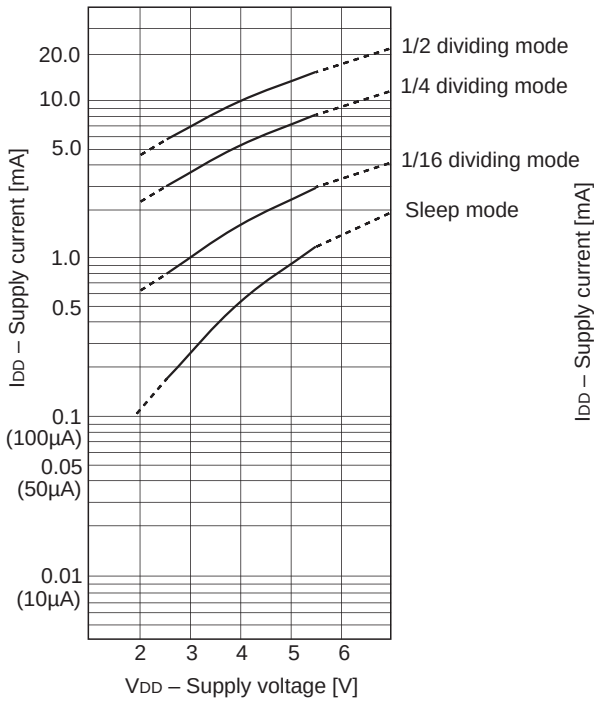
IDD vs. VDD
(fc = 24MHz, Ta = 25°C, Typical)



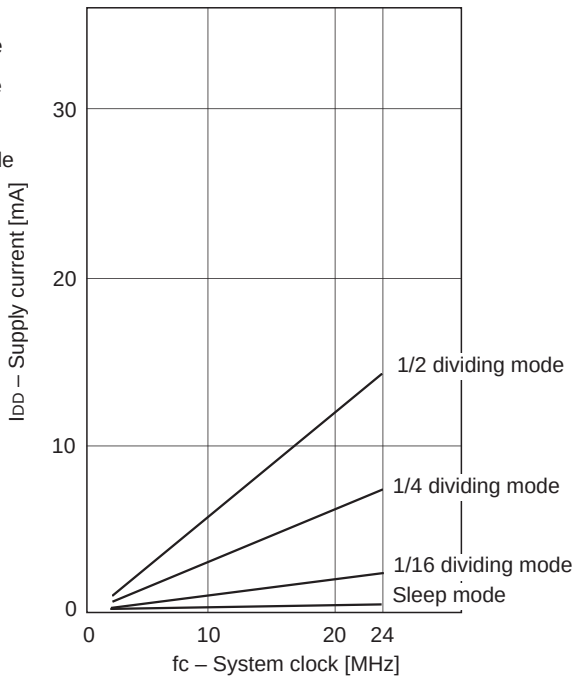
IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)



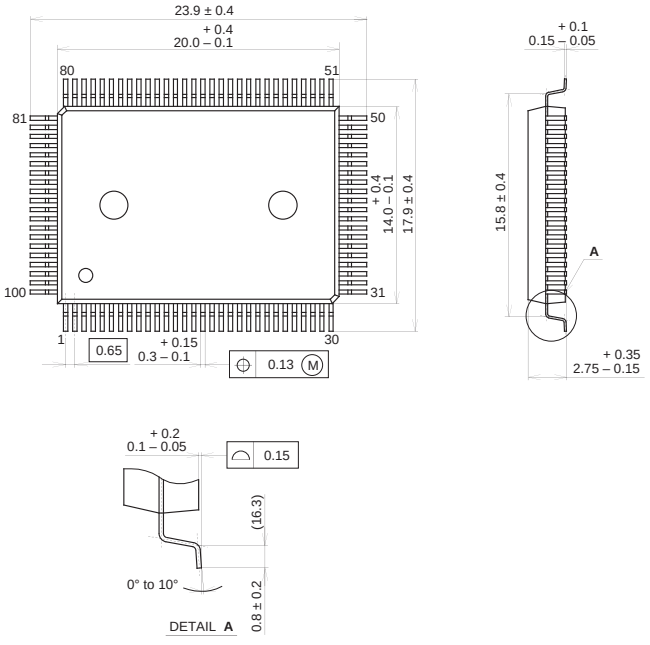
IDD vs. fc
(VDD = 3.0V, Ta = 25°C, Typical)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

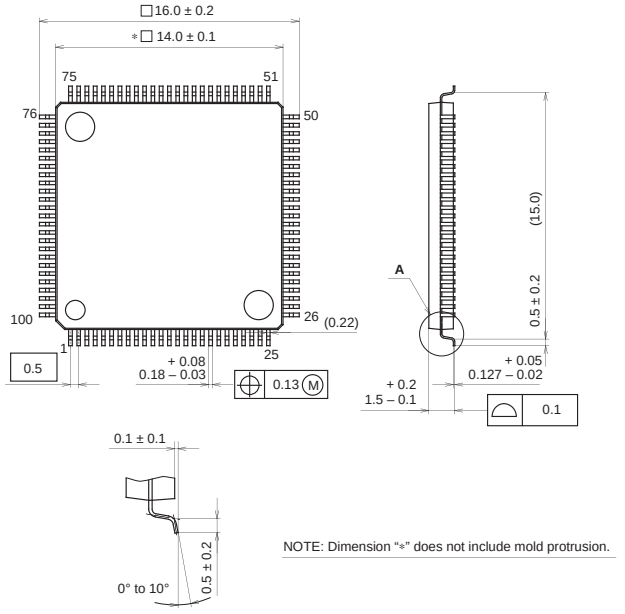


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g