**SONY**

CXP81952/81960

CMOS 8-bit Single Chip Microcomputer

Description

The CXP81952/81960 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control receiving circuit, general purpose prescaler, and external signal, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP81952/81960 provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

100 pin QFP (Plastic)   100 pin LQFP (Plastic)
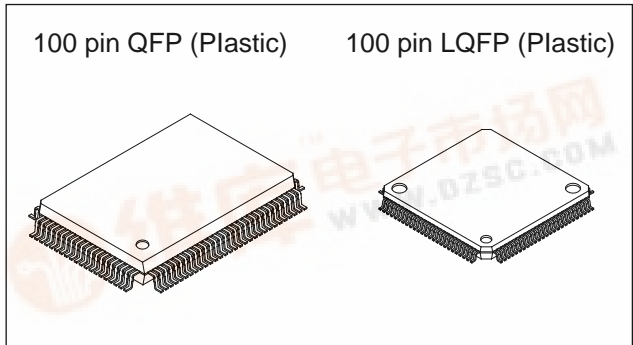
Structure
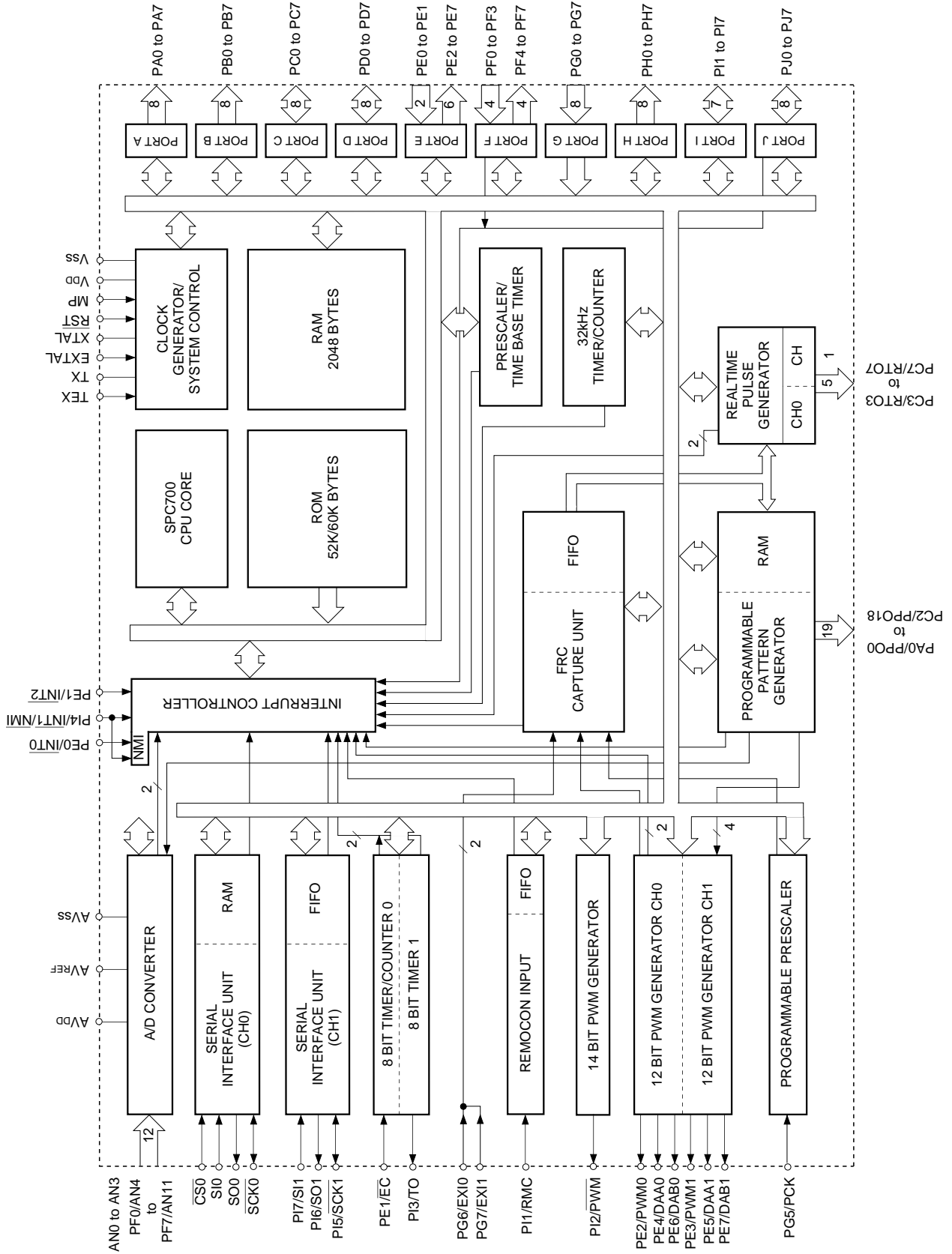
Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit operation/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle   250ns at 16MHz operation
       122μs at 32kHz operation
- Incorporated ROM capacity   52K bytes (CXP81952), 60K bytes (CXP81960)
- Incorporated RAM capacity   2048 bytes
- Peripheral functions
  - — A/D converter   8-bit, 12-channel, successive approximation system
    (Conversion time 20.0μs/16MHz)
  - — Serial Interface   Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel
    Incorporated 8-bit and 8-stage FIFO for data
    (1 to 8 bytes auto transfer) 1-channel
  - — Timer   8-bit timer, 8-bit timer/counter, 19-bit time base timer,
    32kHz timer/counter
  - — High precision timing pattern generator   PPG 19-pin 32-stage programmable
    RTG 5-pin 2-channel
  - — PWM/DA gate output   PWM 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
    DA gate pulse output 13-bit, 4-channel
  - — FRC capture unit   Incorporated 26-bit and 8-stage FIFO
  - — PWM output   14-bit, 1-channel
  - — Remote control receiving circuit   8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - — General purpose prescaler   7-bit (PG5 input frequency divided, FRC capture possible)
- Interruption   20 factors, 15 vectors, multi-interruption possible
- Standby mode   SLEEP/STOP
- Package   100-pin plastic QFP/LQFP
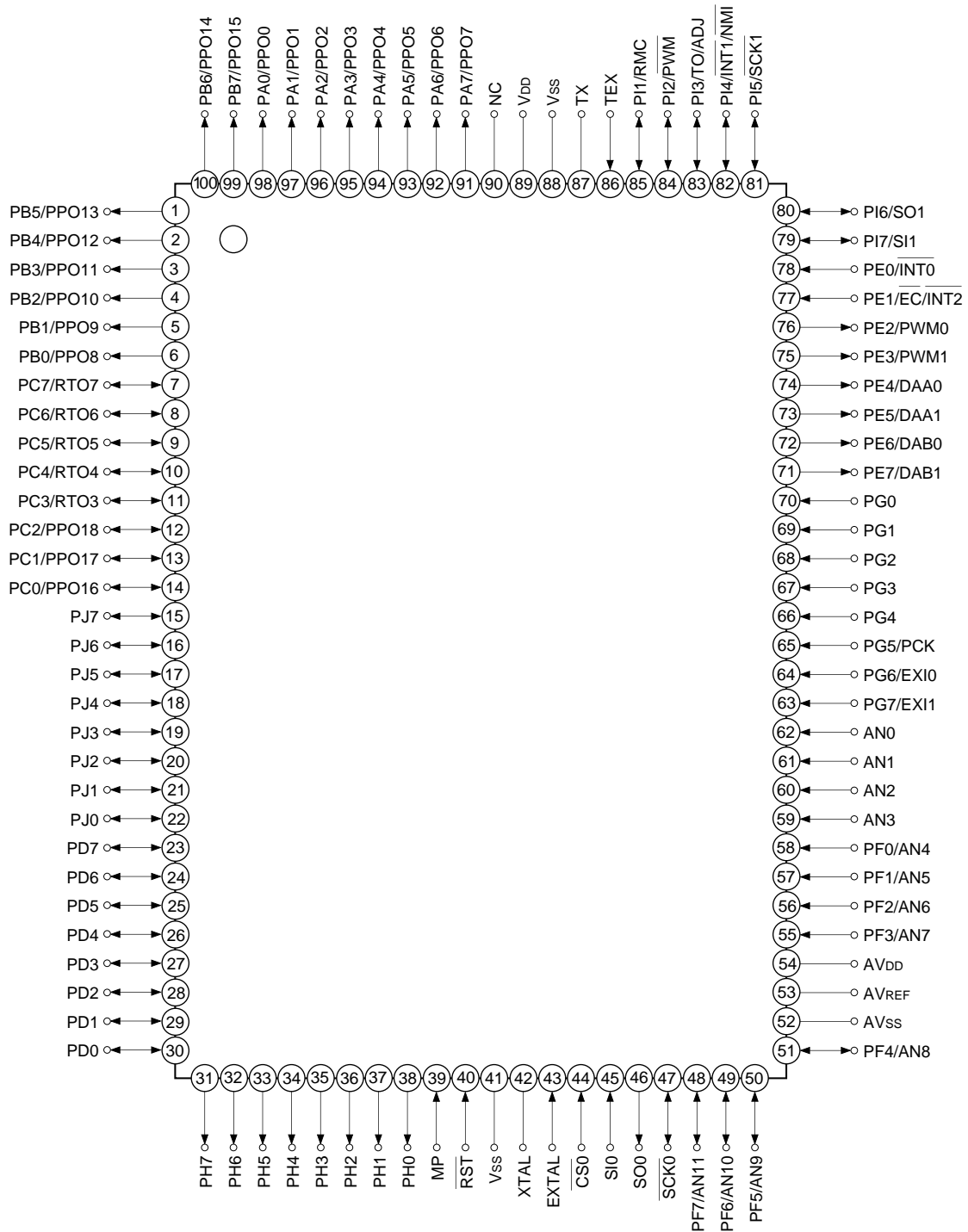- Piggyback/evaluation chip   CXP81900 100-pin ceramic QFP/LQFP

Block Diagram

Block diagram showing the SPC700 CPU CORE, ROM 52K/60K BYTES, RAM 2048 BYTES, CLOCK GENERATOR/SYSTEM CONTROL, PRESCALER/TIME BASE TIMER, 32kHz TIMER/COUNTER, REALTIME PULSE GENERATOR (CH0, CH), PROGRAMMABLE PATTERN GENERATOR (RAM), FRC CAPTURE UNIT (FIFO), INTERRUPT CONTROLLER (NMI), A/D CONVERTER, SERIAL INTERFACE UNIT (CH0) RAM, SERIAL INTERFACE UNIT (CH1) FIFO, 8 BIT TIMER/COUNTER 0, 8 BIT TIMER 1, REMOCON INPUT FIFO, 14 BIT PWM GENERATOR, 12 BIT PWM GENERATOR CH0, 12 BIT PWM GENERATOR CH1, PROGRAMMABLE PRESCALER, PORT A through PORT J.

Ports: PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE1, PE2 to PE7, PF0 to PF3, PF4 to PF7, PG0 to PG7, PH0 to PH7, PI1 to PI7, PJ0 to PJ7.

Signals: VSS, VDD, MP, RST, XTAL, EXTAL, TX, TEX, AVSS, AVREF, AVDD.

Interrupt inputs: PE1/INT2, PI4/INT1/NMI, PE0/INT0.

Pins: AN0 to AN3, PF0/AN4 to PF7/AN11, CS0, SI0, SO0, SCK0, PI7/SI1, PI6/SO1, PI5/SCK1, PE1/EC, PI3/TO, PG6/EXI0, PG7/EXI1, PI1/RMC, PI2/PWM, PE2/PWM0, PE4/DAA0, PE6/DAB0, PE3/PWM1, PE5/DAA1, PE7/DAB1, PG5/PCK.

Outputs: PC3/RTO3 to PC7/RTO7, PA0/PPO0 to PC2/PPO18.

Pin Configuration 1 (Top View) 100-pin QFP package

Left side (top to bottom):
- 1 PB5/PPO13
- 2 PB4/PPO12
- 3 PB3/PPO11
- 4 PB2/PPO10
- 5 PB1/PPO9
- 6 PB0/PPO8
- 7 PC7/RTO7
- 8 PC6/RTO6
- 9 PC5/RTO5
- 10 PC4/RTO4
- 11 PC3/RTO3
- 12 PC2/PPO18
- 13 PC1/PPO17
- 14 PC0/PPO16
- 15 PJ7
- 16 PJ6
- 17 PJ5
- 18 PJ4
- 19 PJ3
- 20 PJ2
- 21 PJ1
- 22 PJ0
- 23 PD7
- 24 PD6
- 25 PD5
- 26 PD4
- 27 PD3
- 28 PD2
- 29 PD1
- 30 PD0

Top side (100 to 81):
- 100 PB6/PPO14
- 99 PB7/PPO15
- 98 PA0/PPO0
- 97 PA1/PPO1
- 96 PA2/PPO2
- 95 PA3/PPO3
- 94 PA4/PPO4
- 93 PA5/PPO5
- 92 PA6/PPO6
- 91 PA7/PPO7
- 90 NC
- 89 V$_{DD}$
- 88 V$_{SS}$
- 87 TX
- 86 TEX
- 85 PI1/RMC
- 84 PI2/PWM
- 83 PI3/TO/ADJ
- 82 PI4/INT1/NMI
- 81 PI5/SCK1

Bottom side (31 to 50):
- 31 PH7
- 32 PH6
- 33 PH5
- 34 PH4
- 35 PH3
- 36 PH2
- 37 PH1
- 38 PH0
- 39 MP
- 40 RST
- 41 V$_{SS}$
- 42 XTAL
- 43 EXTAL
- 44 CS0
- 45 SI0
- 46 SO0
- 47 SCK0
- 48 PF7/AN11
- 49 PF6/AN10
- 50 PF5/AN9

Right side (top to bottom):
- 80 PI6/SO1
- 79 PI7/SI1
- 78 PE0/INT0
- 77 PE1/EC/INT2
- 76 PE2/PWM0
- 75 PE3/PWM1
- 74 PE4/DAA0
- 73 PE5/DAA1
- 72 PE6/DAB0
- 71 PE7/DAB1
- 70 PG0
- 69 PG1
- 68 PG2
- 67 PG3
- 66 PG4
- 65 PG5/PCK
- 64 PG6/EXI0
- 63 PG7/EXI1
- 62 AN0
- 61 AN1
- 60 AN2
- 59 AN3
- 58 PF0/AN4
- 57 PF1/AN5
- 56 PF2/AN6
- 55 PF3/AN7
- 54 AV$_{DD}$
- 53 AV$_{REF}$
- 52 AV$_{SS}$
- 51 PF4/AN8

Note) 1. NC (Pin 90) is always connected to V$_{DD}$.

2. Vss (Pins 41 and 88) are both connected to GND.

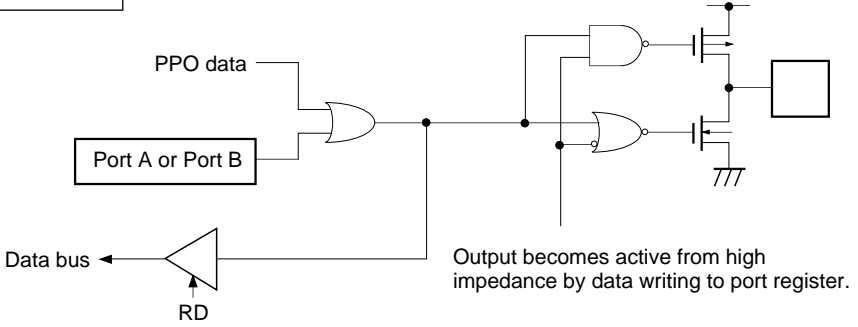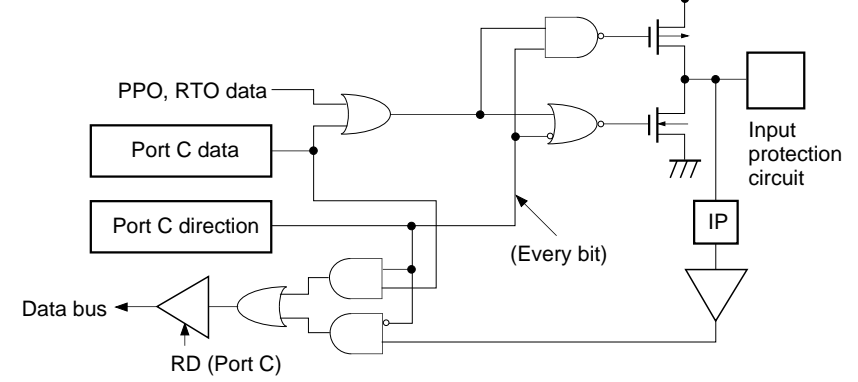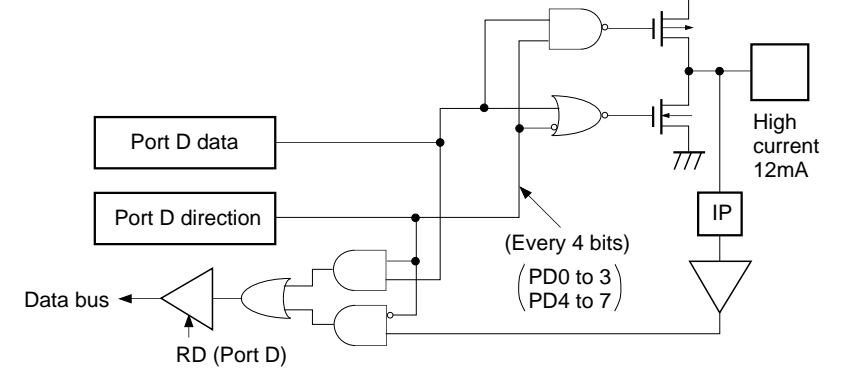**Pin Configuration 2** (Top View) 100-pin LQFP package

Top pins (left to right, 100–76):
PB4/PPO12, PB5/PPO13, PB6/PPO14, PB7/PPO15, PA0/PPO0, PA1/PPO1, PA2/PPO2, PA3/PPO3, PA4/PPO4, PA5/PPO5, PA6/PPO6, PA7/PPO7, NC, VDD, VSS, TX, TEX, PI1/RMC, PI2/PWM, PI3/TO/ADJ, PI4/INT1/NMI, PI5/SCK1, PI6/SO1, PI7/SI1, PE0/INT0

Left pins (1–25):
1 PB3/PPO11
2 PB2/PPO10
3 PB1/PPO9
4 PB0/PPO8
5 PC7/RTO7
6 PC6/RTO6
7 PC5/RTO5
8 PC4/RTO4
9 PC3/RTO3
10 PC2/PPO18
11 PC1/PPO17
12 PC0/PPO16
13 PJ7
14 PJ6
15 PJ5
16 PJ4
17 PJ3
18 PJ2
19 PJ1
20 PJ0
21 PD7
22 PD6
23 PD5
24 PD4
25 PD3

Right pins (75–51):
75 PE1/EC/INT2
74 PE2/PWM0
73 PE3/PWM1
72 PE4/DAA0
71 PE5/DAA1
70 PE6/DAB0
69 PE7/DAB1
68 PG0
67 PG1
66 PG2
65 PG3
64 PG4
63 PG5/PCK
62 PG6/EXI0
61 PG7/EXI1
60 AN0
59 AN1
58 AN2
57 AN3
56 PF0/AN4
55 PF1/AN5
54 PF2/AN6
53 PF3/AN7
52 AVDD
51 AVREF

Bottom pins (26–50):
26 PD2
27 PD1
28 PD0
29 PH7
30 PH6
31 PH5
32 PH4
33 PH3
34 PH2
35 PH1
36 PH0
37 MP
38 RST
39 VSS
40 XTAL
41 EXTAL
42 CS0
43 SI0
44 SO0
45 SCK0
46 PF7/AN11
47 PF6/AN10
48 PF5/AN9
49 PF4/AN8
50 AVSS

Note) 1. NC (Pin 88) is always connected to VDD.

2. VSS (Pins 39 and 86) are both connected to GND.

– 4 –
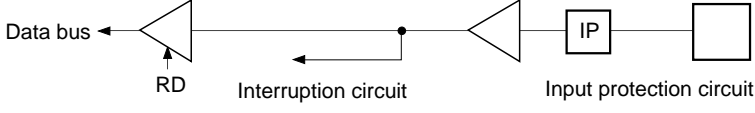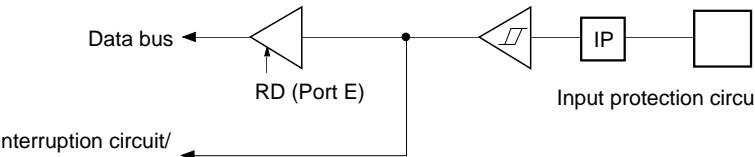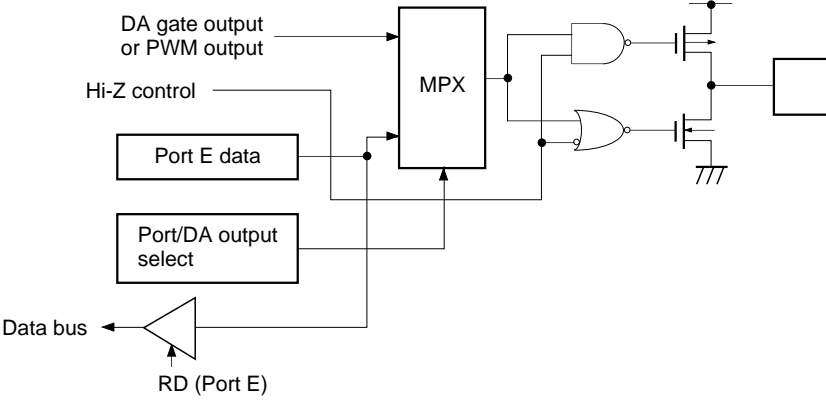
Pin Description

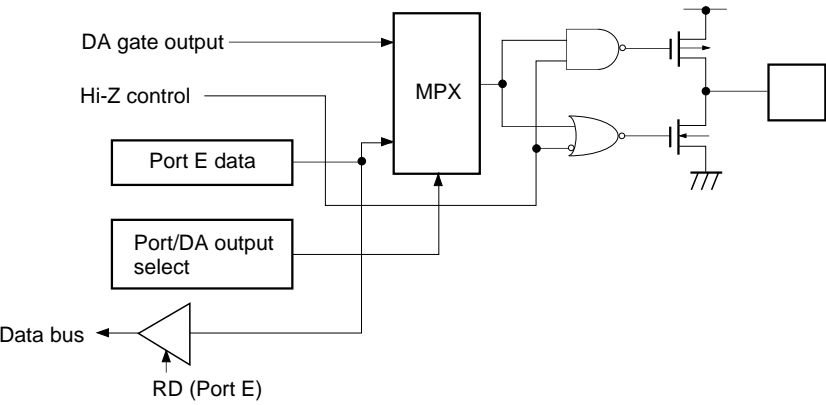| Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real time output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)		
PE0/$\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output		DA gate pulse output pins. (4 pins)	
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Ouput	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

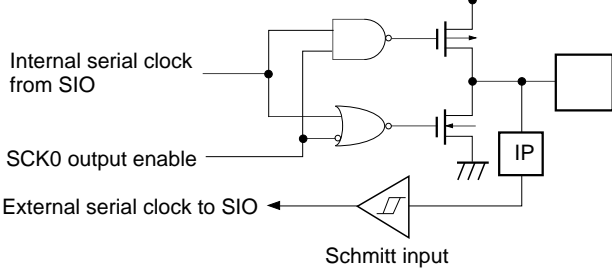| Symbol	I/O	Description	
PG0 to PG4	Input	(Port G) 8-bit input port. (8 pins)	
PG5/PCK			7 bit general purpose prescaler input pin.
PG6/EXI0			External input pin to FRC capture unit.
PG7/EXI1			
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/Output/Output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active when falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV$_{DD}$		Positive power supply pin of A/D converter.	
AV$_{REF}$	Input	Reference voltage input pin of A/D converter.	
AV$_{ss}$		GND pin of A/D converter.	
V$_{DD}$		Positive power supply pin.	
V$_{ss}$		GND pin. Connect both Vss pins to GND.	

Input/Output Circuit Formats for Pins
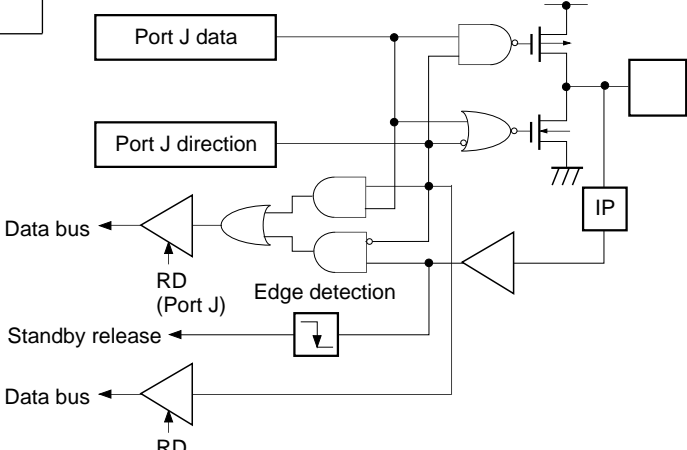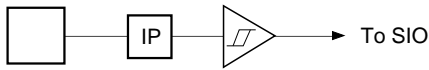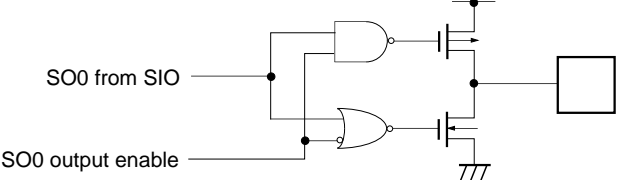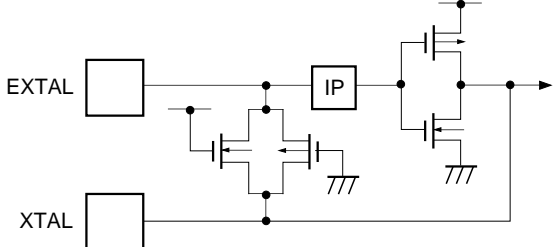
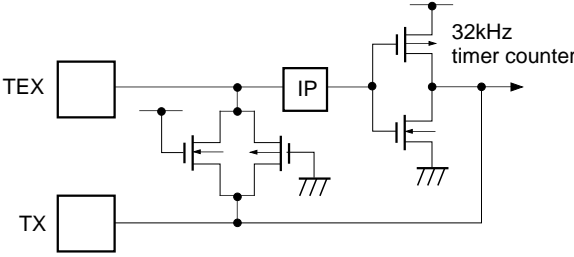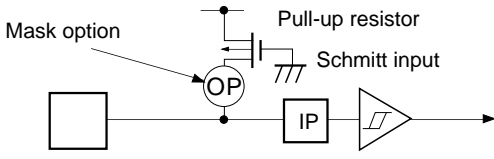| Pin	Circuit format	When reset
PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	**Port A** **Port B** PPO data Port A or Port B Data bus ← RD Output becomes active from high impedance by data writing to port register.	Hi-Z
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	**Port C** PPO, RTO data Port C data Port C direction Data bus ← RD (Port C) (Every bit) Input protection circuit IP	Hi-Z
PD0 to PD7 8 pins	**Port D** Port D data Port D direction Data bus ← RD (Port D) (Every 4 bits) (PD0 to 3 / PD4 to 7) High current 12mA IP	Hi-Z
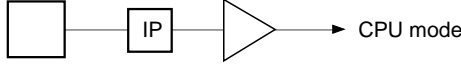
Pin	Circuit format	When reset
PE0/INT0 1 pin	**Port E** Data bus ← [RD] ● ← Interruption circuit ← [IP] □ Input protection circuit	Hi-Z
PE1/EC/INT2 1 pin	**Port E** Data bus ← RD (Port E) ● ← [IP] □ Input protection circuit Interruption circuit/ event counter	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	**Port E** DA gate output or PWM output → MPX Hi-Z control → Port E data → Port/DA output select Data bus ← RD (Port E)	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	**Port E** DA gate output → MPX Hi-Z control → Port E data → Port/DA output select Data bus ← RD (Port E)	H level

Pin	Circuit format	When reset
AN0 to AN3 4 pins	Input multiplexer IP → A/D converter	Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F Input multiplexer IP → A/D converter → Data bus RD (Port F)	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F Port F data Data bus ← RD (Port F) Port/AD select IP A/D converter Input multiplexer	Hi-Z
PG0 to PG4 PG5/PCK 6 pins	Port G Schmitt input IP → Data bus RD (Port G) PG5: To general purpose prescaler	Hi-Z
PG6/EXI0 PG7/EXI1 2 pins	Port G Schmitt input IP → FRC capture unit → Data bus RD (Port G)	Hi-Z
PH0 to PH7 8 pins	Port H Medium withstand voltage 12V Port H data Data bus ← RD (Port H) Large current 12mA	Hi-Z

Pin	Circuit format	When reset
PI2/$\overline{\text{PWM}}$ PI3/TO/ADJ 2 pins	**Port I** PI2: From 14-bit PWM PI3: From timer/counter, 32kHz timer	Hi-Z
PI1/RMC PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ PI7/SI1 3 pins	**Port I** PI1: To remote control circuit PI4: To interruption circuit PI7: To serial CH1 Schmitt input	Hi-Z
PI5/$\overline{\text{SCK1}}$ PI6/SO1 2 pins	**Port I** Note) PI5 is schmitt input PI6 is inverter input To serial CH1	Hi-Z

Pin	Circuit format	When reset
PJ0 to PJ7 8 pins	Port J Port J data Port J direction Data bus RD (Port J) Edge detection Standby release Data bus RD IP	Hi-Z
$\overline{CS0}$ SI0 2 pins	Schmitt input IP → To SIO	Hi-Z
SO0 1 pin	SO0 from SIO SO0 output enable	Hi-Z
$\overline{SCK0}$ 1 pin	Internal serial clock from SIO SCK0 output enable External serial clock to SIO IP Schmitt input	Hi-Z
EXTAL XTAL 2 pins	EXTAL IP XTAL • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation

Pin	Circuit format	When reset
TEX TX 2 pins	• Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin		L level
MP 1 pin	CPU mode	Hi-Z

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0[*1]	V	
	AV_{SS}	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0[*2]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*2]	V	
Medium withstand output voltage	V_{OUTP}	−0.3 to +15.0	V	PH pin
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output pins: per pin
	I_{OLC}	20	mA	Large current port pin[*3]: per pin
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type
		380		LQFP package type

[*1] AV_{DD} and V_{DD} should be set to a same voltage.

[*2] V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

[*3] The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions   (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV_{DD}	3.0	5.5	V	[1]
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[2]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input[3] and PE0/$\overline{INT0}$ pin
			5.5	V	CMOS schmitt input[6]
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin[4, 7] and TEX pin[5, 7]
		$V_{DD} - 0.2$	$V_{DD} + 0.2$	V	EXTAL pin[4, 8] and TEX pin[5, 8]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[2, 7]
		0	$0.2V_{DD}$	V	[2, 8]
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input[3] and PE0/$\overline{INT0}$ pin
	V_{ILEX}	−0.3	0.4	V	EXTAL pin[4, 7] and TEX pin[5, 7]
		−0.3	0.2	V	EXTAL pin[4, 8] and TEX pin[5, 8]
Operating temperature	Topr	−20	+75	°C	

[1] AV_{DD} and V_{DD} should be set to a same voltage.

[2] Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

[3] Each pin of $\overline{SCK0}$, $\overline{RST}$, PE1/$\overline{EC}$/$\overline{INT2}$, PI1/RMC, PI4/$\overline{INT1}$/NMI, PI5/$\overline{SCK1}$ and PI7/SI1.

[4] It specifies only when the external clock is input.

[5] It specifies only when the external event count clock is input.

[6] Each pin of $\overline{CS0}$, SI0, and PG.

[7] In case of 4.5 to 5.5V supply voltage (V_{DD}).

[8] In case of 3.0 to 3.6V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = −20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	µA
	I_{ILR}	$\overline{RST}$[*1]		−1.5		−400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$[*1]	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA
Supply current[*2]	I_{DD1}	V_{DD}	16MHz crystal oscillation (C1 = C2 = 15pF) V_{DD} = 5V ± 0.5V[*3]		31	50	mA
	I_{DDS1}		SLEEP mode V_{DD} = 5V ± 0.5V		2.0	8	mA
	I_{DD2}		32kHz crystal oscillation (C1 = C2 = 47pF) V_{DD} = 3V ± 0.3V		46	110	µA
	I_{DDS2}		SLEEP mode V_{DD} = 3V ± 0.3V		9	35	µA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V ± 0.5V			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

[*1] $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

[*2] When entire output pins are open.

[*3] When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics (V_{DD} = 3.0 to 3.6V) (Ta = −20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 3.0V, I_{OH} = −0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = 0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PD, PH	V_{DD} = 3.0V, I_{OL} = 5mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	−0.3		−20	µA
	I_{IHT}	TEX	V_{DD} = 3.6V, V_{IH} = 3.6V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.6V, V_{IL} = 0.3V	−0.1		−10	µA
	I_{ILR}	$\overline{RST}$[1]		−0.9		−200	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$[1]	V_{DD} = 3.6V, V_I = 0, 3.6V			±10	µA
Open drain output leakage current	I_{LOH}	PH	V_{DD} = 3.6V, V_{OH} = 12V			50	µA
Supply current[2]	I_{DD1}	V_{DD}	12MHz crystal oscillation (C_1 = C_2 = 15pF) / V_{DD} = 3.3V ± 0.3V[3]		15	30	mA
	I_{DDS1}		SLEEP mode / V_{DD} = 3.3V ± 0.3V		0.8	2.5	mA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) / V_{DD} = 3.3V ± 0.3V			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

[1] $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

[2] When entire output pins are open.

[3] When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing (Ta = −20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1,	V_{DD} = 4.5 to 5.5V	1	16	MHz
			Fig. 2		1	12	
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1,	V_{DD} = 4.5 to 5.5V	28		ns
			Fig. 2 (External clock drive)		37.5		
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3		$t_{sys} \times 4^*$		ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ns
System clock frequency	f_C	TEX TX	Fig. 2　V_{DD} = 2.7 to 5.5V (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3		10		μs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
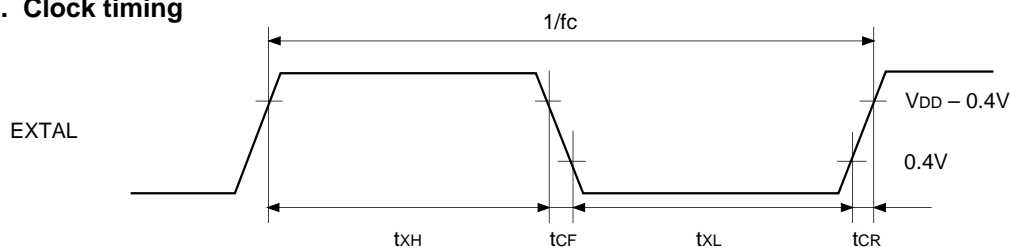
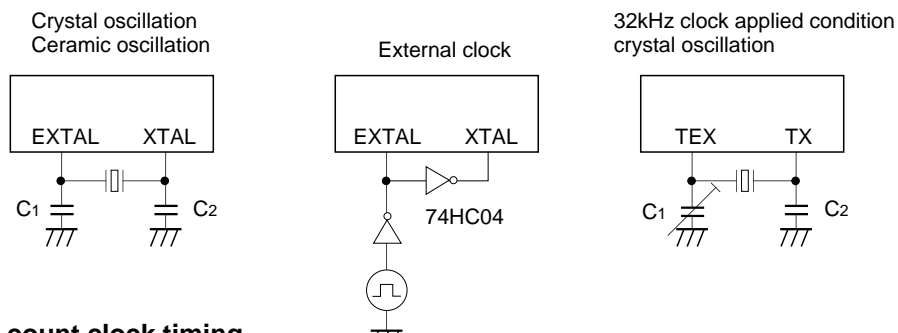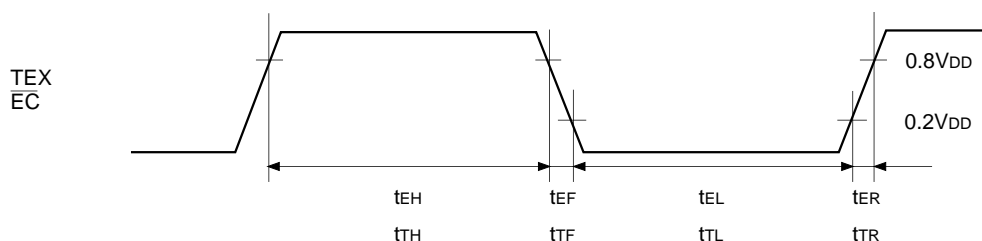### Fig. 1. Clock timing

Fig. 2. Clock applied condition

Fig. 3. Event count clock timing

(2) Serial transfer (CH0)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	8000/fc − 100		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	$-t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	$2t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		$2t_{sys} + 200$	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow$ SCK0, SI $\rightarrow$ SI0, and SO $\rightarrow$ SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)   (Ta = −20 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc − 150		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	−tsys+100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys+100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow SCK0$, SI $\rightarrow$ SI0, and SO $\rightarrow$ SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)

Serial transfer (CH1)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

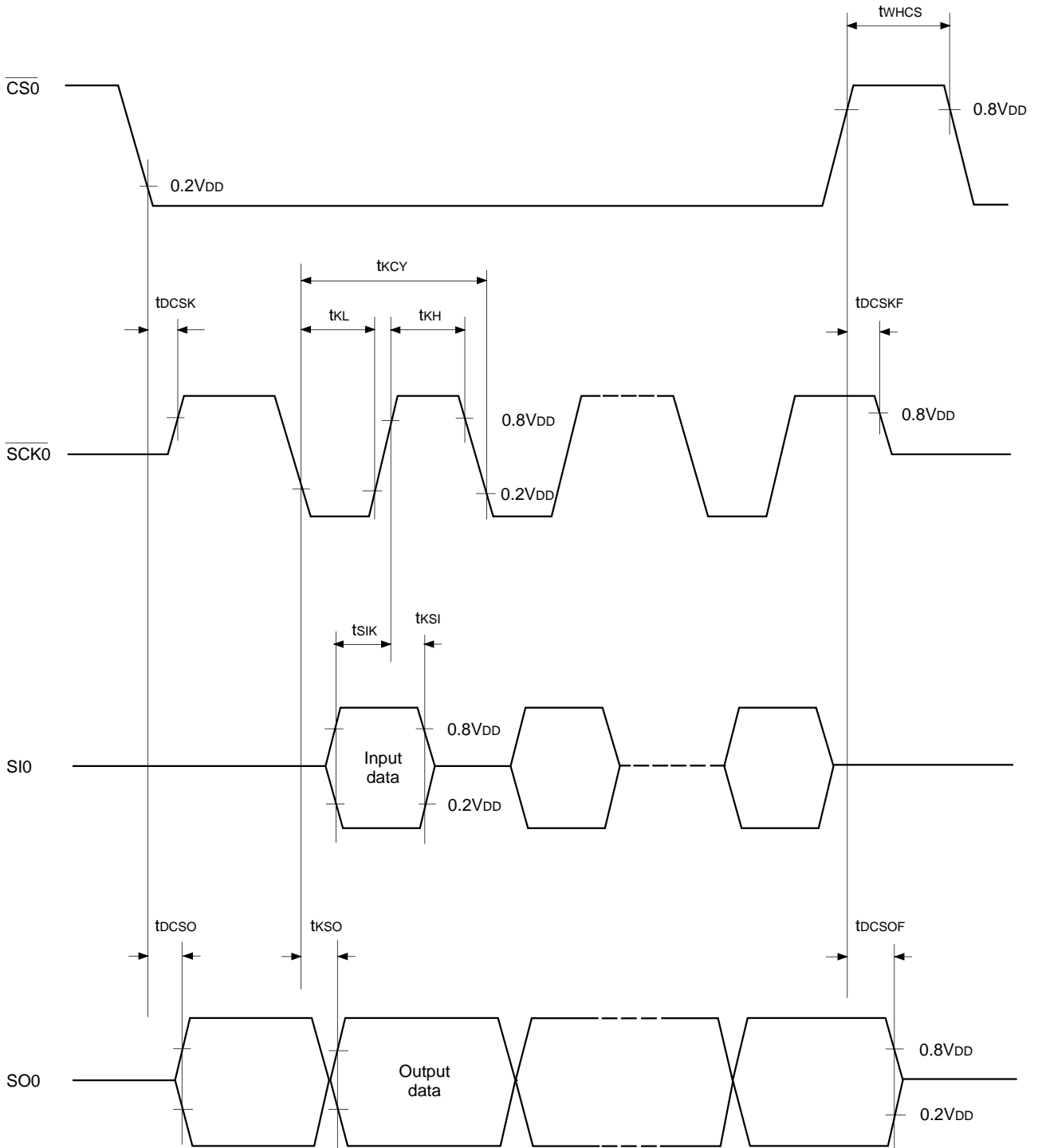| Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	$2t_{sys}$ + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	t_{sys} + 100		ns
			Output mode	4000/fc − 100		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	t_{sys} + 200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		t_{sys} + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

**Serial transfer (CH1)**   (Ta = −20 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	$2t_{sys}$ + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	t_{sys} + 100		ns
			Output mode	4000/fc − 150		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	t_{sys} + 200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		t_{sys} + 250	ns
			$\overline{SCK1}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing
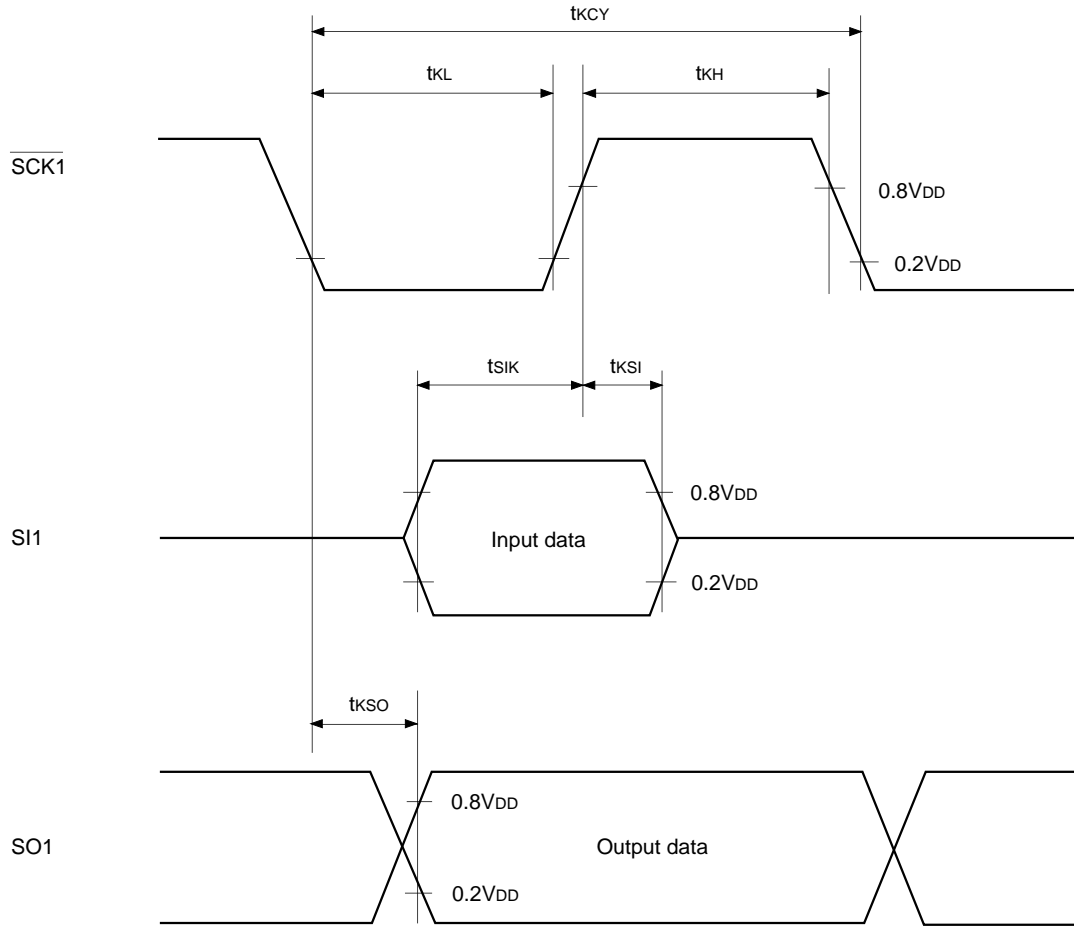
(3) General purpose prescaler (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	PCK		33			ns
External clock input rise and fall times	t_R, t_F	PCK				200	ns

Fig. 6. General purpose prescaler timing
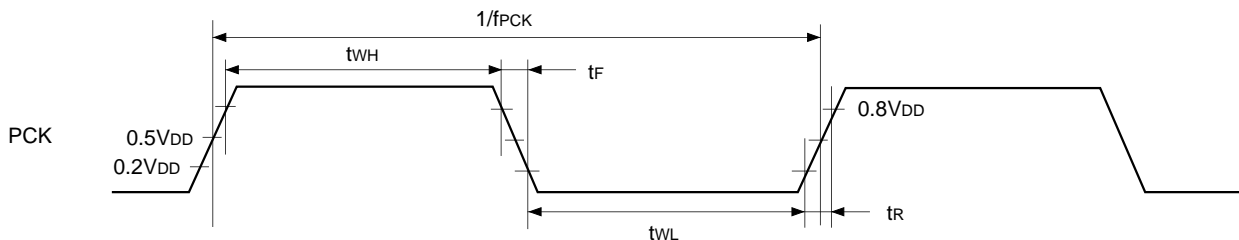
(4) A/D converter characteristics   (Ta = −20 to +75°C, $V_{DD} = AV_{DD} = 4.5$ to 5.5V, $AV_{REF} = 4.0$ to AV_{DD}, $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C $V_{DD} = AV_{DD} = AV_{REF} = 5.0V$ $V_{SS} = AV_{SS} = 0V$			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}$*			μs
Sampling time	t_{SAMP}			$12/f_{ADC}$*			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

(Ta = −20 to +75°C, $V_{DD} = AV_{DD} = 3.0$ to 3.6V, $AV_{REF} = 2.7$ to AV_{DD}, $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C $V_{DD} = AV_{DD} = AV_{REF} = 5.0V$ $V_{SS} = AV_{SS} = 0V$			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}$*			μs
Sampling time	t_{SAMP}			$12/f_{ADC}$*			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

Fig. 7. Definitions of A/D converter terms
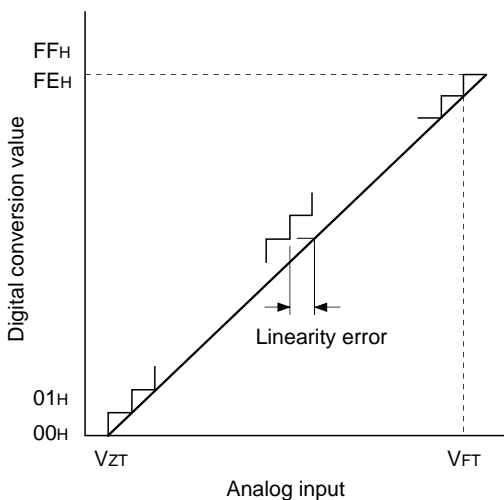
* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FF$_H$ bit 0).

When PS2 is selected, $f_{ADC} = fc/2$

When PS1 is selected, $f_{ADC} = fc$

(5) Interruption, reset input   (Ta = −20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		μs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig. 8. Interruption input timing
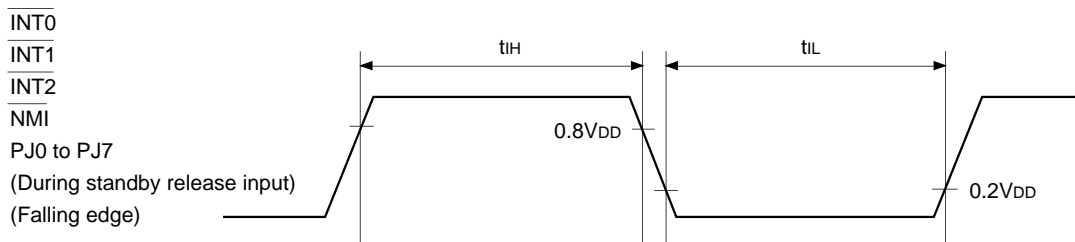
Fig. 9. Reset input timing
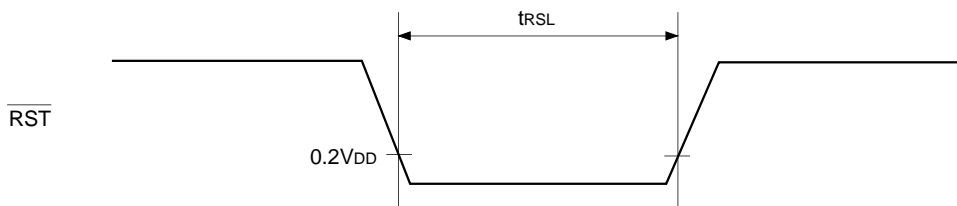
(6) Others   (Ta = −20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	t_{sys} = 2000/fc	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

t_{FRC} = 1000/fc [ns]

Fig. 10. Other timings
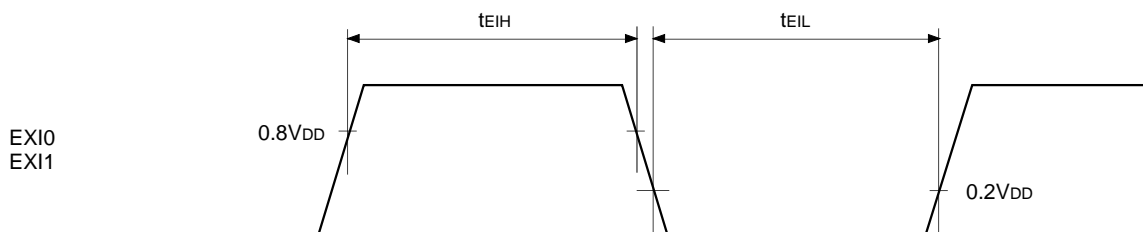
Supplement

Fig. 11. Recommended oscillation circuit

(i)

(ii)

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

IDD – Supply current [mA]
VDD – Supply voltage [V]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- SLEEP mode
- 32kHz mode (instruction)
- 32kHz SLEEP mode

IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)

IDD – Supply current [mA]
Frequency [MHz]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- SLEEP mode

IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)

IDD – Supply current [mA]
VDD – Supply voltage [V]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- SLEEP mode

IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)

IDD – Supply current [mA]
Frequency [MHz]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- SLEEP mode

Package Outline   Unit: mm

100PIN QFP (PLASTIC)

DETAIL **A**

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	——————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)

NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	——————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	——————