SONY

CXP82532/82540

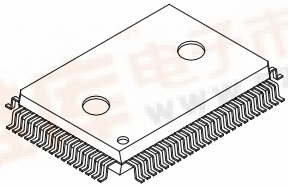
CMOS 8-bit Single Chip Microcomputer

Description

The CXP82532/82540 microcomputer is composed of a CPU, ROM RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, fluorescent display controller/driver, remote control receiver.

This device also includes a power-on reset function and sleep/stop functions which can be used to achieve low power consumption.

80 pin QFP (Plastic)



Features

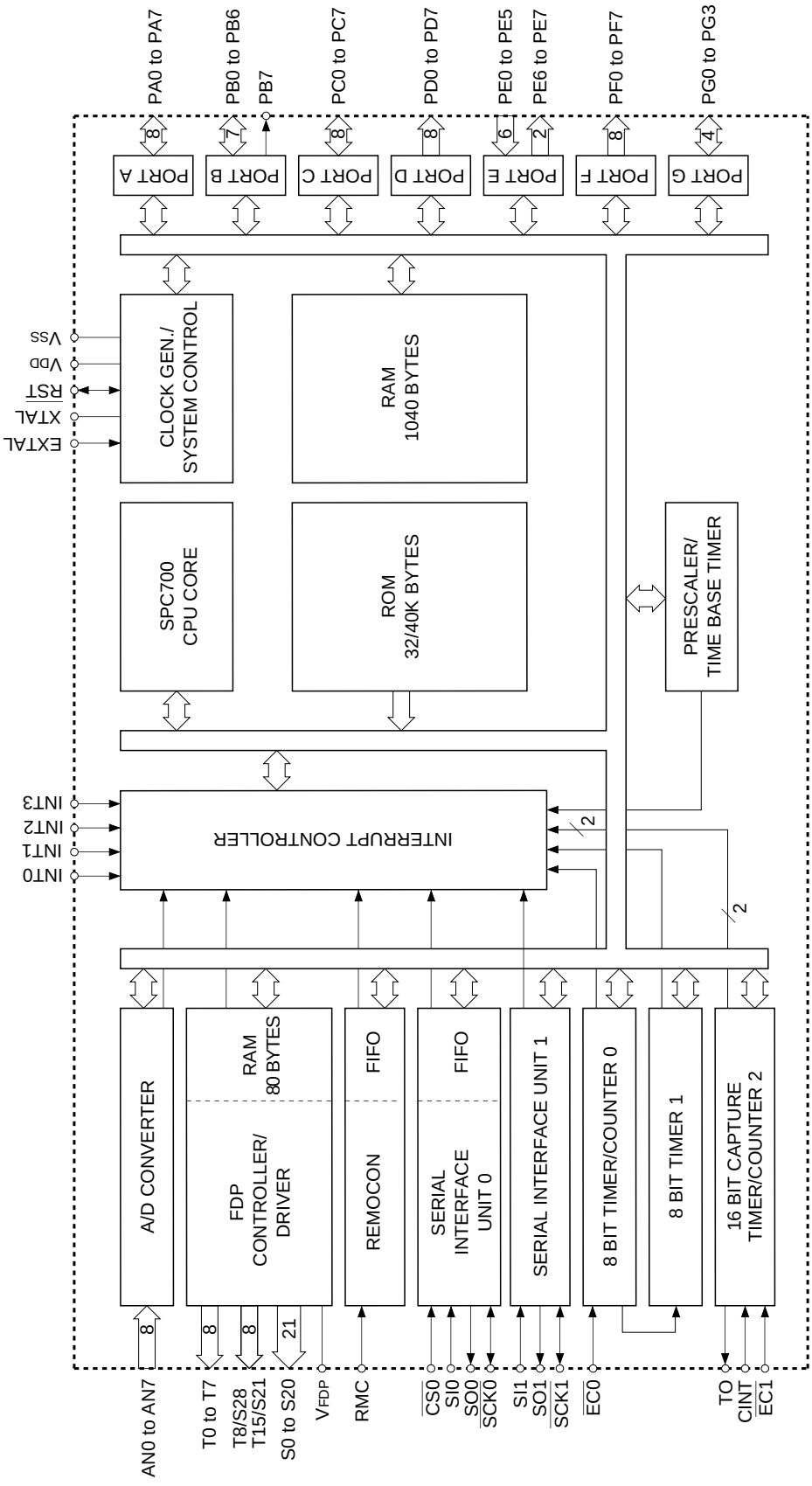
- Instruction set which supports a wide array of data types
  - — 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle 400ns for 10MHz operation
- On-chip ROM 32K bytes (CXP82532)
  40K bytes (CXP82540)
- On-chip RAM 1120 bytes (Including fluorescent display data area)
- Peripheral functions:
  - — A/D converter 8-bit, 8-channel, successive approximation system
    (conversion time 32µs/10MHz)
  - — Serial interface On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer) 1 channel
    8-bit clock synchronized 1 channel
  - — Timers 8-bit timer
    8-bit timer/counter
    19-bit time-base timer
    16-bit capture timer/counter
  - — Fluorescent display controller/driver
    Maximum of 336 segment display available
    1 to 16 digits dynamic display
    Dimmer function
    High voltage tolerance output (40V)
    On-chip pull-down resistor (Mask option)
  - — Remote control receiver circuit
    On-chip noise elimination circuit
    On-chip 6 stage FIFO 8-bit pulse measurement counter
- Interrupts 14 factors, 15 vectors multi-interruption possible
- Standby mode Sleep/stop
- Package 80-pin plastic QFP
- Piggyback/evaluator CXP82500 80-pin ceramic QFP

Structure

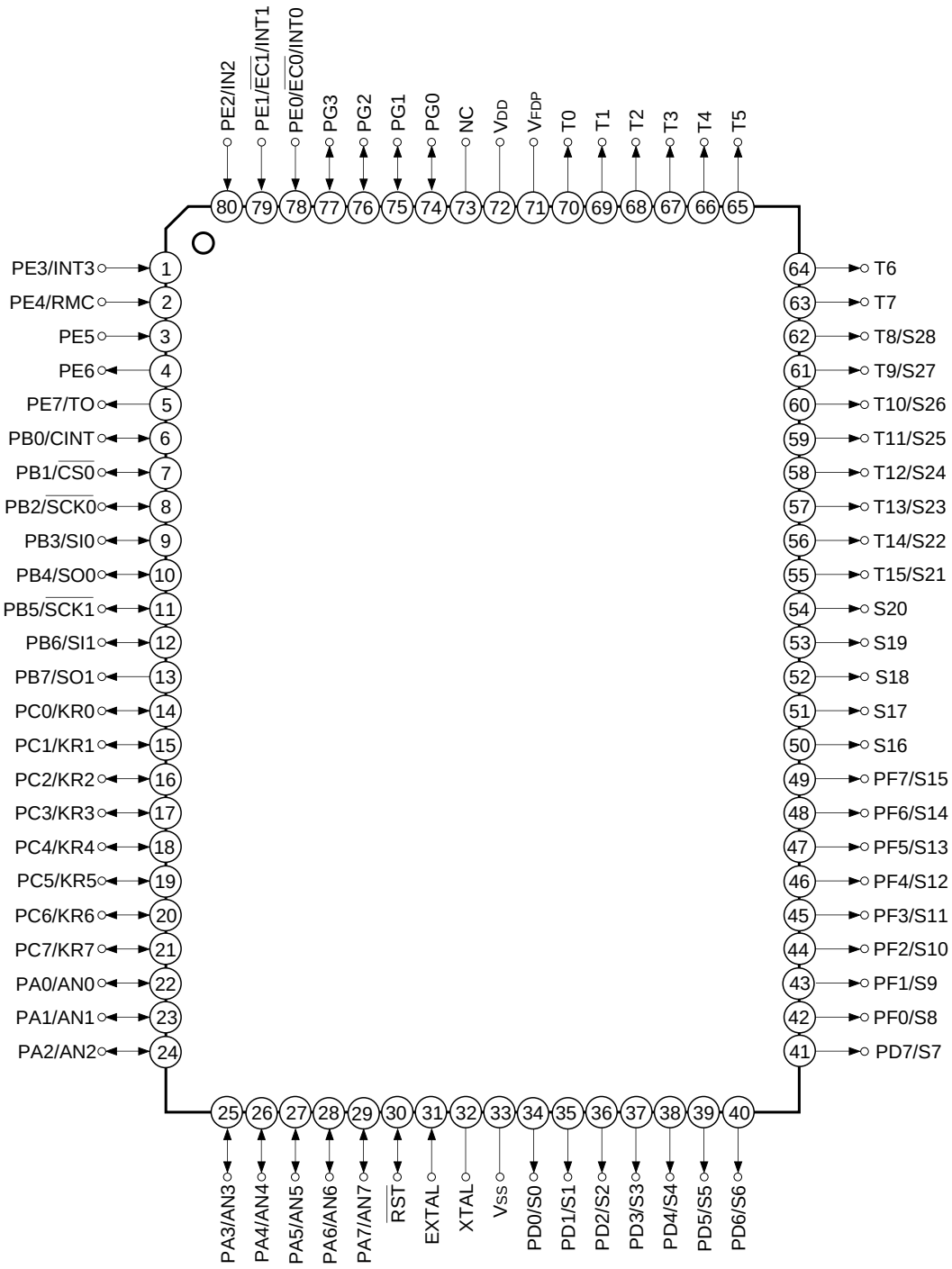
Silicon gate CMOS IC

E92Y32A78-PS

Block Diagram



Pin Assignment (Top View)



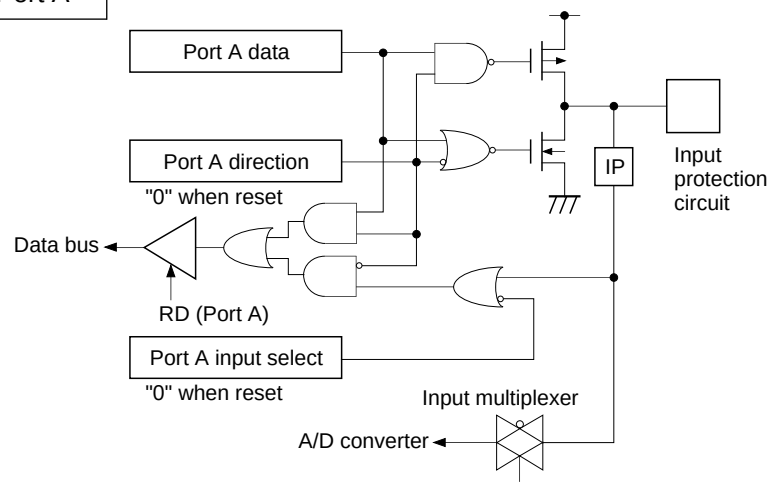
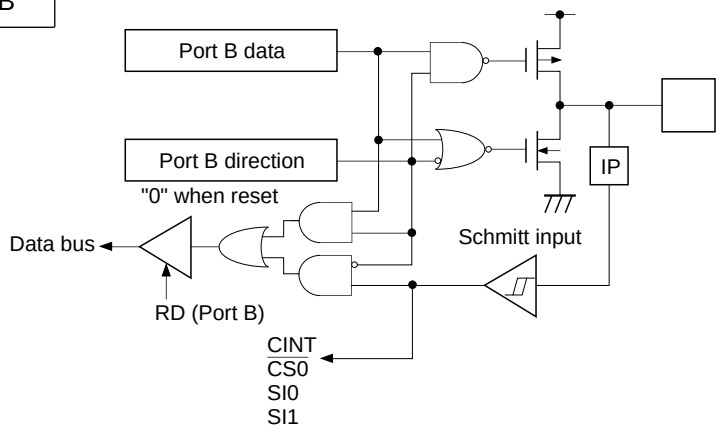
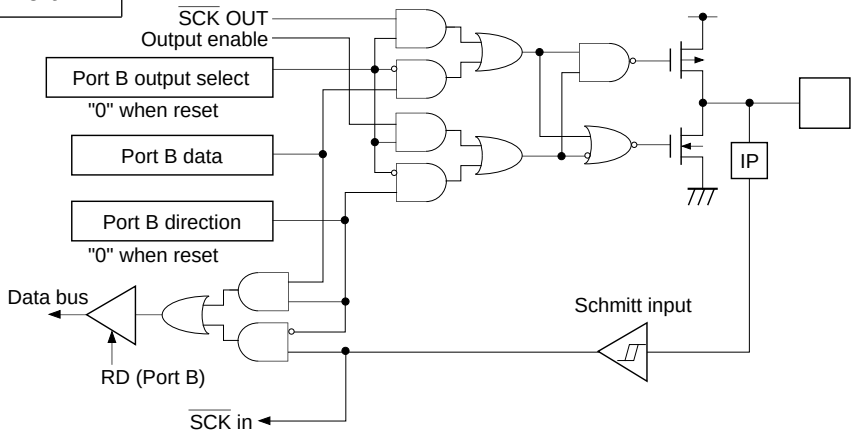
Note) NC (Pin 73) is always connected to V_{DD}.

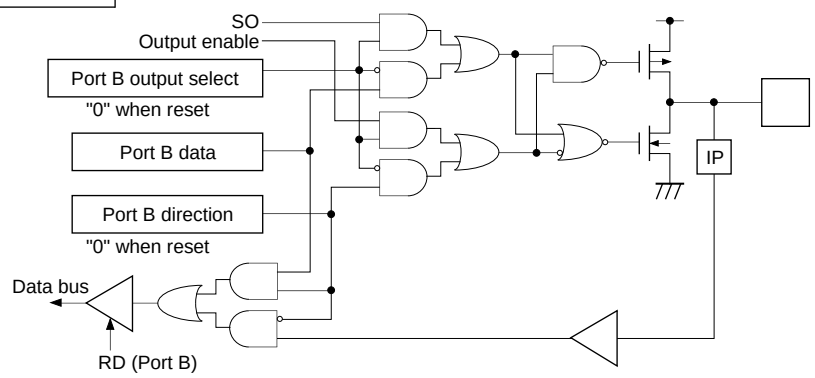
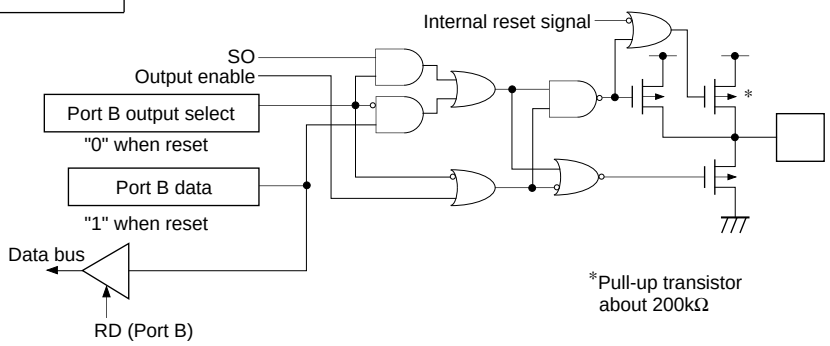
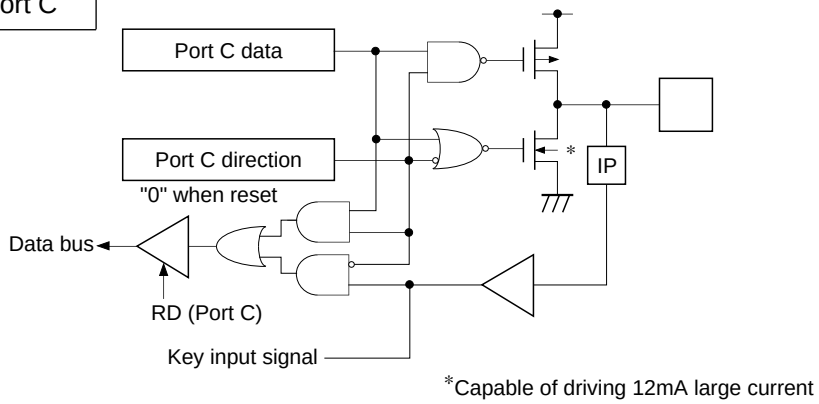
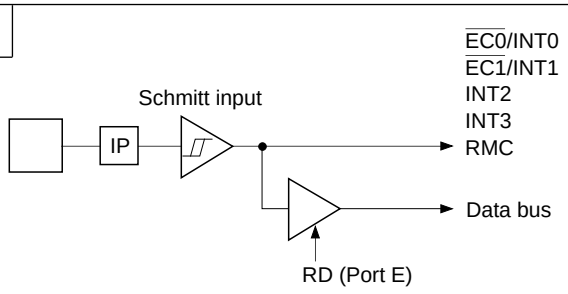
Pin Description

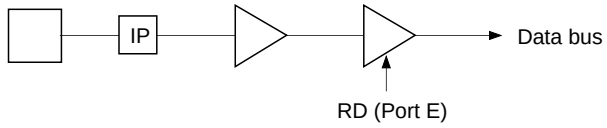
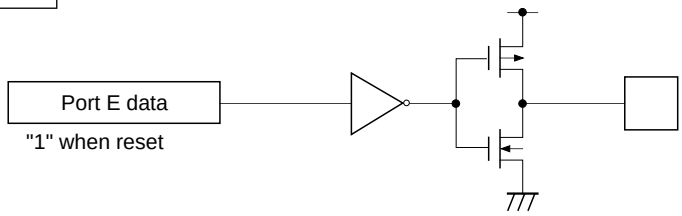
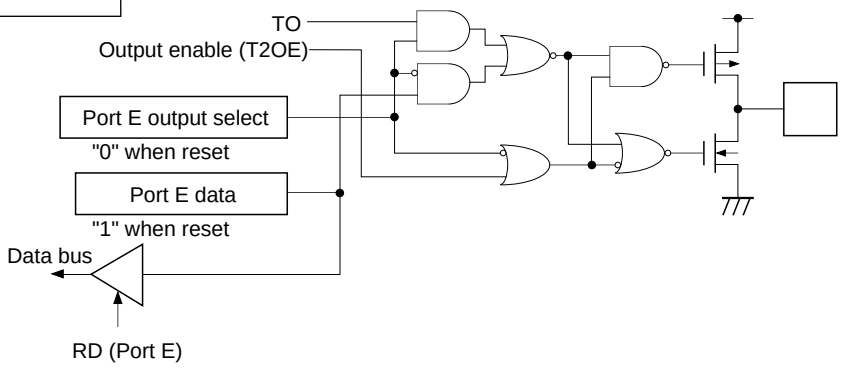
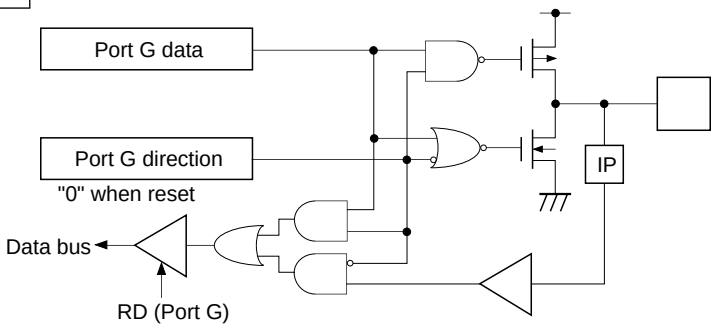
Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit port; single bit addressable. (8 pins)	Analog input to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Single bit addressable from amongst lower 7 bits; highest bit (PB7) dedicated to output. (8 pins)	External capture input for 16-bit timer/counter.
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock (CH0) input/output.
PB3/SI0	I/O/Input		Serial data (CH0) input.
PB4/SO0	I/O/Output		Serial data (CH0) output.
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock (CH1) input/output.
PB6/SI1	I/O/Input		Serial data (CH1) input.
PB7/SO1	Output/Output		Serial data (CH1) output.
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit port; single bit addressable. Can provide 12mA sink current. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/$\overline{EC0}$	Input/Input/Input	(Port E) 8-bit port with lower 6 bits dedicated to input and upper 2 bits dedicated to output. (8 pins)	Input for external interrupt requests. (4 pins) / External event input to timer/counter. (2 pins)
PE1/INT1/$\overline{EC1}$	Input/Input/Input		
PE2/INT2	Input/Input		
PE3/INT3	Input/Input		
PE4/RMC	Input/Input		Input for remote control receiver circuit.
PE5	Input		
PE6	Output		
PE7/TO	Output/Output		Output pin for 16-bit timer/counter rectangular waveform.
PG0 to PG3	I/O	(Port G) 4-bit input/output port; single bit addressable. (4 pins)	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit dedicated output port. (8 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Dual purpose output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit dedicated output port. (8 pins)	Segment signal output for FDP.

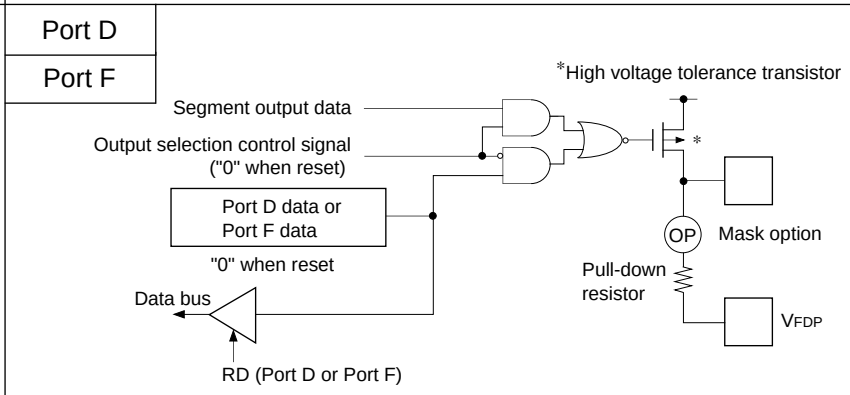
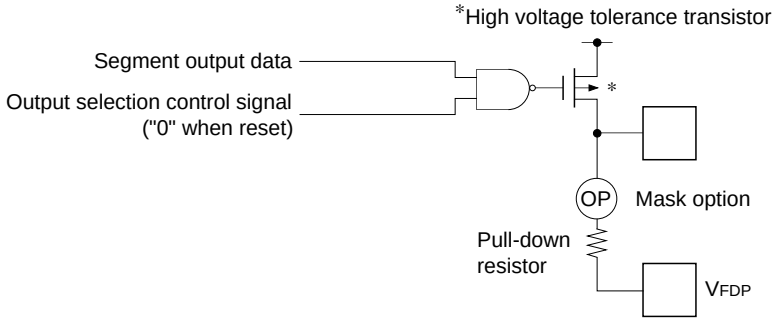
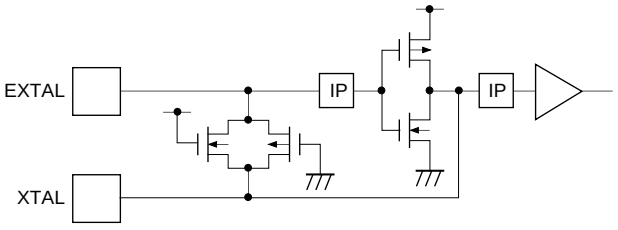
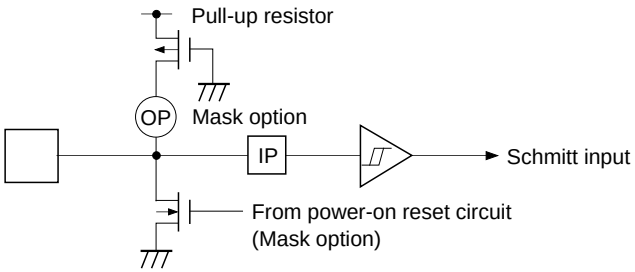
Symbol	I/O	Description
V_{FDP}		Provides voltage for FDP when on-chip resistor is selected under mask option.
EXTAL	Input	Connection for system clock oscillation crystal. When using an external clock, input normal signal to EXTAL and reverse phase signal to the XTAL pin.
XTAL	Output	
$\overline{RST}$	I/O	System reset, active "L". The $\overline{RST}$ pin is an input/output pin which outputs a "L" level from the on-chip power-on reset circuit when the power is turned on. (Mask option)
NC		NC pin is always connected to V_{DD}.
V_{DD}		Positive power supply pin.
V_{SS}		GND

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/CINT PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	Port B 	Hi-Z
PB7/SO1 1 pin	Port B 	High level
PC0/KR0 to PC7/KR7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 PE3/INT3 PE4/RMC 5 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE5 1 pin	Port E 	Hi-Z
PE6 1 pin	Port E 	High level
PE7/TO 1 pin	Port E 	High level
PG0 to PG3 4 pins	Port G 	Hi-Z

Pin	Circuit format	When reset
PD0/S0 to PD7/S7 PF0/S8 to PF7/S15 16 pins	Port D Port F 	Hi-Z or Low level (when PD resistor is connected)
S16 to S20 T15/S21 to T8/S28 T0 to T7 21 pins		Hi-Z or Low level (when PD resistor is connected)
EXTAL XTAL 2 pins	 *Diagram shows circuit construction for oscillation. *During stop feedback resistor is disconnected.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Display output voltage	V_{OD}	V_{DD} – 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standerd.
High level output current	I_{OH}	–5	mA	Other than display output pins*2 : per pin
	I_{ODH1}	–15	mA	Display outputs S0 to S20: per pin
	I_{ODH2}	–35	mA	Display outputs T0 to T7, T8/S28 to T15/S21: per pin
High level total output current	$\sum I_{OH}$	–40	mA	Total of other than display output pins
	$\sum I_{ODH}$	–100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	Large current port pin *3
Low level total output current	$\sum I_{OL}$	100	mA	Entire pin total
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1 V_{IN} and V_{OUT} cannot exceed V_{DD} + 0.3V.

*2 Rating for output current of general input/output port.

*3 The large current drive transistor is an N-channel transistor of Port C.

Note) If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High-speed mode (1/2, 1/4 clock) guaranteed range during operation
		3.5	5.5		Low-speed mode (1/16 clock) guaranteed range during operation
		2.5	5.5		Guaranteed data hold range during stop
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*1
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin*3
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*1
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	–20	+75	°C	

*1 All regular input ports (PA, PB3, PB4, PB6, PC, PE5, PG).

*2 For pins $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$/INT0, $\overline{EC1}$/INT1 , INT2, INT3, RMC.

*3 Rating only for external clock input.

Electrical Characteristics

DC Characteristics

(Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PC,PE6, PE7, PG, $\overline{RST}$*1 (for V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
Display output current	I_{OH}	S0 to S20	V_{DD} = 4.5V V_{OH} = V_{DD} – 2.5V	–8			mA
		S21/T15 to S28/T8 T0 to T7		–20			mA
Open drain output leak current (P-CH Tr off state)	I_{LOL}	S0 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} – 35V V_{FDP} = V_{DD} – 35V			–20	µA
Pull-down resistor*3	R_L	S0 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5V V_{OD} – V_{FDP} = 30V	60	100	270	kΩ
Input/output leak current	I_{IZ}	PA to PC, PE, PG, $\overline{RST}$*2	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Supply current*4	I_{DD1}	V_{DD}	V_{DD} = 5.5V High-speed mode (1/2 clock) operation 10MHz crystal oscillator (C_1 = C_2 = 15pF)		25	40	mA
	I_{DDSL}		Sleep mode		3	8	mA
	I_{DDST}		Stop mode			10	µA
Input capacitance	C_{IN}	For pins other than S0 to S28, T0 to T7, PB7, PE6, PE7, V_{DD}, V_{SS}, V_{FDP}	1MHz clock 0V other than measured		10	20	pF

*1 $\overline{RST}$ pin is rated only when the power-on circuit is selected under the mask option.
*2 $\overline{RST}$ pin is rated for input current when the pull-up resistor is selected; otherwise it is rated for leak current.
*3 Applies when the on-chip pull-down resistor is selected under the mask option.
*4 All output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1	10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock driver	45		ns
System clock input rising and falling times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock driver		200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$, EC1	Fig. 3	tsys + 50*1		ns
Event count input clock rising and falling times	t_{ER}, t_{EF}	$\overline{EC0}$, EC1	Fig. 3		20	ms

*1 tsys is determind by the upper two bits of the clock control resister (Address: 00FE$_H$; CPU clock selected) resulting in one of the 3 following values:
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

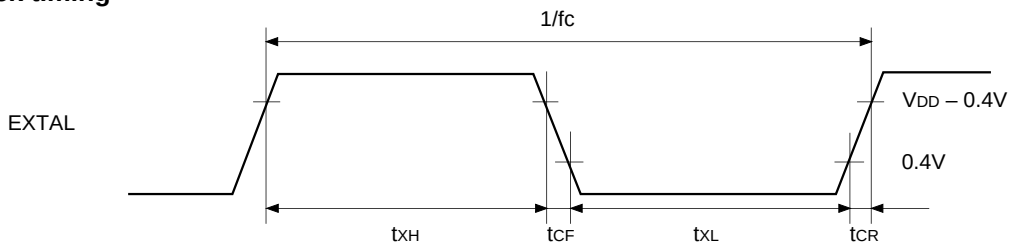


Fig. 2. Clock applying condition

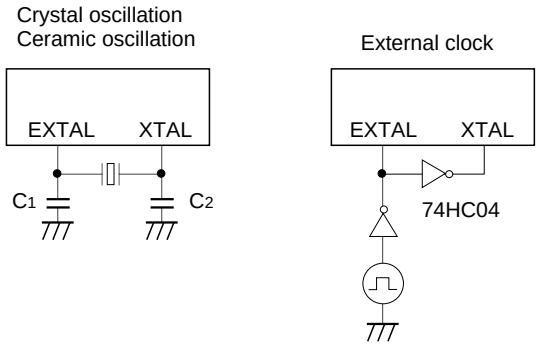
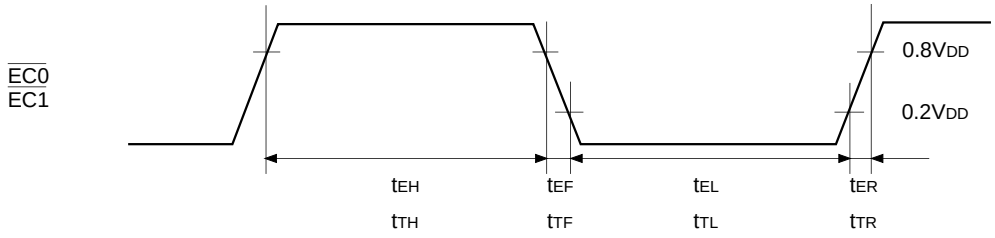


Fig. 3. Event count clock timing



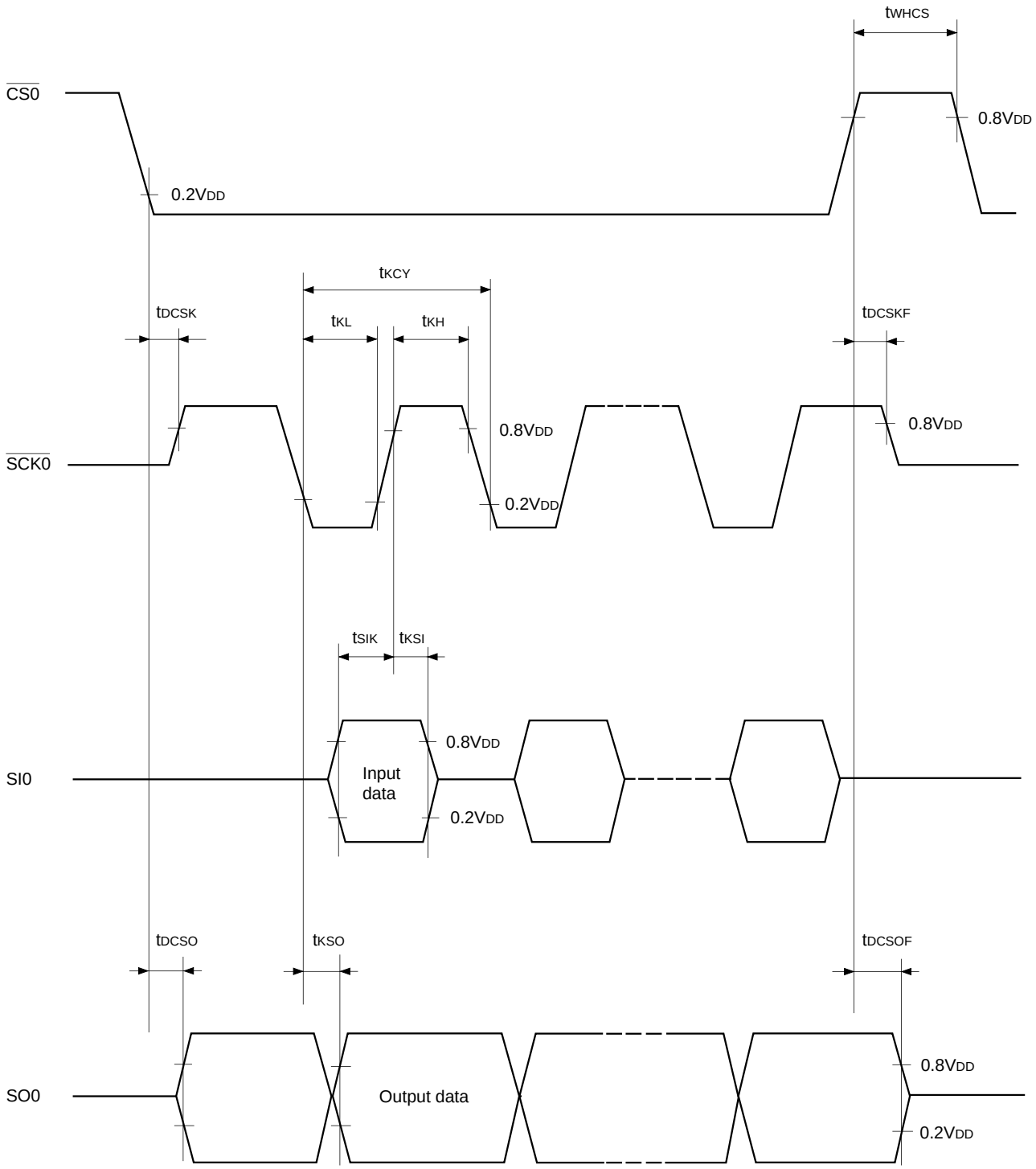
(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input setup time (against $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys is determind by the upper two bits of the clock control resister (Address: $00FE_H$; CPU clock selected) resulting in one of the 3 following values:
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

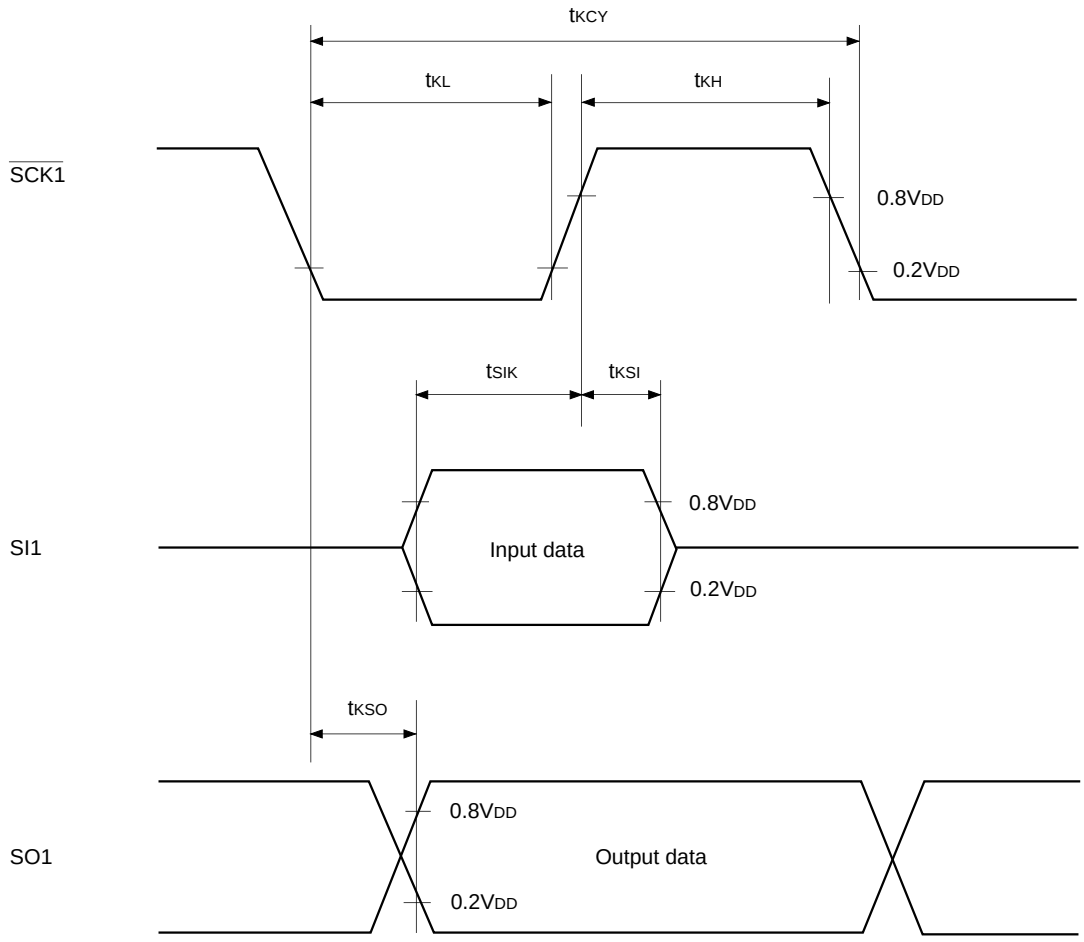


Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

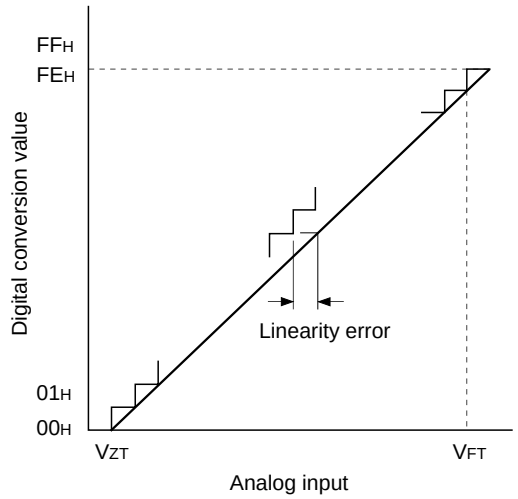
Fig. 5. Serial transfer CH1 timing



(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			A/D converter operation only Ta = 25°C V_{DD} = 5.0V V_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	70	150	mV
Full-scale transition voltage	V_{FT}*2			4930	5050	5120	mV
Conversion time	t_{CONV}			160/f_{ADC} *3			µs
Sampling time	t_{SAMP}			12/f_{ADC} *3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V

Fig. 6. Definition of A/D converter terms



*1 V_{ZT} : Digital Value converted between 00H to 01H.
*2 V_{FT} : Digital Value converted between FEH and FFH.
*3 f_{ADC} : ADC operation clock selection (MSC: Bit 0 of address 01FFH) and assumes following values:
f_{ADC} = fc/2 when PS2 is selected.
f_{ADC} = fc when PS1 is selected.

(4) Interrupts, reset inputs (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt High and Low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 7. Interrupt input timing

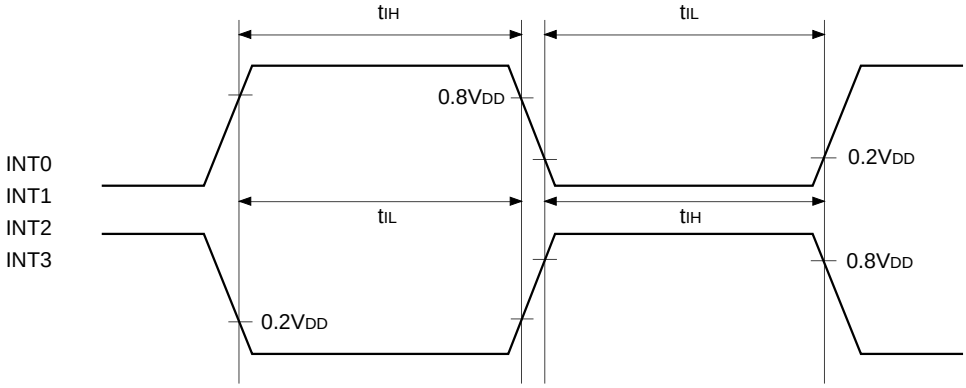
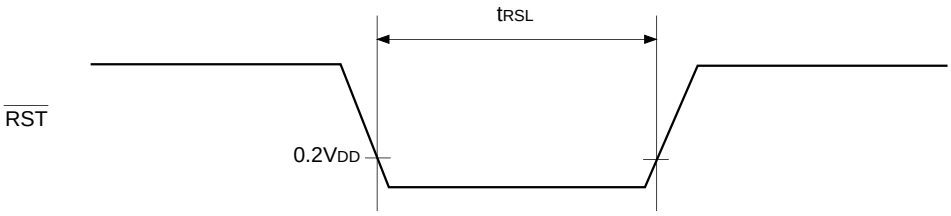


Fig. 8. $\overline{RST}$ input timing



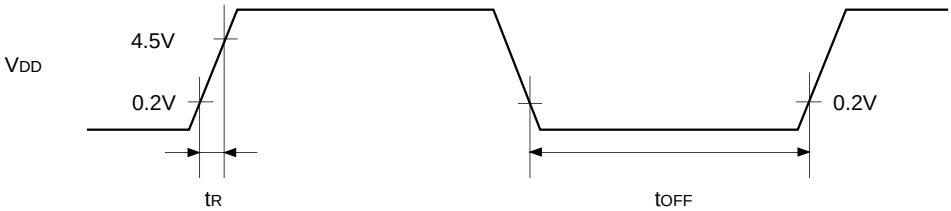
(5) Power-on reset

Power-on reset* (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

* Specifies only when power-on reset function is selected.

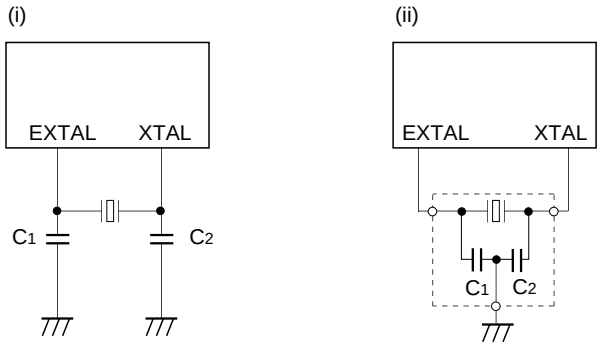
Fig. 9. Power-on reset



The power supply should be rise smoothly.

Supplement

Fig. 10. Recommended Oscillation Circuit

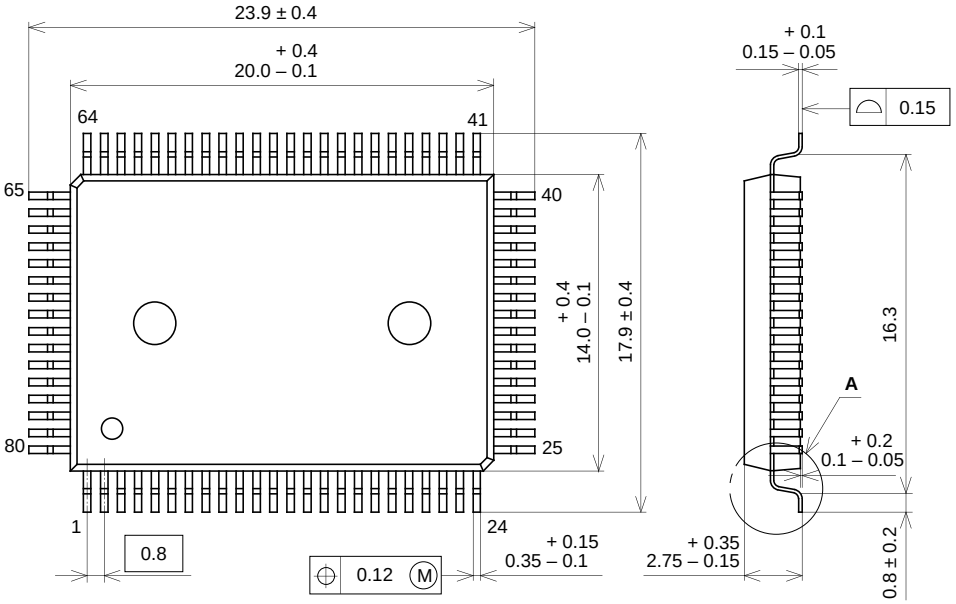


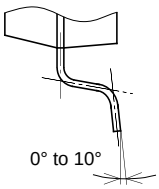
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Circuit Example
MURATA MFG CO., LTD	CSA4.19MG	4.19	30	30	(i)
	CSA8.00MG	8.00			
	CSA10.0MT	10.00			
	CST4.19MGW*	4.19			(ii)
	CST8.00MTW*	8.00			
	CST10.00MTW*	10.00			
FUJI SANGYO CO., LTD	HC-49/U03	4.19	15	15	(i)
		8.00			
		10.00			
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	
		8.00			
		10.00			

* Indicates types with on-chip grounding capacitors (C_1 and C_2).

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g