SONY

CXP82712/82716

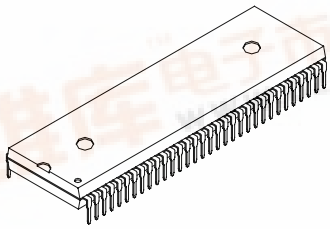
CMOS 8-bit Single Chip Microcomputer

Description

The CXP82712/82716 microcomputer is composed of a 8-bit CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time base timer, fluorescent display controller/driver, remote control receiver, PWM output circuit and 32kHz timer/counter.

This device also includes sleep/stop functions which can be used to achieve low power consumption.

64 pin SDIP (Plastic)



Structure

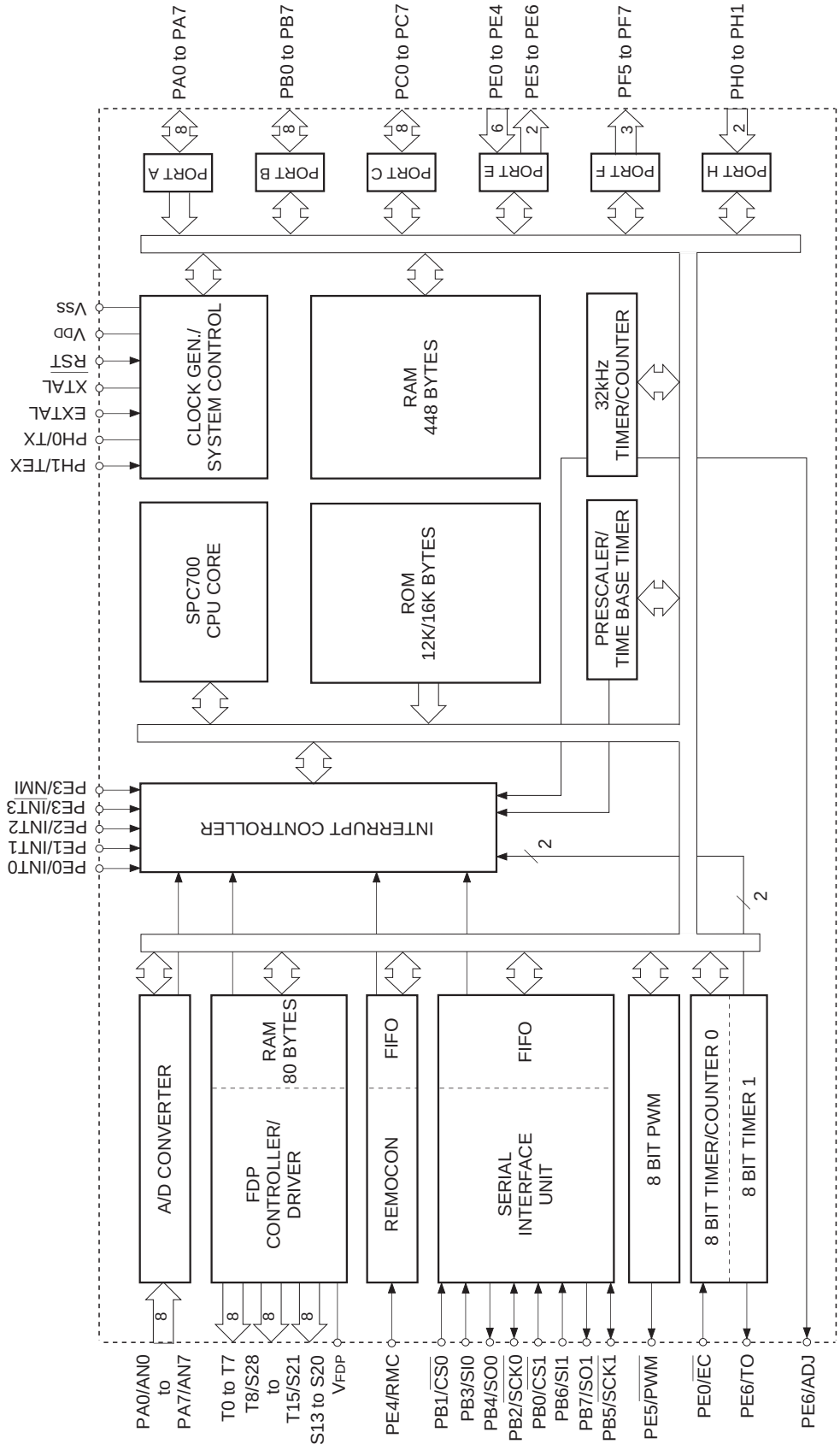
Silicon gate CMOS IC

Features

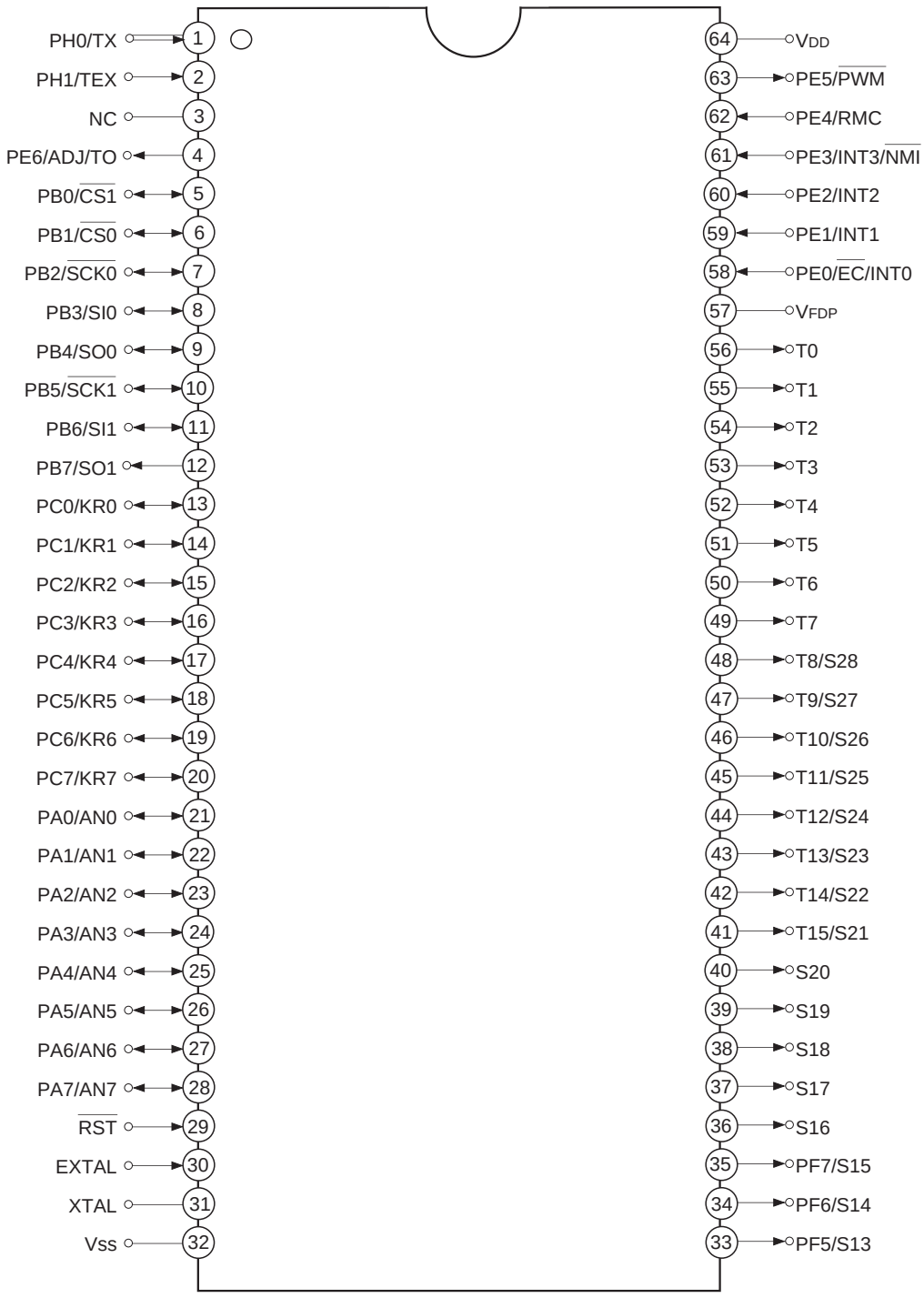
- Instruction set which supports a wide array of data types
  - — 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle — 400ns for 10MHz, 122µs for 32kHz operation
- On-chip ROM — 12K bytes (CXP82712)
  16K bytes (CXP82716)
- On-chip RAM — 448 bytes (Including fluorescent display data area)
- Peripheral functions
  - — A/D converter — 8-bit, 8-channel, successive approximation system (conversion rate 32µs/10MHz)
  - — Serial interface — On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer), 1 circuit 2-channel
  - — Timers — 8-bit timer
    8-bit timer/counter
    19-bit time base timer
    32kHz timer/counter
  - — Fluorescent display controller/driver — 24 high voltage tolerance output ports
    Maximum of 144 segments display available
    1 to 16 digits dynamic display
    Dimmer function
    High voltage tolerance output (40V)
    On-chip pull-down resistor (Mask option)
    Hardware key scan function (Maximum of 8 × 8 key matrix available)
  - — Remote control receiver circuit — On-chip 6-stage FIFO 8-bit pulse measurement counter
  - — PWM output — 8-bit, 1-channel
- Interruption — 13 factors, 13 vectors, multi-interruption possible
- Standby mode — Sleep/stop
- Package — 64-pin plastic SDIP
- Piggyback/evaluator — CXP82700 64-pin ceramic SDIP

E93Y23A79-PS

Block Diagram



Pin Assignment (Top View)



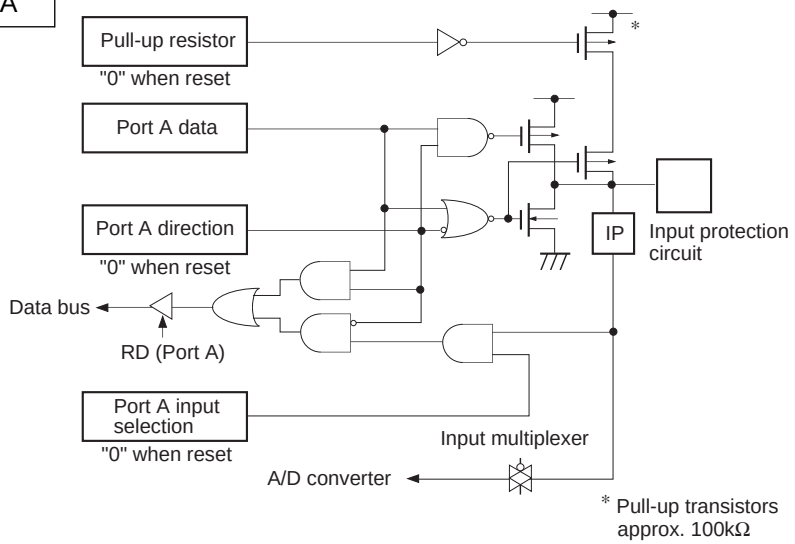
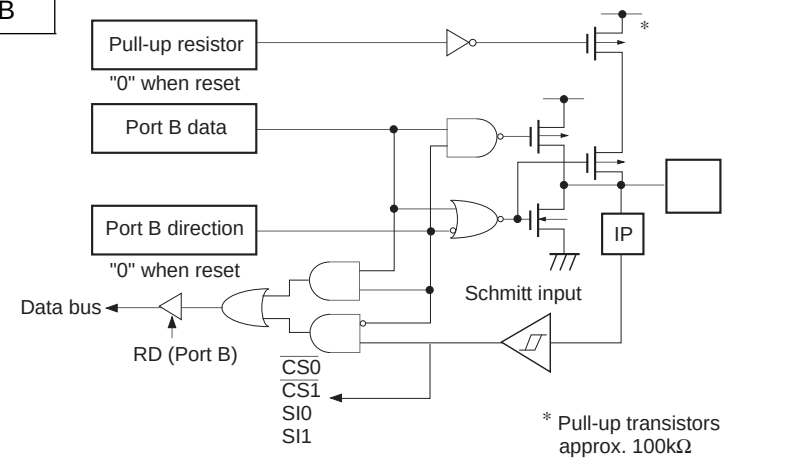
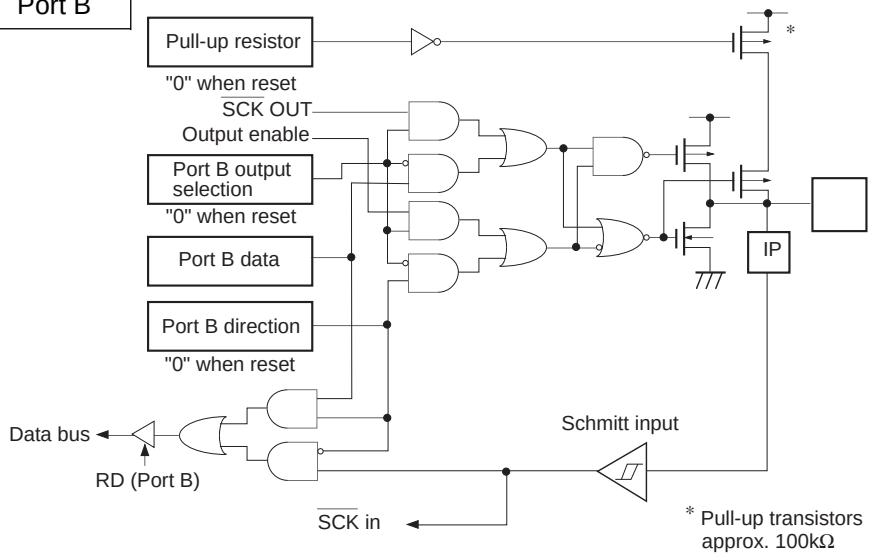
Note) 1. NC (Pin 3) is always connected to V_{DD}.
2. PH0/TX (Pin 1) is input port during port selection;
oscillation output during oscillation selection

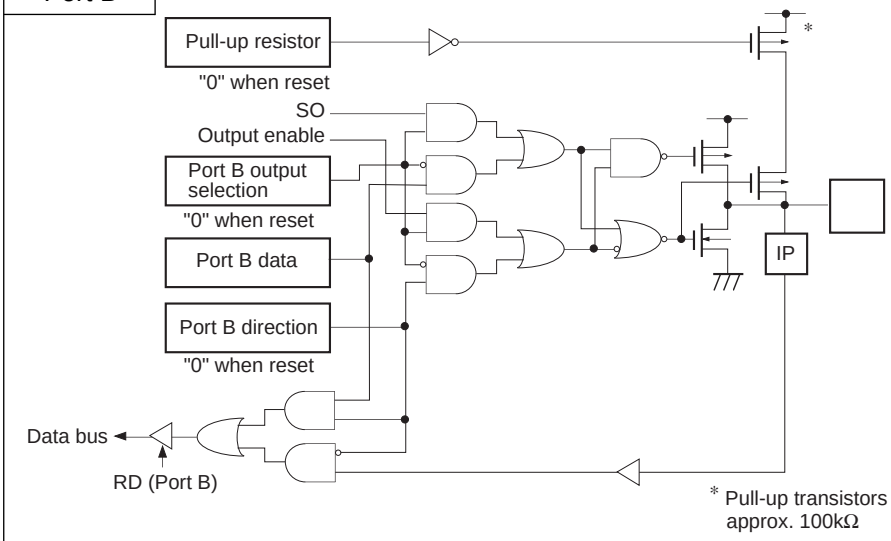
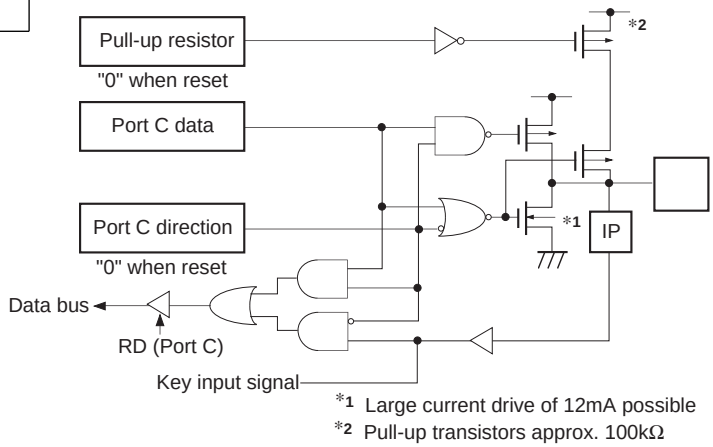
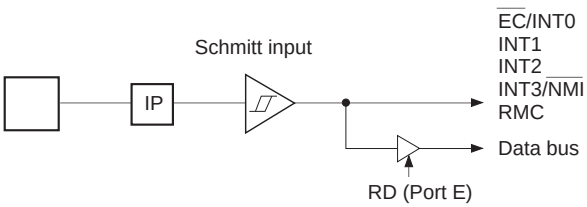
Pin Description

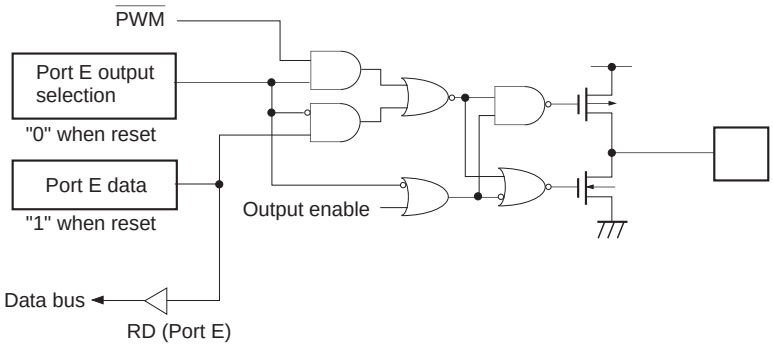
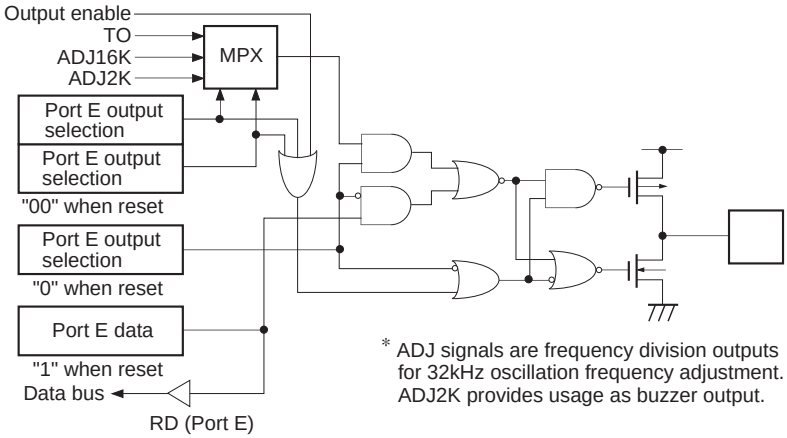
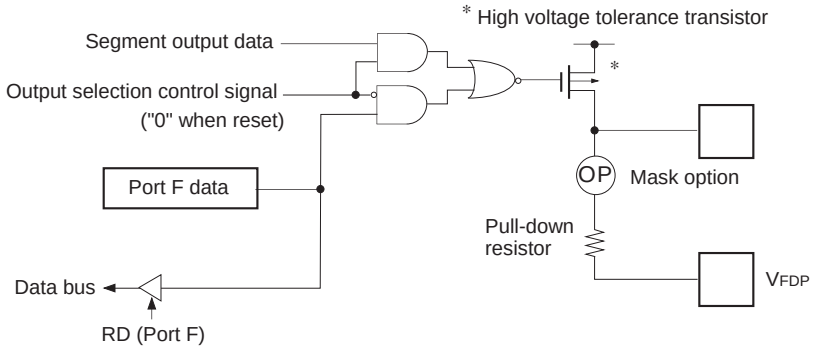
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog Input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/$\overline{CS1}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/ $\overline{EC0}$	Input/Input/ Input	(Port E) Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External interrupt requests. (4 pins) — External event input to timer/counter. (1 pin)
PE1/INT1	Input/Input		External interrupt requests. (4 pins)
PE2/INT2	Input/Input		External interrupt requests. (4 pins)
PE3/INT3/ $\overline{NMI}$	Input/Input/ Input		External interrupt requests. (4 pins) — Non-maskable interruption request input.
PE4/RMC	Input/Input		Input for remote control receiver circuit.
PE5/$\overline{PWM}$	Output/Output		8-bit PWM output.
PE6/ADJ/TO	Output		Output for timer/counter rectangular waveform and 32kHz oscillation frequency division.

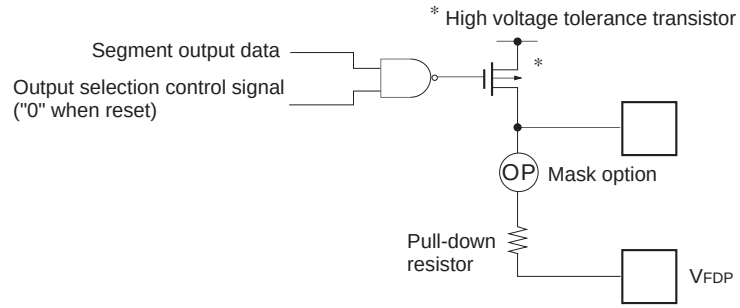
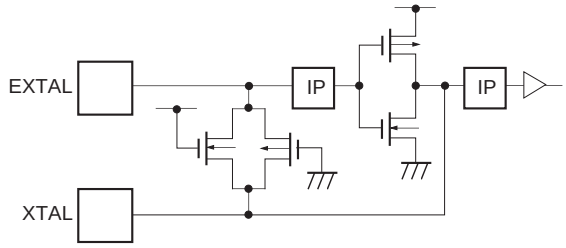
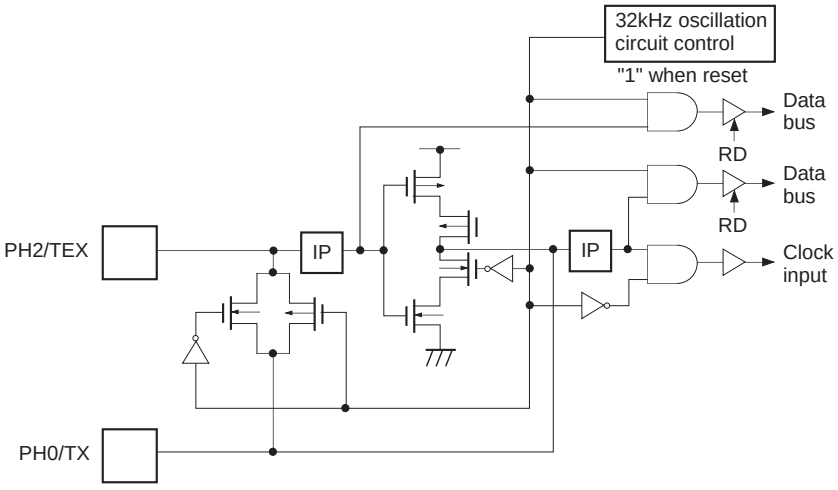
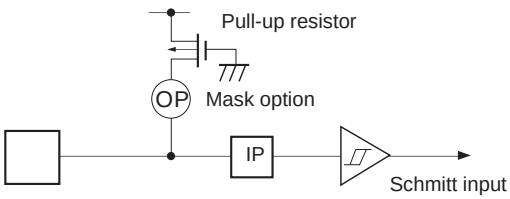
Symbol	I/O	Functions	
PF5/S13 to PF7/S15	Output/Output	(Port F) 3-bit output port. (3 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Dual purpose output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
V_{FDP}		Provides voltage for FDP when on-chip resistor is selected under mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
PH1/TEX	Input/Input	(Port H) 2-bit input port. (2 pins)	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.
PH0/TX	Input/Output		
$\overline{RST}$	Input	System reset pin of active "L" level. $\overline{RST}$ is input pin.	
NC		NC. Under normal operating conditions, connect to V_{DD}.	
V_{DD}		Vcc supply.	
Vss		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/$\overline{CS1}$ PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B 	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC}$/INT0 PE1/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE5/$\overline{\text{PWM}}$ 1 pin	Port E 	High level
PE6/TO/ADJ 1 pin	Port H 	High level (High level with 150kΩ resistor when reset)
PF5/S13 to PF7/S15 3 pins	Port F 	Hi-Z or Low level (When PD resistor is connected

Pin	Circuit format	When reset
S16 to S20 T15/S21 to T8/S28 T0 to T7 21 pins		Hi-Z or Low level (When PD resistor is connected)
EXTAL XTAL 2 pins		Oscillation
PH1/TEX PH0/TX 2 pins		Oscillation halted port input
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Display output voltage	V_{OD}	V_{DD} – 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current	I_{OH}	–5	mA	Other than display output pins*2: per pin
	I_{ODH1}	–15	mA	Display output S13 to S20: per pin
	I_{ODH2}	–35	mA	Display output T0 to T7, T8/S28 to T15/S21: per pin
High level total output current	$\sum I_{OH}$	–40	mA	Total of pins other than display output pins
	$\sum I_{ODH}$	–100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	Large current port*3 : per pin
Low level total output current	$\sum I_{OL}$	100	mA	Entire pin total
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 Specifies output current of general-purpose I/O ports.

*3 The large current drive transistor is an N-ch transistor of Port C (PC).

Note) If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High speed mode (1/2, 1/4 dividing clock) guaranteed operation range
		3.5	5.5	V	Low speed mode (1/16 dividing clock) guaranteed operation range
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during stop
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*1
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin*3
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*1
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*2
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	–20	+75	°C	

*1 All regular input port (PA, PB4, PB7, PC, PH).

*2 For pins $\overline{RST}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, SI0, SI1, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, INT3/$\overline{NMI}$, RMC.

*3 Specifies only for external clock input.

Electrical Characteristics

DC Characteristics (Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PC, PE5, PE6	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IH}	PA to PC*2	V_{DD} = 4.5V, V_{IH} = 4.0V	3.3			µA
	I_{IL}		V_{DD} = 5.5V, V_{IL} = 0.4V			50	µA
Display output current	I_{OH}	S13 to S20	V_{DD} = 4.5V V_{OH} = V_{DD} – 2.5V	–8			mA
		S21/T15 to S28/T8 T0 to T7		–20			mA
Open drain output leak current (P-CH Tr off state)	I_{LOL}	S13 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} – 35V V_{FDP} = V_{DD} – 35V			–20	µA
Pull-down resistor*3	R_L	S13 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5V V_{FDP} = V_{DD} – 35V	60	100	270	kΩ
Input/Output leak current	I_{IZ}	PA to PC*2, PE0 to PE4 $\overline{RST}$*2	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Supply current*4	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency dividing clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		20	40	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		35	100	µA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		1.2	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		Stop mode V_{DD} = 5.5V, 10MHz termination of 10MHz and 32kHz crystal oscillation.			10	µA

Item	Symbol	Pin	Codition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	Pins other than S13 to S28, T0 to T7, PE5, PE6, V_{DD}, Vss, V_{FDP}	1MHz clock 0V for pins other than the measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*2 Pins PA to PC specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 Applies when the on-chip pull-down resistor is selected under the mask option.

*4 All output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*			ns
Event count input clock rise and fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

* tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).
tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

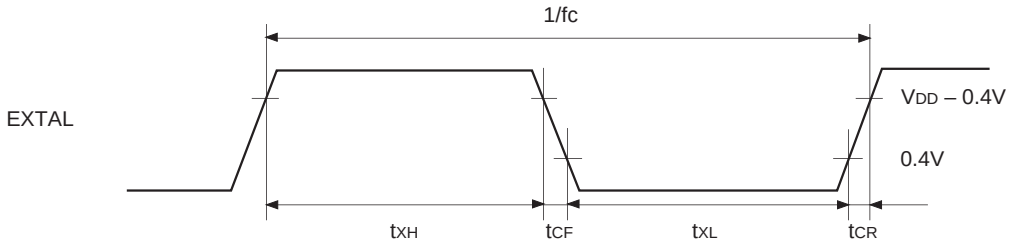


Fig. 1. Clock timing

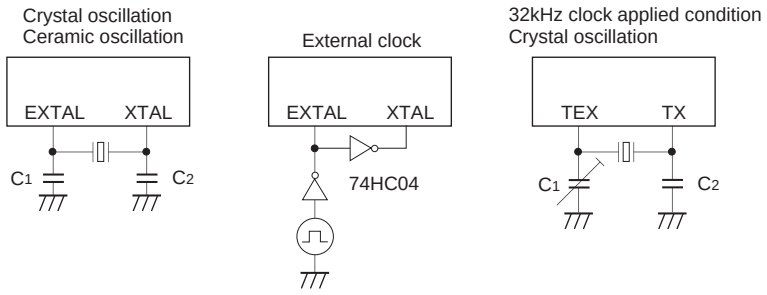


Fig. 2. Clock applied conditions

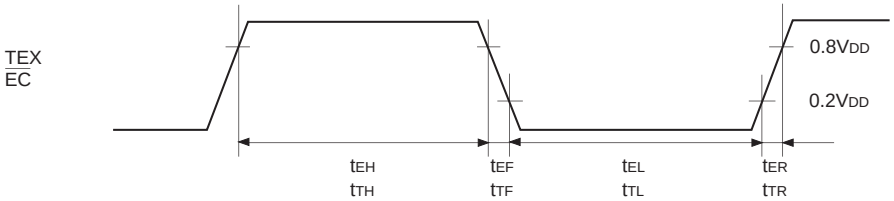


Fig. 3. Event count clock timing

(2) Serial transfer (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\downarrow\rightarrow\overline{SCK1}$) delay time	t_{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		1.5tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\uparrow\rightarrow\overline{SCK1}$) float delay time	t_{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		1.5tsys + 200	ns
$\overline{CS0}\downarrow\rightarrow$ SO0 ($\overline{CS1}\downarrow\rightarrow$ SO1) delay time	t_{DCSO}	SO0 (SO1)	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow$ SO0 ($\overline{CS1}\uparrow\rightarrow$ SO1) float delay time	t_{DCSOF}	SO0 (SO1)	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) high level width	t_{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t_{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	tsys+100		ns
			Output mode	8000/fc – 50		ns
SI0 (SI1) input seup time (for SCK0 ↑ ($\overline{SCK1}$ ↑))	t_{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for SCK0 ↑ ($\overline{SCK1}$ ↑))	t_{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	tsys + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 ($\overline{SCK1}\downarrow\rightarrow$ SO1) delay time	t_{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		tsys + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).
tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

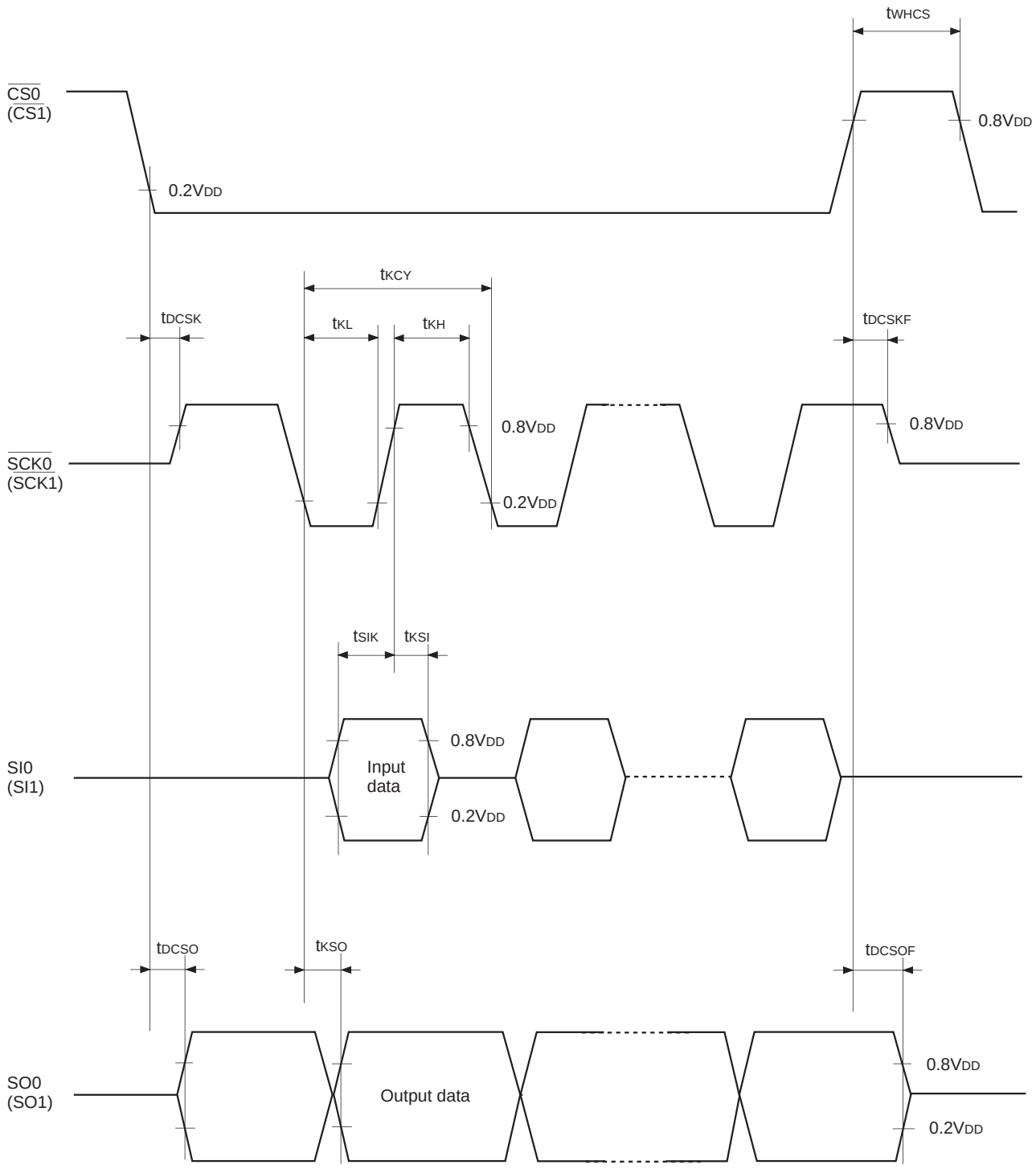


Fig. 4. Serial transfer timing

(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AVss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	70	150	mV
Full-scale transition voltage	V_{FT}*2			4930	5050	5120	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V

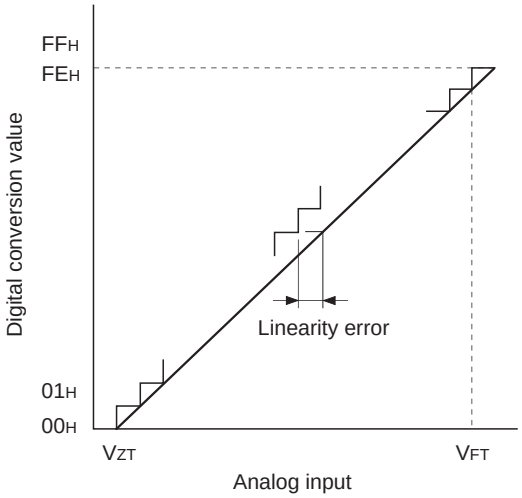


Fig. 5. Definition of A/D converter terms

*1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the Bit6 (CKS) of A/D control register (address: 00F9H) and the Bit7 (PCK1) and Bit6 (PCK0) of clock control register (address: 00FEH)

CSK / PCK1, 0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

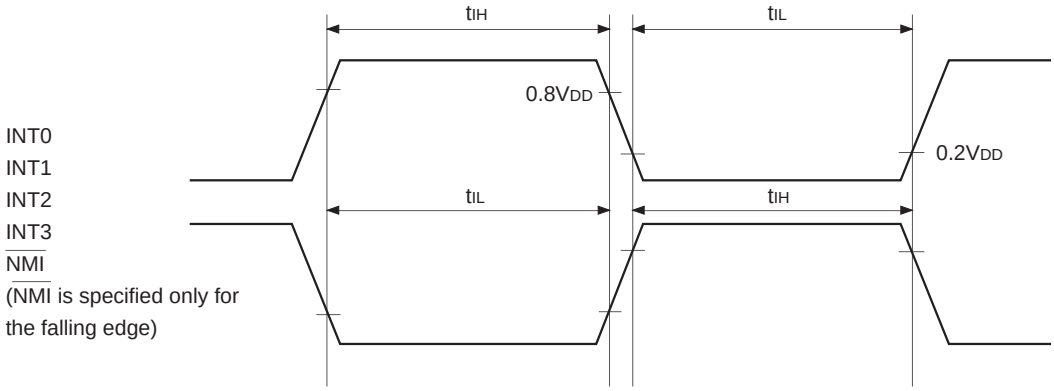


Fig 6. Interruption input timing

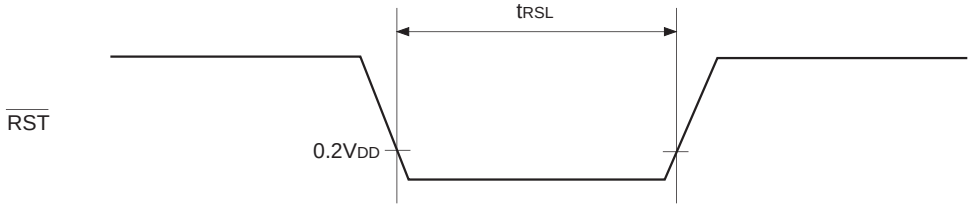


Fig. 7. $\overline{RST}$ input timing

Appendix

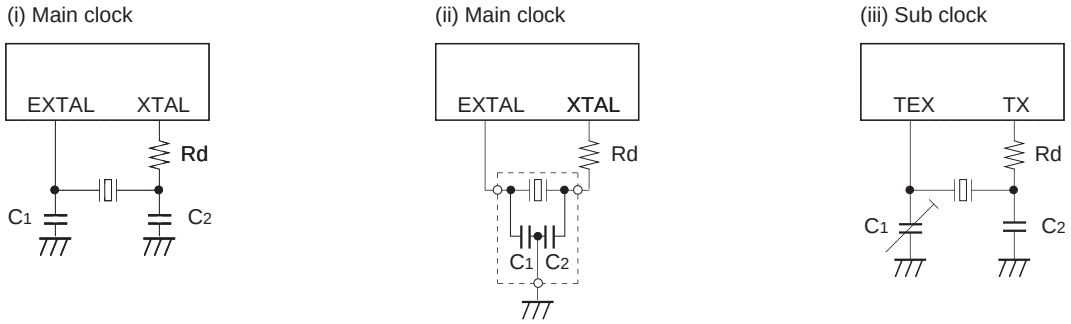


Fig. 8. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION.	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

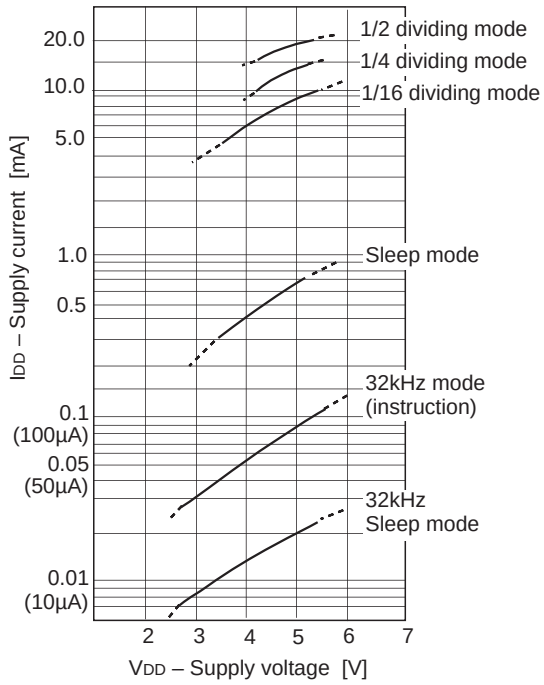
Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
High tension proof pull-down resistor	Non-existent	Existent (selected every pin)

Characteristics Curves

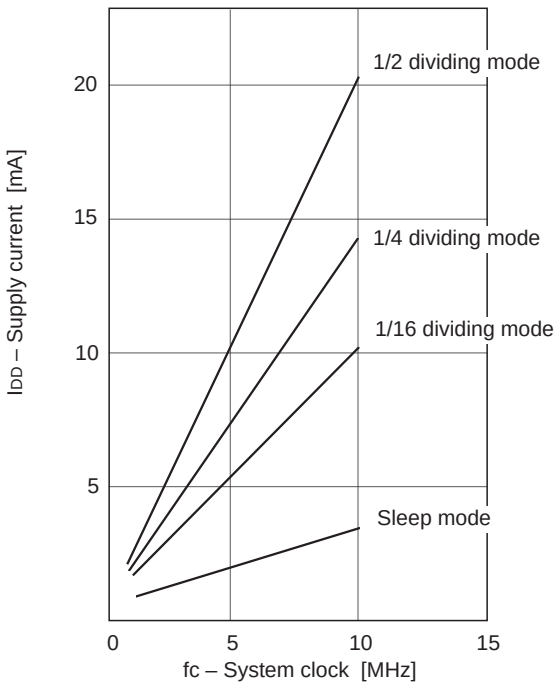
IDD vs. VDD

(fc = 10MHz, Ta = 25°C, Typical)



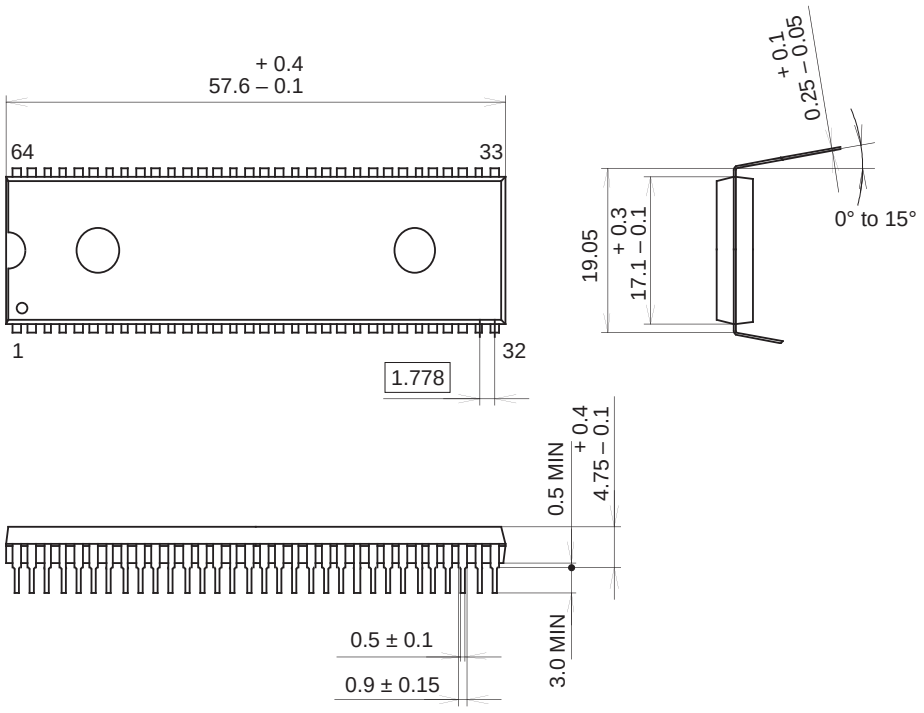
IDD vs. fc

(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit: mm

64PIN SDIP (PLASTIC)



SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g