

SONY

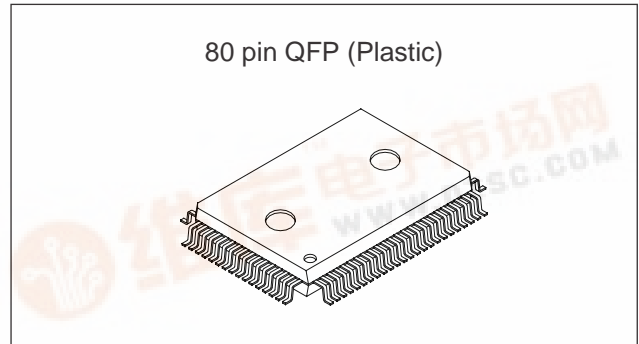
CXP84332/84340

CMOS 8-bit Single Chip Microcomputer

Description

CXP84332/84340 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, remote control reception circuit, and the like besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84332/84340 also provides a power-on reset function and a sleep/stop function that enables lower power consumption.



80 pin QFP (Plastic)

Features

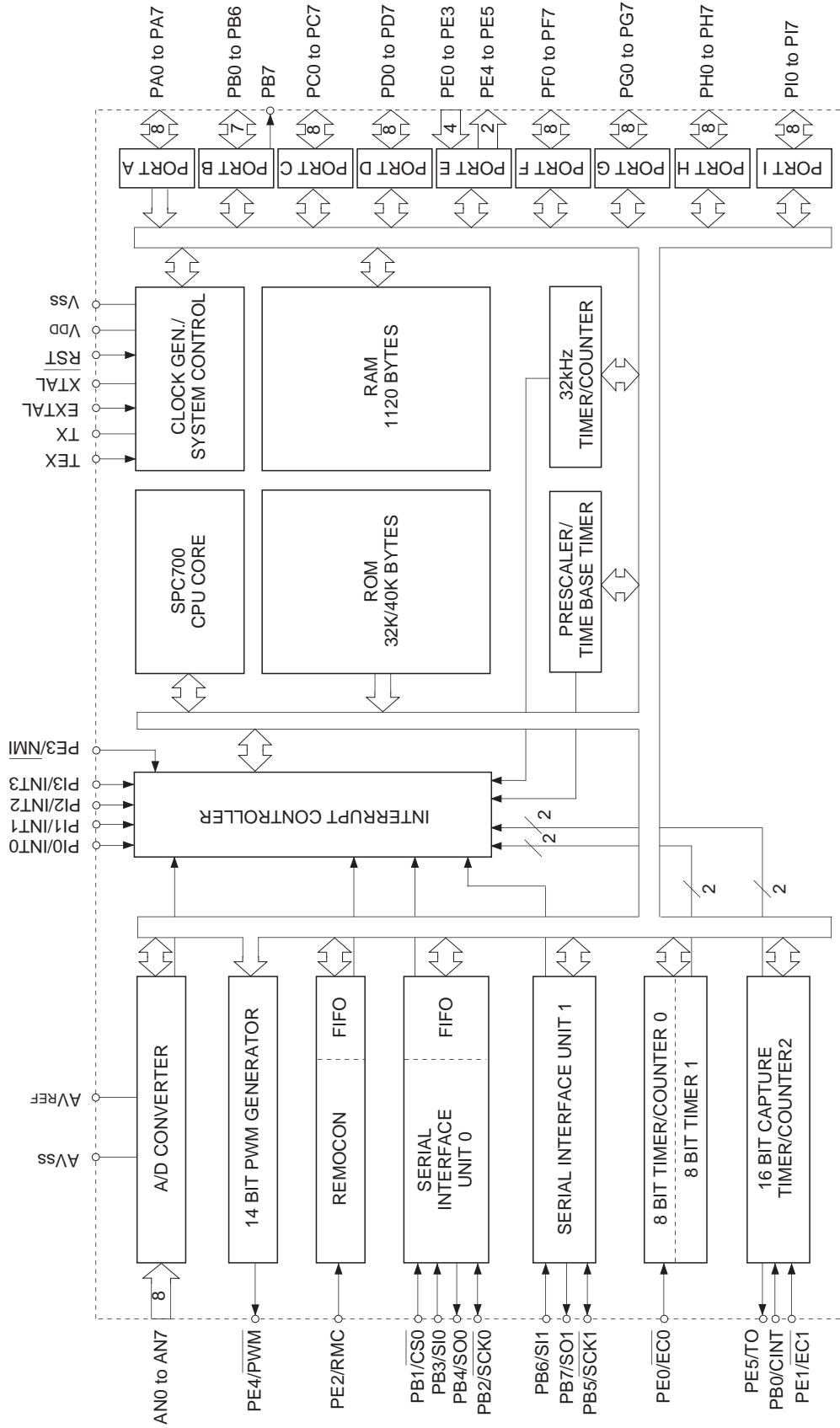
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
 - 400ns at 10MHz operation
 - 122μs at 32kHz operation
- Incorporated ROM capacity
 - 32K bytes (CXP84332)
 - 40K bytes (CXP84340)
- Incorporated RAM capacity
 - 1120 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time of 32μs/10MHz)
 - Serial interface
 - Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
 - 8-bit clock synchronization, 1 channel
 - Timers
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time base timer
 - 16-bit capture timer/counter
 - 32kHz timer/counter
 - Remote control reception circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
 - PWM output
 - 14 bits, 1 channel
- Interruption
 - 15 factors, 15 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 80-pin plastic QFP
- Piggyback/evaluation chip
 - CXP84300 80-pin ceramic QFP

Structure

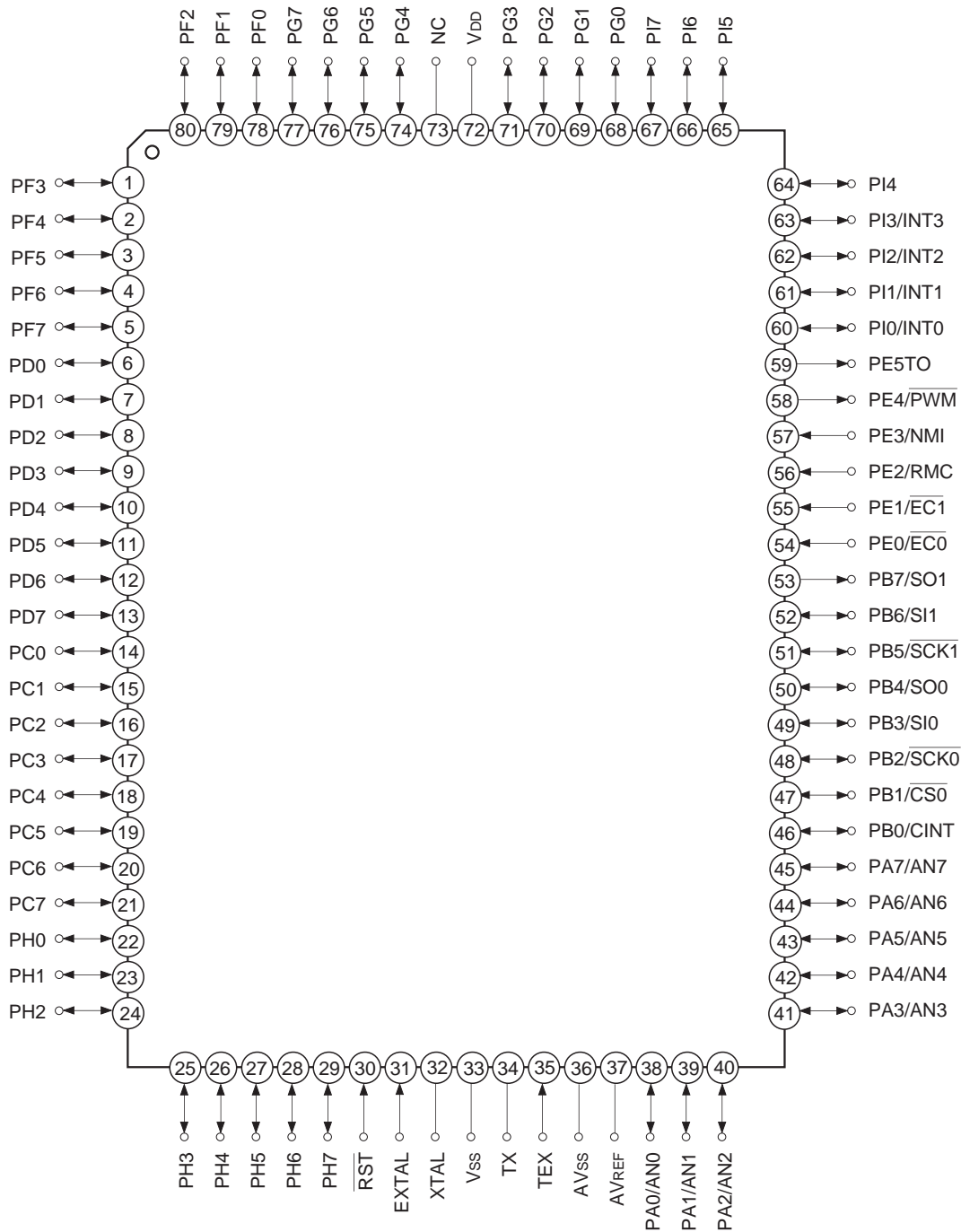
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



Note NC (Pin 73) must be connected to V_{DD}.

Pin Description

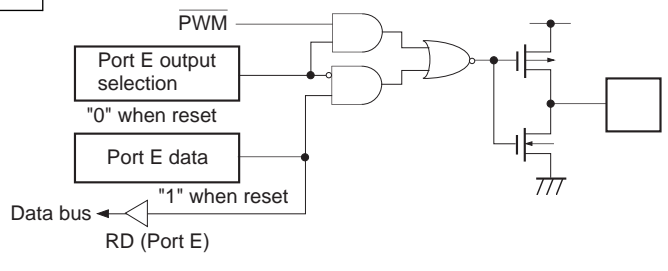
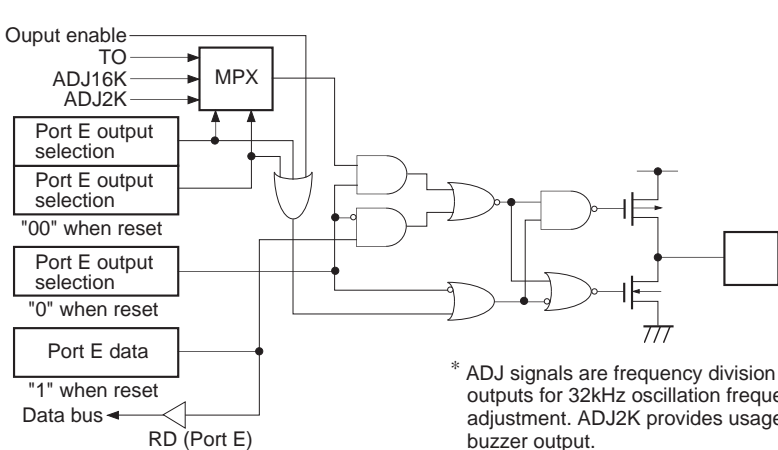
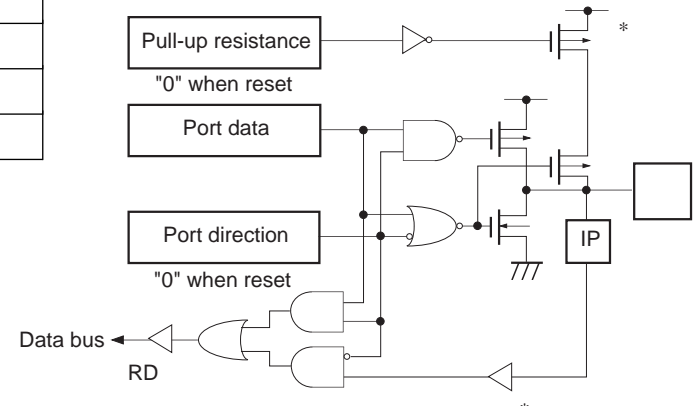
Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Lower 7-bit I/O port in which I/O can be set in a unit of single bits. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/CS0	I/O/Input		Chip select input for serial interface (CH0).
PB2/SCK0	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/SCK1	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/EC0	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (8 pins)	External event inputs for timer/counter. (2 pins)
PE1/EC1	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/NMI	Input/Input		Non-maskable interruption request input.
PE4/PWM	Output/Output		14-bit PWM output.
PE5/TO/ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter . Output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

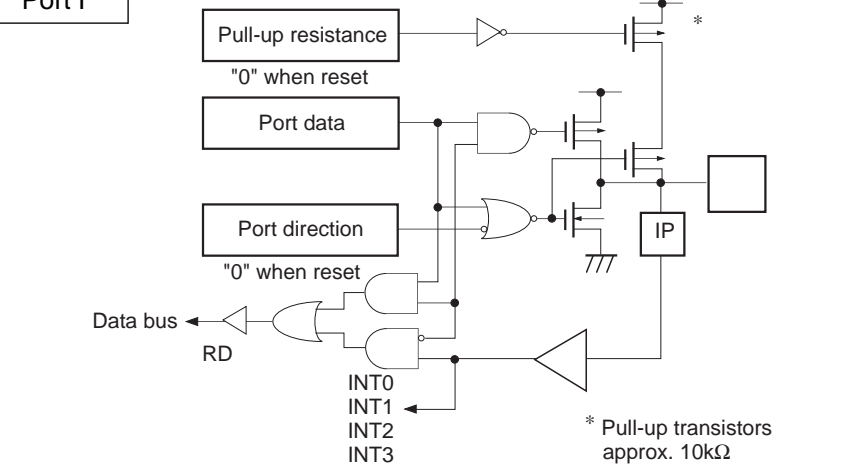
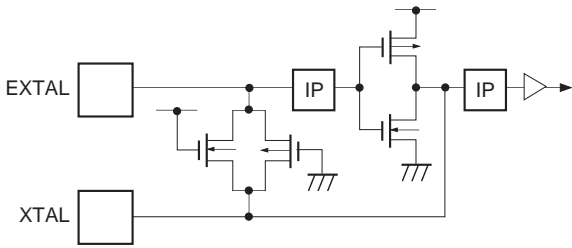
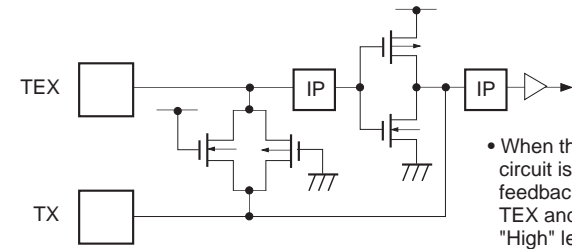
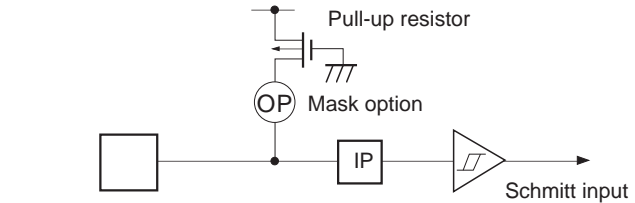
Symbol	I/O	Description	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs.
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V _{DD} .	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		Positive power supply.	
V _{SS}		GND	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus ← RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ← RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>SCK OUT</p> <p>Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ← RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p> <p>* Pull-up transistors approx. 200kΩ</p>	<p>High level</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p> <p>*1 High current drive of 12mA possible *2 Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PE0/EC0 PE1/EC1 PE2/RMC PE3/NMI</p> <p>4 pins</p>	<p>Port E</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE4/PWM</p> <p>1 pin</p>	<p>Port E</p>  <p>PWM</p> <p>Port E output selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus ← RD (Port E)</p>	<p>High level</p>
<p>PE5/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>Output enable</p> <p>TO</p> <p>ADJ16K</p> <p>ADJ2K</p> <p>MPX</p> <p>Port E output selection "00" when reset</p> <p>Port E output selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus ← RD (Port E)</p> <p>* ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p>	<p>High level</p>
<p>PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7</p> <p>36 pins</p>	<p>Port D</p> <p>Port F</p> <p>Port G</p> <p>Port H</p> <p>Port I</p>  <p>Pull-up resistance "0" when reset</p> <p>Port data</p> <p>Port direction "0" when reset</p> <p>Data bus ← RD</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI0/INT0 to PI3/INT3</p> <p>4 pins</p>	<p>Port I</p>  <p>Pull-up resistance "0" when reset</p> <p>Port data</p> <p>Port direction "0" when reset</p> <p>Data bus ← RD</p> <p>INT0 INT1 INT2 INT3</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>OP Mask option</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	Output per pin
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding large current outputs
	I _{OLC}	20	mA	Value per pin*2 for large current outputs
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The high current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode guaranteed operation range*1
		3.5	5.5		Low-speed mode guaranteed operation range*1
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during stop
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*3
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*4
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*3
	V _{ILEX}	-0.3	0.4	V	EXTAL*4
Operating temperature	T _{opr}	-20	+75	°C	

*1 High-speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

*2 Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF to PH, PI4 to PI7).

*3 Value of the following pins: RST, CINT, CS0, SCK0, SCK1, EC0, EC1, RMC, NMI, INT0, INT1, INT2, INT3.

*4 Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
			V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
			V _{DD} = 5.5V, V _{IL} = 0.4V	-0.1		-10	μA
	I _{ILR}	$\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400	μA
	I _{IL}	PA to PD* ² , PF to PI* ²	V _{DD} = 5.5V, V _{IL} = 0.4V			-2.0	mA
V _{DD} = 4.5V, V _{IL} = 4.0V			-10			μA	
I/O leakage current	I _{Iz}	PE0 to PE3, $\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Power supply current* ³	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency demultiplier clock)		20	42	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		35	100	μA
	I _{DDs1}		Sleep mode		1.1	8	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
I _{DDs2}	V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA		
I _{DDs3}	Stop mode			10	μA		
	V _{DD} = 5.5V, termination of 10MHz and 32kHz crystal oscillation						
Input capacity	C _{IN}	Pins other than PB7, PE4, PE5, AV _{REF} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 Pins PA to PD, and PF to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*3 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	tXL, tXH	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	tCR, tCF	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	tEH, tEL	EC0 EC1	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	tER, tEF	EC0 EC1	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	tTL, tTH	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	tTR, tTF	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

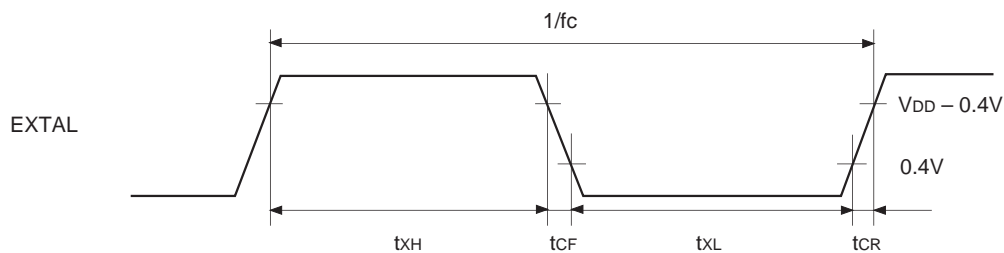


Fig. 1. Clock timing

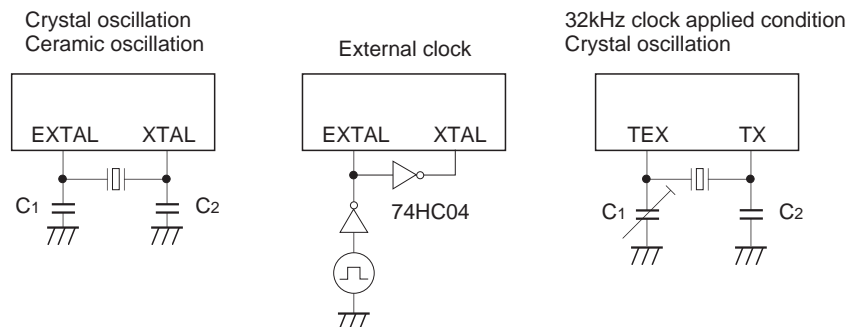


Fig. 2. Clock applied condition

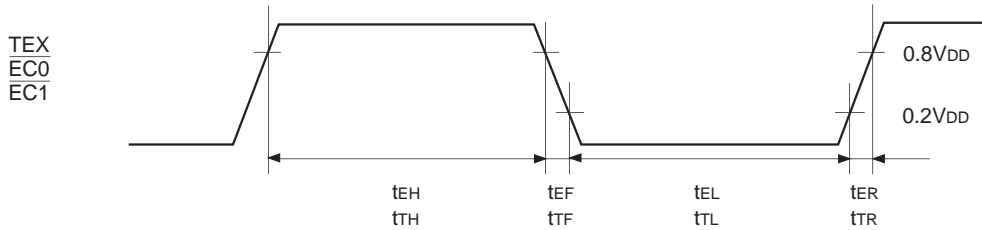


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{D_{CSK}}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{D_{CSKF}}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{D_{CSO}}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{D_{CSOF}}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ High level width	t _{WH_{CS}}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ cycle time	t _{K_{CY}}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High and Low level widths	t _{K_H} t _{K_L}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{K_{SI}}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{K_{SO}}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

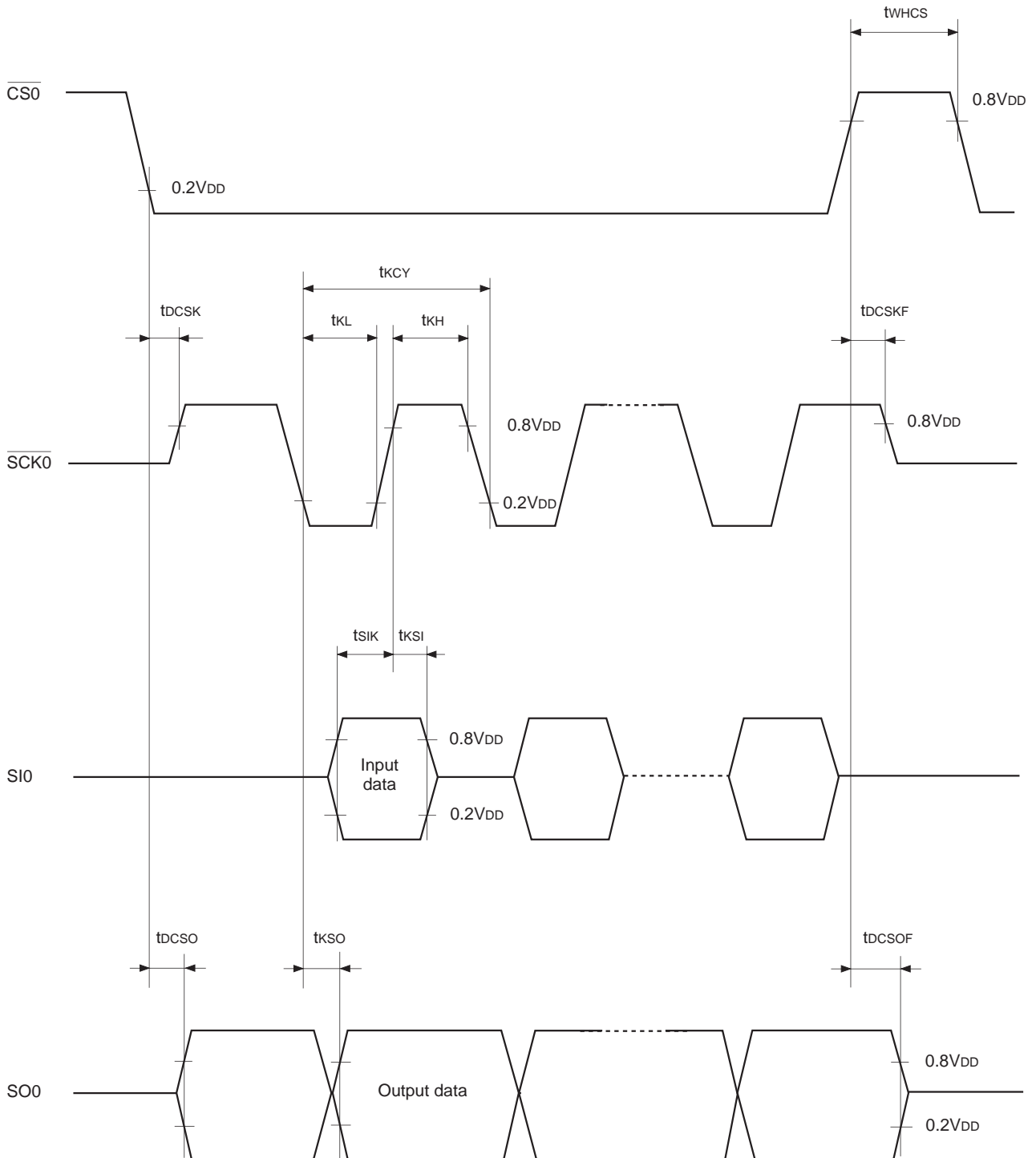


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High and Low level widths	t_{KH}	$\overline{\text{SCK1}}$	Input mode	400		ns
	t_{KL}		Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

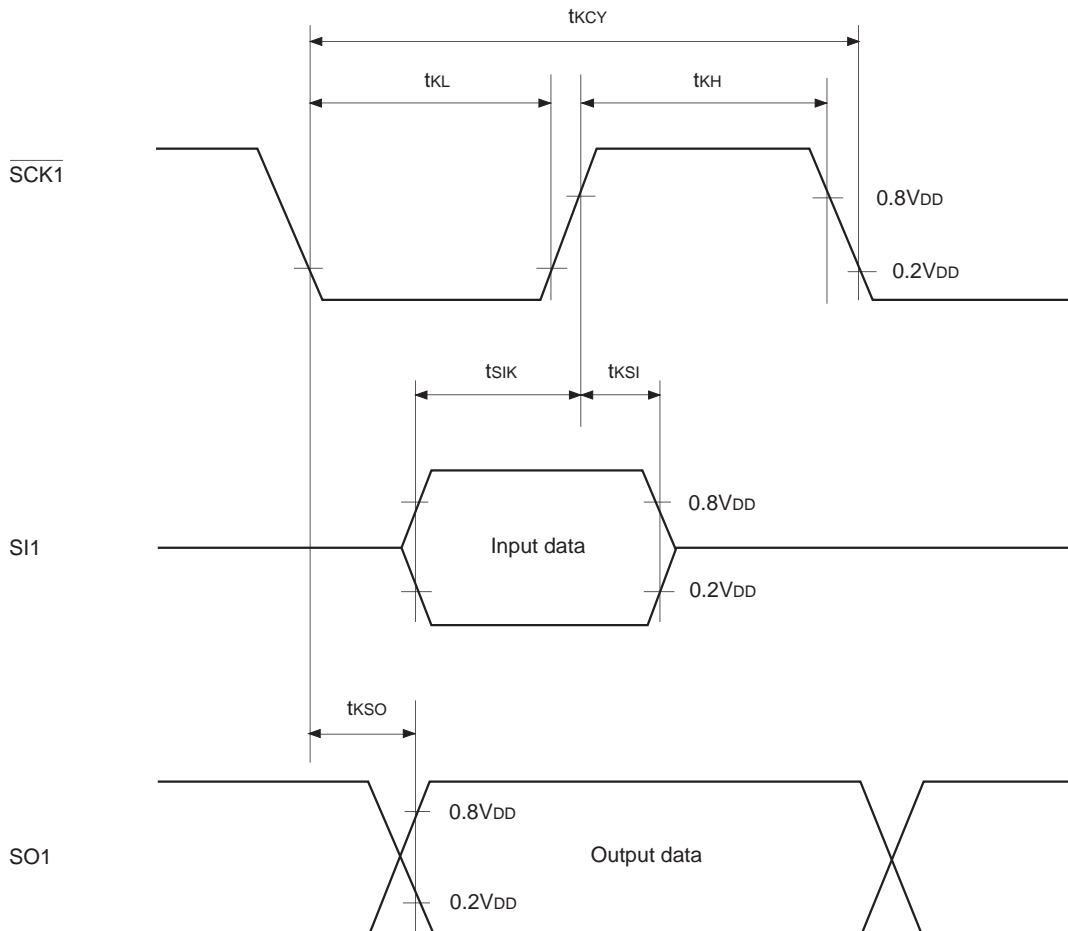
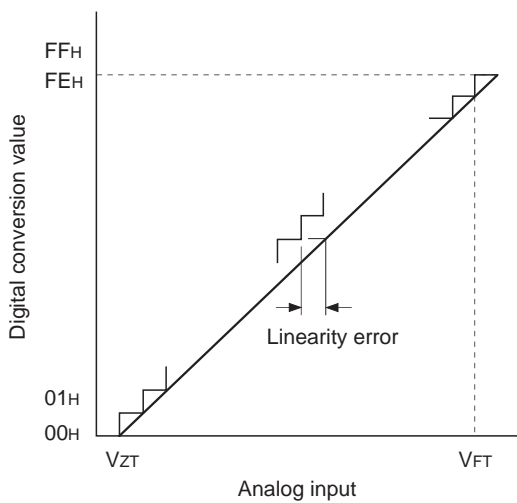


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 5	LSB
Zero transition voltage	V_{ZT}^{*1}			-10	70	150	mV
Full-scale transition voltage	V_{FT}^{*2}			4930	5050	5120	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA



*1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to ADC operation clock selection.

During PS2 selection, $f_{ADC} = f_c/2$

During PS1 selection, $f_{ADC} = f_c$

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High and Low level widths	t _{IH} t _{IL}	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		8/fc		μs

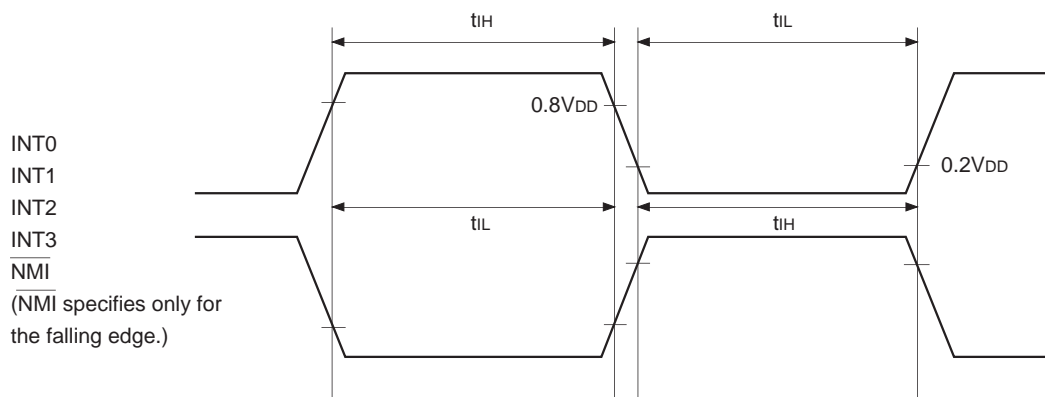


Fig 7. Interruption input timing

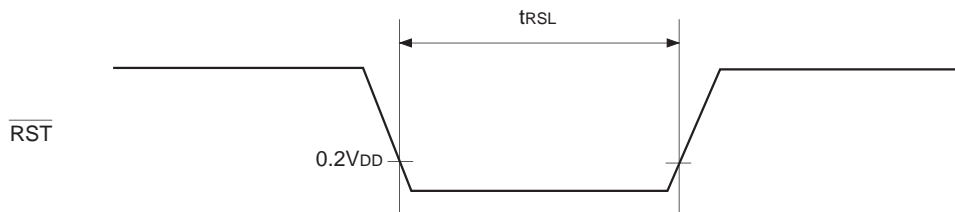


Fig. 8. $\overline{\text{RST}}$ input timing

Appendix

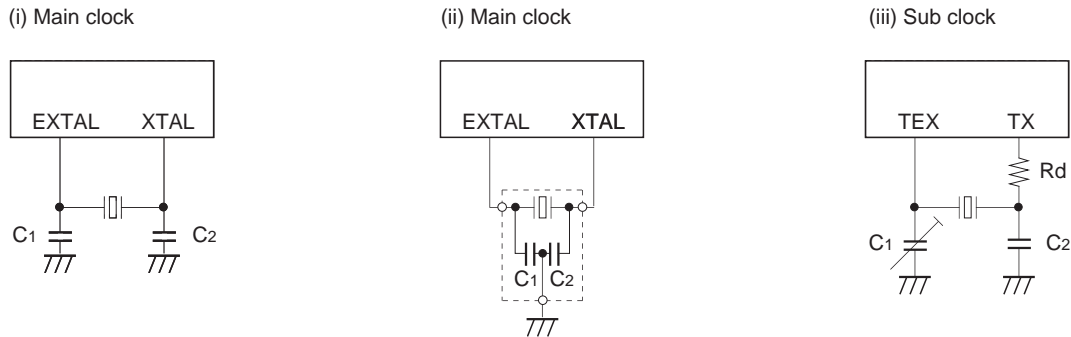


Fig. 9. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

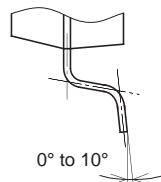
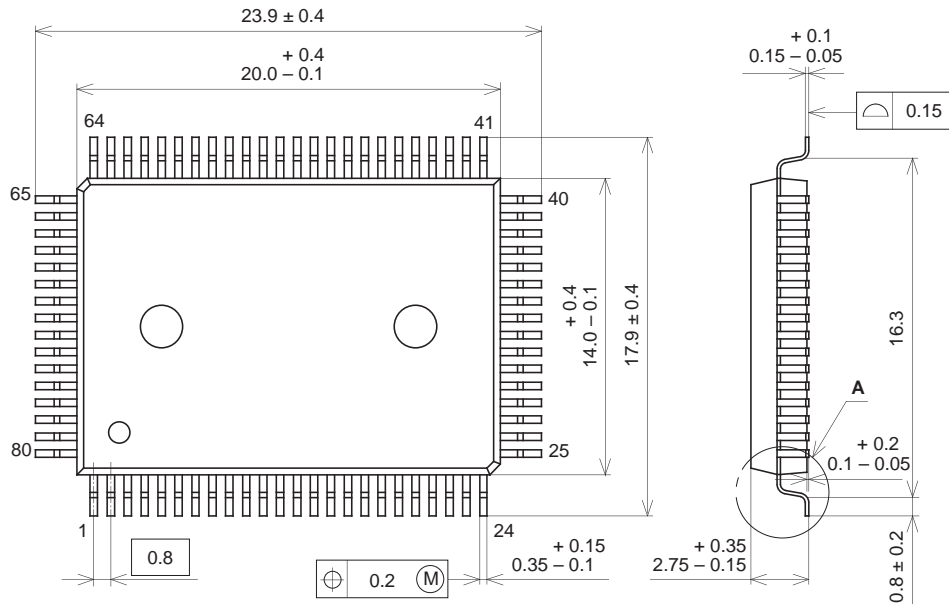
Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Mask option table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g