SONY

CXP843P40

CMOS 8-bit Single Chip Microcomputer

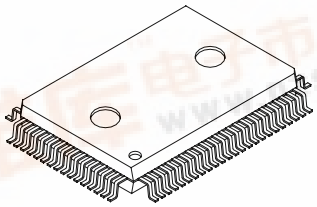
Description

The CXP843P40 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, and remote control reception circuit besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP843P40 also provides a sleep/stop function that enables lower power consumption.

This IC is the PROM-incorporated version of the CXP84340 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

80 pin QFP (Plastic)



Structure

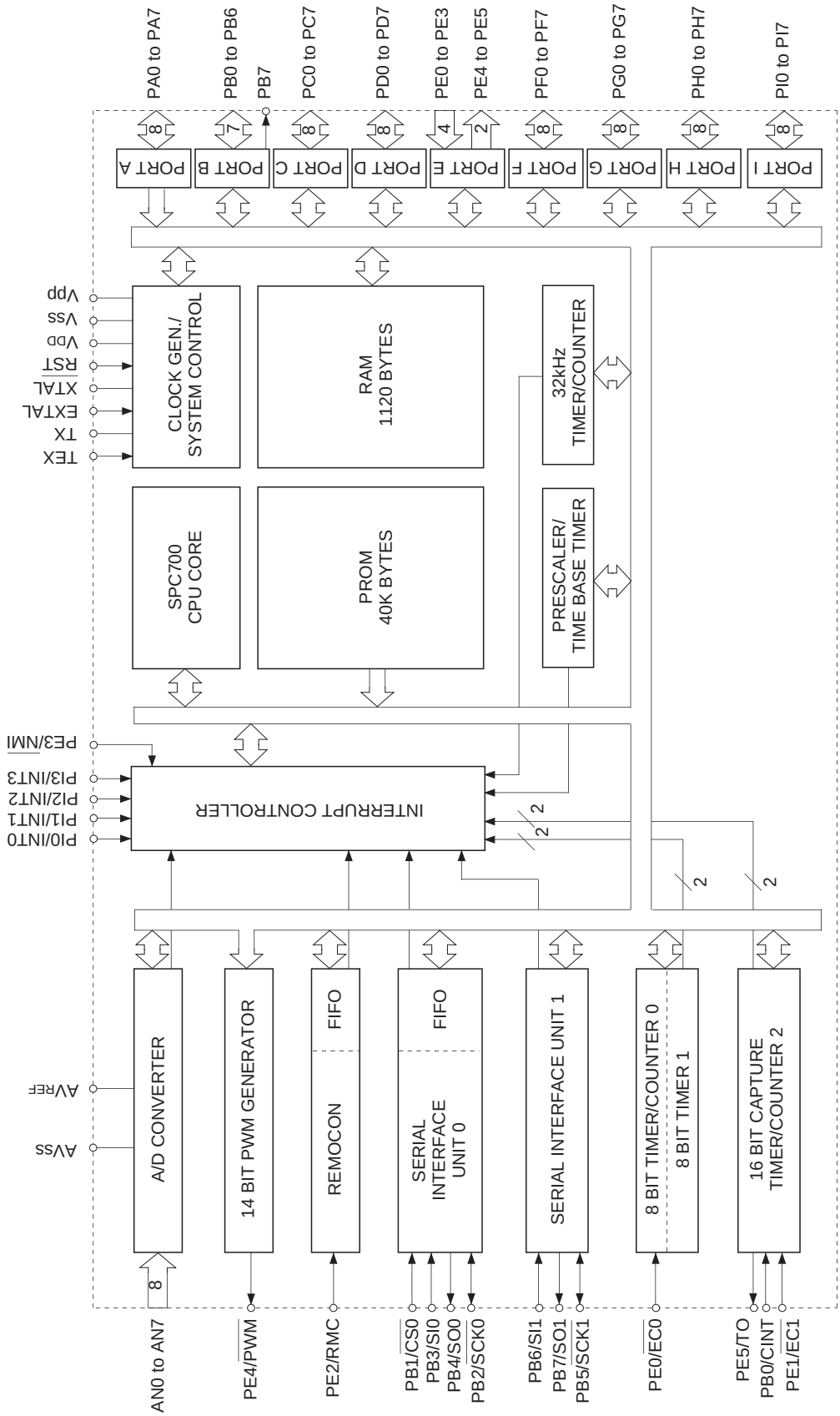
Silicon gate CMOS IC

Features

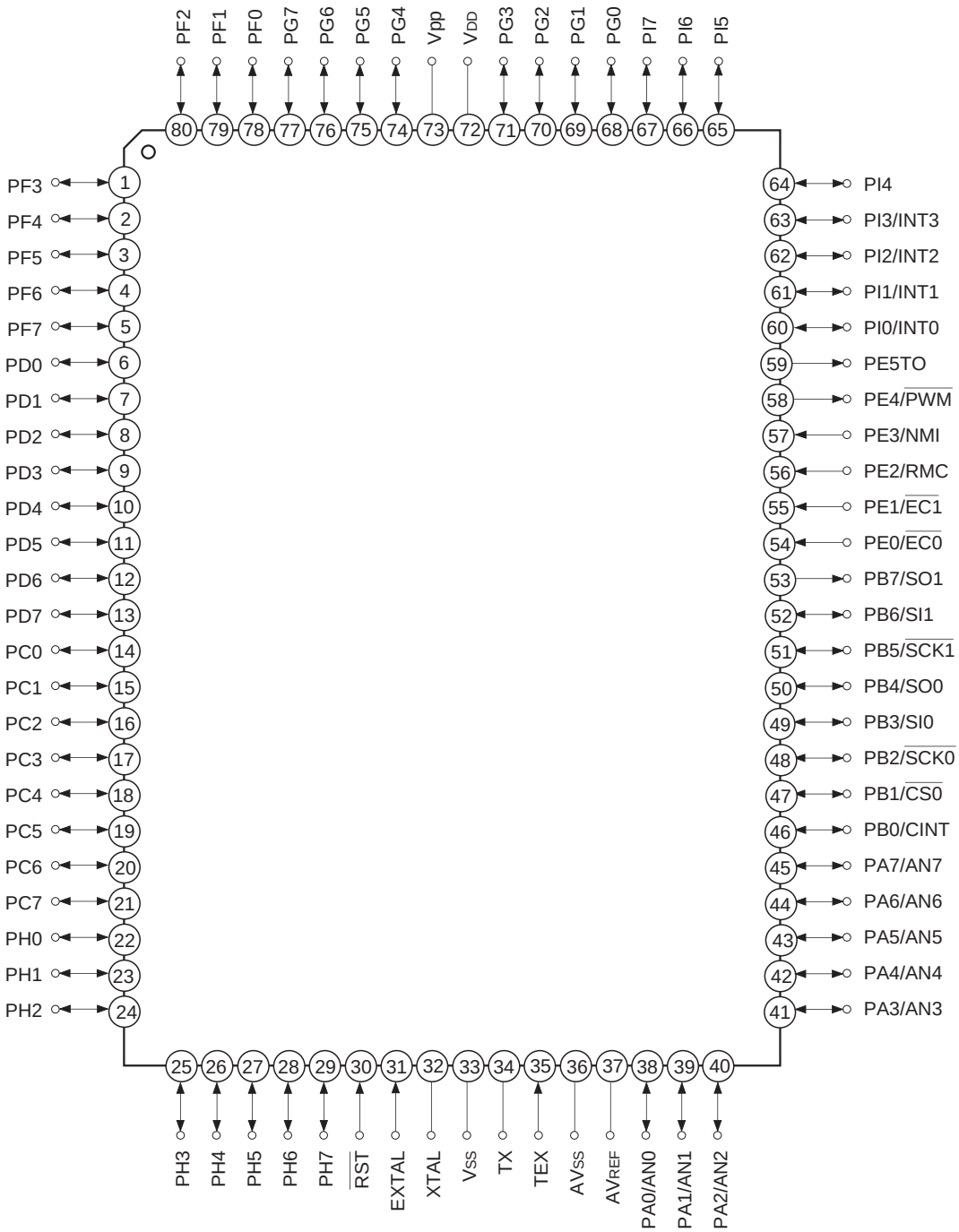
- Wide-range instruction system (213 instructions) to cover various types of data
  - — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 400ns at 10MHz operation; 122µs at 32kHz operation
- Incorporated PROM capacity — 40K bytes
- Incorporated RAM capacity — 1120 bytes
- Peripheral functions
  - — A/D converter — 8 bits, 8 channels, successive approximation method (Conversion time of 32µs/10MHz)
  - — Serial interface — Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock synchronization, 1 channel
  - — Timer — 8-bit timer; 8-bit timer/counter; 19-bit time base timer; 16-bit capture timer/counter; 32kHz timer/counter
  - — Remote control reception circuit — 8-bit pulse measuring counter, 6-stage FIFO
  - — PWM output — 14 bits, 1 channel
- Interruption — 15 factors, 15 vectors, multi-interruption possible
- Standby mode — Sleep/stop
- Package — 80-pin plastic QFP

E93840A7Y-PS

Block Diagram



Pin Assignment (Top View)



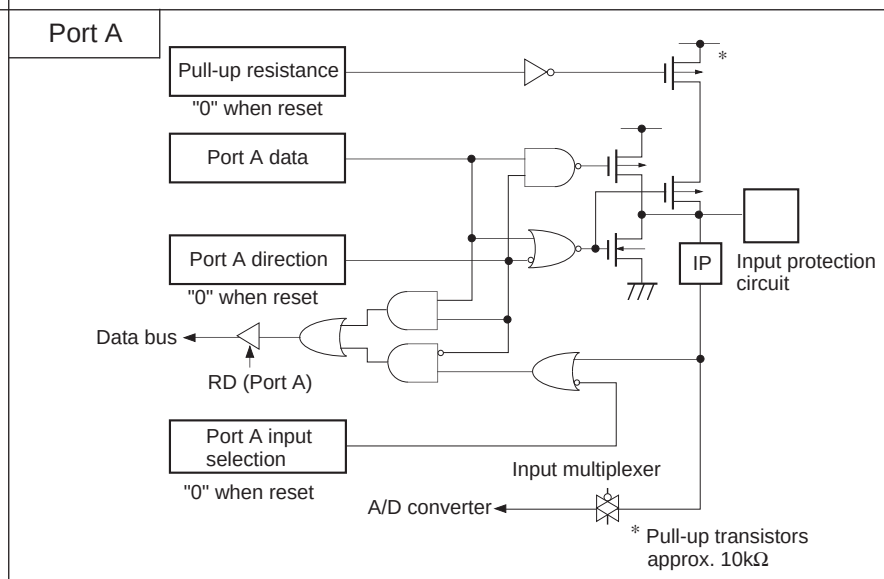
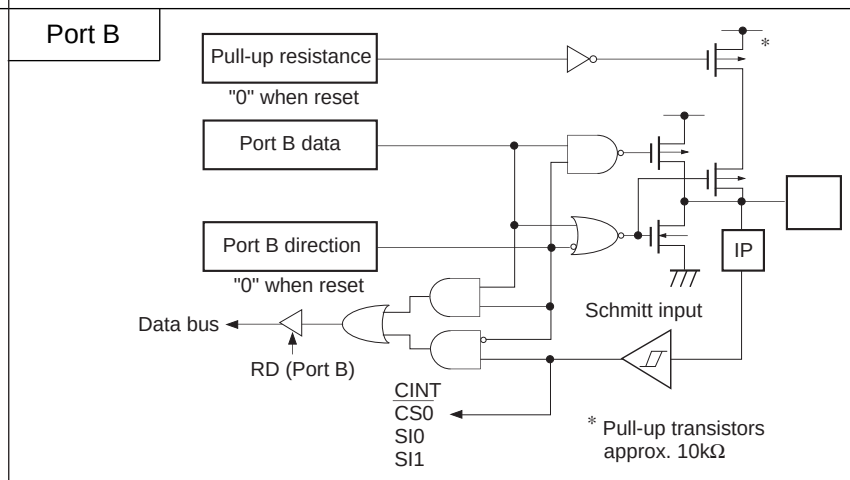
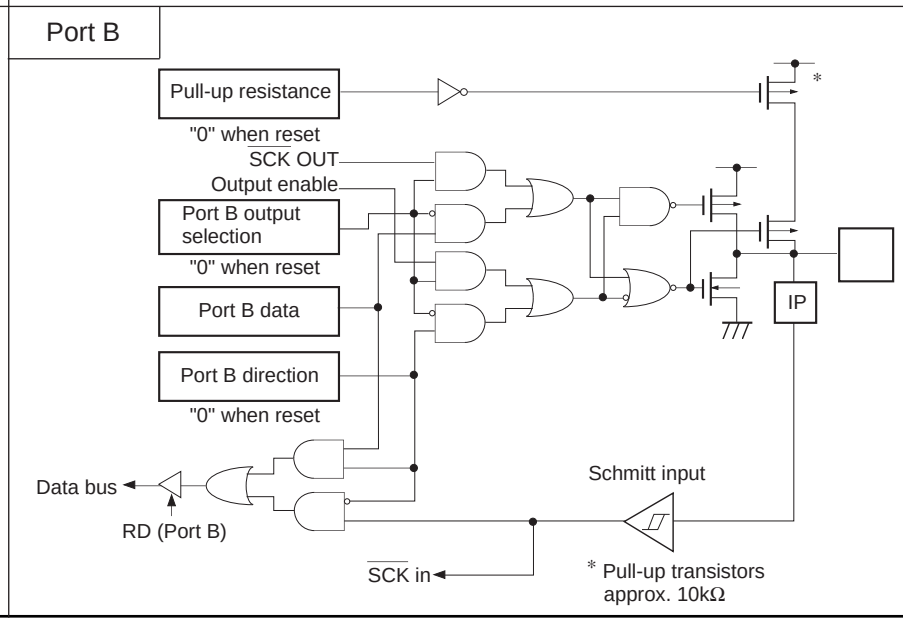
Note) Vpp (Pin 73) must be connected to V_{DD}.

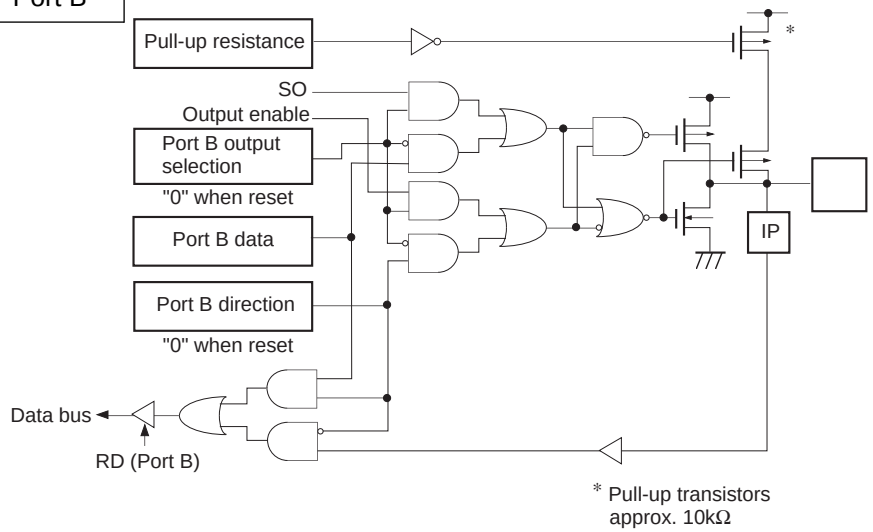
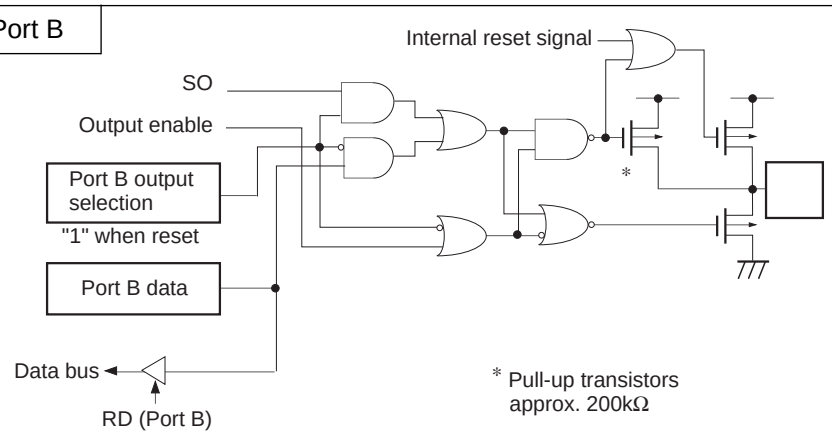
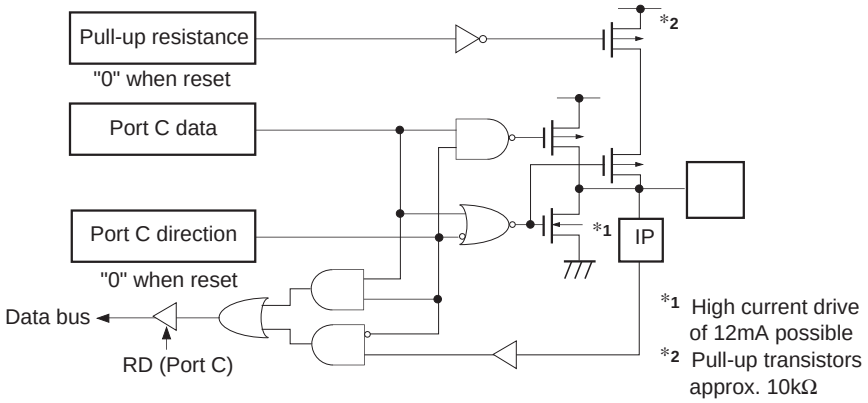
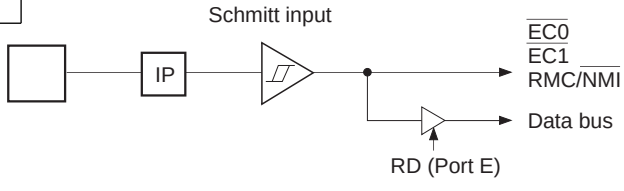
Pin Description

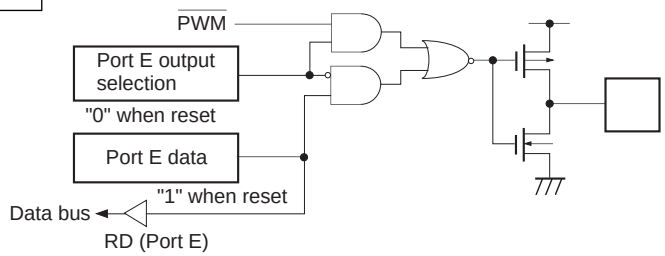
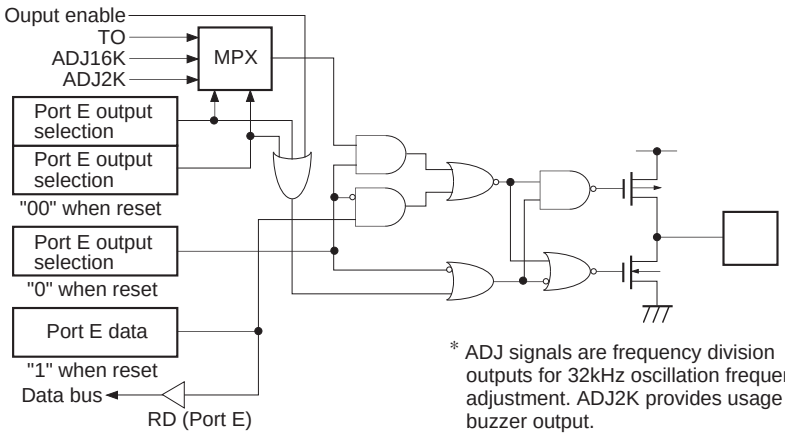
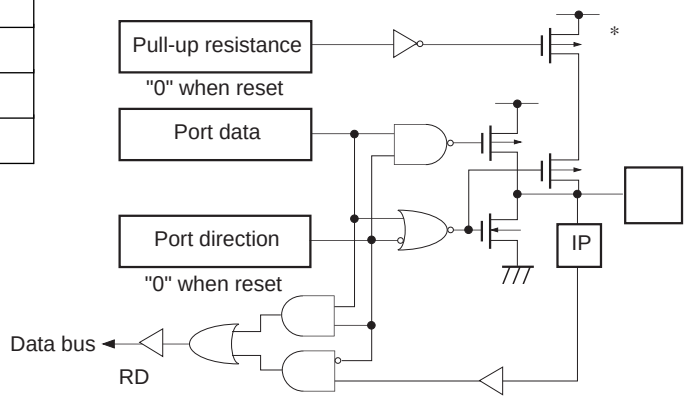
Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Lower 7-bit I/O port in which I/O can be set in a unit of single bits. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/$\overline{EC0}$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/$\overline{EC1}$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/$\overline{NMI}$	Input/Input		Non-maskable interruption request input.
PE4/$\overline{PWM}$	Output/Output		14-bit PWM output.
PE5/TO/ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter . Output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

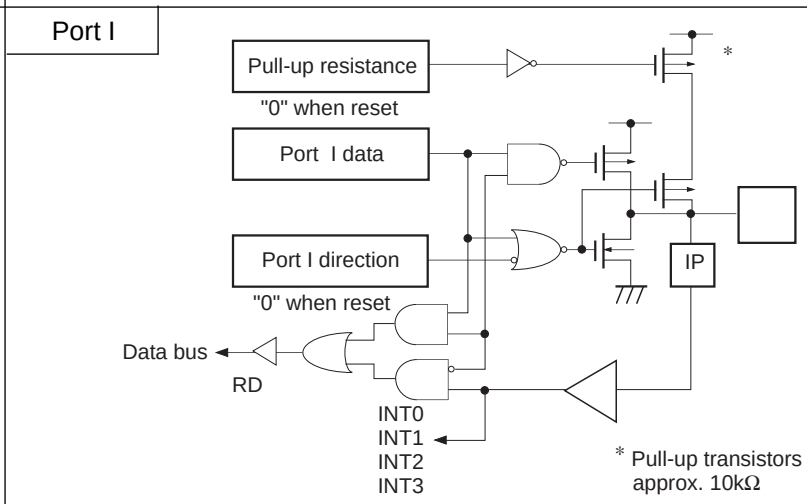
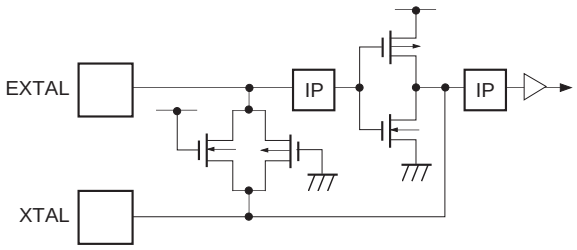
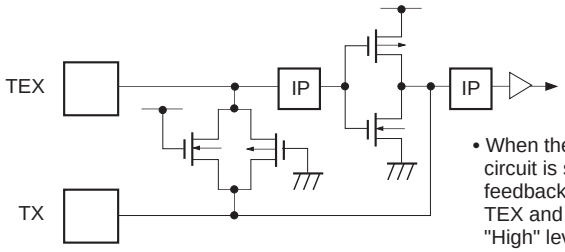
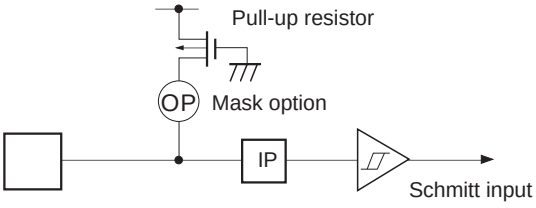
Symbol	I/O	Description
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) External interruption request inputs.
PI4 to PI7	I/O	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.
XTAL	Output	
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.
TX	Output	
$\overline{RST}$	Input	Low-level active, system reset.
AV_{REF}	Input	Reference voltage input for A/D converter.
AVss		A/D converter GND.
V_{DD}		Positive power supply.
Vpp		Positive power supply for incorporated PROM writing. Connect to V_{DD} during normal operation.
Vss		GND

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins		Hi-Z
PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1 4 pins		Hi-Z
PB2/SCK0 PB5/SCK1 2 pins		Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	Port B 	Hi-Z
PB7/SO1 1 pin	Port B 	High level
PC0 to PC7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC0}$ PE1/EC1 PE2/$\overline{RMC}$ PE3/$\overline{NMI}$ 4 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE4/$\overline{\text{PWM}}$ 1 pin	Port E 	High level
PE5/TO/ADJ 1 pin	Port E  * ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.	High level
PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7 36 pins	Port D Port F Port G Port H Port I  * Pull-up transistors approx. 10kΩ	Hi-Z

Pin	Circuit format	When reset
PI0/INT0 to PI3/INT3 4 pins	Port I  	Hi-Z
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin	 	Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output per pin
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Value per pin, excluding large current outputs
	I_{OLC}	20	mA	Value per pin*2 for large current outputs
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High-speed mode guaranteed operation range*1
		3.5	5.5		Low-speed mode guaranteed operation range*1
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during stop
	Vpp	Vpp = V_{DD}		V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL*4
Operating temperature	Topr	–10	+75	°C	

*1 High-speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

*2 Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF to PH, PI4 to PI7).

*3 Value of the following pins: $\overline{\text{RST}}$, CINT, $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0}}$, $\overline{\text{EC1}}$, RMC, $\overline{\text{NMI}}$, INT0, INT1, INT2, INT3.

*4 Specifies only during external clock input.

*5 Vpp and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4, PE5, PF to PI	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
	I_{IL}	PA to PD*1, PF to PI*1				–2.0	mA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–10			µA
I/O leakage current	I_{IZ}	PE0 to PE3	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Power supply current*2	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency demultiplier clock)				
			V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		18	40	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		400	1000	µA
	I_{DDS1}		Sleep mode				
			V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		1.1	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		Stop mode				
			V_{DD} = 5.5V, termination of 10MHz and 32kHz crystal oscillation			30	µA
Input capacity	C_{IN}	Pins other than PB7, PE4, PE5, AV_{REF}, V_{DD}, V_{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Pins PA to PD, and PF to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*2 When all pins are open.

AC Characteristics

(1) Clock timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$ EC1	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC0}$ EC1	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise time, fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FE$_H$).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

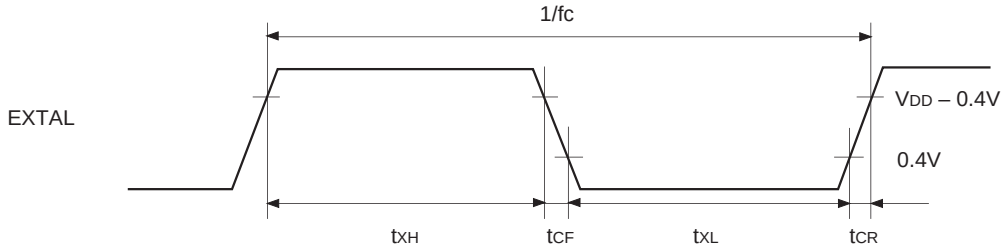


Fig. 1. Clock timing

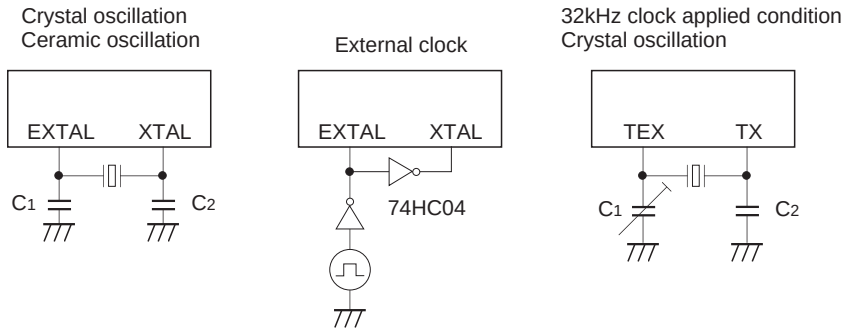


Fig. 2. Clock applied condition

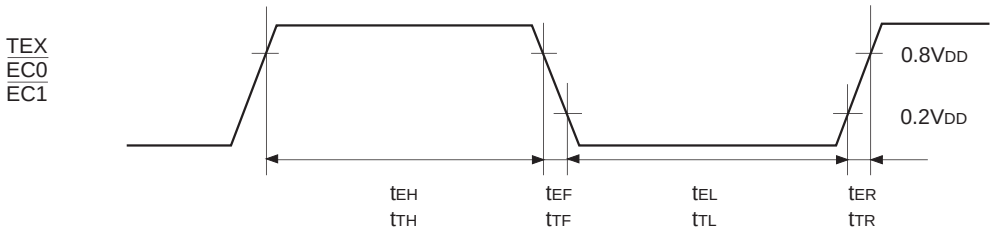


Fig. 3. Event count clock timing

(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FE$_H$).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

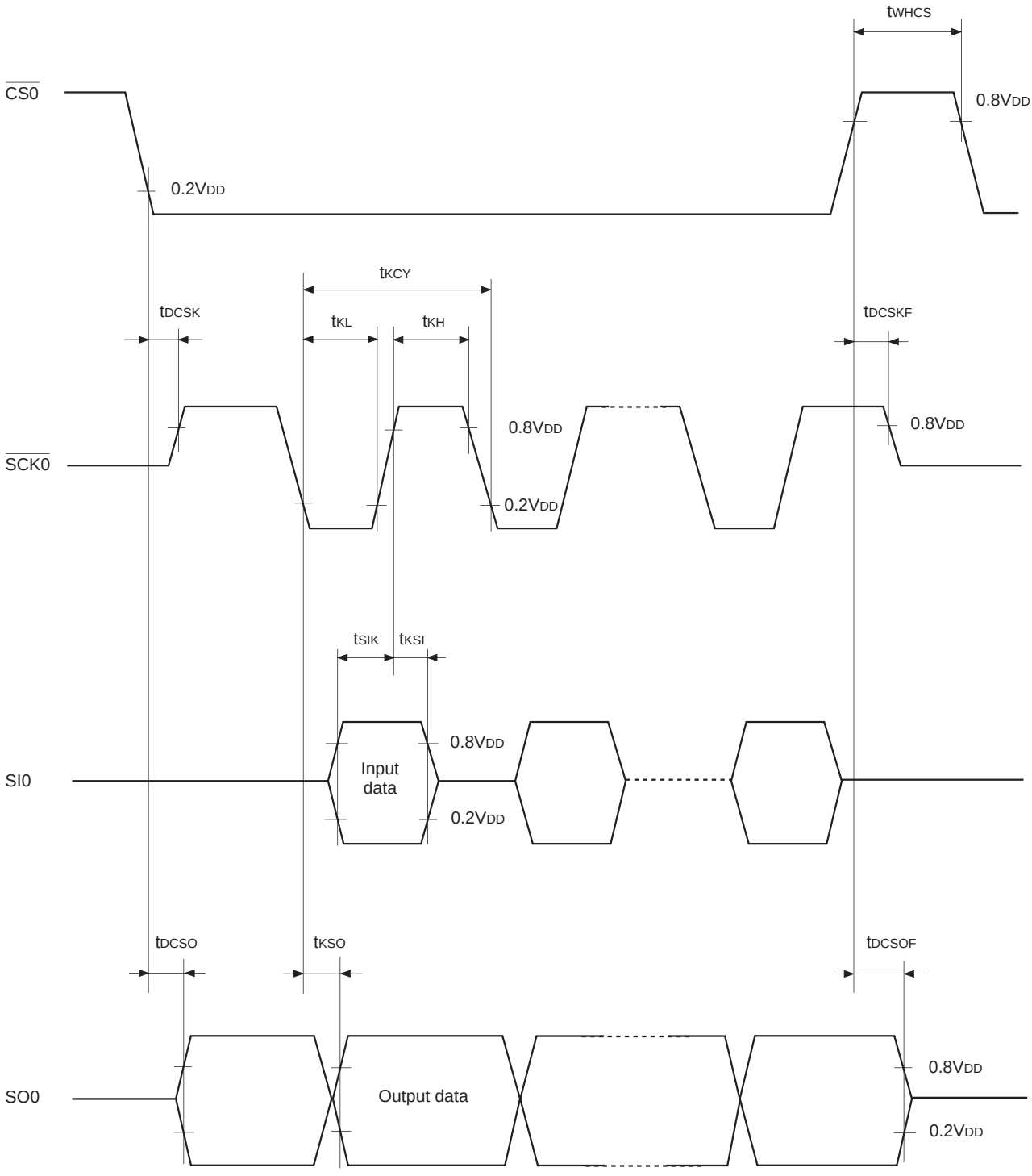


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

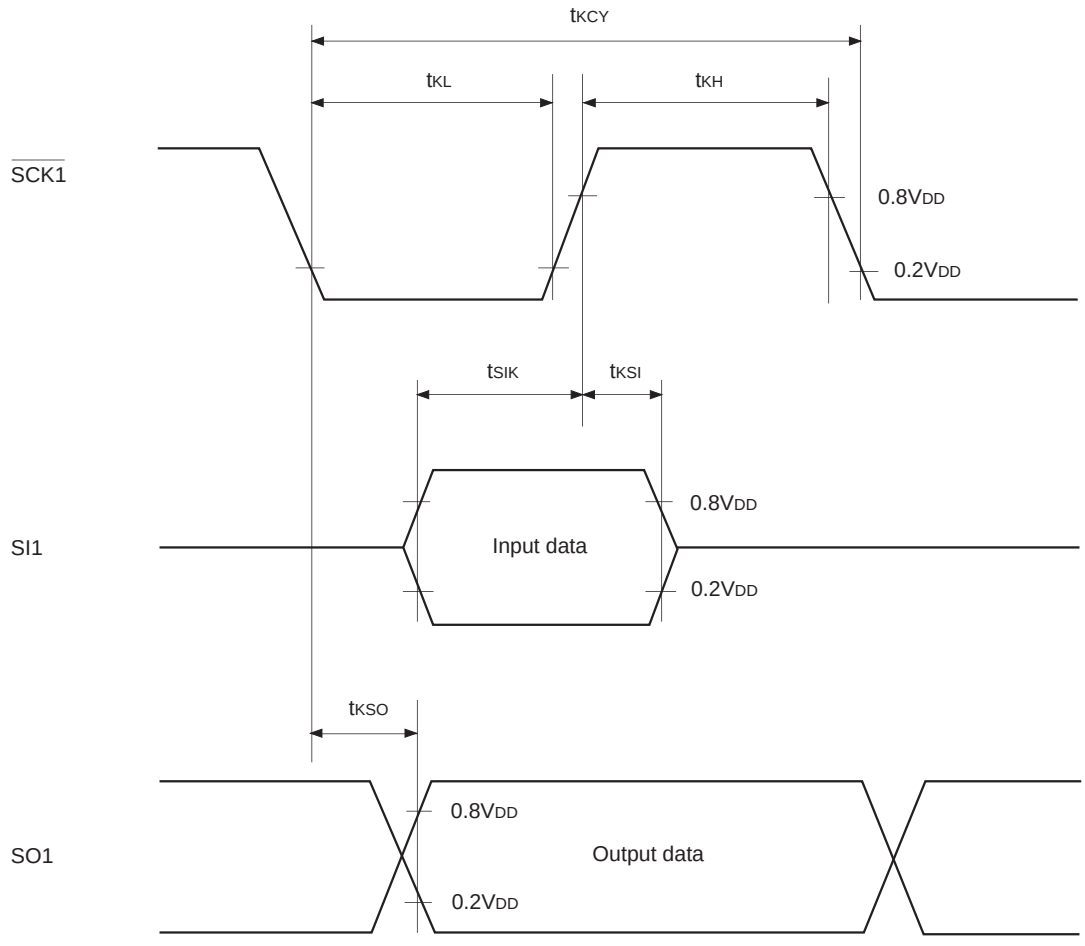
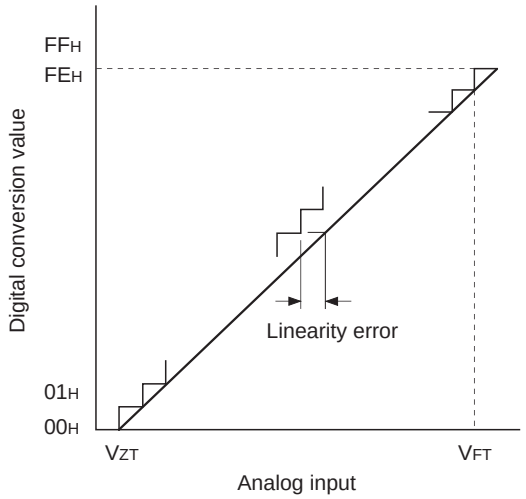


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = AV_{SS} = 0V			±5	LSB
Zero transition voltage	V_{ZT}*1			–10	70	150	mV
Full-scale transition voltage	V_{FT}*2			4930	5050	5120	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	µA



*1 V_{ZT} : Value at which the digital conversion value changes from 00_H to 01_H and vice versa.

*2 V_{FT} : Value at which the digita l conversion value changes from FE_H to FF_H and vice versa.

*3 f_{ADC} indicates the below values due to ADC operation clock selection.

During PS2 selection, f_{ADC} = fc/2

During PS1 selection, f_{ADC} = fc

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

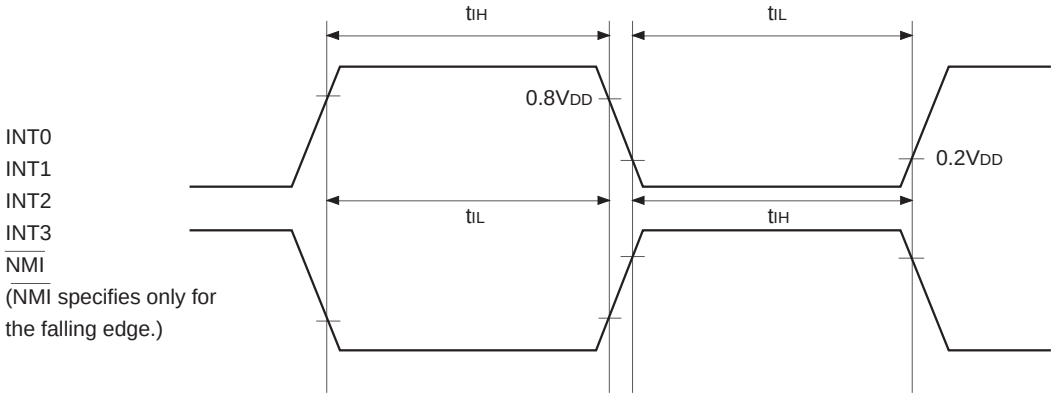


Fig 7. Interruption input timing

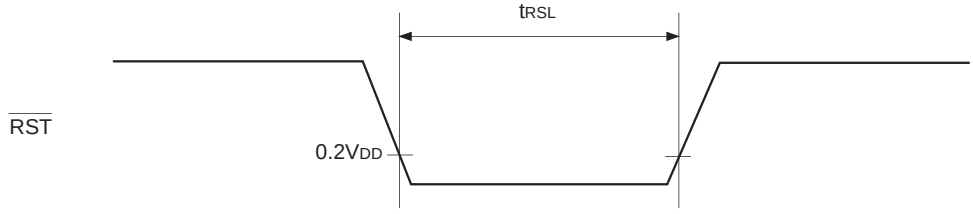


Fig. 8. $\overline{RST}$ input timing

Appendix

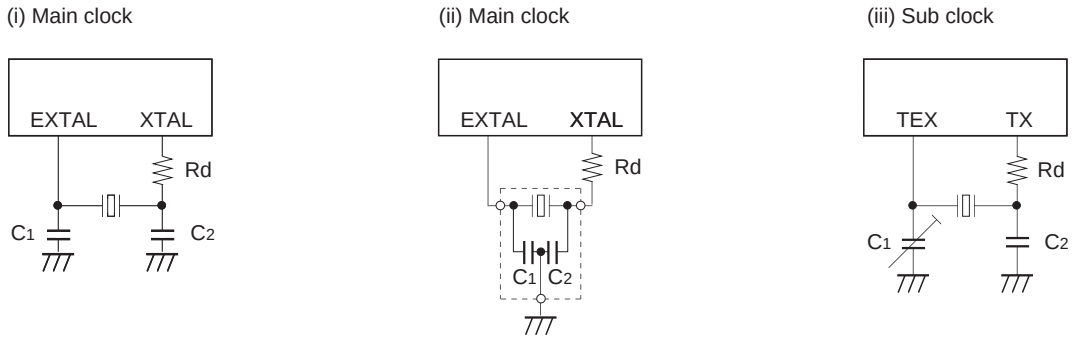


Fig. 9. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

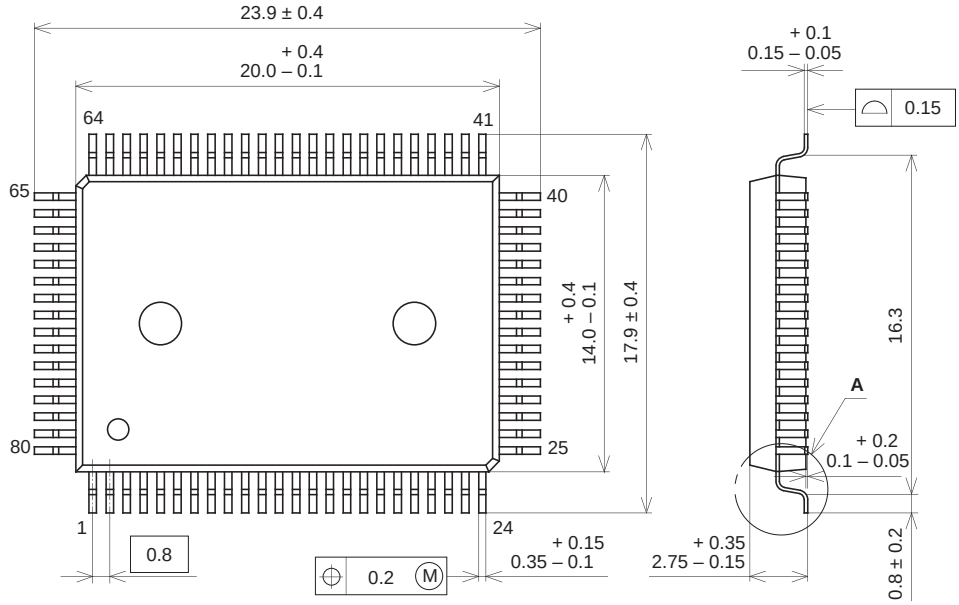
Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

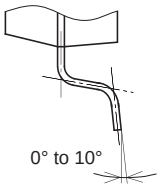
Product List

Optional item	Mask product	CXP843P40Q-1-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacity	32K bytes/40K bytes	PROM 40K bytes
Reset pin pull-up resistor	Existent/Non existent	Existent

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g